BIPOLAR HIGH-SPEED 8-BIT FLASH A/D CONVERTER

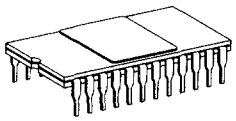
DESCRIPTION

Designed to be user-friendly, the TS 83068 is a complete monolithic flash analog-to-digital converter that combines all circuitry required to convertor high-speed analog signals into 8-bit digital data at rates of up to 35 MHz. Based on the TS 83048 monolithic flash analog-to-digital converter, the TS 83068 contains a wideband analog input amplifier, precision voltage reference and three-state outputs as well as zero-scale and full-scale flags.

The TS 83068 offers significant advantages in space efficiency and ease of use. Combining all analog front-end circuitry with the A/D converter in an easy to use package results in savings of board space, component and assembly cost. Furthermore, labor intensive circuit adjustments are eliminated.

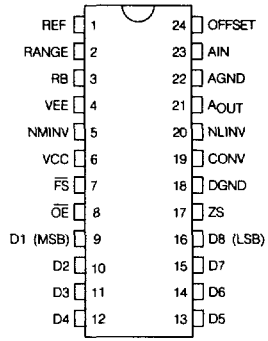
The TS 83068 is a monolithic alternate source to the THC 1068, but offers enhancements over it predecessors.

The TS 83068 is designed to meet the demanding requirements of military applications. It is available in a 24-pin hermetic package and operates with guaranteed performance over the full −55°C to +125°C case operating temperature range. Available also in die form.



C
DIL 24
(Ceramic package)

PIN CONNECTIONS
(Top view)
DIL Ceramic - 24 pins



Note : For details, see «pin description»

MAIN FEATURES

- 8-bit resolution.
- 35 MHz sampling rate.
- Excellent SNR.
- Low power : 0.8 W.
- Dual power supply : 5 V and −5.2 V.
- −55°C / +125°C specified.
- Guaranteed monotonicity.
- High slew rate of input stages.
- Compatible with THC 1068.
- No sample & hold required.
- Evaluation board : TSEV 83068.
- TTL compatible input and output.
- Three state outputs.
- Very low input capacitance.
- 45 MHz full power analog input bandwidth.

APPLICATIONS

- Military systems.
- Radar pulse analysis.
- Video digitizing.
- Image processing.
- Medical imaging.
- High-energy physics.
- X-Ray and ultrasound imaging.
- Communication/signal intelligence.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Positive supply voltages (Note 2)	V_{CC}	+4 to +6	V
Negative supply voltages (Note 2)	V_{EE}	−6.2 to −4	V
Maximum current	Ref	±5	mA
Analog control pins	Range, Offset, R_B, A_{OUT}	V_{EE} to V_{CC}	V
Analog input (Note 2)	A_{IN}	V_{EE} to V_{CC}	V
Digital input voltage (Note 2)	CONV, $\overline{OE}$, NMINV, NLINV	GND to V_{CC}	V
Digital output currents	D1 → D8, $\overline{FS}$ ZS	30	mA
Junction temperature	T_j	175	°C
Storage temperature	T_{stg}	−65 to +150	°C
Operating temperature range	T_{case}	−55 to +125	°C
Lead temperature (soldering 10 s)	T_{leads}	+260	°C

Note 1 : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.

Note 2 : With respect to AGND = DGND.

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

V_{CC} = 5 V ; V_{EE} = −5.2 V ; T_C = 25°C (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION				8		Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility				TTL		
Digital inputs						
• Logic «0» voltage	full	IV	0		0.8	V
• Logic «1» voltage	full	IV	2		5	V
Output data						
• Logic «0» voltage (Note 1)	full	II, D	0		0.4	V
• Logic «1» voltage	full	II, D	2.4			V
• Output delay (Note 2)		IV			5	ns
MAXIMUM CLOCK FREQUENCY		I	30	35		MHz
ANALOG INPUT						
Voltage range (Note 3)		V		−0.5 ; 0.5		V
		V		−1 ; 0		V
		V		0 ; +1		V
Input capacitance		IV		8		pF
Input resistance		V		1		kΩ
Analog bandwidth (Note 4)		V		45		MHz
ANALOG CONTROL						
Ref		V		1.2		V
Range (Note 5)		V		1		V
Offset		V		0 → 1.2		V
RB		V		−2		V
POWER REQUIREMENTS						
Power supply						
• Positive supply		I, D	4.5	5	5.5	V
	full	II	4.5	5	5.5	V
• Negative supply		I, D	−5.7	−5.2	−4.7	V
	full	II	−5.7	−5.2	−4.7	V
Power dissipation						
• Positive supply		I, D		200	350	mW
	full	II			400	mW
• Negative supply		I, D		600	700	mW
	full	II			750	mW
THERMAL RESISTANCE		V				
Junction-to-ambient (still air)				45		°C/W
Junction-to-case				5		°C/W
ACCURACY (Note 6)						
Differential nonlinearity		I, D		±0.5	±0.8	LSB
	full	II		±0.6	±0.9	LSB
Integral nonlinearity		I, D		±0.5	±0.8	LSB
	full	II		±0.6	±0.9	LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

V_{CC} = 5 V ; V_{EE} = −5.2 V ; T_C = 25°C (unless otherwise specified)

Parameter	Test level	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS (Note 7)					
Signal to noise ratio					
F_S = 30 MHz F_{in} = 1 MHz	V		43.9		dB
F_S = 1 MHz F_{in} = 0.1 MHz	I, D	43.9	45.7		dB
F_S = 20 MHz F_{in} = 1 MHz	I	39.7	45.1		dB
F_S = 20 MHz F_{in} = 2.5 MHz	I	37.9	41.5		dB
Total harmonic distorsion					
F_S = 30 MHz F_{in} = 1 MHz	V		52		dB
F_S = 1 MHz F_{in} = 0.1 MHz	I, D	48	55		dB
F_S = 20 MHz F_{in} = 1 MHz	I	45	52		dB
F_S = 20 MHz F_{in} = 2.5 MHz	I	40	44		dB
Number of effective bits					
F_S = 30 MHz F_{in} = 1 MHz	V		7.0		Bits
F_S = 1 MHz F_{in} = 0.1 MHz	I, D	7.0	7.3		Bits
F_S = 20 MHz F_{in} = 1 MHz	I	6.3	7.2		Bits
F_S = 20 MHz F_{in} = 2.5 MHz	I	6.0	6.6		Bits
Aperture uncertainty	V		20		ps
Differential phase	V		1		degree
Differential gain	V		2		%

Note 1 : With I_{OUT} = 4 mA.

Note 2 : See timing diagram.

Note 3 : Depending upon offset pin connection.

Note 4 : The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Note 5 : The reference gain control voltage can be adjusted between 0.5 V and 1.2 V (see Figure 3).

Note 6 : Histogram based on sampling of 100 kHz sinusoïdal analog signal with and encoding rate of 1 MHz.

Note 7 : Dynamic measurements are performed with an analog input signal 1 dB below full scale.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at +25°C, and sample tested at specified temperature
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at T_{amb} = +25°C.

TIMING DIAGRAM

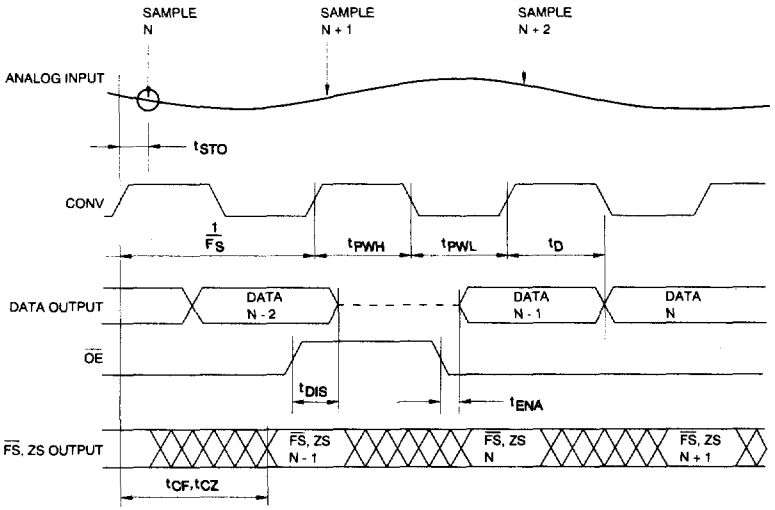


Figure 1

SWITCHING PERFORMANCES

Parameter	Symbol	Test conditions	Typ.	Unit
Maximum conversion rate	F_S	V_{CC}, V_{EE} = Min	35	MHz
Sampling time offset	t_{STO}		−8	ns
Digital output delay	t_D		10	ns
HIGH impedance enable	t_{ENA}		12	ns
HIGH impedance disable	t_{DIS}		12	ns
Full-scale flag delay	t_{CF}		20	ns
Zero-scale flag delay	t_{CZ}		20	ns

FUNCTIONAL BLOCK DIAGRAM

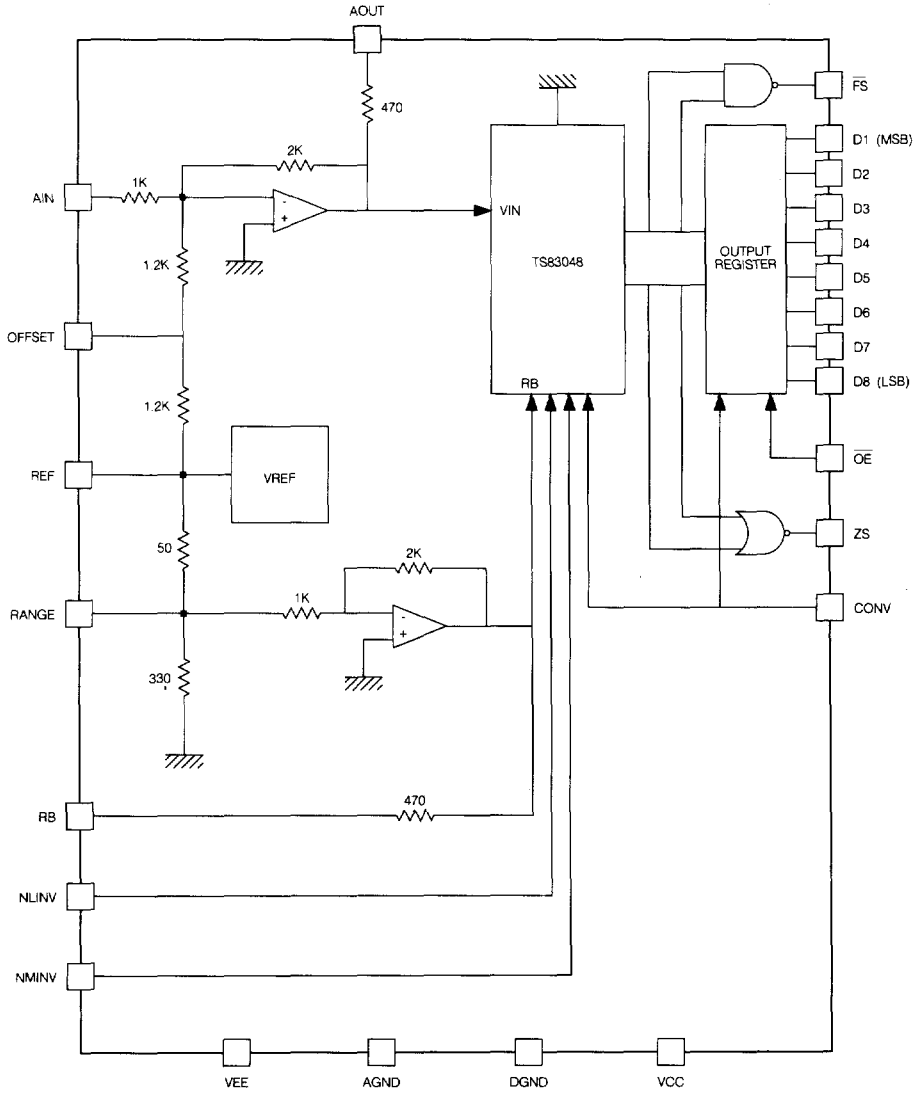


Figure 2

PIN DESCRIPTION

Pin DIL	Symbol	Function	Description
1	REF	Reference voltage output	+1.2 V
2	RANGE	Reference gain control	+1 V
3	R_B	Reference voltage monitor point	−2 V
4	V_{EE}	Negative power supply	−5.2 V
5	NMINV	Not most significant bit invert	TTL compatible active low
6	V_{CC}	Positive power supply	+5 V
7	$\overline{FS}$	Full scale flag	TTL compatible
8	$\overline{OE}$	Output enable	TTL compatible active low
9	D1	Digital output (MSB)	TTL tri state compatible
10	D2	Digital output	
11	D3	Digital output	
12	D4	Digital output	
13	D5	Digital output	
14	D6	Digital output	
15	D7	Digital output	
16	D8	Digital output (LSB)	
17	ZS	Zero scale flag	TTL compatible
18	D_{GND}	Digital ground	
19	CONV	Convert	TTL compatible
20	NLINV	Not least significant bit invert	TTL compatible active low
21	A_{OUT}	Amplifier output monitor point	0 to −2 V
22	A_{GND}	Analog ground	
23	A_{IN}	Analog input	−1 to +1 V depending of offset connection
24	OFFSET	Input range offset control	0 to +1.2 V

OUTPUT CODING

Step	Midpoints	Binary						Offset two's complement					
		True			Inverted			True			Inverted		
	1 LSB = 3.92 mV	NMINV = 1 NLINV = 1			NMINV = 0 NLINV = 0			NMINV = 0 NLINV = 1			NMINV = 1 NLINV = 0		
		$D_1...D_8$	$\overline{FS}$	ZS	$D_1...D_8$	$\overline{FS}$	ZS	$D_1...D_8$	$\overline{FS}$	ZS	$D_1...D_8$	$\overline{FS}$	ZS
000	−0.5000 V	00000000	1	1	11111111	0	0	10000000	1	0	01111111	1	0
001	−0.4961 V	00000001	1	0	11111110	1	0	10000001	1	0	01111110	1	0
•	•	•			•			•			•		
•	•	•			•			•			•		
•	•	•			•			•			•		
126	−0.0059 V	01111110	1	0	10000001	1	0	11111110	1	0	00000001	1	0
127	−0.0020 V	01111111	1	0	10000000	1	0	11111111	0	0	00000000	1	1
128	+0.0020 V	10000000	1	0	01111111	1	0	00000000	1	1	11111111	0	0
129	−0.0059 V	10000001	1	0	01111110	1	0	00000001	1	0	11111110	1	0
•	•	•			•			•			•		
•	•	•			•			•			•		
•	•	•			•			•			•		
254	+0.4961 V	11111110	1	0	00000001	1	0	01111110	1	0	10000001	1	0
255	+0.5000 V	11111111	0	0	00000000	1	1	01111111	1	0	10000000	1	0

THEORY OF OPERATION

The TS 83068 is a complete 8 bit A/D monolithic converter. The TS 83068 has four fonctional sections : a wideband input amplifier, a reference generation circuit, an 8 bit flash A/D converter, and an 8 bit three state output register.

The wideband amplifier provides the current necessary to drive the input capacitance of the flash converter while translating the bipolar input to the unipolar range of the flash converter. The input amplifier has a gain of -2 and the stable reference needs no adjustment. The analog input voltage range is -0.5 to 0.5 V but can be configured for a 0 to $+1.0$ V range by shorting OFFSET to A_{GND}. Likewise, the input can be configured for a 0 to -1.0 V range by connecting the OFFSET pin to the REF pin.

The converter stage is derived from the TS 83048 8 bit A/D converter. The TS 83048 is a flash converter : it compares the signal in an array of 255 comparators referenced by 256 resistors. An encoding stage converts the thermometer code to the 8-bit binary output code. Details of the TS 83048 operation are reported in its data sheet.

The three-state output register holds the output data between convert cycles and can be set into the high-impedance state with the $\overline{OE}$ control pin.

APPLICATIONS

User warning

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

Functional description

The TS 83068 operates with analog input signals of 1 V amplitude. It is designed for bipolar (± 0.5 V) or unipolar positive (0 ; +1 V) or negative (-1 V ; 0 V) input voltage.

For bipolar input, the offset pin is not connected. For unipolar positive, the offset pin is connected to A_{GND}. For unipolar negative the offset pin is connected to the REF pin. A 2 kΩ potentiometer can be connected between A_{GND}, OFFSET and REF to vary the DC offset of the input amplifier as shown in Figure 3.

The A_{OUT} pin allows monitoring the analog signal at the input to the flash converter and is normally left unconnected. It has a nominal series resistance of 470 Ω.

A precision voltage reference is used for the flash converter reference as well as for DC level shifting. The REF pin can sink or source up to 2 mA but is normally left unconnected.

The range pin allows optional adjustment of the negative reference voltage (thus the gain) of the flash converter and is normaly left unconnected. For gain adjustment a 2 kΩ potentiometer can be connected between REF, RANGE and A_{GND} as shown in Figure 3. The nominal input resistance is 300 Ω. The R_B pin allows monitoring of the full scale reference voltage to the flash converter through a 470 Ω series resistor.

The wideband input amplifier of the TS 83068 provides the current necessary to drive the input capacitance of the flash converter. The amplifier provides a gain -2 and has a nominal input impedance of 1 000 Ω. For lower impedances, a termination resistor should be added as close to the A_{IN} pin as possible. The TS 83068 is capable of digitizing sinusoidal signals up to 25 MHz. The input amplifier has pulse response as shown in the Typical Performance Curves, with a full-power bandwidth in excess of 40 MHz.

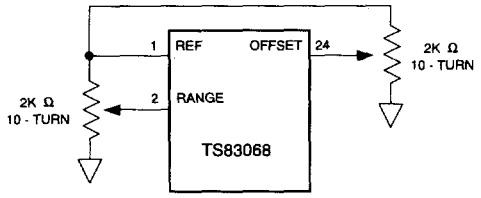


Figure 3 : Connection of RANGE, REF and OFFSET.

The digital output of the TS 83068 can be formatted with the NMINV and NLINV control pins. These pins are for D.C. (steady state) use and allow either straight binary or offset two's complement, in either thue or inverted sense. The Output Coding Table shows the output formats possible with these pins. Note that in offset two's complement format, $\overline{FS}$ and ZS indicate midscale codes rather than full and zero scale codes, as shown in the Output Coding Table. When left unconnected, internal pull-up resistors keep the outputs in true straight binary format.

The data outputs of the TS 83068 can be set into the high-impedance state with the $\overline{OE}$ control pin. The outputs become high-impedance points withing t_{DIS} after the $\overline{OE}$ is switched HIGH and likewise become valid within t_{ENA} after switching $\overline{OE}$ LOW.

The output data are three state TTL compatible.

The output flags of the TS 83068 are not latched : they are active even when the data outputs are in the high-impedance state. The $\overline{FS}$ (active LOW) flag indicates that the output bits of the flash converter are all HIGH. Likewise, the ZS (active HIGH) flag indicates that the output bits of the flash converter are all LOW. ZS and $\overline{FS}$ represent zero-scale and full-scale analog inputs only when the output code is in the straight binary format. The Output Coding Table shows the status of the output flags for various input voltages and output code formats. Note that the flags indicate the status of the flash converter output one clock cycle before it appears at the output pins of the TS 83068.

Packaging

The TS 83068 is mounted in ceramic 24-pin DIL package.
Sockets may be used for prototype evaluation, but **should be avoided afterwards**, because **it leads to limitations of TS 83068 dynamic performance**, and increased decoupling difficulties.

LAYOUT AND POWER SUPPLY

The TS 83068 is a monolithic converter. Integration of internal (on chip) decoupling capacitors like those used in hybrid circuits is not possible.

So, proper layout of evaluation on board, always critical, is particularly important.

To insure optimum performance, a very quiet V_{CC} supply is recommended. A 8.2 Ω serial resistance between external V_{CC} and the converter is necessary. Power supplies (V_{CC} and V_{EE}) should be capacitively coupled to ground with three high quality capacitors (4.7 µF, 100 nF and 470 pF) to reduce noise in the circuit. These capacitors should be kept as close as possible to circuit package. All ground pins should be connected to ground plane.

Digital switching noise may also have an impact on SNR. This noise can be minimized with 33 Ω serial resistances on the digital outputs. The commutation peak current will be limited.

The use of a socket with parasitic inductances may limit dynamic performances (noise floor increases), and is not recommended except for prototype or evaluation purposes.

The length of digital input/output signal paths should be matched and kept short, to avoid propagation delay mismatches, increased output bits time skew, and over or undershoot caused by reflections.

So long as propagation delay along the line is shorter than digital signal rise or fall time, the reflection has little effect on the waveform.

50 Ω impedance microstrip line with 50 Ω termination chip resistors should be used to drive analog and clock input pins.

TYPICAL EVALUATION BOARD

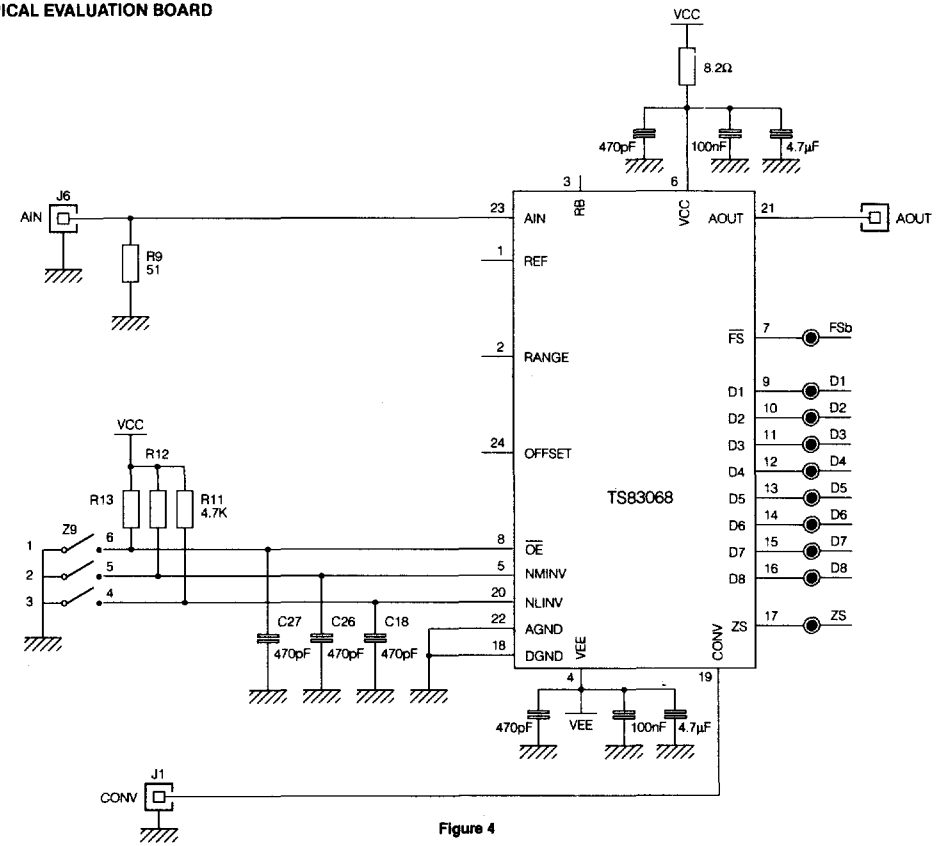


Figure 4

DEFINITION OF TERMS

Signal-to-noise ratio (SNR)

determined by FFT analysis,

$$SNR = 10.\log\left[\frac{P(F_{IN})}{P_n}\right] = 10.\log\left[\frac{A^2(F_{IN})}{\Sigma A^2(j)}\right] \quad j \neq F_{in}$$

with :

- $P(F_{IN})$ spectral power of the input frequency F_{IN},
- P_n noise power, which is defined as the sum of the powers of all spectral components, except F_{IN},
- A(j) amplitude of the spectral component of frequency j.

Total harmonic distorsion (THD)

determined by FFT analysis,

$$THD = 10.\log\left[\frac{P(F_{IN})}{P_{hn}}\right] = 10.\log\left[\frac{A^2(F_{IN})}{\Sigma A^2(k.F_{IN})}\right] \quad k \geqslant 2$$

with : P_{hn} harmonic noise power, which is defined as the sum of the powers of all harmonics of F_{IN}.

Number of effective bits (N_{eff})

determined by FFT analysis,

$$N_{eff} = \frac{SNR - 1.76}{6.02}$$

Gain error (G_e)

$$G_e = \frac{G - G_O}{G_O}$$

with :

- G_O slope of theoretical straight line of the ADC transfer function.
- G slope of the real best-fit straight line.

Integral nonlinearity (INL)

Measured after trimming the offset and gain errors to zero.

The integral nonlinearity for an output code i, INL (i), is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.

The ADC integral nonlinearity INL is the maximum value of all |INL(i)|.

Differential nonlinearity (DNL)

Measured after trimming the offset and gain errors to zero.

The differential nonlinearity for an output code i, DNL(i), is the difference between the measured step size of code i and the ideal LSB step size.

The ADC differential nonlinearity DNL is the maximum value of all |DNL(i)|.

TYPICAL PERFORMANCE CURVES

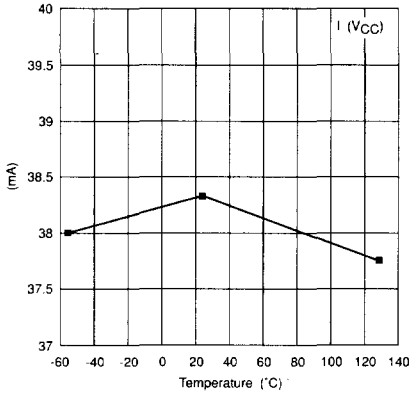


Figure 5 : Supply currents.

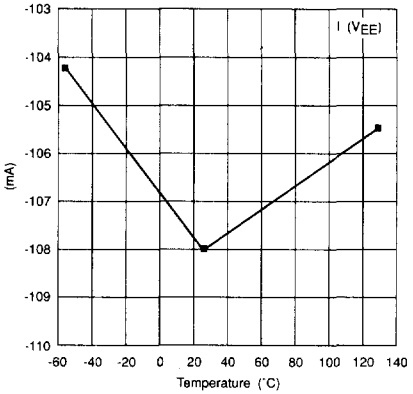


Figure 6 : Supply currents.

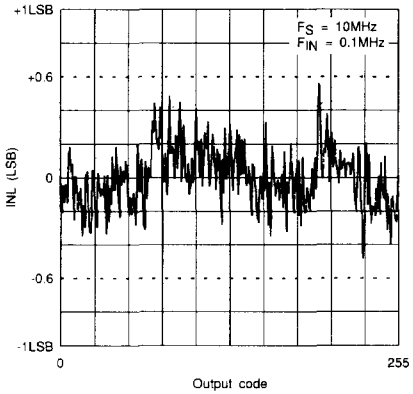


Figure 7 : Integral non linearity.

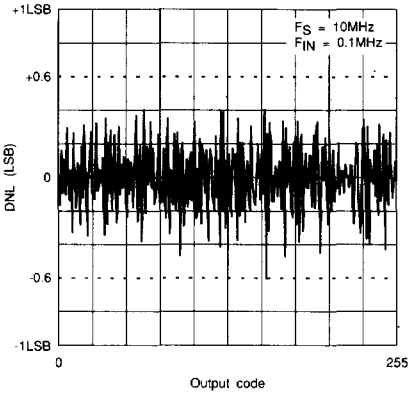


Figure 8 : Differential non linearity.

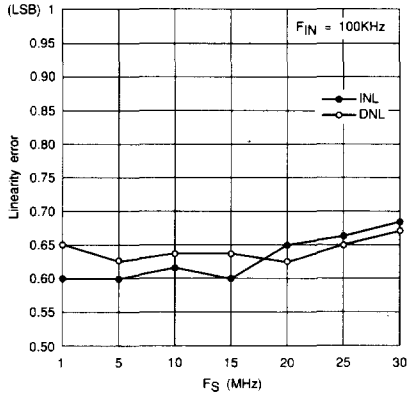


Figure 9 : Linearity error versus F_S.

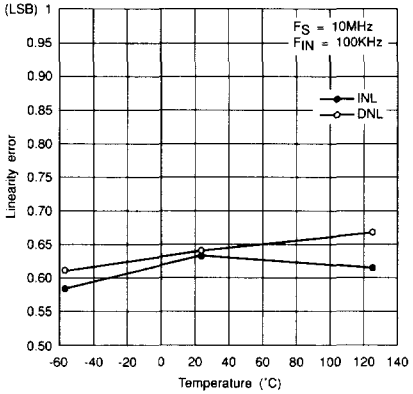


Figure 10 : Linearity error versus temperature.

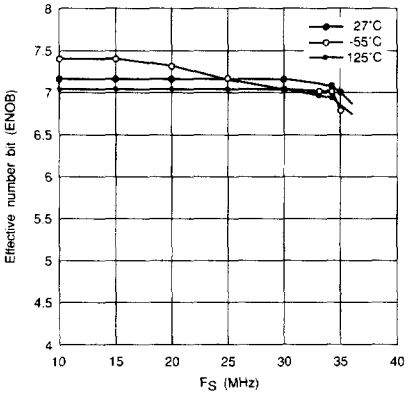


Figure 11

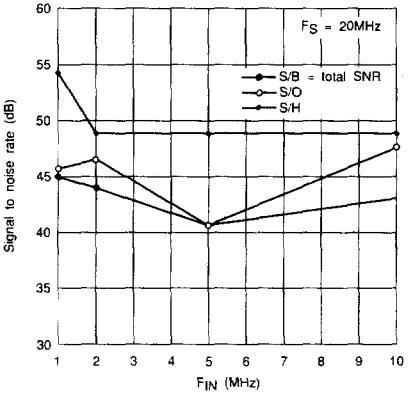


Figure 12

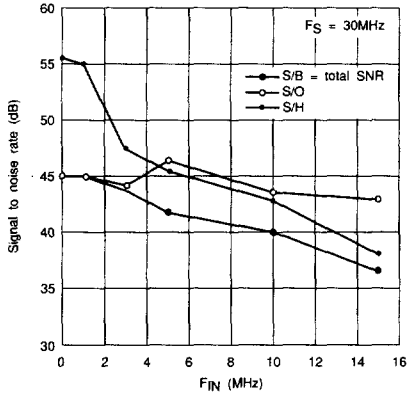


Figure 13

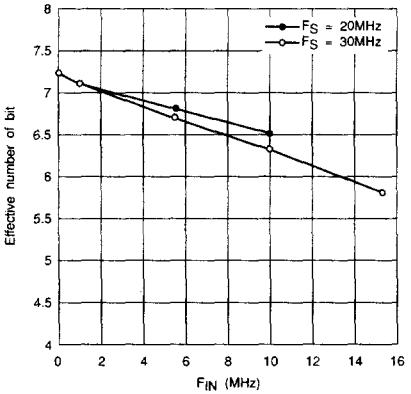


Figure 14

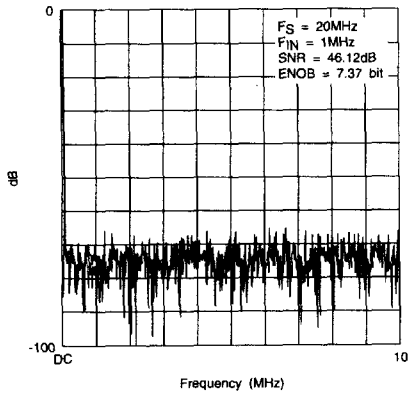


Figure 15 : FFT of TS 83068.

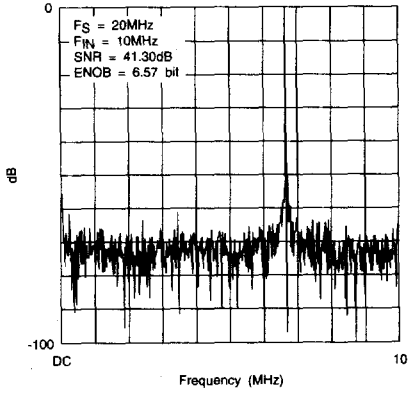


Figure 16 : FFT of TS 83068.

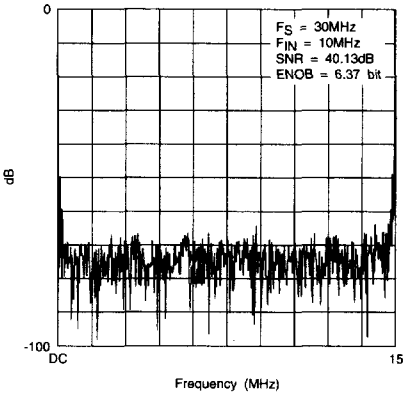


Figure 17 : FFT of TS 83068.

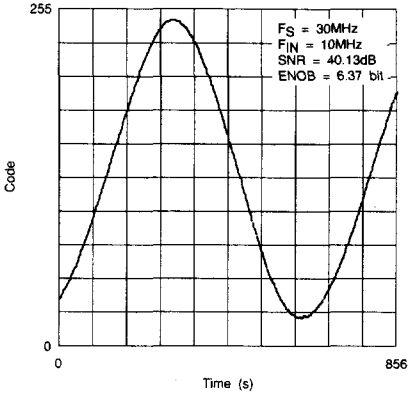
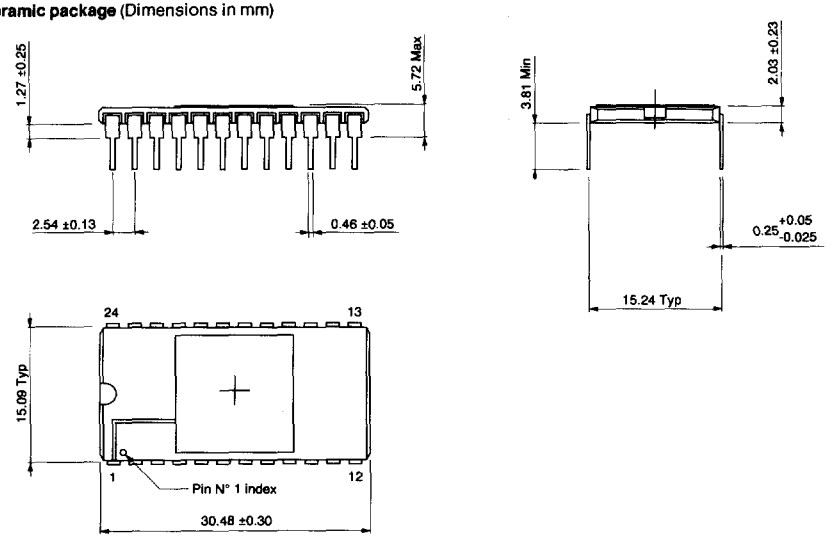


Figure 18 : Reconstructed waveform 30 MHz sampling rate, 15 MHz input frequency.

2

MECHANICAL PACKAGE DATA

DIL 24 - Ceramic package (Dimensions in mm)



DIE MECHANICAL INFORMATION : JTS 83068

Pad layout : V676

Pad size : 0.120 × 0.120 mm

Die size : 5.470 × 4.250 mm

Die thickness : 380 μm

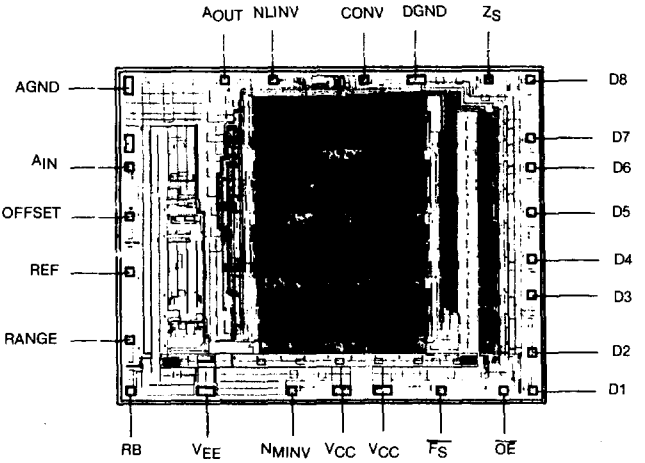
Metallization : Al-Ni-Au (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

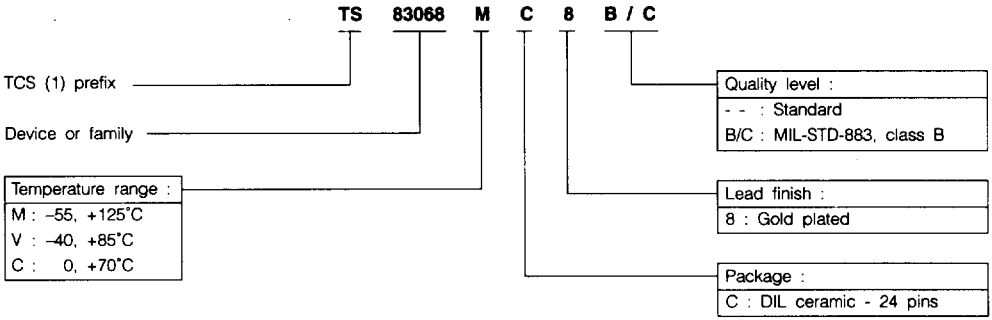
Qualification lot package : DIL 24

Back side potential : V_{EE}

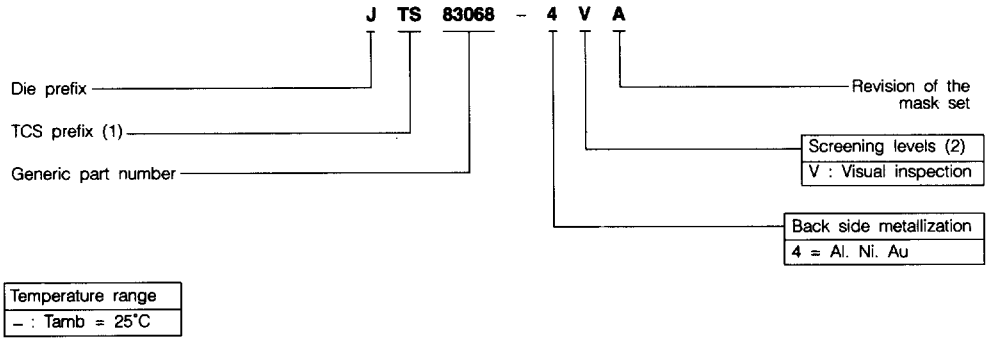


ORDERING INFORMATION

Packaged device



Die form



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of the different available versions contact your TCS sales office.