

## Improved Quad SPST CMOS Analog Switches

### DESCRIPTION

The DG444B, DG445B are monolithic quad analog switches designed to provide high speed, low error switching of analog and audio signals. The DG444B, DG445B are upgrades to the original DG444, DG445.

Combining low on-resistance (45  $\Omega$ , typ.) with high speed ( $t_{ON}$  120 ns, typ.), the DG444B, DG445B are ideally suited for Data Acquisition, Communication Systems, Automatic Test Equipment, or Medical Instrumentation. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

The DG444B, DG445B are built using Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

When on, each switch conducts equally well in both directions and blocks input voltages to the supply levels when off.

### FEATURES

- Low On-Resistance: 45  $\Omega$
- Low Power Consumption: 1 mW
- Fast Switching Action -  $t_{ON}$ : 120 ns
- Low Charge Injection
- TTL/CMOS-Compatible Logic
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

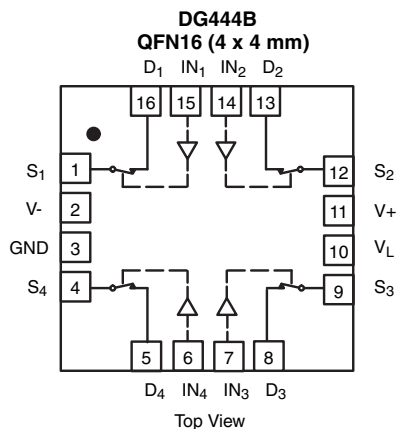
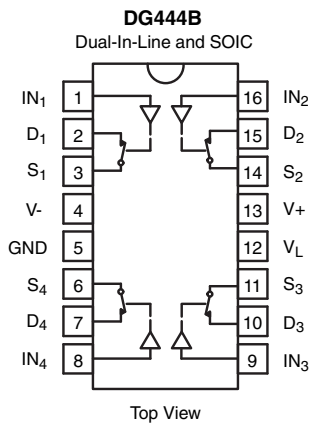
### BENEFITS

- Low Signal Errors and Distortion
- Reduced Power Supply Consumption
- Faster Throughput
- Reduced Pedestal Errors
- Simple Interfacing

### APPLICATIONS

- Audio Switching
- Data Acquisition
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Medical Instruments

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG444B	DG445B
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

ORDERING INFORMATION		
Temp Range	Package	Part Number
- 40 °C to 85 °C	16-pin Plastic DIP	DG444BDJ
		DG444BDJ-E3
		DG445BDJ
		DG445BDJ-E3
	16-pin Narrow SOIC	DG444BDY-E3
		DG444BDY-T1-E3
		DG445BDY-E3
		DG445BDY-T1-E3
	16 pin QFN 4 x 4 mm (Variation 1)	DG444BDN-T1-E4
		DG445BDN-T1-E4

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)			
Parameter	Symbol	Limit	Unit
V+ to V-		44	V
GND to V-		25	
$V_L$		(GND - 0.3 V) to (V+) + 0.3 V	
Digital Inputs <sup>a</sup> , $V_S$ , $V_D$		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Continuous Current (Any Terminal)		30	mA
Current, S or D (Pulsed at 1 ms, 10 % duty cycle)		100	
Storage Temperature		- 65 to 125	$^\circ\text{C}$
Power Dissipation (Package) <sup>b</sup>	16-pin Plastic DIP <sup>c</sup>	470	mW
	16-pin Narrow Body SOIC <sup>d</sup>	640	
	QFN-16	850	

Notes:

- a. Signals on  $S_X$ ,  $D_X$ , or  $IN_X$  exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6 mW/ $^\circ\text{C}$  above 75  $^\circ\text{C}$ .
- d. Derate 8 mW/ $^\circ\text{C}$  above 75  $^\circ\text{C}$ .



SPECIFICATIONS (for dual supplies)							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ , $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	Temp. <sup>a</sup>	Limits - 40 °C to 85 °C			Unit
				Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	- 15		15	V
Drain-Source On-Resistance	$R_{DS(on)}$	$I_S = 1\text{ mA}$ , $V_D = \pm 10\text{ V}$	Room Full		45	80 95	$\Omega$
Switch Off Leakage Current	$I_{S(off)}$	$V_D = \pm 14\text{ V}$ , $V_S = \pm 14\text{ V}$	Room Full	- 0.5 - 5	$\pm 0.01$	0.5 5	nA
	$I_{D(off)}$		Room Full	- 0.5 - 5	$\pm 0.01$	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 14\text{ V}$	Room Full	- 0.5 - 10	$\pm 0.02$	0.5 10	
<b>Digital Control</b>							
Input Voltage Low	$V_{INL}$		Full			0.8	V
Input Voltage High	$V_{INH}$		Full	2.4			
Input Current $V_{IN}$ Low	$I_{INL}$	$V_{IN}$ under test = 0.8 V All Other = 2.4 V	Full	- 1	- 0.01	1	$\mu\text{A}$
Input Current $V_{IN}$ High	$I_{INH}$	$V_{IN}$ under test = 2.4 V All Other = 0.8 V	Full	- 1	0.01	1	
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$ , See Figure 2	Room			300	ns
Turn-Off Time	$t_{OFF}$		Room			200	
Charge Injection <sup>e</sup>	Q	$C_L = 1\text{ nF}$ , $V_S = 0\text{ V}$ $V_{gen} = 0\text{ V}$ , $R_{gen} = 0\ \Omega$	Room		1		pC
Off Isolation <sup>e</sup>	OIRR	$R_L = 50\ \Omega$ , $C_L = 15\text{ pF}$ $V_S = 1\text{ V}_{RMS}$ , $f = 100\text{ kHz}$	Room		- 90		dB
Crosstalk (Channel-to-Channel) <sup>d</sup>	$X_{TALK}$		Room		- 95		
Source Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$ , $f = 100\text{ kHz}$	Room		5		pF
Drain Off Capacitance	$C_{D(off)}$		Room		5		
Channel On Capacitance	$C_{D(on)}$		Room		16		
<b>Power Supplies</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}$ or $5\text{ V}$	Room Full			1 5	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	- 1 - 5			
Logic Supply Current	$I_{IN}$		Room Full			1 5	

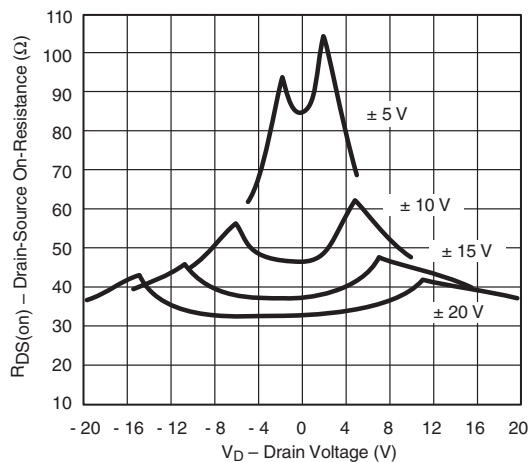
SPECIFICATIONS (for unipolar supplies)							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^e$	Temp. <sup>a</sup>	D Suffix -40 °C to 85 °C			Unit
				Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		Full	0		12	V
Drain-Source On-Resistance <sup>d</sup>	$R_{DS(on)}$	$I_S = 1\text{ mA}, V_D = 3\text{ V}, 8\text{ V}$	Room Full		90	160 200	$\Omega$
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}, V_S = 8\text{ V}$ See Figure 2	Room		120	300	ns
Turn-Off Time	$t_{OFF}$		Room		60	200	
Charge Injection	Q	$C_L = 1\text{ nF}, V_{gen} = 6\text{ V}, R_{gen} = 0\ \Omega$	Room		4		pC
<b>Power Supplies</b>							
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			1 5	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	-1 -5			
Logic Supply Current	$I_{IN}$	$V_L = 5.25\text{ V}, V_{IN} = 0\text{ or }5\text{ V}$	Room Full			1 5	

**Notes:**

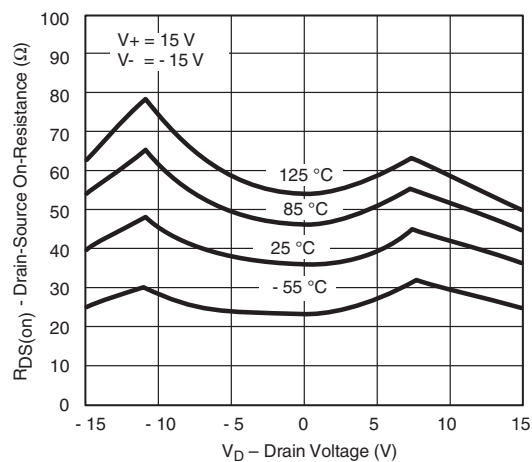
- a. Room = 25 °C, Full = as determined by the operating temperature suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Guaranteed by design, not subject to production test.
- e.  $V_{IN}$  = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



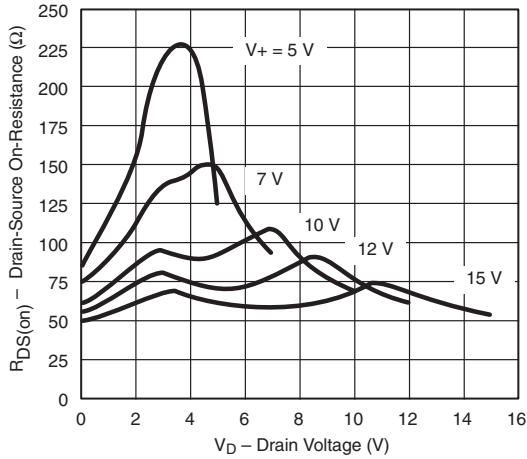
**$R_{DS(on)}$  vs.  $V_D$  and Power Supply Voltages**



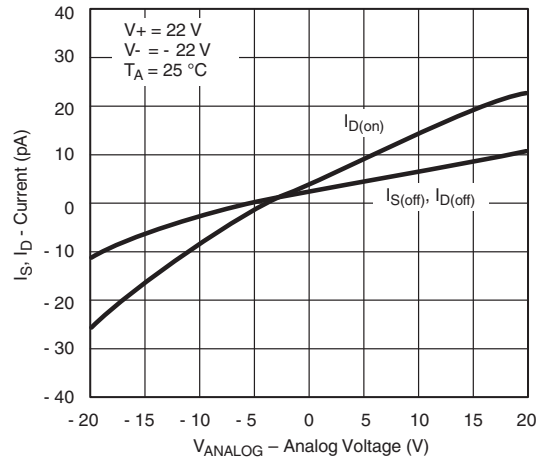
**$R_{DS(on)}$  vs.  $V_D$  and Temperature**



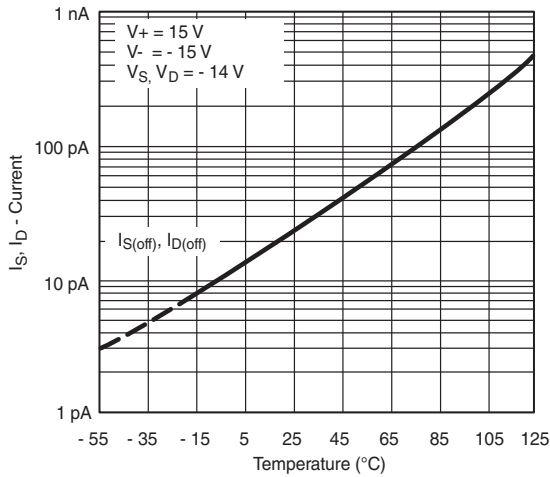
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



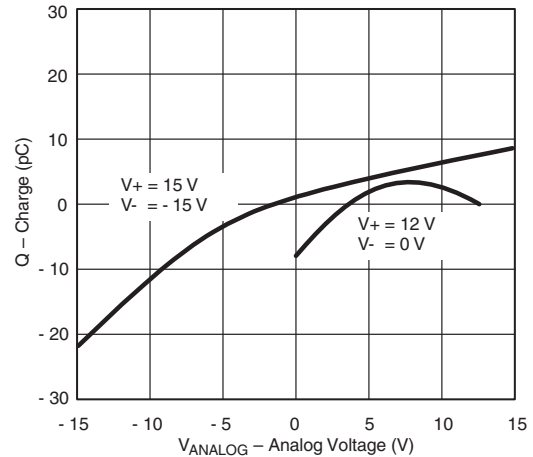
**$R_{DS(on)}$  vs.  $V_D$  and Single Power Supply Voltages**



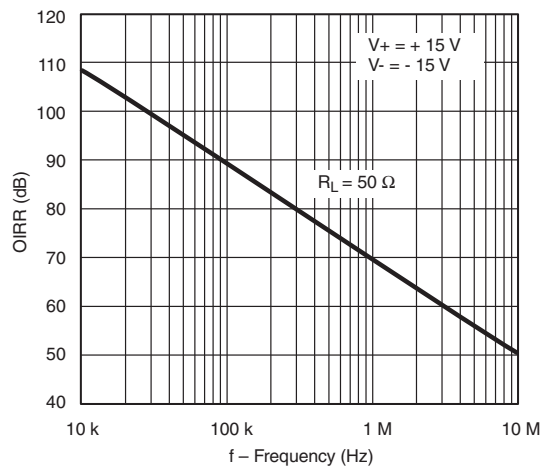
**Leakage Currents vs. Analog Voltage**



**Leakage Current vs. Temperature**



**$Q_S, Q_D$  - Charge Injection vs. Analog Voltage**



**Off Isolation vs. Frequency**

## SCHEMATIC DIAGRAM (typical channel)

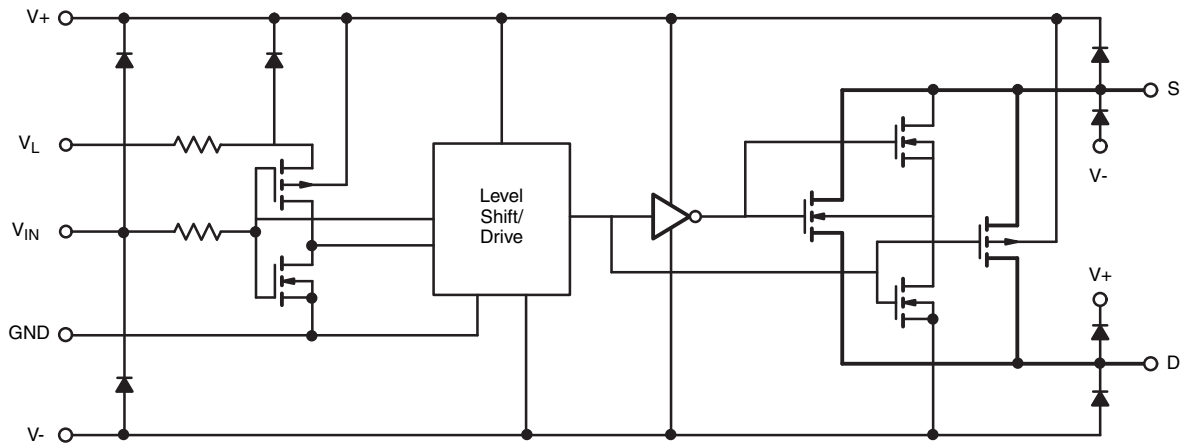
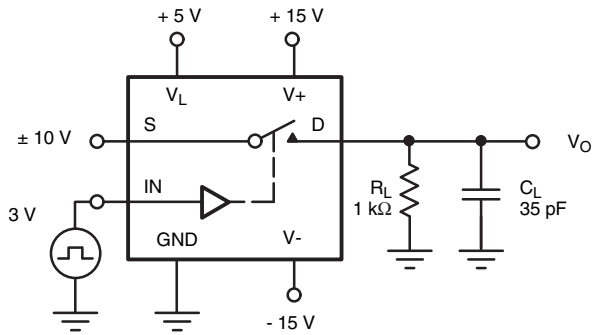
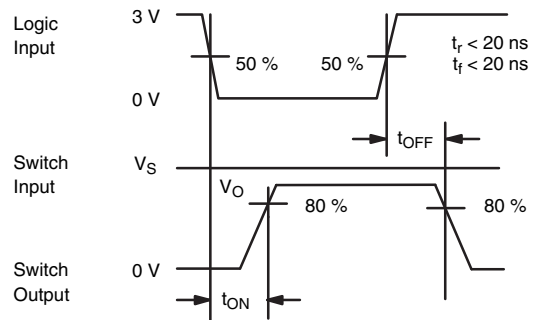


Figure 1.

## TEST CIRCUITS



$C_L$  (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG445.

Figure 2. Switching Time

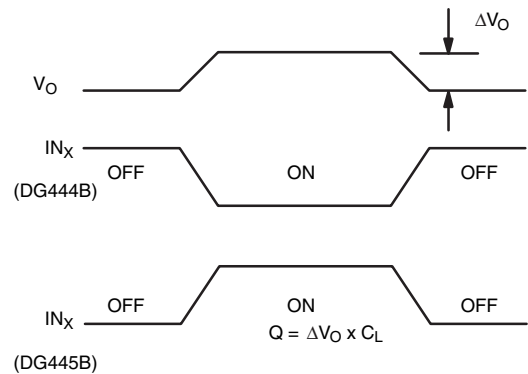
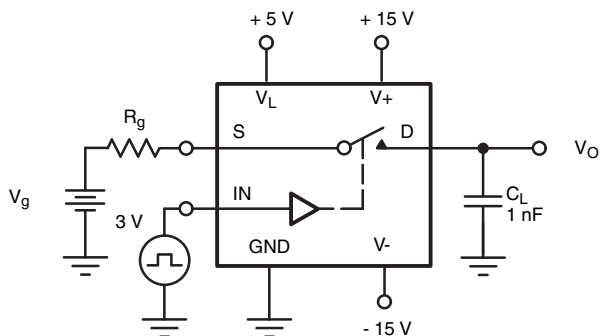


Figure 3. Charge Injection

## TEST CIRCUITS

C = 1 mF tantalum in parallel with 0.01 mF ceramic

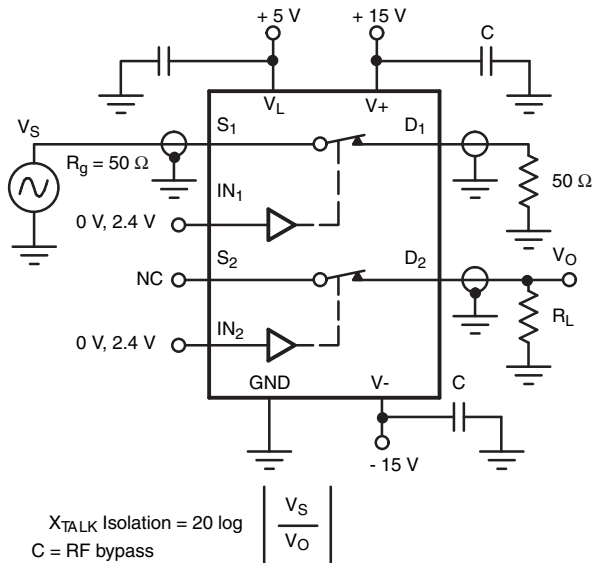


Figure 4. Crosstalk

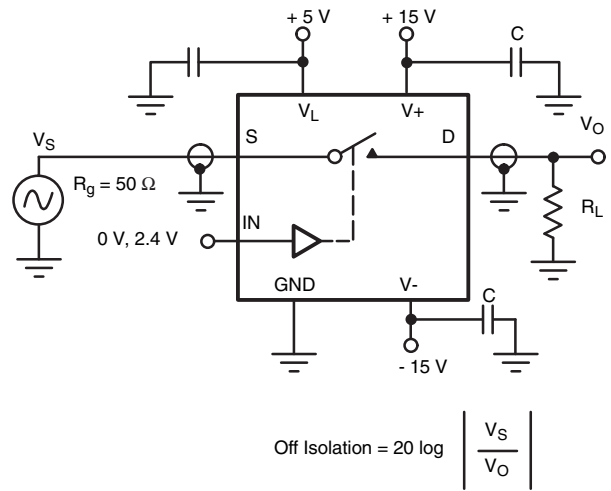


Figure 5. Off Isolation

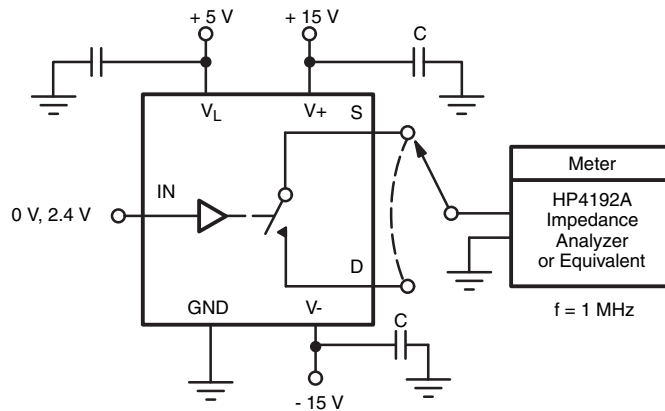


Figure 6. Source/Drain Capacitances

## APPLICATIONS

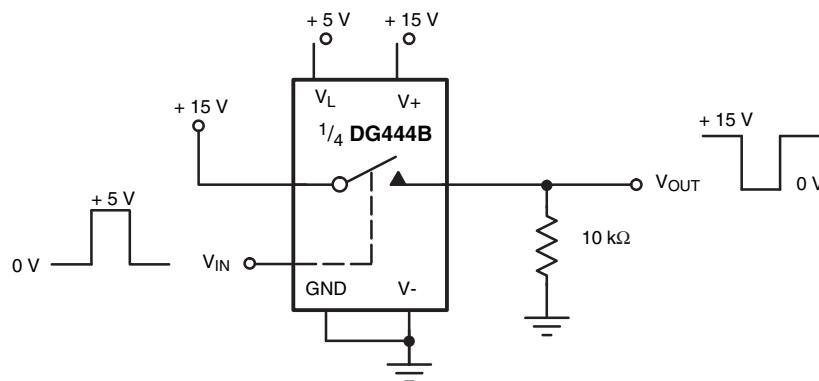


Figure 7. Level Shifter

### APPLICATIONS

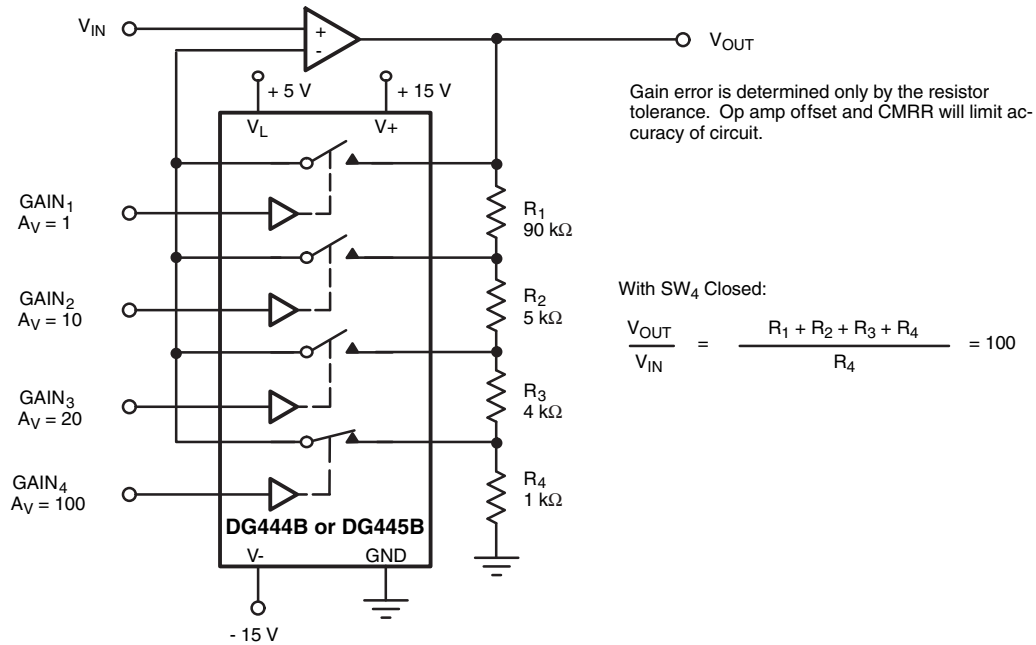


Figure 8. Precision-Weighted Resistor Programmable-Gain Amplifier

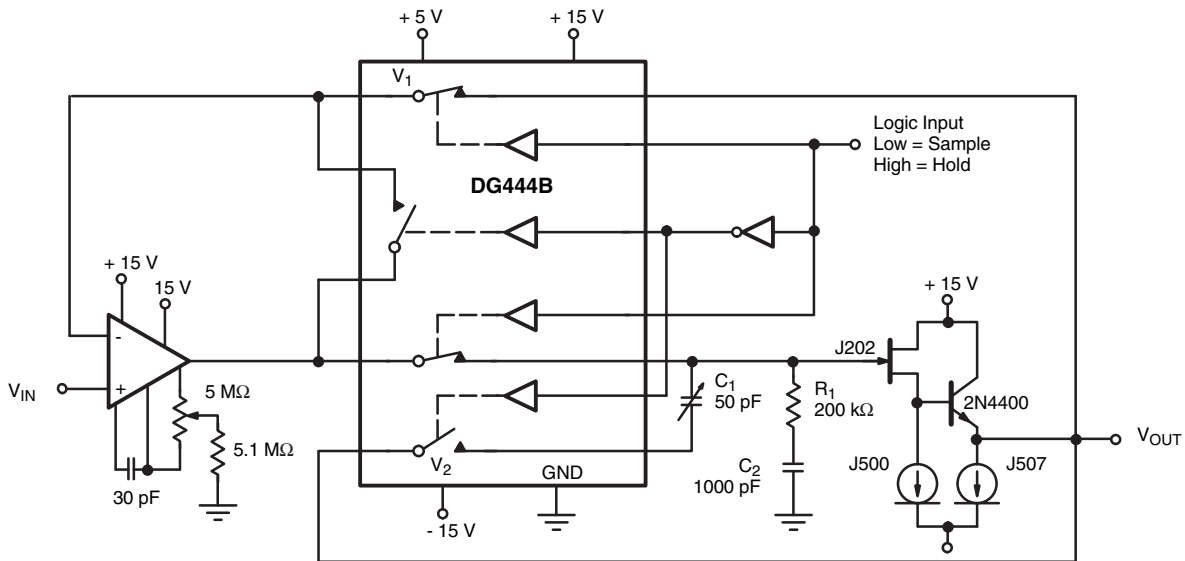


Figure 9. Precision Sample-and-Hold

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?72626](http://www.vishay.com/ppg?72626).





**SOIC (NARROW): 16-LEAD**  
JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01  
DWG: 5300



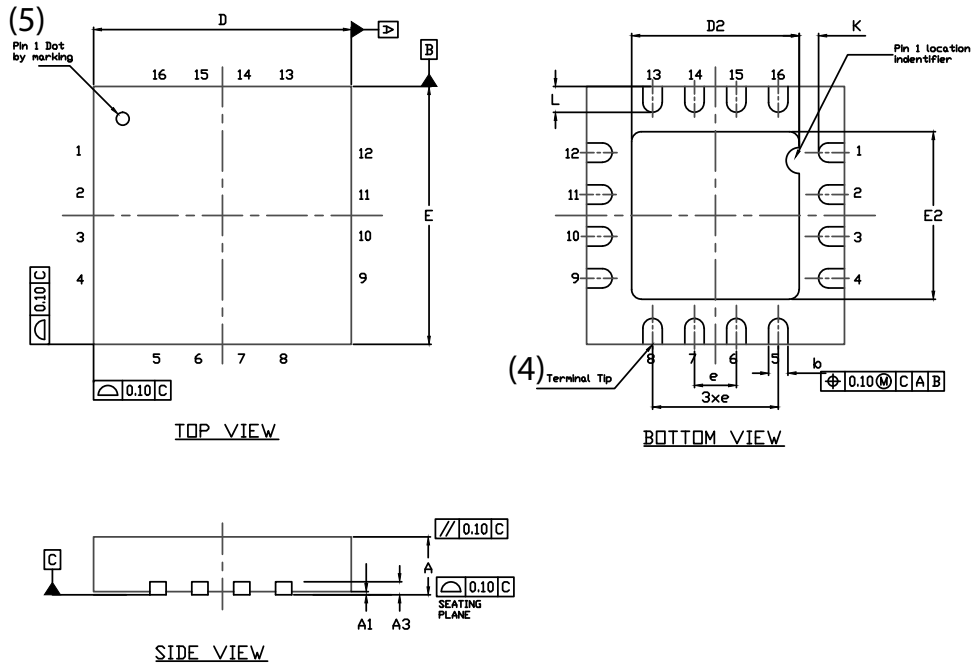
### PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.150	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	18.93	21.33	0.745	0.840
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	5.59	7.11	0.220	0.280
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>Q<sub>1</sub></b>	1.27	2.03	0.050	0.080
<b>S</b>	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01  
DWG: 5482

### QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS <sup>(1)</sup>			INCHES			MILLIMETERS <sup>(1)</sup>			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N <sup>(3)</sup>	16			16			16			16		
Nd <sup>(3)</sup>	4			4			4			4		
Ne <sup>(3)</sup>	4			4			4			4		

**Notes**

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: S13-0893-Rev. B, 22-Apr-13  
 DWG: 5890

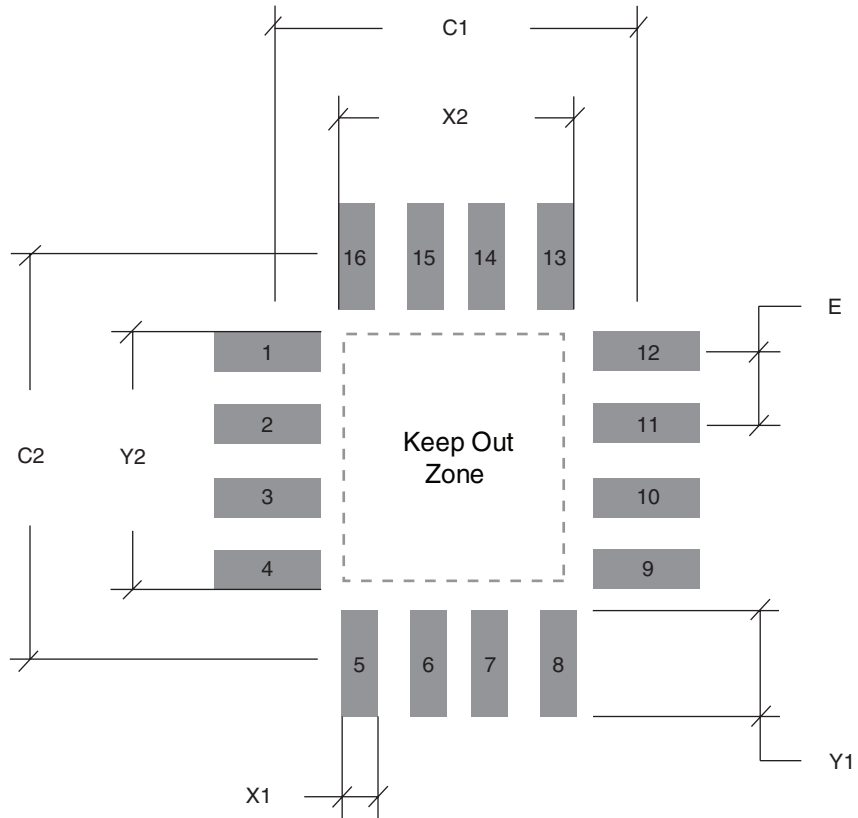
## RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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**RECOMMENDED MINIMUM PADS FOR QFN-16 (4 x 4 MM BODY)**



	Inches	Millimeters
C1	0.142	3.60
C2	0.142	3.60
E	0.026	0.65
X1	0.014	0.35
X2	0.089	2.25
Y1	0.037	0.95
Y2	0.089	2.25

Note:  
QFN-16 (4 x 4) has an exposed center pad that must not come into contact with any metalized structure on the PCB. This area is considered a Keep Out Zone.



## Disclaimer

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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