

# Am29C821/Am29C823 Am29C921/Am29C923

## High-Performance CMOS Bus Interface Registers

Am29C821/Am29C823  
Am29C921/Am29C923

### DISTINCTIVE CHARACTERISTICS

- High-speed parallel positive edge-triggered registers with D-type flip-flops
  - CP-Y propagation delay = 8 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- $I_{OL} = 24$  mA, Commercial and Military
- Extra-wide (9- and 10-bit) data paths
- Am29C900 DIP pinout option reduces lead inductance on  $V_{CC}$  and GND pins

### GENERAL DESCRIPTION

The Am29C821 and Am29C823 CMOS Bus Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800 registers are produced with AMD's exclusive CS-11 CMOS process, and feature typical propagation delays of 8 ns, as well as an output current drive of 24 mA.

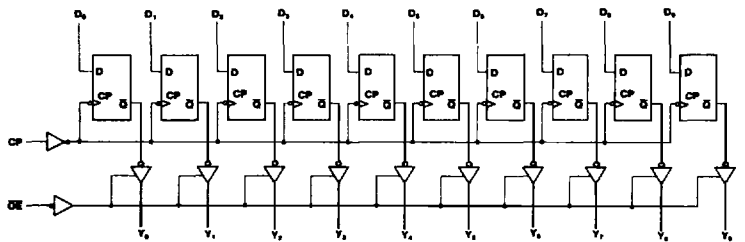
The Am29C821 is a buffered, 10-bit version of the popular '374/'534 function. The Am29C823 is a 9-bit buffered

register with Clock Enable ( $\overline{EN}$ ) and Clear ( $\overline{CLR}$ ) — ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C821 and Am29C823 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpaks. In addition, a DIP pinout option, featuring center  $V_{CC}$  and GND pins, reduces the lead inductance of the  $V_{CC}$  and GND pins. The ordering part numbers for CMOS registers with this pinout are the Am29C921 and Am29C923; their pinouts are shown later in this data sheet.

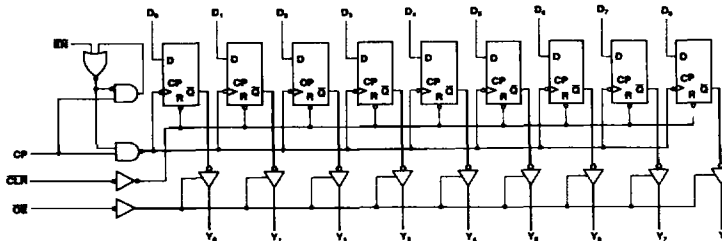
### BLOCK DIAGRAMS

**Am29C821**



BD005471

**Am29C823**



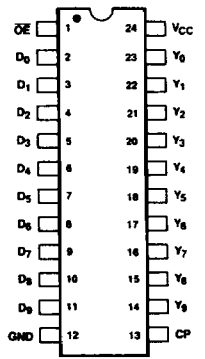
BD005481

Publication #	Rev.	Amendment
07135	C	/0
Issue Date: January 1983		

CONNECTION DIAGRAMS  
Top View

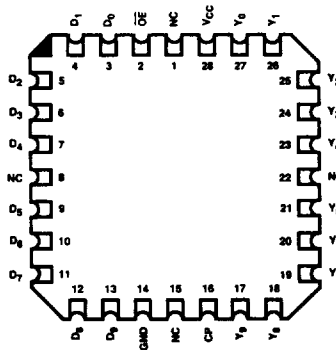
Am29C821

DIPs\*



CD001360

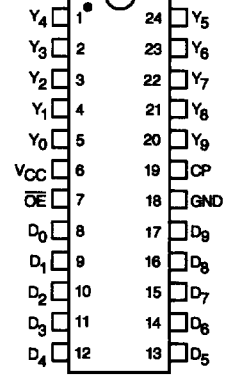
LCC\*\*



CD001370

Am29C921

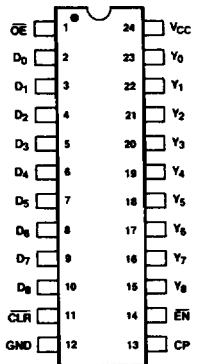
DIPs



CD010716

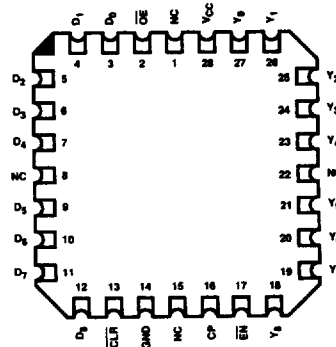
Am29C823

DIPs\*



CD001220

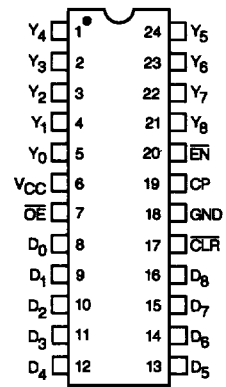
LCC\*\*



CD001230

Am29C923

DIPs



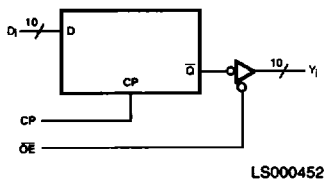
CD010717

\*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.

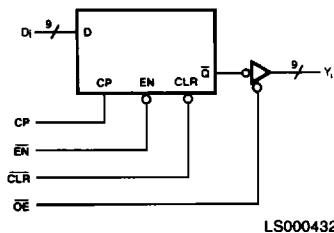
\*\*Also available in 28-Pin PLCC; pinout identical to LCC.

## LOGIC SYMBOLS

**Am29C821**



**Am29C823**



## FUNCTION TABLES

**Am29C821**

Inputs			Internal	Outputs	Function
OE	D <sub>1</sub>	CP	Q <sub>i</sub>	Y <sub>1</sub>	
H	L	↑	H	Z	Hi-Z
H	H	↑	L	Z	
L	L	↑	H	L	Load
L	H	↑	L	H	

**Am29C823**

Inputs					Internal	Outputs	Function
OE	CLR	EN	D <sub>1</sub>	CP	Q <sub>i</sub>	Y <sub>1</sub>	
H	H	L	L	↑	H	Z	Hi-Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	L	
L	H	L	H	↑	L	H	

H = HIGH  
L = LOW  
X = Don't Care

NC = No Change  
↑ = LOW-to-HIGH Transition  
Z = High Impedance

## ORDERING INFORMATION Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM29C821

P

C

B

**e. OPTIONAL PROCESSING**  
Blank = Standard processing  
B = Burn-in

**d. TEMPERATURE RANGE**  
C = Commercial (0 to +70°C)  
E = Extended Commercial (-55 to +125°C)

**c. PACKAGE TYPE**  
P = 24-Pin Slim Plastic DIP (PD3024)  
D = 24-Pin Slim Ceramic DIP (CD3024)  
S = 24-Pin Plastic Small Outline Package (SO 024)  
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)  
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

**b. SPEED OPTION**  
Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**  
Am29C821 CMOS 10-Bit Register  
Am29C823 CMOS 9-Bit Register  
Am29C921 CMOS 10-Bit Register (Center-V<sub>CC</sub>-and-GND Pinout)  
Am29C923 CMOS 9-Bit Register (Center-V<sub>CC</sub>-and-GND Pinout)

Valid Combinations	
AM29C821	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C823	
AM29C921	PC, PCB, DC, DCB, DE
AM29C923	

### Valid Combinations

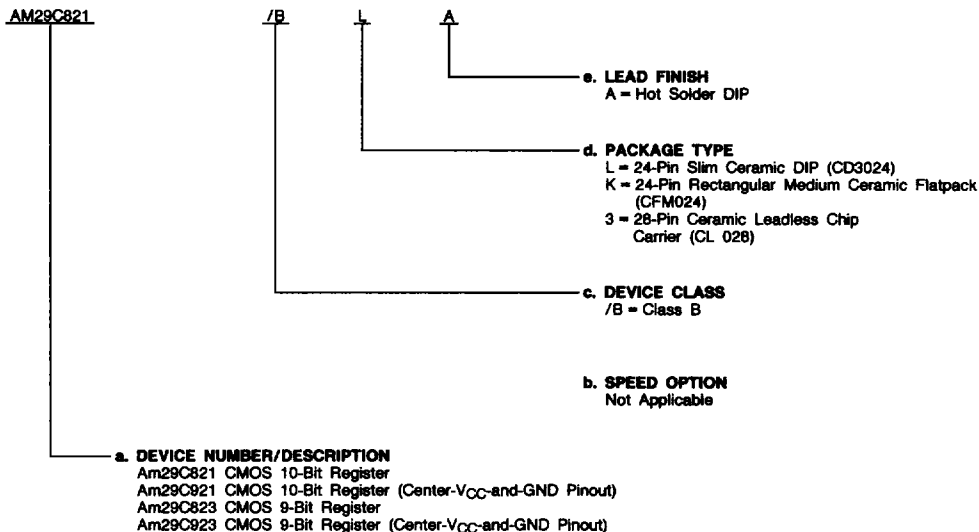
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION (Cont'd.)

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM29C821	/BLA, /BKA, /B3A
AM29C823	
AM29C921	/BLA
AM29C923	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### Am29C821/Am29C823

#### **D<sub>i</sub> Data Input (Input)**

D<sub>i</sub> are the register data inputs.

#### **CP Clock Pulse (Input, LOW-to-HIGH Transition)**

Clock Pulse is the clock input for the registers. Data is entered into the registers on the LOW-to-HIGH transitions.

#### **Y<sub>i</sub> Data Outputs (Output)**

Y<sub>i</sub> are the three-state outputs.

#### **OE Output Enable (Input, Active LOW)**

When the OE input is HIGH, the Y<sub>i</sub> outputs are in the high-impedance state. When OE is LOW, the register data is present at the Y<sub>i</sub> outputs.

### Am29C823 only:

#### **EN Clock Enable (Input, Active LOW)**

When EN is LOW, data on the D<sub>i</sub> inputs are transferred to the Q<sub>i</sub> outputs on the LOW-to-HIGH clock transition. When EN is HIGH, the Q<sub>i</sub> outputs do not change state, regardless of the data or clock input transitions.

#### **CLR Clear (Input, Active LOW)**

When CLR is LOW, the internal register is cleared. When CLR is LOW and OE is LOW, the Q<sub>i</sub> outputs are HIGH. When CLR is HIGH, data can be entered into the register.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65 to +150°C
Supply Voltage to Ground Potential	
Continuous .....	-0.5 V to +7.0 V
DC Output Voltage.....	-0.5 V to $V_{CC} + 0.5$ V
DC Input Voltage.....	-0.5 V to $V_{CC} + 0.5$ V
DC Output Diode Current: Into Output.....	+50 mA
Out of Output .....	-50 mA
DC Input Diode Current: Into Input.....	+20 mA
Out of Input .....	-20 mA
DC Output Current per Pin: $I_{Sink}$ .....	+48 mA (2 x $I_{OL}$ )
$I_{Source}$ .....	-30 mA (2 x $I_{OH}$ )
Total DC Ground Current (n x $I_{OL}$ + m x $I_{CCT}$ ) mA (Note 1)	
Total DC $V_{CC}$ Current .... (n x $I_{OH}$ + m x $I_{CCT}$ ) mA (Note 1)	

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Commercial (C) Devices	
Temperature ( $T_A$ ).....	0 to +70°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V
Military (M) and Extended Commercial (E) Devices	
Temperature ( $T_A$ ).....	-55 to +125°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.






**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 4.5$ V $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -15$ mA	2.4		Volts	
$V_{OL}$	Output LOW Voltage	$V_{CC} = 4.5$ V $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 24$ mA		0.5	Volts	
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)		2.0		Volts	
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)			0.8	Volts	
$V_I$	Input Clamp Voltage	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA			-1.2	Volts	
$I_{IL}$	Input LOW Current	$V_{CC} = 5.5$ V, $V_{IN} = GND$			-10	$\mu$ A	
		$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V			-5		
$I_{IH}$	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 2.7$ V			5	$\mu$ A	
		$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V			10		
$I_{OZH}$	Output Off-State Current (High Impedance)	$V_{CC} = 5.5$ V, $V_O = 5.5$ V or 2.7 V (Note 3)			+10	$\mu$ A	
$I_{OZL}$		$V_{CC} = 5.5$ V, $V_O = 0.4$ V or GND (Note 3)			-10		
$I_{SC}$	Output Short-Circuit Current	$V_{CC} = 5.5$ V, $V_O = 0$ V (Note 4)		-60		mA	
$I_{CCQ}$	Static Supply Current	$V_{CC} = 5.5$ V Outputs Open	$V_{IN} = V_{CC}$ or GND	MIL		160	$\mu$ A
				COM'L		120	
$I_{CCT}$			$V_{IN} = 3.4$ V	Data Input		1.5	mA/Bit
		$\overline{OE}$ , CLR, CP, EN		3.0			
$I_{CCD}^\dagger$	Dynamic Supply Current	$V_{CC} = 5.5$ V (Note 5)			275	$\mu$ A/MHz/Bit	

- Notes: 1. n = number of outputs, m = number of inputs.  
 2. Input thresholds are tested in combination with other DC parameters or by correlation.  
 3. Off-state currents are only tested at worst-case conditions of  $V_{OUT} = 5.5$  V or 0.0 V.  
 4. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.  
 5. Measured at a frequency  $\leq 10$  MHz with 50% duty cycle.

† Not included in Group A tests.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL		MILITARY		Units	
			Min.	Max.	Min.	Max.		
t <sub>PLH</sub>	Propagation Delay Clock to Y <sub>i</sub> (OE = LOW)	C <sub>L</sub> = 50 pF R <sub>1</sub> = 500 Ω R <sub>2</sub> = 500 Ω		12		14	ns	
t <sub>PHL</sub>				12		14	ns	
t <sub>S</sub>	Data to CP Setup Time		4		6		ns	
t <sub>H</sub>	Data to CP Hold Time		2		3		ns	
t <sub>S</sub>	Enable (EN  ) to CP Setup Time		4		6		ns	
t <sub>S</sub>	Enable (EN  ) to CP Setup Time		4		6		ns	
t <sub>H</sub>	Enable (EN) Hold Time		2		3		ns	
t <sub>PHL</sub>	Propagation Delay, Clear to Y <sub>i</sub>			13		15	ns	
t <sub>REC</sub>	Clear (CLR  ) to CP Setup Time		4		6		ns	
t <sub>PWH</sub>	Clock Pulse Width		HIGH	7		11		ns
t <sub>PWL</sub>			LOW	7		11		ns
t <sub>PWL</sub>	Clear Pulse Width		LOW	7		11		ns
t <sub>ZH</sub>			Output Enable Time OE  ) to Y <sub>i</sub>		12		14	ns
t <sub>ZL</sub>				12		14	ns	
t <sub>HZ</sub>	Output Disable Time OE  ) to Y <sub>i</sub>				12		14	ns
t <sub>LZ</sub>				12		14	ns	

\*See Test Circuit and Waveforms.