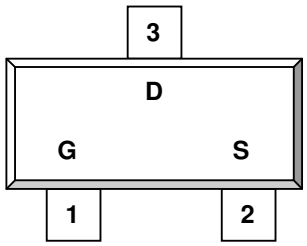
ST3401SRG

DESCRIPTION

ST3401RSG is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION
SOT-23

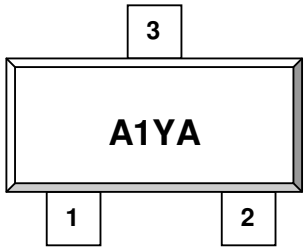


1.Gate 2.Source 3.Drain

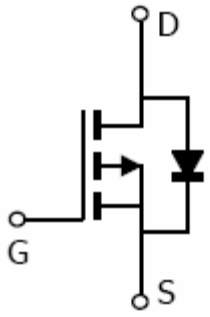
FEATURE

- -30V/-4.0A, $R_{DS(ON)}$ = 55mΩ (Typ.)
  @V_{GS} = -10V
- -30V/-3.2A, $R_{DS(ON)}$ = 62mΩ
  @V_{GS} = -4.5V
- -30V/-1.2A, $R_{DS(ON)}$ = 90mΩ
  @V_{GS} = -2.5V
- Super high density cell design for Extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PART MARKING
SOT-23



Y: Year Code A: Process Code



ST3401SRG

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain CurrentTJ=150℃)	T_A=25℃ T_A=70℃	I_D	-4.0 -3.2	A
Pulsed Drain Current		I_{DM}	-15	A
Continuous Source Current (Diode Conduction)		I_S	-1.0	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.20 0.8	W
Operation Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	120	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.4		-1.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	uA
		V_{DS}=-24V,V_{GS}=0V T_J=55℃			-10	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-4.0A V_{GS}=-4.5V,I_D=-3.2A V_{GS}=-2.5V,I_D=-1.2A		55 62 90	61 70 98	mΩ
Forward Transconductance	g_{fs}	V_{DS}=-5V,I_D=-4.0V		10		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A,V_{GS}=0V			-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V V_{GS}=-10V I_D≡-4.0A		14	21	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			3.7		
Input Capacitance	C_{iss}	V_{DS}=-15V V_{GS}=0V F=1MHz		540		pF
Output Capacitance	C_{oss}			131		
Reverse Transfer Capacitance	C_{rss}			105		
Turn-On Time	$t_{d(on)}$ tr	V_{DS}=-15V V_{GS}=-15V I_D=-1A R_L=6Ω R_G=-10Ω		10	15	nS
				15	25	
Turn-Off Time	$t_{d(off)}$ tf			31	50	
				20	30	