DDR SDRAM DIMM MODULE

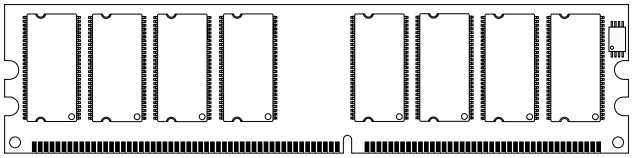
MT8VDDT1664A - 128MB

For the latest data sheet, please refer to the Micron Web site: www.micron.com/moduleds

FEATURES

- 184-pin dual in-line memory module (DIMM)
- Fast data transfer rates PC3200
- Utilizes 400 MT/s DDR SDRAM components
- 128MB (16 Meg x 64)
- V_{DD}= V_{DD}Q= +2.65V ±0.10V
- V_{DDSPD} = +2.3V to +3.6V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Gold-plated edge contacts

184-Pin DIMM
MO-206



OPTIONS — MARKING

- Package
  - Unbuffered — A
  - 184-pin DIMM (gold) — G
- Memory Clock/Speed, CAS Latency
  - 5ns (200 MHz), 400 MT/s, CL = 3 — -403

ADDRESS TABLE

	128MB
Refresh Count	4K
Row Addressing	4K (A0–A11)
Device Bank Addressing	4 (BA0, BA1)
Device Configuration	16 Meg x 8
Column Addressing	1K (A0–A9)
Module Bank Addressing	1 (S0#)

PART NUMBERS AND TIMING PARAMETERS

PART NUMBER	PART MARKING	MODULE DENSITY	CONFIGURATION	MODULE BANDWITH	MEMORY CLOCK/ DATA RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT8VDDT1664AG-403_	-403	128MB	16 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-4-4

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8VDDT1664AG-403A1

‡THIS DATA SHEET CONTAINS THE PRESENT DESCRIPTION OF A PRODUCT IN DEFINITION WITH NO FORMAL DESIGN IN PROGRESS.

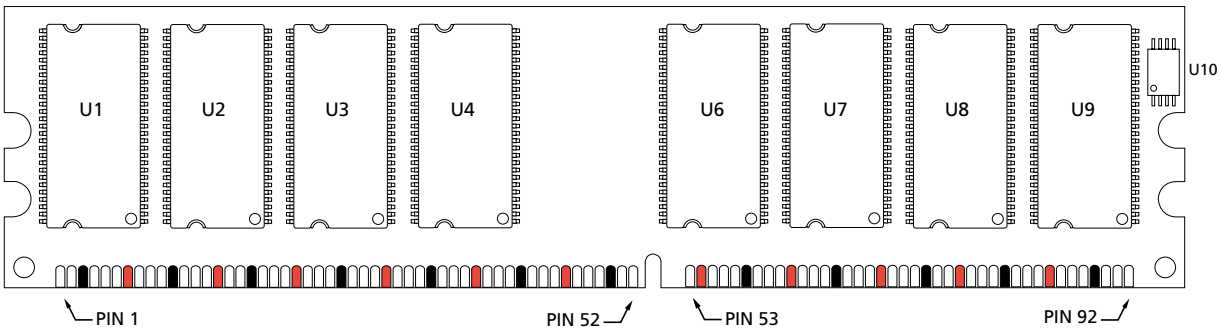
Pin Assignment (184-Pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DNU	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	DNU	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	DNU	74	VSS
6	DQ2	29	A7	52	BA1	75	CK2#
7	VDD	30	VDDQ	53	DQ32	76	CK2
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ
9	NC	32	A5	55	DQ33	78	DQS6
10	NC	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	CK1	39	DQ26	62	VDDQ	85	VDD
17	CK1#	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	DNU	67	DQS5	90	NC
22	VDDQ	45	DNU	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

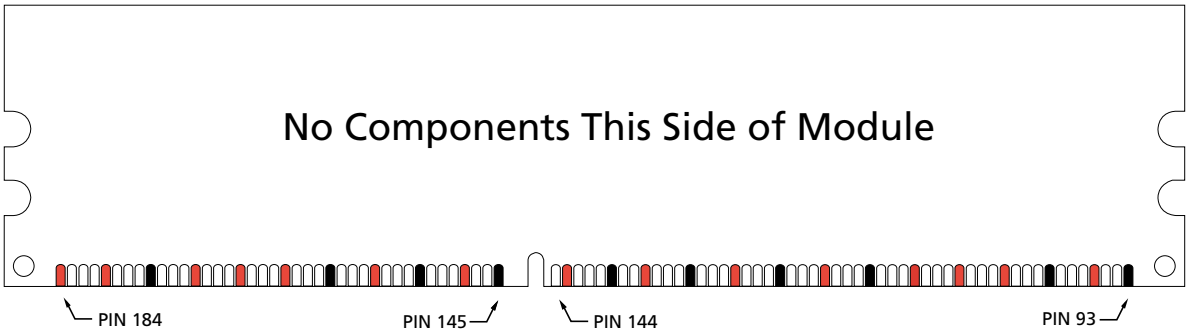
PIN ASSIGNMENT (184-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DNU	163	NC
95	DQ5	118	A11	141	A10	164	VDDQ
96	VDDQ	119	DQS11/DM2	142	DNU	165	DQ52
97	DQS9/DM0	120	VDD	143	VDDQ	166	DQ53
98	DQ6	121	DQ22	144	DNU	167	NC
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DQS15/DM6
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DQS13/DM4	172	VDD
104	VDDQ	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDDQ	151	DQ39	174	DQ60
106	DQ13	129	DQS12/DM3	152	VSS	175	DQ61
107	DQS10/DM1	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DQS16/DM7
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDDQ	179	DQ63
111	DNU	134	DNU	157	S0#	180	VDDQ
112	VDDQ	135	DNU	158	DNU	181	SA0
113	NC	136	VDDQ	159	DQS14/DM5	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	NC	138	CK0#	161	DQ46	184	VDDSPD

Front View



Back View



Indicates a VDD or VDDQ pin Indicates a VSS pin

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	V_{REF}	Input	SSTL_2 reference voltage.
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S0# and S1#) define the command being entered.
16, 17, 75, 76, 137, 138	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
21	CKE0	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is a SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied.
157	S0#	Input	Chip Select: S0# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S0# is registered HIGH. S0# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 118, 122, 125, 130, 141	A0-A11	Input	Address Inputs: A0-A11 provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
91	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.

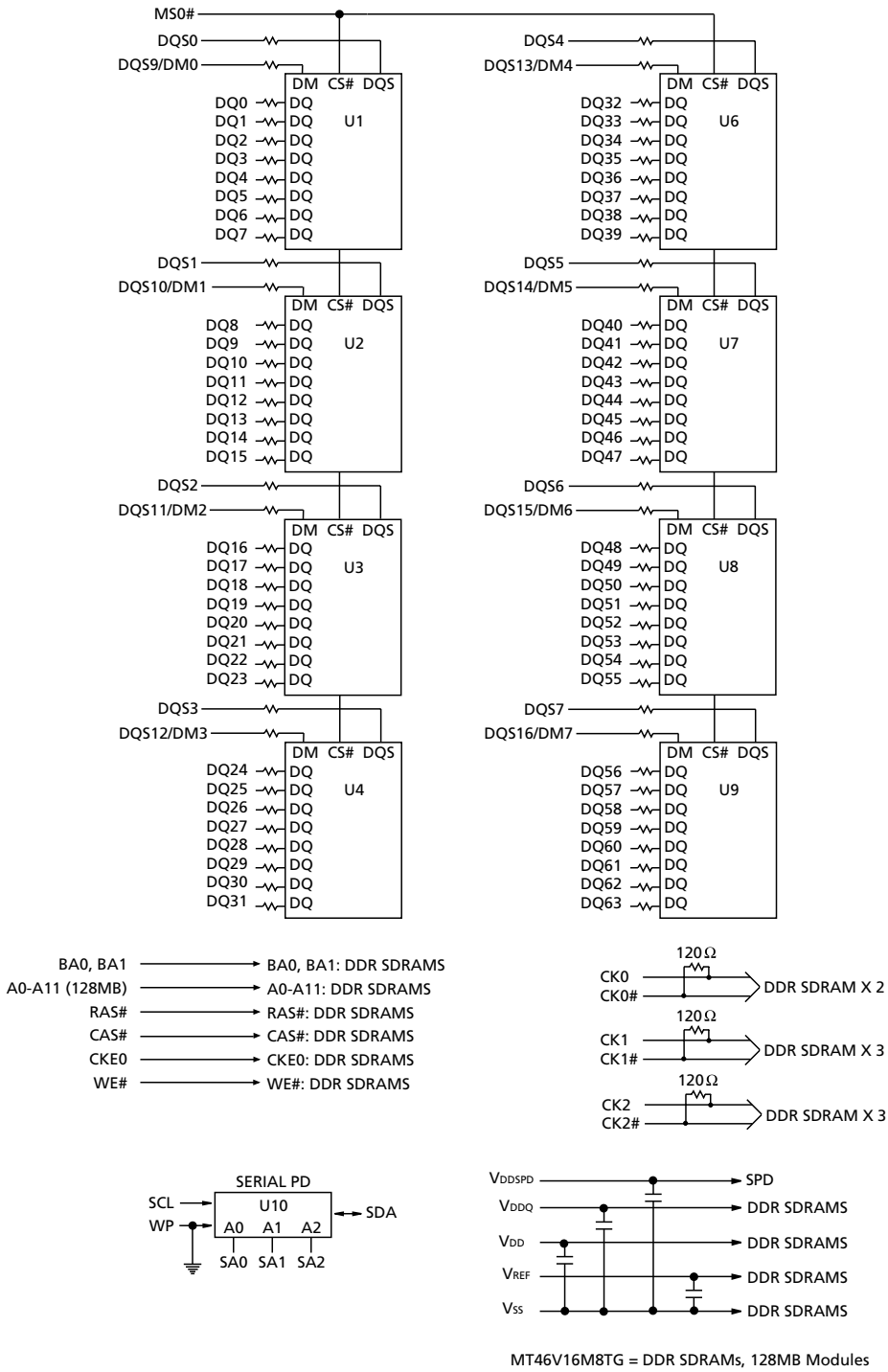
NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number and symbol information.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
181, 182, 183	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
5, 14, 25, 36, 56, 67, 78, 86, 97, 107, 119, 129, 149, 159, 169, 177	DQS0-DQS16	Input/ Output	Data Strobe: DQS0-DQS7, Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data. Data Mask: DQS9-DQS16 function as DM0-DM7 to mask WRITE data when when HIGH.
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	Supply	DQ Power Supply: +2.65V ±0.10V.
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	Supply	Power Supply: +2.65V ±0.10V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	Supply	Ground.
184	V_{DDSPD}	Supply	Serial EEPROM positive power supply, 2.3V to 3.6V.
9, 10, 71, 82, 90, 101, 102, 103, 113, 115, 163, 167, 173	NC	—	No Connect: These pins should be left unconnected.
44, 45, 47, 49, 51, 111, 134, 135, 140, 142, 144, 158	DNU	—	Do Not Use: These pins are not connected on this module but are assigned pins on other modules in this product family.

NOTE: Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables for pin number and symbol information.

FUNCTIONAL BLOCK DIAGRAM



MT46V16M8TG = DDR SDRAMs, 128MB Modules

NOTE: 1. All resistor values are 22 ohms unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.
3. To optimize system and loading and signal integrity for -403 speed grade modules, 3Ω (single bank modules) or 5Ω (dual bank modules) stub resistors may be placed on command/address and control lines. Contact Micron CCG Applications for additional information.

GENERAL DESCRIPTION

The MT8VDDT1664A is a high-speed CMOS, dynamic random-access, 128MB memory module organized in a x64 configuration. This module uses internally configured quad-bank DDR SDRAM devices.

This DDR SDRAM module uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

This DDR SDRAM module operates from multiple differential clocks (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM module is burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select devices bank; A0-A11 select device row). The address bits registered coincident with the READ or WRITE command (A0-A9) are used to select the device bank and the starting device column location for the burst access.

These DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 128Mb and 256Mb DDR SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

REGISTER DEFINITION

MODE REGISTER

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in the Mode Register Diagram. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A11 specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

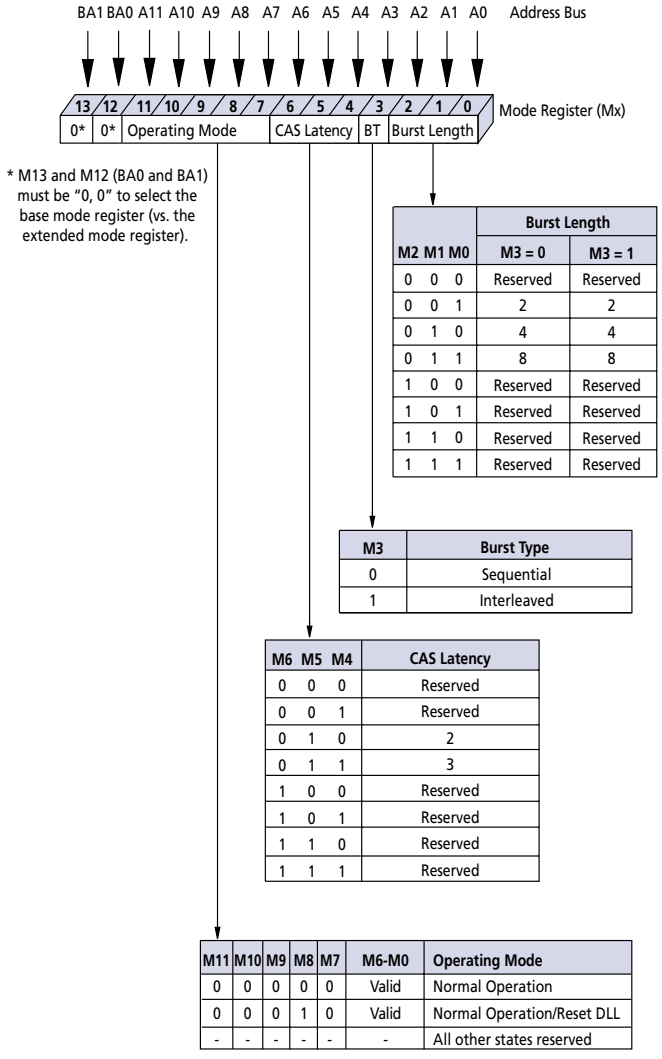
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A11 when the burst length is set to two, by A2-A11 when the burst length is set to four and by A3-A11 when the burst length is set to eight (where A11 is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition Table.

Mode Register Definition Diagram



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	Valid	Normal Operation
0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	All other states reserved

Burst Definition Table

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:
1. For a burst length of two, A1-A11 select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A11 select the four-data-element block; A0-A1 select the first access within the block.
3. For a burst length of eight, A3-A11 select the eight-data-element block; A0-A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

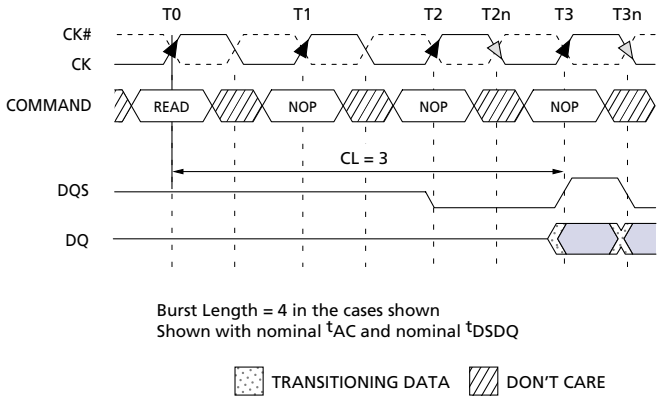
Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency should be set to 3 clocks, as shown in CAS Latency Diagram and the Mode Register Definition Diagram.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latency Diagram



CAS Latency (CL) Table

	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)
SPEED	CL = 3
-403	200

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7-A11 (for the 128MB), or A7-A12 (for the 256MB module) each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9-A11 (for 128MB module), or A7 and A9-A12 (for 256MB module) each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7-A11, or A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

EXTENDED MODE REGISTER

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, and QFC#. These functions are controlled via the bits shown in the Extended Mode Register Definition Diagram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

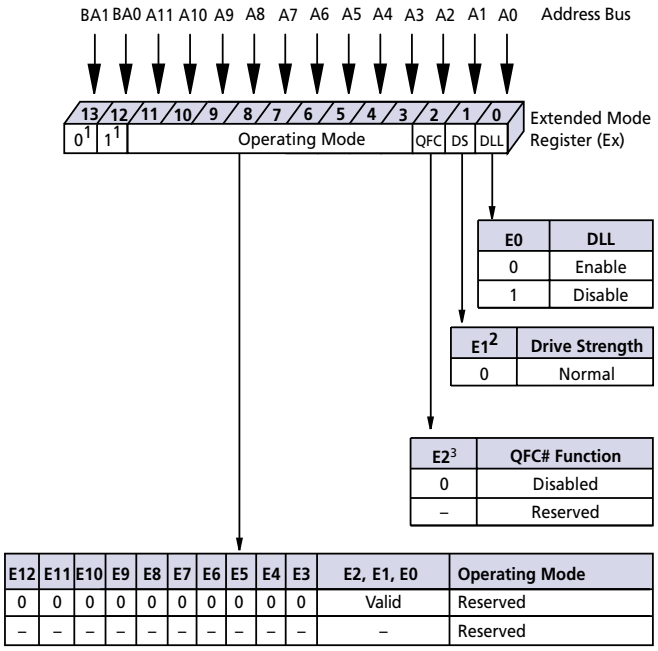
Output Drive Strength

The normal full drive strength for all outputs is specified to be SSTL2, Class II. For detailed information on output drive strength option, refer to the 128Mb DDR SDRAM data sheet.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Extended Mode Register Definition Diagram



NOTE: 1. E13 and E12 (BA1 and BA0) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

COMMANDS

The Truth Tables below provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb DDR SDRAM data sheet.

TRUTH TABLE – COMMANDS

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

TRUTH TABLE – DM OPERATION

(Note: 10)

NAME (FUNCTION)	DM	DQ
WRITE Enable	L	Valid
WRITE Inhibit	H	X

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A11 provide the op-code to be written to the selected mode register.
3. BA0-BA1 provide device bank address and A0-A11 provide device row address.
4. BA0-BA1 provide device bank address; A0-A9 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls device row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write data; provided coincident with the corresponding data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} ..... -1V to +3.6V
Voltage on $V_{DD}Q$ Supply
Relative to V_{SS} ..... -1V to +3.6V
Voltage on V_{REF} and Inputs
Relative to V_{SS} ..... -1V to +3.6V
Voltage on I/O Pins
Relative to V_{SS} ..... -0.5V to $V_{DD}Q$ +0.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Refer to standard 128Mb DDR SDRAM data sheet for full functionality and notes)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.65V ±0.10V, $V_{DD}Q$ = +2.65V ±0.10V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{DD}	2.45	2.75	V
I/O Supply Voltage		$V_{DD}Q$	2.45	2.75	V
I/O Reference Voltage		V_{REF}	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V
I/O Termination Voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V
Input High (Logic 1) Voltage		V_{IH}(DC)	V_{REF} + 0.15	V_{DD} + 0.3	V
Input Low (Logic 0) Voltage		V_{IL}(DC)	-0.3	V_{REF} - 0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Command/ Address, S0#, CKE0	I_I	-16	16	µA
	CK1, CK1#, CK2,CK2#	I_I	-6	6	µA
	CK0, CK0#	I_I	-4	4	µA
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)		I_{OZ}	-5	5	µA
OUTPUT LEVELS: High Current (V_{OUT} = $V_{DD}Q$-0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	-16.8	–	mA
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA

AC INPUT OPERATING CONDITIONS

(Refer to standard 128Mb DDR SDRAM data sheet for full functionality and notes)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.65V ±0.10V, $V_{DD}Q$ = +2.65V ±0.10V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.310	–	V
Input Low (Logic 0) Voltage	V_{IL}(AC)	–	V_{REF} - 0.310	V
I/O Reference Voltage	V_{REF}(AC)	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS*

(Refer to standard 128Mb DDR SDRAM data sheet for full functionality and notes)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.65V ±0.10V, $V_{DD}Q$ = +2.65V ±0.10V)

AC CHARACTERISTICS			-403		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**UNITS**
Access window of DQs from CK/CK#		^tAC	-0.60	+0.60	ns
CK high-level width		^tCH	0.45	0.55	^tCK
CK low-level width		^tCL	0.45	0.55	^tCK
Clock cycle time	CL = 3	^tCK (3)	5	5	ns
DQ and DM input hold time relative to DQS		^tDH	0.45		ns
DQ and DM input setup time relative to DQS		^tDS	0.45		ns
DQ and DM input pulse width (for each input)		^tDIPW	1.4		ns
Access window of DQS from CK/CK#		^tDQSCK	-0.50	+0.50	ns
DQS input high pulse width		^tDQSH	0.40		^tCK
DQS input low pulse width		^tDQSL	0.40		^tCK
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.35	ns
Write command to first DQS latching transition		^tDQSS	0.75	1.25	^tCK
DQS falling edge to CK rising - setup time		^tDSS	0.22		^tCK
DQS falling edge from CK rising - hold time		^tDSH	0.22		^tCK
Half clock period		^tHP	^tCH, ^tCL		ns
Data-out high-impedance window from CK/CK#		^tHZ		+0.60	ns
Data-out low-impedance window from CK/CK#		^tLZ	-0.60		ns
Address and control input hold time (fast slew rate)		^tIH_F	0.75		ns
Address and control input setup time (fast slew rate)		^tIS_F	0.75		ns
Address and control input hold time (slow slew rate)		^tIH_S	na		ns
Address and control input setup time (slow slew rate)		^tIS_S	na		ns
LOAD MODE REGISTER command cycle time		^tMRD	10		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP-^tQHS		ns
Data hold skew factor		^tQHS		0.50	ns
ACTIVE to PRECHARGE command		^tRAS	40	70,000	ns
ACTIVE to READ with auto precharge command		^tRAP	15		ns
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	60		ns
AUTO REFRESH command period		^tRFC	70		ns
ACTIVE to READ or WRITE delay		^tRCD	20		ns
PRECHARGE command period		^tRP	20		ns
DQS read preamble		^tRPRE	0.9	1.1	^tCK
DQS read postamble		^tRPST	0.4	0.6	^tCK
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	10		ns
DQS write preamble		^tWPRE	0.25		^tCK
DQS write preamble setup time		^tWPRES	0		ns
DQS write postamble		^tWPST	0.4	0.6	^tCK
Write recovery time		^tWR	15		ns
Internal WRITE to READ command delay		^tWTR	2		^tCK

* Module AC timing parameters comply with PC3200 design specifications, based on DDR SDRAM component performance parameters.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS*

(Refer to standard 128Mb DDR SDRAM data sheet for full functionality and notes)
(0°C ≤ T_A ≤ +70°C; V_{DD} = +2.65V ±0.10V, $V_{DD}Q$ = +2.65V ±0.10V)

AC CHARACTERISTICS		-403		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**
Data valid output window	na	^{t}QH - ^{t}DQSQ		ns
REFRESH to REFRESH command interval	^{t}REFC		140.6	µs
Average periodic refresh interval	^{t}REFI		15.6	µs
Terminating voltage delay to V_{DD}	^{t}VTD	0		ns
Exit SELF REFRESH to non-READ command	^{t}XSNR	75		ns
Exit SELF REFRESH to READ command	^{t}XSRD	200		^{t}CK

* Module AC timing parameters comply with PC3200 design specifications, based on DDR SDRAM component performance parameters.

CAPACITANCE (All Modules)

(Refer to standard 128Mb DDR SDRAM data sheet for full functionality and notes)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C_{IO}	4.0	5.0	pF
Input Capacitance: Command and Address, S0#	C_{I1}	16.0	24.0	pF
Input Capacitance: CK0, CK0#	C_{I2_a}	4.0	6.0	pF
Input Capacitance: CK1, CK1#; CK2, CK2#	C_{I2_b}	6.0	9.0	pF
Input Capacitance: CKE0	C_{I3}	16.0	24.0	pF

SERIAL PRESENCE-DETECT MATRIX

(Note: 1)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8VDDT1664A
0	NUMBER OF BYTES USED BY MICRON	128	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08
2	MEMORY TYPE	SDRAM DDR	07
3	NUMBER OF ROW ADDRESSES	12 or 13	0C
4	NUMBER OF COLUMN ADDRESSES	10	0A
5	NUMBER OF BANKS	1	01
6	MODULE DATA WIDTH	64	40
7	MODULE DATA WIDTH (continued)	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	SSTL 2.5V	04
9	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 3)	5ns	50
10	SDRAM ACCESS FROM CLOCK, ^{t}AC (CAS LATENCY = 3)	0.60ns	60
11	MODULE CONFIGURATION TYPE	None	00
12	REFRESH RATE/TYPE	15.6µs/SELF	80
13	SDRAM WIDTH (PRIMARY SDRAM)	8	08
14	ERROR-CHECKING SDRAM DATA WIDTH	None	00
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	1	01
16	BURST LENGTHS SUPPORTED	2, 4, 8	0E
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04
18	CAS LATENCIES SUPPORTED	2, 2.5	0C
19	CS LATENCY	0	01
20	WE LATENCY	1	02
21	SDRAM MODULE ATTRIBUTES	Diff. CLK input	20
22	SDRAM DEVICE ATTRIBUTES: GENERAL	Fast / Concurrent Auto Precharge	C0
23	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2)	–	00
24	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2)	–	00
25	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 1)	–	00
26	SDRAM ACCESS FROM CK , ^{t}AC (CAS LATENCY = 1)	–	00
27	MINIMUM ROW PRECHARGE TIME, ^{t}RP	20ns	50
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	10ns	28
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD	20ns	50

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

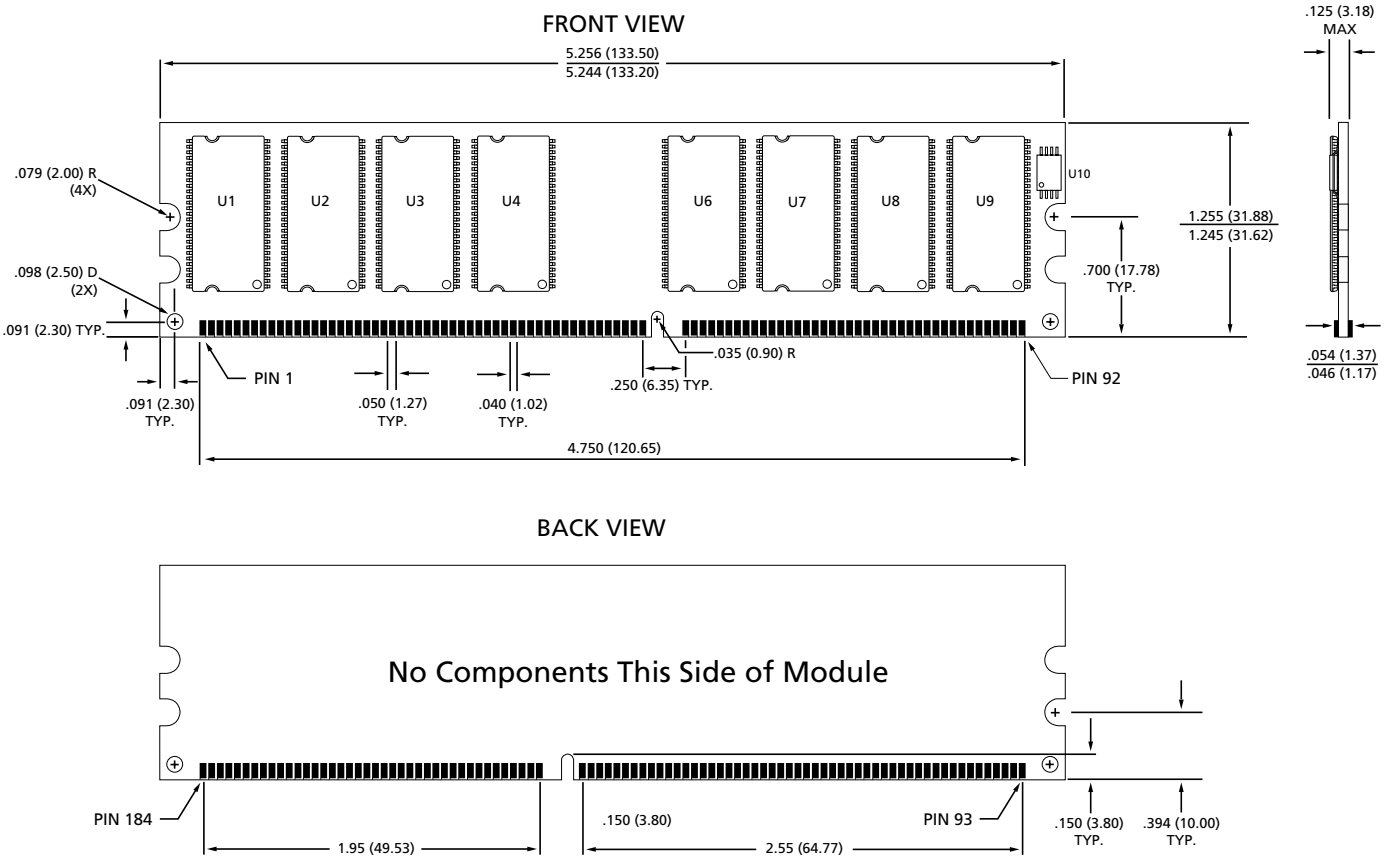
SERIAL PRESENCE-DETECT MATRIX (continued)

(Notes: 1, 2)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8VDDT1664A
30	MINIMUM RAS# PULSE WIDTH, ^{t}RAS	40ns	28
31	MODULE BANK DENSITY	128MB or 256MB	20
32	ADDRESS AND COMMAND SETUP TIME, ^{t}IS [Value set to slow slew rate ($^{t}IS_{S}$)] (Note 3)	0.75ns	75
33	ADDRESS AND COMMAND HOLD TIME, ^{t}IH [Value set to slow slew rate ($^{t}IH_{S}$)] (Note 3)	0.75ns	75
34	DATA/DATA MASK INPUT SETUP TIME, ^{t}DS	0.45ns	45
35	DATA/DATA MASK INPUT HOLD TIME, ^{t}DH	0.45ns	45
36-40	RESERVED		00
41	MINIMUM ACTIVE/AUTO REFRESH TIME,	60ns	3C
42	MINIMUM AUTO REFRESH TO ACTIVE/AUTO REFRESH COMMAND PERIOD, (^{t}RFC)	70ns	46
43	MAXIMUM CYCLE TIME, (^{t}CK (MAX))	5ns	14
44	MAXIMUM DQS-DQ SKEW TIME, (^{t}DQSQ)	0.35ns	23
45	MAXIMUM READ DATA HOLD SKEW	0.50ns	50
46-61	RESERVED	00	00
62	SPD REVISION	Release 0.0	00
63	CHECKSUM FOR BYTES 0-62	-403	B5
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C
65-71	MANUFACTURER'S JEDEC ID CODE	(continued)	FF
72	MANUFACTURING LOCATION	1 - 11	01 - 0B
73-90	MODULE PART NUMBER (ASCII)	x	
91	PCB IDENTIFICATION CODE	1 - 9	01 - 09
92	IDENTIFICATION CODE (continued)	0	00
93	YEAR OF MANUFACTURE IN BCD	x	
94	WEEK OF MANUFACTURE IN BCD	x	
95-98	MODULE SERIAL NUMBER	x	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	–	

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

184-PIN DIMM



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

DATA SHEET DESIGNATION

Preview: This data sheet contains the present description of a products in definition with no formal design in progress.

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