MN3718FT,MN3718AT

6.0mm (type-1/3) 768H CCD Area Image Sensors

■ Overview

The MN3718FT and MN3718AT are 6.0mm (type-1/3) interline transfer CCD (IT-CCD) solid state image sensor devices.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made an exposure time of 1/10000 seconds possible. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

This device has a total of 400,634 pixels (811 horizontal × 494 vertical) and provides stable and clear images with a resolution of 550 horizontal TV-lines and 350 vertical TV-lines.

Part Number	Size	System	Color or B/W			
MN3718FT	(0(1/2)	NTSC	Color			
MN3718AT	6.0mm(type-1/3)	EIA	B/W			

■ Features

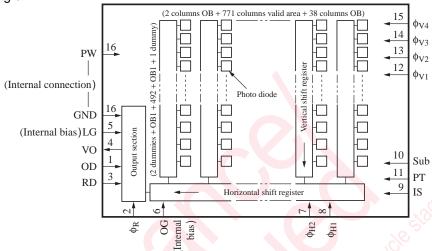
- Total number of pixels: 811 (horizontal) × 494 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter
- No image distortion
- Small size enables design of compact equipment
- · High reliability
- 16-pin DIL plastic package

Applications

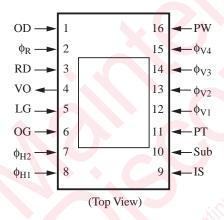
 Compact lightweight camcorders. Cameras for surveillance, measurement, and medical use



■ Block Diagram



■ Pin Assignments



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	11	PT	P-well for protection circuit
2	φ _R	Reset pulse	12	ϕ_{V1}	Vertical shift register
3	RD	Reset drain	J WO		clock pulse 1
4	VO	Video output	13	$\phi_{\mathrm{V}2}$	Vertical shift register
5	LG	Output load transistor gate			clock pulse 2
6	OG	Output gate	14	ф _{V3}	Vertical shift register
7	ф _{H2}	Horizontal register clock pulse 2			clock pulse 3
8	фн1	Horizontal register clock pulse 1	15	ϕ_{V4}	Vertical shift register
9	IS	Horizontal CCD input source			clock pulse 4
10	Sub	Substrate	16	PW	P-well

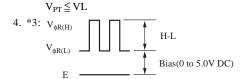
■ Absolute Maximum Ratings and Operating Conditions

Parameter			Rating		Operating condition				
		Symbol	min	max	min	typ	max	Unit	
Reset drain voltage		V_{RD}	- 0.2	18.0	14.5	15.0	15.5	V	
Output drain voltage		V _{OD}	- 0.2	18.0	14.5	15.0	15.5	V	
Output load transistor gate voltage		V_{LG}		Supplied internally					
Output gate volta	ge	V_{OG}		Supplied internally					
Horizontal CCD input s	ource voltage	V _{IS}	- 0.2	18.0	14.5	15.0	15.5	V	
Protection P-well voltage		V _{PT} *2	- 10.0	0.2	φ _{V(L)} - 1.2	φ _{V(L)} - 1.0	φ _{V(L)} - 0.7	V	
P-well voltage		V _{PW}	Referenc	Reference voltage		0	300	V	
Reset	H-L	V _{φR(H-L)} *3		18.0	4.7	5.0	5.3	V	
pulse voltage	Bias	$V_{\phi R(Bias)}$	- 0.2	_	0	Adjust	5.0	V	
Horizontal registe	Horizontal register		-	18.0	4.7	5.0	5.3	V	
clock pulse voltage 1		$V_{\phi H1(L)}$	- 0.2		0 0	0	0		
Horizontal register		V _{ϕH2(H)}	_	18.0	4.7	5.0	5.3	V	
clock pulse voltage 2		$V_{\phi H2(L)}$	- 0.2	— <u>ķ</u> (0	0	0		
Vertical shift register clock pulse voltage 1		V _{\phiV1(H)} *2	_	18.0	14.5	15.0	15.5	Ŷ.	
		V _{\phiV1(M)} *2		10/1/2	-0.2	0	0.2		
		V _{\phiV1(L)} *2	- 9.0	1. 40/1.	- 7.3	7.0	- 6.7		
Vertical shift register		V _{\phi V2(M)} *2	1963	15.0	0.8	1.0	1.2	⊗ v	
clock pulse voltage 2		V _{\phiV2(L)} *2	- 9.0	-	-7.3	- 7.0	- 6.7		
Vertical shift register clock pulse voltage 3		V _{\(\phi\V3(H)\)} *2	, 0	18.0	14.5	15.0	15.5	V	
		V _{\phiV3(M)} *2	19, -10	145	-0.2	000	0.2		
		V _{\$\phi V_3(L)\$} *2	- 9.0	80-05	-7.3	-7.0	- 6.7		
Vertical shift regi	Vertical shift register		90	15.0	0.8	1.0	1.2	V	
clock pulse voltag	clock pulse voltage 4		- 9.0	- 1	- 7.3	- 7.0	- 6.7		
Substrate voltage		$V_{\phi V4(L)}^{*2}$ V_{Sub}^{*1}	- 0.2	45.0	3.0	Adjust	14.5	V	
		φV _{Sub} *4	10	The The	24.5	25.0	25.5		
Operating temper	rature	T_{opr}	- 10	70	_	25	_	°C	
Storage temperature		$T_{\rm stg}$	-30	80	_	_	_	°C	

Note)1. Standard light input defines

Standard light input is the one when the exposure is done at a lens aperture of F8, using a light source of 2856 K and 1050 nt, and placing a color temperature conversion filter LB-40 (HOYA) and an IR cutting filter CAW-500 (t = 2.5 mm) in the light path.

- 2. $^{*}1: V_{Sub}$ internal settings guarantee blooming at 400 times light input of the standard light input.
- 3. *2: V_{PT} is set so that the following conditions are set for VL of the vertical shift clock.



5. *4: V_{Sub} when using electronic shutter function

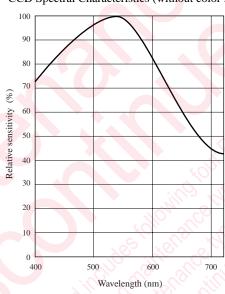


■ Optical Characteristics

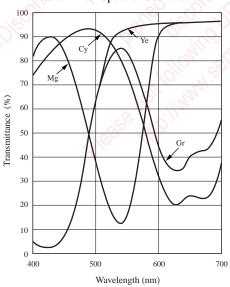
Part Number	Color or	Effe		S/N typ	Saturation output typ	Sensitivity F8 typ	Vertical smear Sm	Image lag typ	Horizontal resolution typ	Vertical resolution typ
	B/W	Н	V	(dB)	(mV)	(mV)	typ(%)	(%)	(TV-lines)	(TV-lines)
MN3718FT	Color	771	492	_	700	300	0.01	_	480	350
MN3718AT	B/W	771	492	_	1,000	350	0.01	_	550	350

■ Graphs of Characteristics

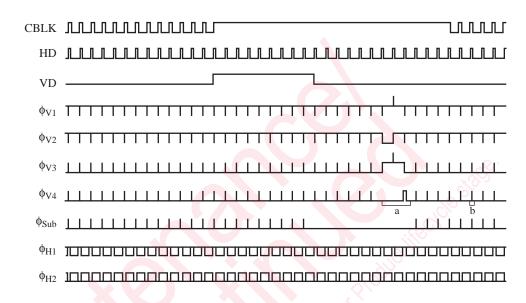
CCD Spectral Characteristics (without color filter)



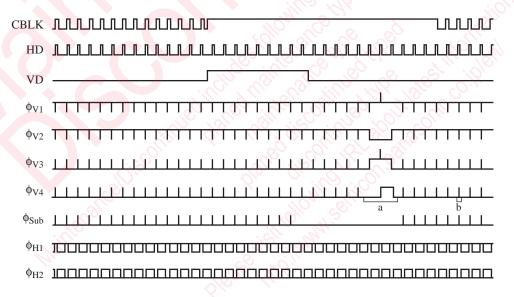
Color Filter Spectral Characteristics



- Timing Diagram
- V Rate timing
 - < Field A >

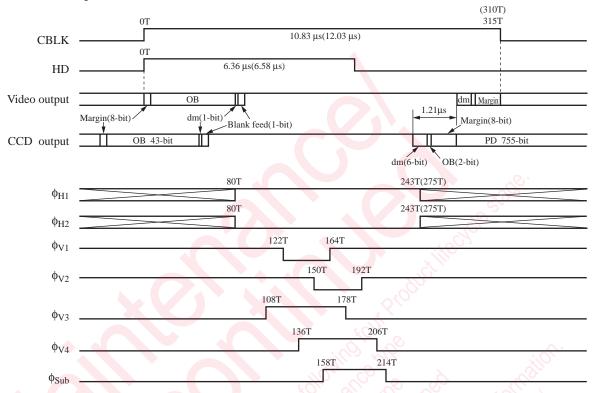


< Field B >

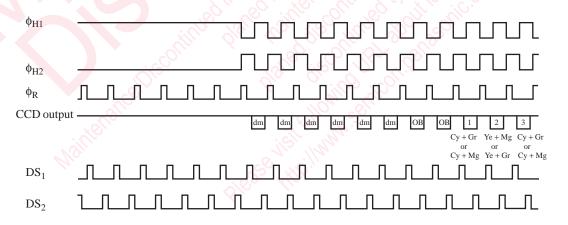


■ Timing Diagram (continued)

• H Rate timing

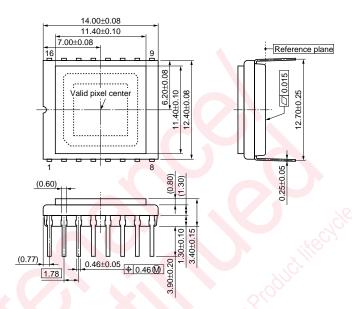


• High speed pulse timing



Note) dm: dummy

- Package Dimensions (Unit:mm)
- WDIP016-P-0500C



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