

# **IT9130 Series**

**DVB-T Front-End Integrated Receiver**

**Product Brief V0.0.4**

**ITE TECH. INC.**

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**IT9130** is a series of highly integrated DVB-T single-chip receiver consisting of high quality RF tuner front-end and COFDM demodulator to aim for **superior performance, ultra-low power consumption, and simple system design** of various DVB-T applications. IT9130 offers very **low total Bill Of Material** solutions. It does not require external SAW filter, LNA, or Balun. IT9130 requires only one power regulator and one crystal to further simplify the system design and reduce the system cost. The ultra-low power consumption feature of the IT9130 makes it the perfect choice for all kinds of DVB-T applications.

**Compliant Specifications:**

- ETSI EN 300 744 V1.5.1 DVB-T Standard, including Annexes F and G.
- NorDig Unified Requirements V2.1
- IEC 62002-2: Edition-2 05-2008 (MBRAI 2.0)
- ISO/IEC 62216-1: 2009 (E), E-Book
- DTG D-book 6, UK Digital Terrestrial Television
- BSMI, Taiwan

**Supported RF Frequencies:**

- VHF band III (170MHz ~ 240MHz)
- UHF band (470MHz ~ 862MHz)

**Supported Host Interfaces:**

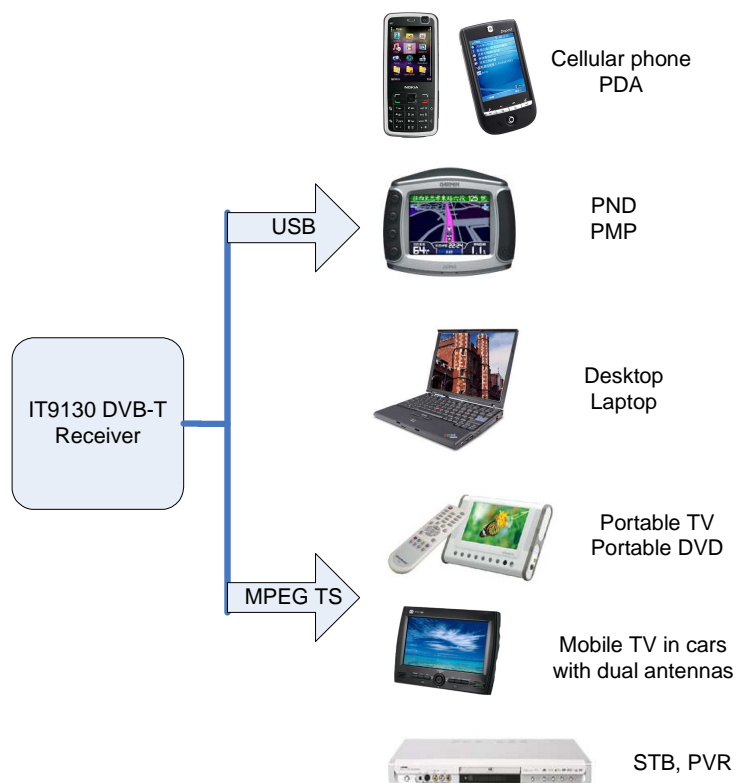
- USB2.0
- MPEG2 TS with 2-wire control bus

**Package Information**

- QFN-48 7mm x 7mm – IT9133, IT9135
- QFN-56 8mm x 8mm – IT9137

**Applications**

- USB stick, Mini Card, Half-Mini Card, and Express Card to enable TV functions for desktops and notebooks
- DVB-T Set-Top Boxes
- Integrated digital DVB-T televisions
- Cellular phone and PDA with mobile TV built-in
- Personal Navigation Device (PND) with TV built-in
- Portable digital TVs or Media Players (PMP) with TV functions
- Mobile DVB-T receivers with dual antennas (diversity receptions)
- Digital Photo Frame with digital TV built-in



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## 1. Features

### ■ Integrated RF Tuner for DVB-T

- **Built-in RF tuner** to support DVB-T receptions at UHF band and VHF band.
- **Zero-IF** direct conversion architecture to achieve low power consumption.
- **Single-ended** RF input eliminates the requirement of Balun.
- No external **SAW filter** is required.
- **Integrated LNA** with low noise figure to meet MBRAI 2.0 requirement and achieve superior sensitivity performance without the need of external LNA.
- Integrated Received Signal Strength Indicator (**RSSI**) for precise AGC adjustment in the environments with Adjacent Channel Interferences (ACI).
- Automatic RF/BB AGC **gain distribution** to properly compromise the performance between noise and linearity.

### ■ Superior DVB-T COFDM Reception

- Complete OFDM demodulation compliant to DVB-T specification ETSI 300 744, including Annexes F and G.
- Performance compliant to NorDig Unified v2.0, D-Book, E-Book, Taiwan BSMT, and MBRAI2.0.
- Robust immunity to Doppler Effect in **mobile/portable** reception.
- Superior dynamic **echo** performance which meets NorDig and MBRAI echo inside and outside guard interval tests.
- **Diversity-enabled dual channel receiving** capability enabling high mobility DVB-T reception, picture-in-picture (PIP), and record while watching (PVR) applications.
- Automatic 2K/4K/8K mode and guard interval detection.
- Digital carrier frequency offset correction up to  $\pm 500\text{KHz}$ .
- Digital crystal frequency jitter compensation up to  $\pm 100\text{ppm}$ .
- All-digital time and frequency synchronization tracking loop.

- All-digital **adjacent channel interference (ACI)** rejection filtering for supporting 5/6/7/8MHz bandwidth.
- Adaptive **co-channel interference (CCI)** filtering for interferences including PAL/ SECAM/NICAM.
- Effective **impulse noise** rejection
- **Fast channel scan** and **switch** time.

### ■ Versatile Interfaces

- Embedded **USB 1.1** and **2.0** compatible interface support with suspend mode.
- Serial and parallel **MPEG2-TS** output interface with simple two-wire control bus.
- Infrared (**IR**) interface provided for remote control.
- Multiple sets of **PWM** and **GPIO** for external control purpose.

### ■ Compact for Application Designs

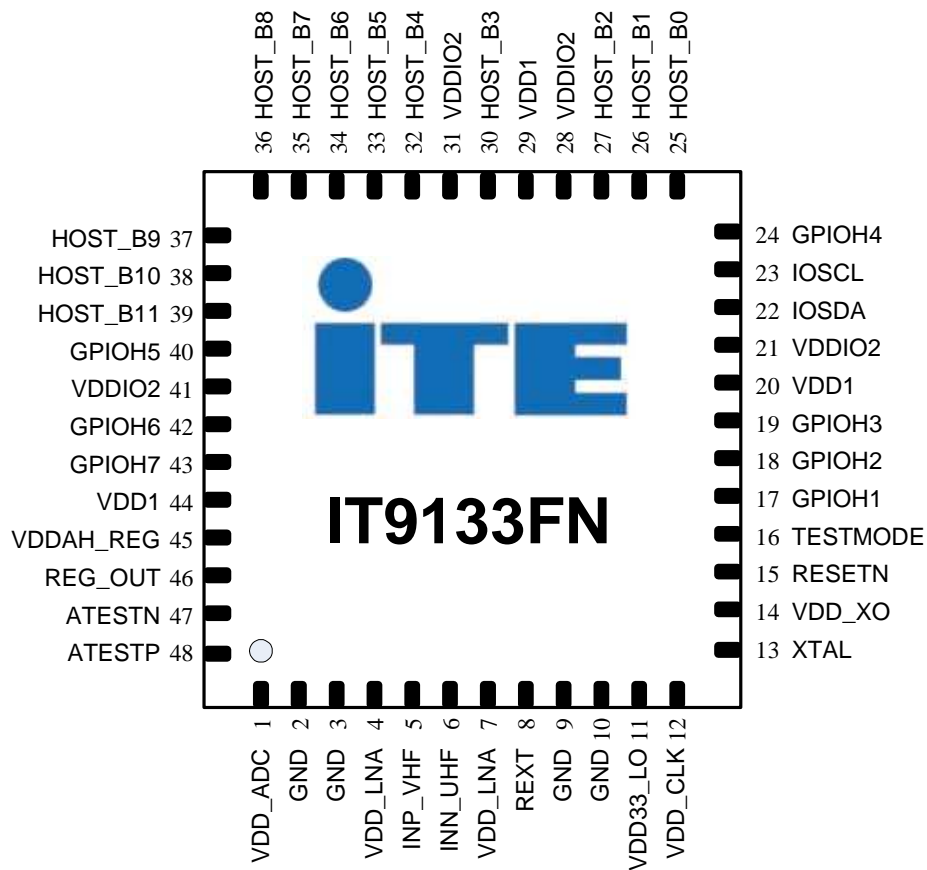
- **Single crystal** (12MHz or 20.48 MHz) is only required to provide all internal clocks.
- **On-chip LDO** provides the flexibility of system-wise power design.
- **Single power supply** (3.3V) is only required, with the option of using external 1.2V.
- Superior all-CMOS SoC technology enables **ultra-low power** consumption (minimum **200mW** core power consumption operating at 8MHz, 8K mode, 64QAM, and code rate 7/8 with Transport Stream output)
- **Single-ended** RF input eliminates the requirement of Balun.
- High sensitivity and ACI immunity are achieved without **external LNA**.

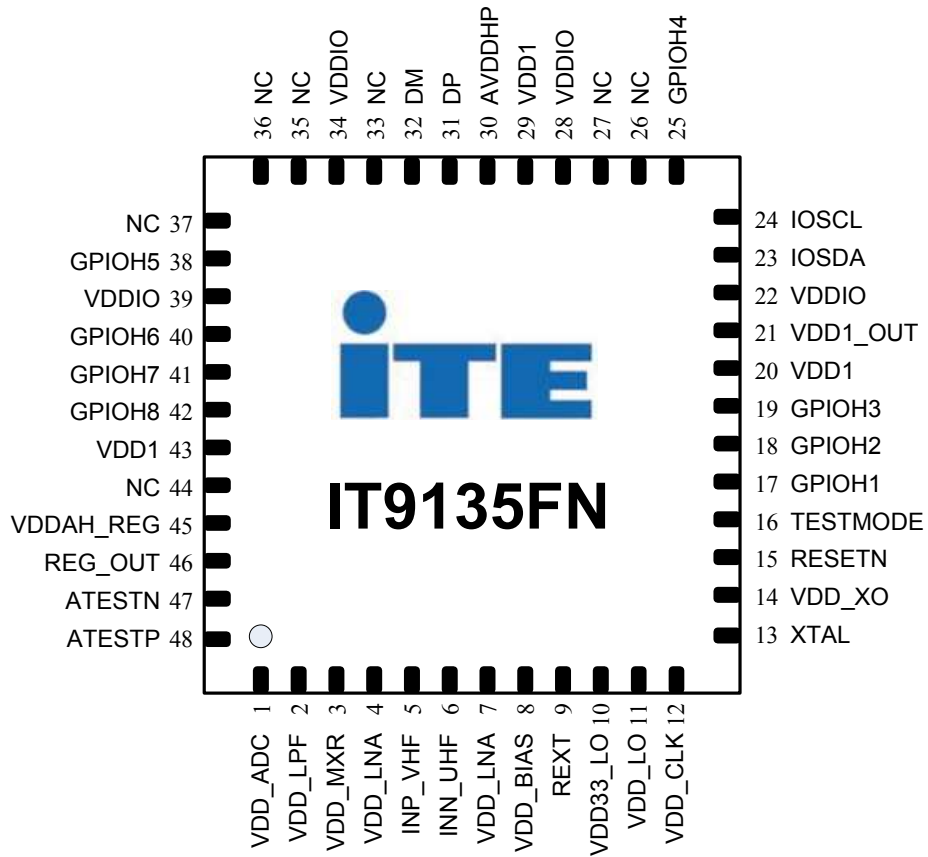
### ■ Simple Application Programming Interface with Complete SW Package

- Complete **API** for fast and easy integration with **application processors, multimedia processors**, or CPU-based platforms.

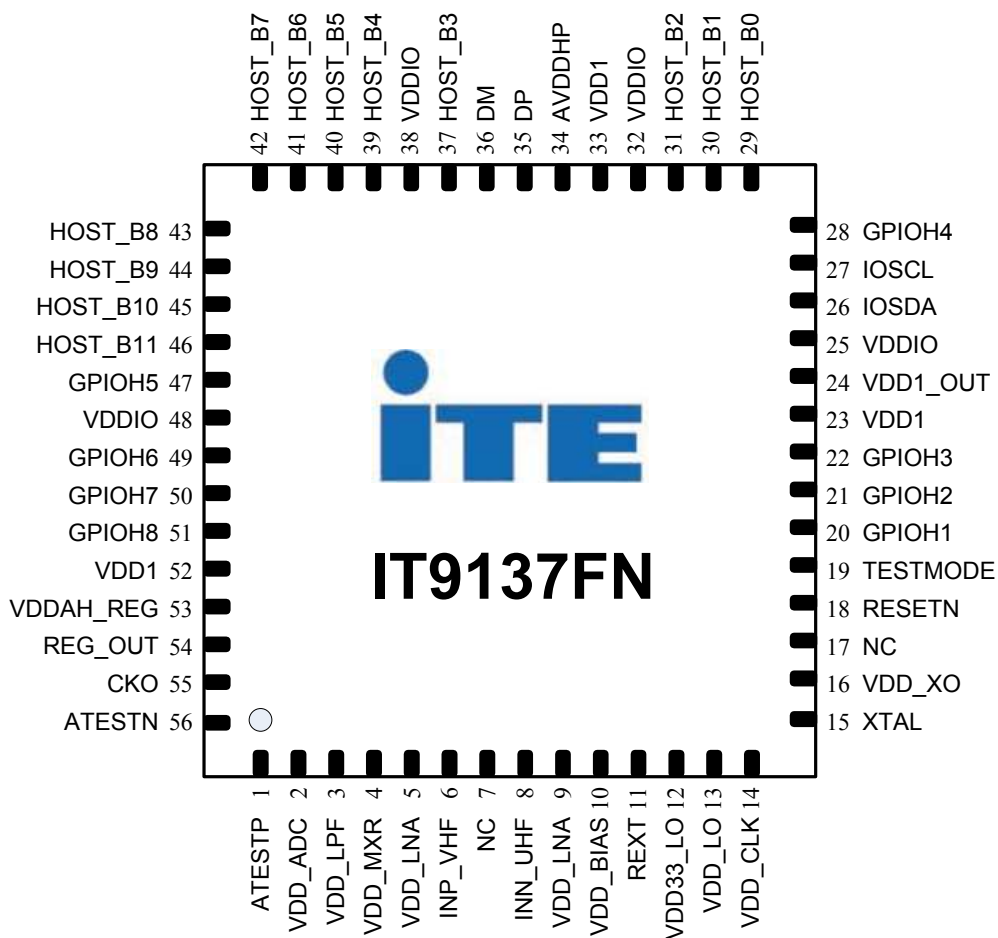
- Integrated transport stream de-multiplexer (**PID filtering**) with bypass mode.
- Comprehensive **performance** and **signal condition** monitoring parameters available through register access.
- **Auto signal re-acquisition** without external programming
- Windows **Mobile/CE** drivers support.
- USB **BDA driver** support for **Windows 7/XP/Vista**.
- **Linux driver** support.

**2. Pin Configuration**









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## 3. Pin Description

Table 3-1. Pin Description of IT9133

Pin(s) No.	Symbol	Attribute	Description
1	VDD_ADC	P	RF analog power supply
2	GND	—	To be grounded
3	GND	—	To be grounded
4	VDD_LNA	P	RF analog power supply
5	INP_VHF	AIO	RF signal input for VHF
6	INN_UHF	AIO	RF signal input for UHF
7	VDD_LNA	P	RF analog power supply
8	REXT	BR	External bias resistor
9	GND	—	To be grounded
10	GND	—	To be grounded
11	VDD33_LO	P	RF analog power supply
12	VDD_CLK	P	RF analog power supply
13	XTAL	AIO	Crystal input
14	VDD_XO	P	RF analog power supply
15	RESETN	DIO	Power-on Reset (Low Active)
16	TESTMODE	DIO	Test mode selection; tied to ground for normal operation.
17	GPIOH1	DIO	General purpose I/O
18	GPIOH2	DIO	General purpose I/O
19	GPIOH3	DIO	General purpose I/O
20	VDD1_OUT	P	Regulator output power for Core Usage
21	VDDIO	P	Digital I/O Power
22	IOSDA	DIO	Two-wire bus serial data line
23	IOSCL	DIO	Two-wire bus clock line
24	GPIOH4	DIO	General purpose I/O
25	HOST_B0	DIO	Host interface
26	HOST_B1	DIO	Host interface
27	HOST_B2	DIO	Host interface
28	VDDIO	P	Digital I/O Power
29	VDD1	P	Core Power
30	HOST_B3	DIO	Host interface
31	VDDIO	P	Digital I/O Power
32	HOST_B4	DIO	Host interface
33	HOST_B5	DIO	Host interface
34	HOST_B6	DIO	Host interface
35	HOST_B7	DIO	Host interface
36	HOST_B8	DIO	Host interface
37	HOST_B9	DIO	Host interface
38	HOST_B10	DIO	Host interface
39	HOST_B11	DIO	Host interface
40	GPIOH5	DIO	General purpose I/O
41	VDDIO	P	Digital I/O Power
42	GPIOH6	DIO	General purpose I/O
43	GPIOH7	DIO	General purpose I/O; IR
44	VDD1	P	Core Power
45	VDDAH_REG	P	RF analog power supply
46	REG_OUT	P	Regulator output for RF usage
47	ATESTN	AIO	Negative I/O for internal testing (Not Connected)
48	ATESTP	AIO	Positive I/O for internal testing (Not Connected)

Note: P: Power, AIO: Analog Input/Output, DIO: Digital Input/Output, BR: Bias Resistor

**Table 3-2. Pin Description of IT9135**

Pin(s) No.	Symbol	Attribute	Description
1	VDD_ADC	P	RF analog power supply
2	VDD_LPF	P	RF analog power supply
3	VDD_MXR	P	RF analog power supply
4	VDD_LNA	P	RF analog power supply
5	INP_VHF	AIO	RF signal input for VHF
6	INN_UHF	AIO	RF signal input for UHF
7	VDD_LNA	P	RF analog power supply
8	VDD_BIAS	P	RF analog power supply
9	REXT	BR	External bias resistor
10	VDD33_LO	P	RF analog power supply
11	VDD_LO	P	RF analog power supply
12	VDD_CLK	P	RF analog power supply
13	XTAL	AIO	Crystal input
14	VDD_XO	P	RF analog power supply
15	RESETN	DIO	Power-on Reset (Low Active)
16	TESTMODE	DIO	Test mode selection; tied to ground for normal operation.
17	GPIOH1	DIO	General purpose I/O
18	GPIOH2	DIO	General purpose I/O
19	GPIOH3	DIO	General purpose I/O
20	VDD1	P	Core Power
21	VDD1_OUT	P	Regulator output power for Core Usage
22	VDDIO	P	Digital I/O Power
23	IOSDA	DIO	Two-wire bus serial data line
24	IOSCL	DIO	Two-wire bus clock line
25	GPIOH4	DIO	General purpose I/O
26	NC	—	Not Connected
27	NC	—	Not Connected
28	VDDIO	P	Digital I/O Power
29	VDD1	P	Core Power
30	AVDDHP	P	Power for USB
31	DP	AIO	Differential Positive signal for USB
32	DM	AIO	Differential Negative signal for USB
33	NC	—	Not Connected
34	VDDIO	P	Digital I/O Power
35	NC	—	Not Connected
36	NC	—	Not Connected
37	NC	—	Not Connected
38	GPIOH5	DIO	General purpose I/O
39	VDDIO	P	Digital I/O Power
40	GPIOH6	DIO	General purpose I/O
41	GPIOH7	DIO	General purpose I/O; IR
42	GPIOH8	DIO	General purpose I/O
43	VDD1	P	Core Power
44	NC	—	Not Connected

Pin(s) No.	Symbol	Attribute	Description
45	VDDAH_REG	P	RF analog power supply
46	REG_OUT	P	Regulator output for RF usage
47	AATESTN	AIO	Negative I/O for internal testing (Not Connected)
48	AATESTP	AIO	Positive I/O for internal testing (Not Connected)

Note: P: Power, AIO: Analog Input/Output, DIO: Digital Input/Output, BR: Bias Resistor

**Table 3-3. Pin Description of IT9137**

Pin(s) No.	Symbol	Attribute	Description
1	AATESTP	AIO	Positive I/O for internal testing (Not Connected)
2	VDD_ADC	P	RF analog power supply
3	VDD_LPF	P	RF analog power supply
4	VDD_MXR	P	RF analog power supply
5	VDD_LNA	P	RF analog power supply
6	INP_VHF	AIO	RF signal input for VHF
7	NC	—	Not Connected.
8	INN_UHF	AIO	RF signal input for UHF
9	VDD_LNA	P	RF analog power supply
10	VDD_BIAS	P	RF analog power supply
11	REXT	BR	External bias resistor
12	VDD33_LO	P	RF analog power supply
13	VDD_LO	P	RF analog power supply
14	VDD_CLK	P	RF analog power supply
15	XTAL	AIO	Crystal input
16	VDD_XO	P	RF analog power supply
17	NC	—	Not Connected
18	RESETN	DIO	Power-on Reset (Low Active)
19	TESTMODE	DIO	Test mode selection; tied to ground for normal operation.
20	GPIOH1	DIO	General purpose I/O
21	GPIOH2	DIO	General purpose I/O
22	GPIOH3	DIO	General purpose I/O
23	VDD1	P	Core Power
24	VDD1_OUT	P	Regular output power for Core Usage
25	VDDIO	P	Digital I/O Power
26	IOSDA	DIO	Two-wire bus serial data line
27	IOSCL	DIO	Two-wire bus clock line
28	GPIOH4	DIO	General purpose I/O
29	HOST_B0	DIO	Host interface
30	HOST_B1	DIO	Host interface
31	HOST_B2	DIO	Host interface
32	VDDIO	P	Digital I/O Power
33	VDD1	P	Core Power
34	AVDDHP	P	Power for USB
35	DP	AIO	Differential Positive signal for USB
36	DM	AIO	Differential Negative signal for USB
37	HOST_B3	DIO	Host interface
38	VDDIO	P	Digital I/O Power
39	HOST_B4	DIO	Host interface

Pin(s) No.	Symbol	Attribute	Description
40	HOST_B5	DIO	Host interface
41	HOST_B6	DIO	Host interface
42	HOST_B7	DIO	Host interface
43	HOST_B8	DIO	Host interface
44	HOST_B9	DIO	Host interface
45	HOST_B10	DIO	Host interface
46	HOST_B11	DIO	Host interface
47	GPIOH5	DIO	General purpose I/O
48	VDDIO	P	Digital I/O Power
49	GPIOH6	DIO	General purpose I/O
50	GPIOH7	DIO	General purpose I/O; IR
51	GPIOH8	DIO	General purpose I/O
52	VDD1	P	Core Power
53	VDDAH_REG	P	RF analog power supply
54	REG_OUT	P	Regulator output power for RF usage
55	CKO	AIO	Clock output for another device
56	ATESTN	AIO	Negative I/O for internal testing (Not Connected)

Note: P: Power, AIO: Analog Input/Output, DIO: Digital Input/Output, BR: Bias Resistor

**Table 3-4. Strapping Pins for Mode and Clock Selections**

Pin Name	Selection
{GPIOH2,GPIOH1}	Crystal frequency: 00 crystal = 12 MHz 01 crystal = 20.48MHz
{GPIOH8,GPIOH7,GPIOH6,GPIOH5}	Mode strapping and 2-wire bus address selection: 00xx TS mode, {GPIOH6, GPIOH5} = 2-wire address[1:0] 0001 Salve device of DCA mode 0101 USB mode

Note: Strapping sampled at the rising edge of the RESET signal

**Table 3-5. Host Interface Pin Descriptions**

Pin \ Mode	TS Output Mode	TS Input Mode	Diversity Master Mode	Diversity Slave Mode
HOST_B0	MPEG Fail	MPEG Data[7]	Output Data[3]	Output Clock
HOST_B1	MPEG Sync	MPEG Data[6]	Output Data[2]	Output Valid
HOST_B2	MPEG Valid	MPEG Data[5]	Output Data[1]	Output Data[0]
HOST_B3	MPEG Clock	MPEG Data[4]	Output Data[0]	Output Data[1]

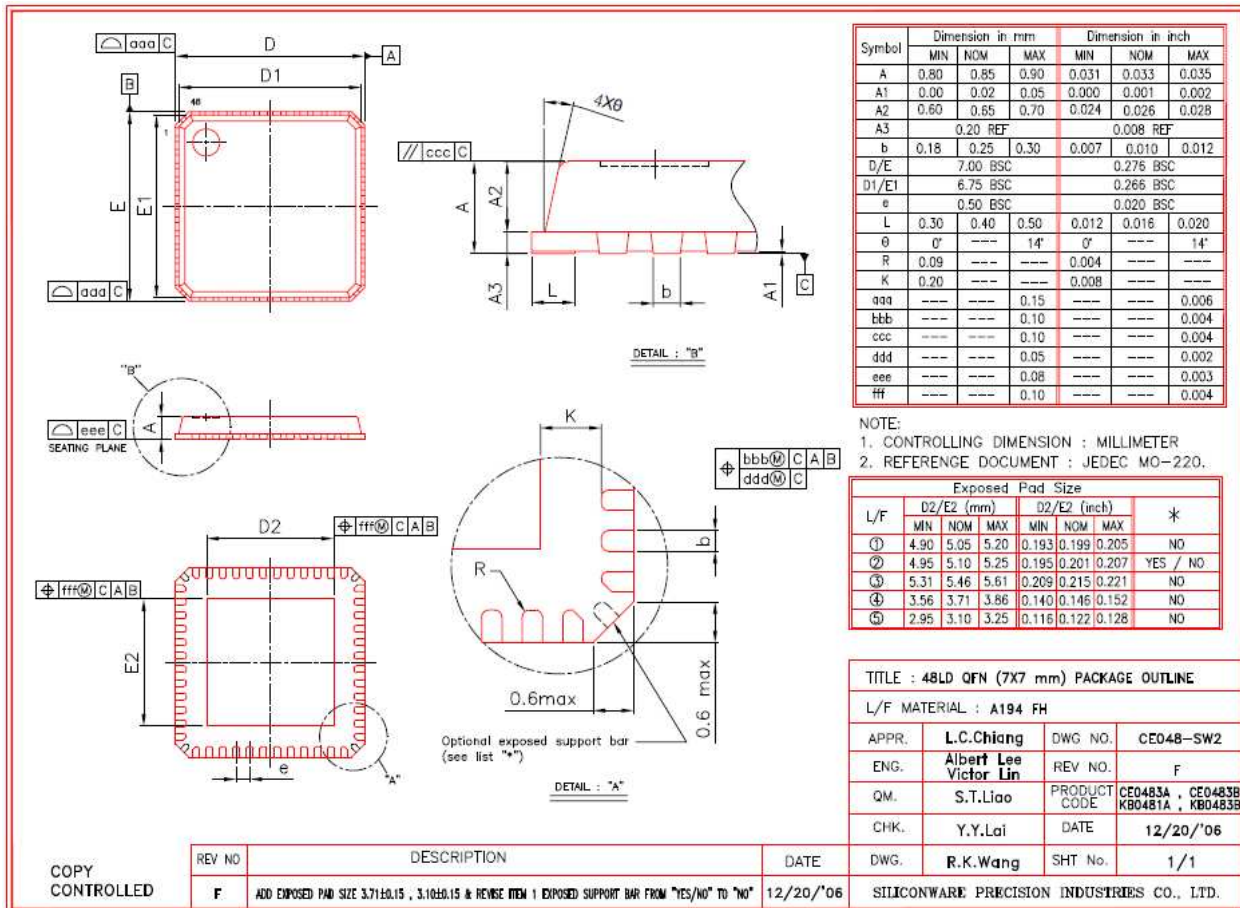
HOST_B4	MPEG Data[0]	MPEG Data[3]	Output Valid	Output Data[2]
HOST_B5	MPEG Data[1]	MPEG Data[2]	Output Clock	Output Data[3]
HOST_B6	MPEG Data[2]	MPEG Data[1]	Input Data[3]	Input Clock
HOST_B7	MPEG Data[3]	MPEG Data[0]	Input Data[2]	Input Valid
HOST_B8	MPEG Data[4]	MPEG Clock	Input Data[1]	Input Data[0]
HOST_B9	MPEG Data[5]	MPEG Valid	Input Data[0]	Input Data[1]
HOST_B10	MPEG Data[6]	MPEG Sync	Input Valid	Input Data[2]
HOST_B11	MPEG Data[7]	MPEG Fail	Input Clock	Input Data[3]

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**4. Package Information**

**IT9133FN/ IT9135FN – QFN48**



IT9137FN – QFN56

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3	0.20	REF		0.008	REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	8.00 BSC			0.315 BSC		
D1/E1	7.75 BSC			0.305 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
Ø	Ø	---	14'	Ø	---	14'
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

NOTE:  
1. CONTROLLING DIMENSION : MILLIMETER  
2. REFERENCE DOCUMENT: JEDEC MO-220.

L/F	Exposed Pad Size					
	D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
⓪	4.22	4.37	4.52	0.166	0.172	0.178
Ⓛ	5.90	6.05	6.20	0.232	0.238	0.244

TITLE : 56LD QFN (8X8 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH			
APPR.	F.D.Tang	DWG NO.	CE056-SW1
ENG.	Albert Lee Terry Tsai	REV NO.	C
QM.	S.T.Liao	PRODUCT CODE	CE0563A , CE0561B KB0561A , KB0562B
CHK.	Y.Y.Lai	DATE	06/20/'05
DWG.	R.K.Wang	SHT No.	1/1

REV NO	DESCRIPTION	DATE
C	UPDATE DIMENSION "b", "D2/E2", ADD "eee", "fff", CHANGE DATUM "C" LOCATION & CANCEL EXPOSED TIE BAR	06/20/'05

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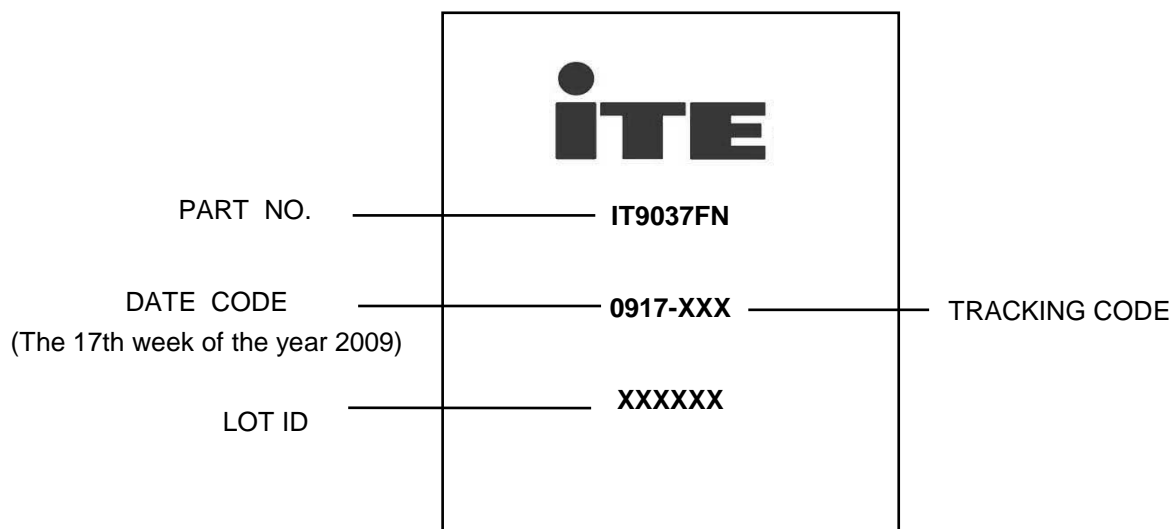
SILICONWARE PRECISION INDUSTRIES CO., LTD.

### 5. Ordering Information

Part Number	Description	Package	Body Size
IT9133FN/AX	DVB-T front-end receiver with MPEG TS interface for UHF/VHF DVB-T receptions.	QFN 48	7mm × 7mm
IT9135FN/AX	DVB-T front-end receiver with USB2.0 interface for UHF/VHF DVB-T receptions.	QFN 48	7mm × 7mm
IT9137FN/AX	DVB-T front-end receiver with USB2.0, diversity receiving, and MPEG TS interfaces for UHF/VHF DVB-T receptions.	QFN 56	8mm × 8mm

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**6. Top Marking Information**



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BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

### 2. DELIVERY

- Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
- Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
- Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

### 3. TERMS OF PAYMENT

- Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
- Seller reserves the right to change credit terms at any time in its sole discretion.

### 4. LIMITED WARRANTY

- Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
- Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
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- This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
- Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
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- Buyer will not return any goods without first obtaining a customer return order number.
- AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.
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- BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

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Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

### 7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

### 8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs. Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

### 9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

### 10. ENTIRE AGREEMENT

- These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
- Buyer is not relying upon any warranty or representation except for those specifically stated here.

### 11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

### 12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

### 13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.