IS31LT3932

High PF universal LED Driver

Preliminary

General Description

IS31LT3932 is a universal LED driver, which can operate in fly-back, buck-boost and buck convertor. For isolation fly-back, it can achieve high PF, high current accuracy, ± 5 % load and line regulation and wide voltage input voltage range, without loop compensation. For buck convertor, it also can achieve high PF, high current accuracy, high efficiency, good load and line regulation and wide voltage input voltage range, without loop compensation. with very few components.

IS31LT3932 has special power line sense and output voltage sense circuits, operates in primary feedback mode without opto-coupler and achieve stable output current control without any loop compensation.

IS31LT3932 has multiple protections to improve the system reliability, including LED open circuit, LED short circuit, UVLO, OVP, current sense resistor short, the primary over current limit and over temperature protections.

Features

- Universal isolation and non-isolation
- Single stage PFC fly-back
- No loop compensation required
- No opto-coupler required
- ± 3 %LED current accuracy
- ± 5 % line regulation and load regulation
- Wide input voltage: 85~265Vac
- Low start-up current(15uA)
- Valley turn-on MOSFET to achieve high efficiency for buck application
- Few external components
- 1A sourcing current and 2A sinking current
- multiple protections
- SOP-8 package

Application

- LED bulb
- LED Tube lamp
- LED PAR

Typical Operating Circuit

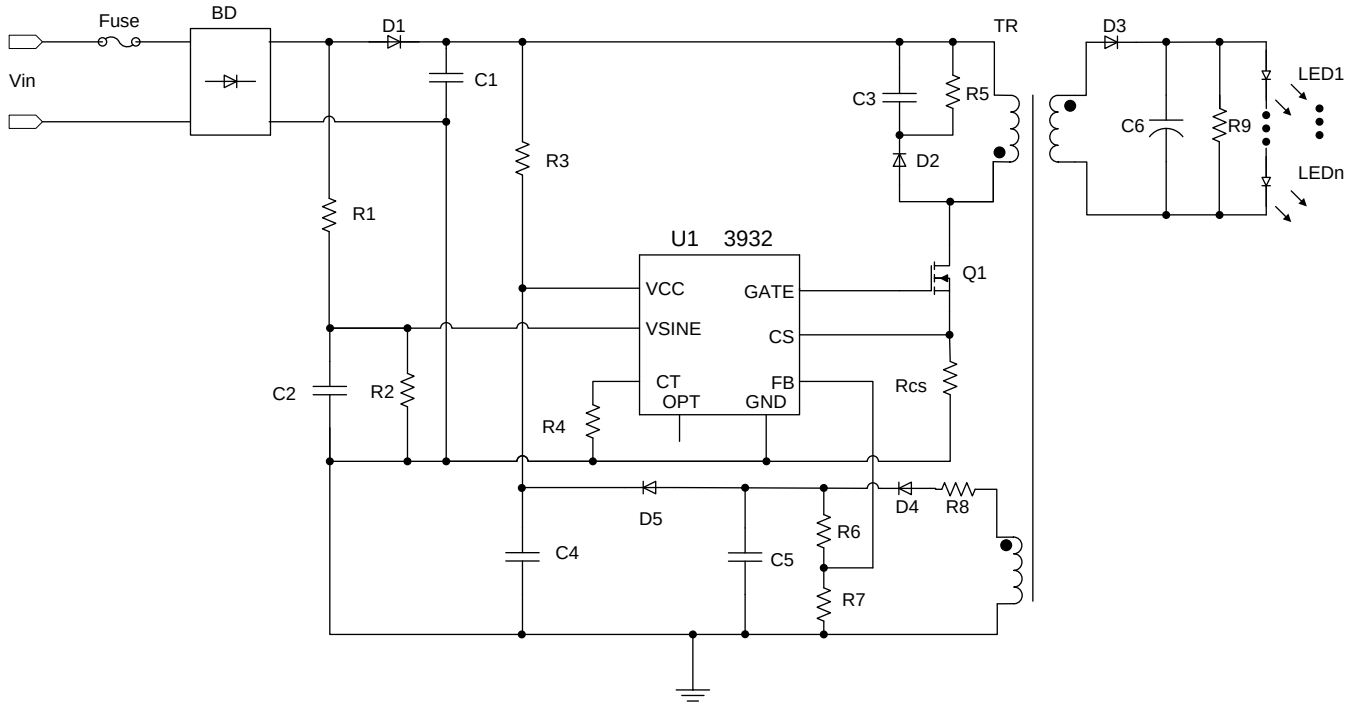
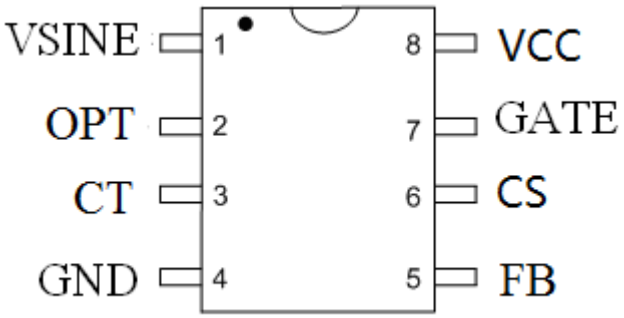


Figure 1 Typical isolated Operating Circuit

Pin Configurations

Package	Top View
SOP-8	

Pin Descriptions

Pin	Name	Function
1	VSINE	Power line voltage detection
2	OPT	Isolation and non-isolation option PIN Floating: fly-back and buck-boost Resistor to ground: buck sinusoidal
3	CT	Time setting through the resistor between PIN and ground Isolation: operation cycle time setting $f = 50k \times \frac{V_{FB}}{0.8V} \times \frac{300}{Rct(k\Omega)}$ Non-isolation: MOS turn-off delay time setting when FB detects zero voltage $Tdelay = 15 \times 10^{-6} \times R_{EXT}$
4	GND	Ground
5	FB	Fly-back and buck-boost: operation frequency is regulated through this PIN to compensate output current Non-isolation: valley turn-on detect PIN, the external MOS turns on after a short delay when FB detects zero voltage
6	CS	Inductor Current sense
7	GATE	Driver output to the external Power MOS
8	VCC	Power supply input PIN, at a range of 7V~30V

Ordering Information

Order Part No.	Package	QTY/Reel
IS31LT3932-GRLS2-TR	SOP-8, Lead-free	2500

Absolute Maximum Ratings

Parameter	Value
VDD,GATE to GND	-0.3 - 33.0
VSINE, OPT, CT, ISEN, FB to GND	-0.3 - 6.0
Operation Temperature Range(T_A=T_J)	-40 - 125
Junction Temperature Range	-40 - 150
Storage Temperature Range	-65 -150
ESD （Human Body Mode）	2000
VDD,GATE to GND	-0.3 - 33.0

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics(Unless otherwise specified, VCC=16V, FB=0V, VSINE=2.5V, RSET=300KΩ, and T_{amb}=25 °C)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{DD}	Power Supply Range		8		30	V
V_{OVP}	V_{DD} Over Voltage Threshold			34		V
T_{OVP}	OVP Reset Time			160		ms
Ust	Startup Voltage		15	16.5	18	V
V_{uvlo}	Under Voltage Lockout			7		
$V_{FB,OVP}$	FB PIN Over voltage threshold			1.25		V
$T_{FB,OVP}$	FB OVP Reset Time	T_{cycle}=20us		160		ms
I_{IN}	Quiescent Current	VDD=16V ， v		700	1000	uA
$I_{IN,ST}$	Startup Current	VDD=10V		15	20	uA
I_{OP}	Operation Current			600	800	uA
V_{CSTH}	Peak Current Voltage Threshold		495	500	505	mV
V_{OCP}	Over Current Voltage Threshold			700		mV
T_{OCP}	OCP Reset Time			40		ms
T_{BLANK}	Current Sense Blanking Time	V_{CS}=V_{CSTH}+50mV		600		ns
T_{OFF_MIN}	Minimum TOFF Time	OPT=0	0.7	1	1.3	us
T_{cycle}	Operating Cycle（note1）	V_{FB}=0.8V, R_{CT}=300KΩ	19.8	20	20.2	us
		V_{FB}=1.04V, R_{CT}=300KΩ	15.0	15.4	15.8	us
		V_{FB}=0.56V, R_{CT}=300KΩ	28.2	28.6	29.0	us
$V_{GATE,MAX}$	GATE output clamp voltage	VDD=20V		17.5		V
Isource	Sourcing Current	Vgate=0V		0.22		A
Isink	Sinking Current	Vgate=16V		0.57		A
T_P	Thermal Shutdown Threshold			150		°C
ΔT_P	Thermal Shutdown Hysteresis			50		°C
T_{re}	ISEN Short Protection Reset Time			40		ms

Typical Performance Characteristics (Vin=85~265Vac,Vout=14~30Vdc,Iout=190mA)

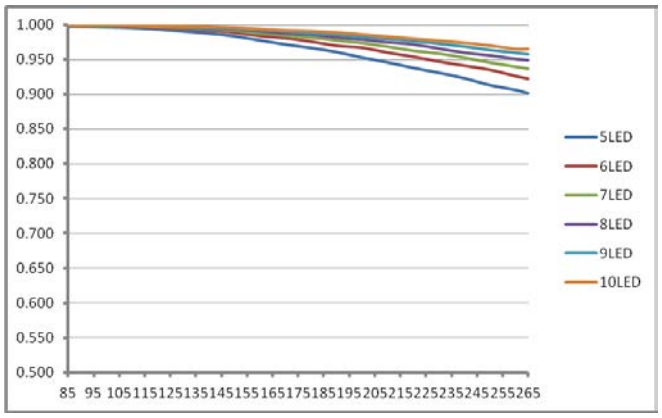


Figure 4 PF

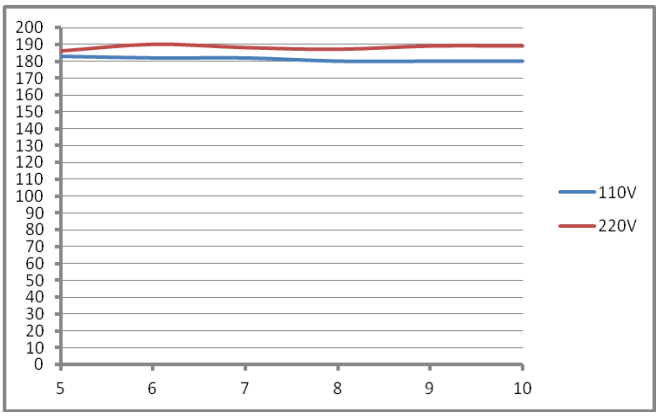


Figure 5 load regulation

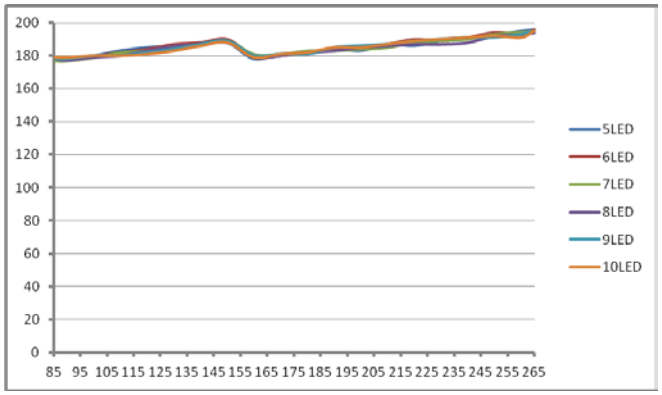


Figure 6 line regulation

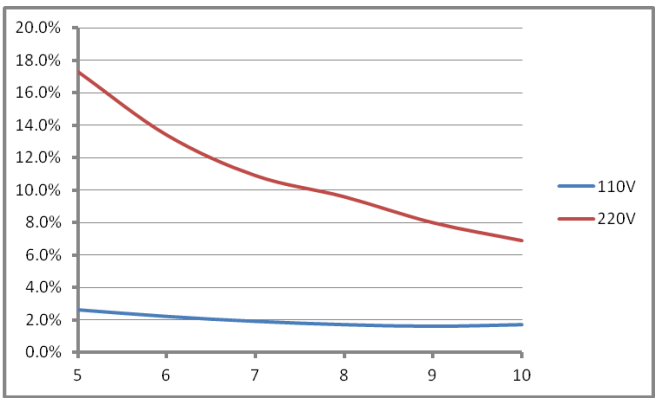


Figure 7 THD vs LEDs

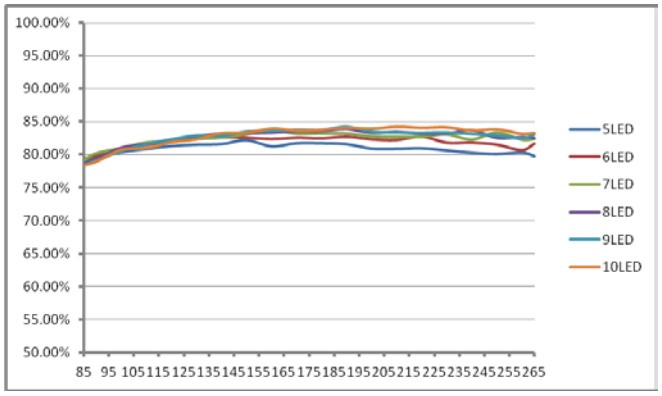


Figure 8 efficiency vs Vin(Vac)

Block Diagram

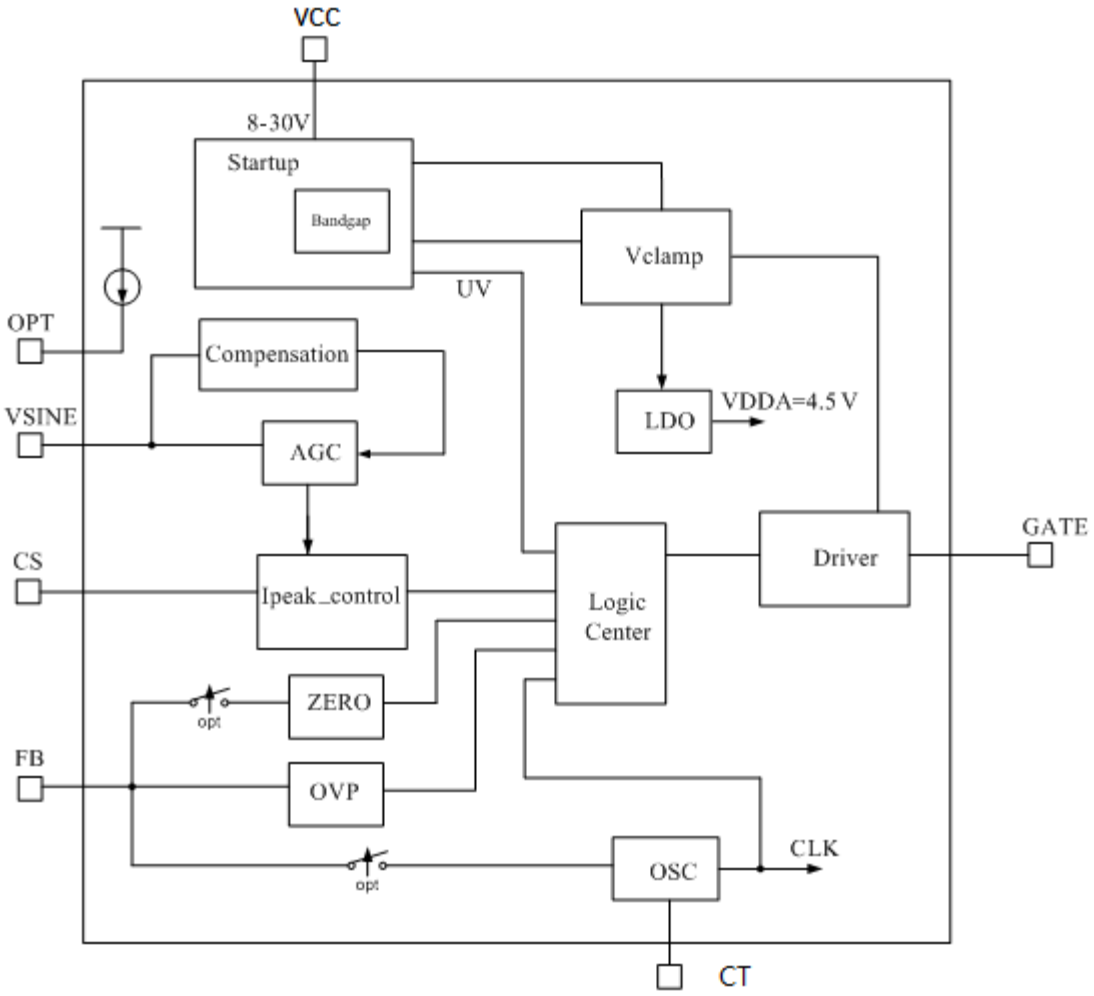


Figure 9 Block Diagram

Application Information (base on Figure 18 Typical Application Circuit)

Startup voltage

When the VCC pin of the IS31LT3932 reaches 16.5V, the IC is allowed to start. After power is applied to the circuit, R6 and R10 provides a trickle current to allow C9 to begin charging. The IC starts working when the voltage of C9 reaches the start threshold for the IC. The value of R6 and R10 & C9 can be determined by the input voltage. Larger values of R6 and R10 increase the startup time, but reduce the losses after the circuit is running. A low ESR capacitor of 10uF, 50V is recommended for C9.

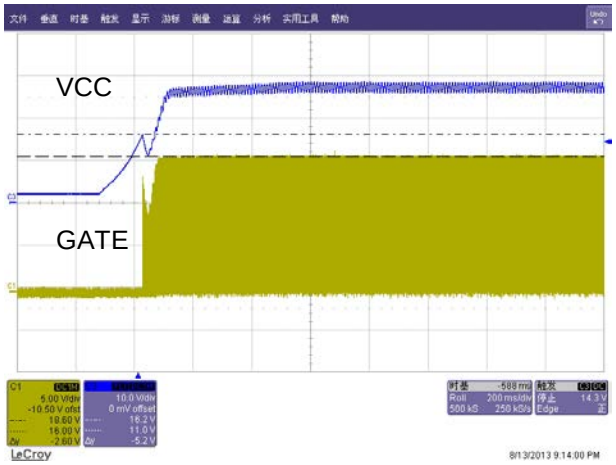


Figure 10 startup

Soft start control

When the device get start the threshold voltage of CS form low level go to 0.5V step by step.

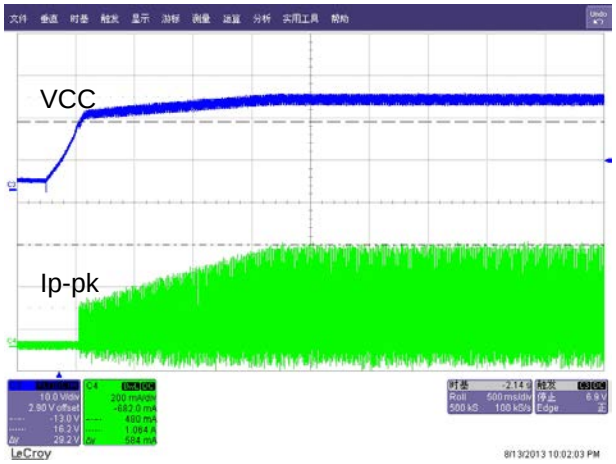


Figure 11 soft start

GATE output voltage clamp

IS31LT3932 has the voltage clamp for GATE output. When the voltage of VCC smaller than the $V_{GATEclp}$ threshold, The voltage of GATE output is about VCC. When the voltage of VCC is greater than $V_{GATEclp}$ threshold, the voltage of GATE is $V_{GATEclp}$ threshold.

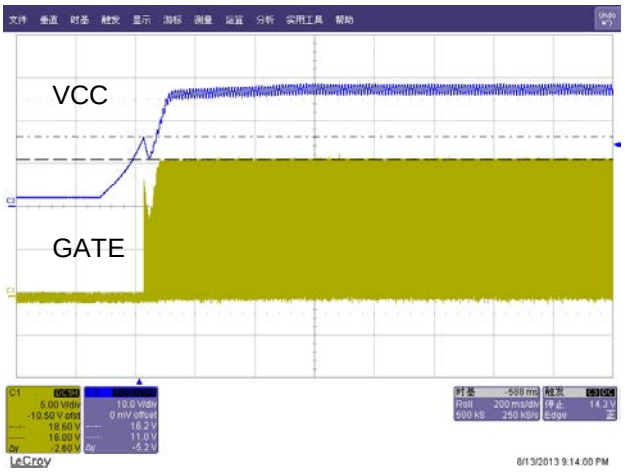


Figure 12 gate clamp

VSINE detection network and active PFC

The voltage of VSINE pin is used to control the waveform of input current make it follow the input voltage waveform, so can get the high PF and low THD. As Figure 11:

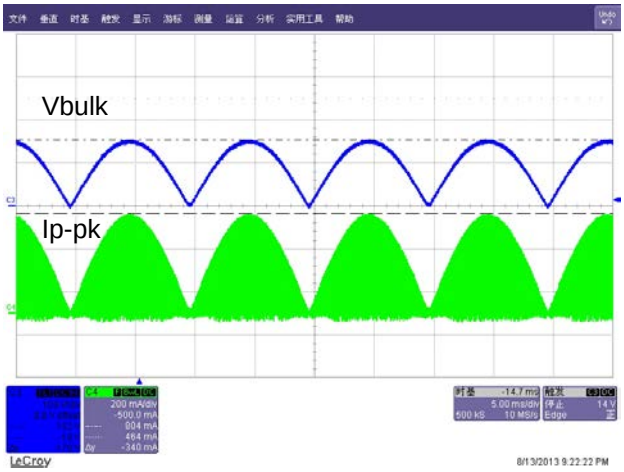


Figure 13 active PFC

The input pin, VSINE is used to detect the input voltage which controls the peak current waveform in the inductor and inside AGC makes the peak current of inductor constant, this allows the IS31LT3932 to actively correct the power factor and constant power during operation. The maximum input voltage of the VSINE pin is 2.5V. This resistor network should be computed such that the peak input voltage condition corresponds to ~2.4VDC. Thus, for 265VAC, the peak voltage is 374.7V. At 374.7V input, the output of the network should be 2.4V, thus values of R5+R9=2M and R18 = 13k are appropriate. High tolerance

resistors of 1% should be used. A small, 1nF capacitor, C7, is used to filter high frequency noise.

Working Frequency

The working frequency is set by connecting a resistor between the FSET pin and ground. The relationship between the frequency and resistance is:

$$f = 50k \times \frac{V_{FB}}{1V} \times \frac{250}{R_{CT}(k\Omega)}$$

Output open circuit protection

Open circuit protection is realized by connecting a resistor network to the FB pin. By sensing the voltage of the auxiliary winding, which is proportional to the output voltage, the IS31LT3932 detects when there is an open circuit condition on the secondary and stop the switching action. The threshold voltage for the FB pin is 1.25V.

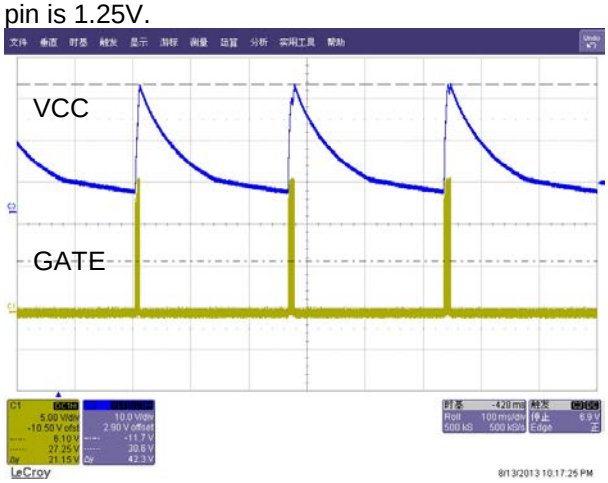


Figure 14 OVP

Output short circuit protection

If the output of the circuit is suddenly shorted, the voltage of the secondary winding is quickly reduced. This in-turn reduces the reflected voltage in the auxiliary winding, so VCC of the device drops rapidly. If the VCC voltage drops below the UVLO, the device will stop switching, thus indirectly achieving output short circuit protection.

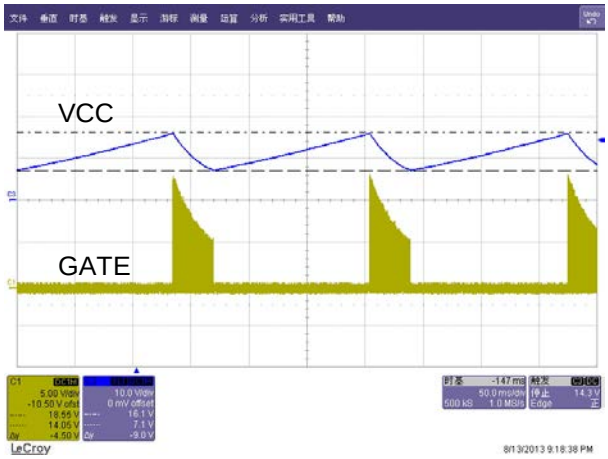


Figure 15 Output short circuit protect

UVLO protection

The device will not operate if the VCC voltage is below the under-voltage lockout threshold. Until the VCC voltage get startup threshold, the device start again.

CS over current and maximum duty cycle protection

If the CS pin is shorted to ground, the device can no longer detect the peak current of the inductor, and thus will quickly cause damage to the power MOS, inductor, or other circuit components. The maximum duty cycle of the gate is limited to 62.5% internally to prevent a shorted CS pin from going into current runaway. when the duty cycle greater than 62.5% the gate will turn off 80ms.

In addition to the duty cycle limit protection, there is also an inductor over current protection. If a fault condition exists wherein the inductor current continues to increase cycle per cycle, this would eventually cause the inductor into an over current condition. However, if the Vcs pin rises to 0.7V, the NMOS will immediately be shut off by the driving the gate low for a period of 40ms, after which the device will attempt a restart.

Load regulation

Frequency control is controlled by the FB pin voltage, when the FB pin voltage in the range of 0.5~1.25V, the control voltage is proportional to the frequency and FB, when the FB voltage is less than 0.5V, the frequency remained unchanged. Because the auxiliary winding voltage and the output voltage is the transformer turns ratio relationship, the FB pin detection auxiliary winding voltage, so, FB voltage follower output voltage changes, namely control frequency following the change of output voltage, in order to achieve constant output current.

Transformer design

The transformer technique is the other document of ISSI, here please use the “3932 calculator” to design the transformer.

PCB design considerations

(1) As Figure 30 and 31 shows, Components such as C7,R17,R18,R20,R21,R22,R23,C9etc. Which are connected to the IC should be mounted as close to the IC as possible.

(2) Bypass capacitors should always be mounted as close to the IC as possible.

(3) Switching signal traces should be kept as short as possible and not be routed parallel to one another so as to prevent coupling.

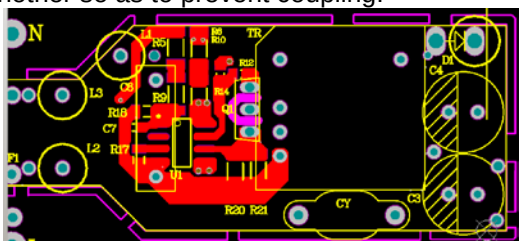


Figure 16 typical PCB top layer out

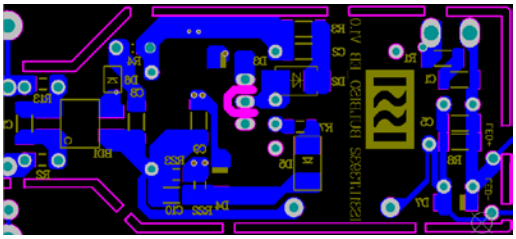


Figure 17 typical PCB bottom layer out

Typical Application Circuit (It is suited to full input voltage 15~30V-0.2A output applications)

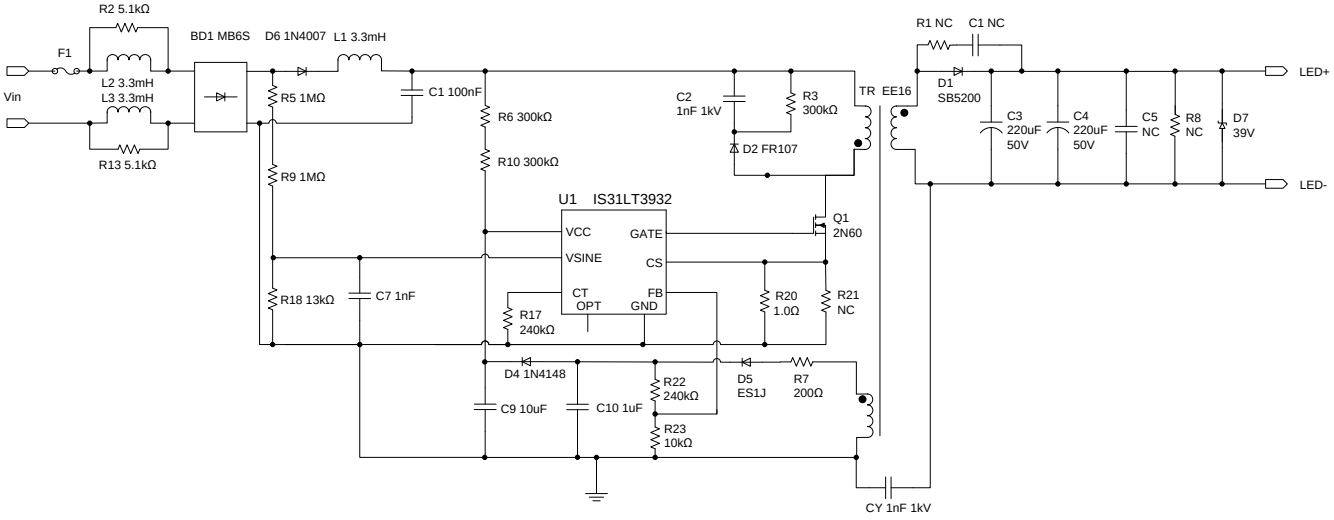
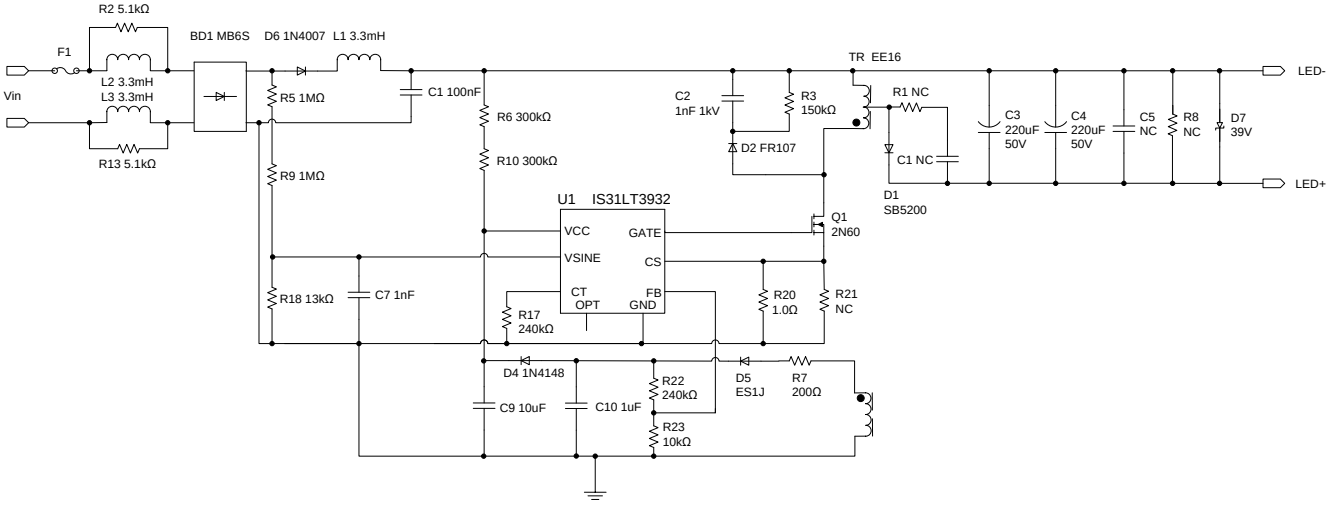


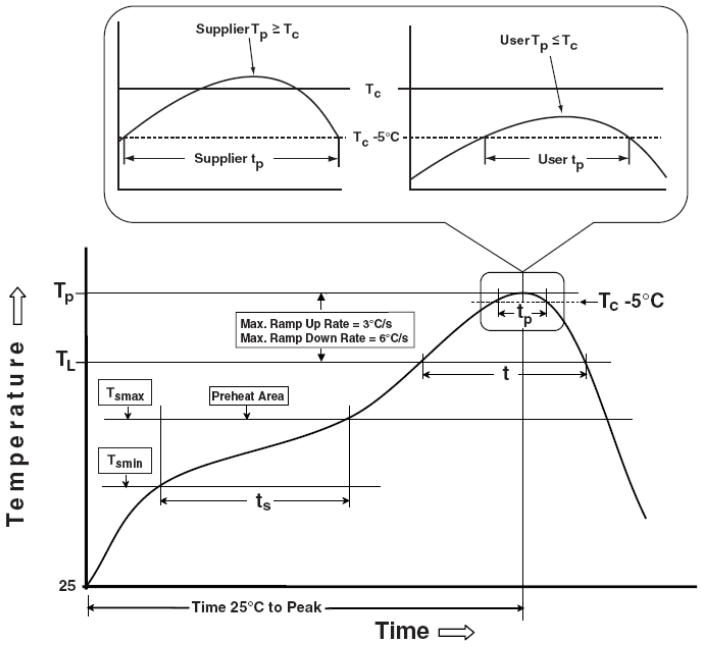
Figure 18 Typical isolated application schematic



. Figure 19 Typical non-isolated application schematic

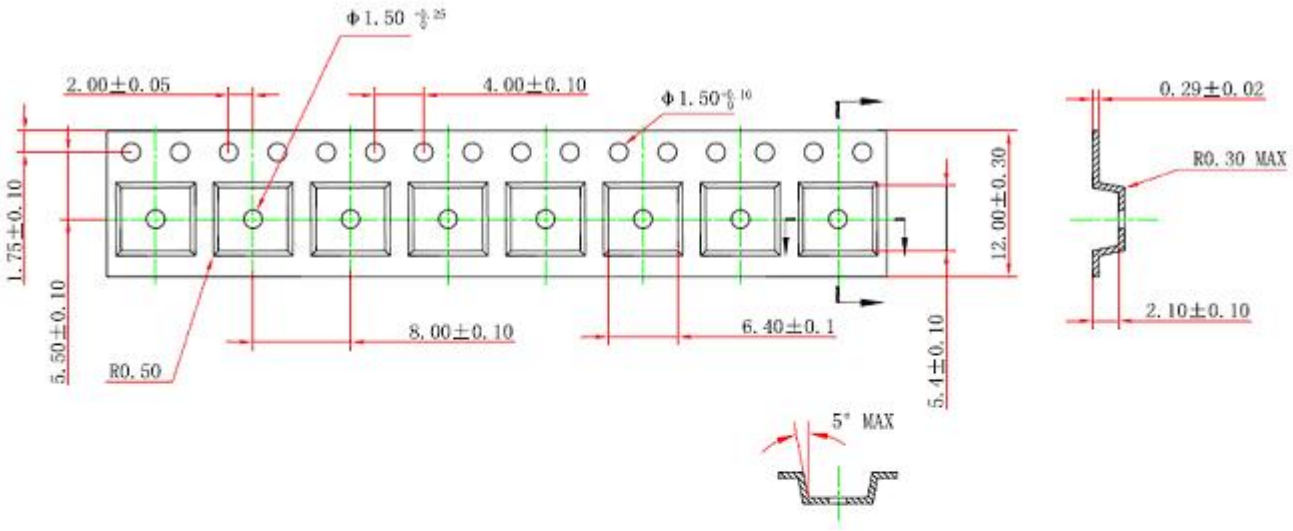
Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.



Classification Profile

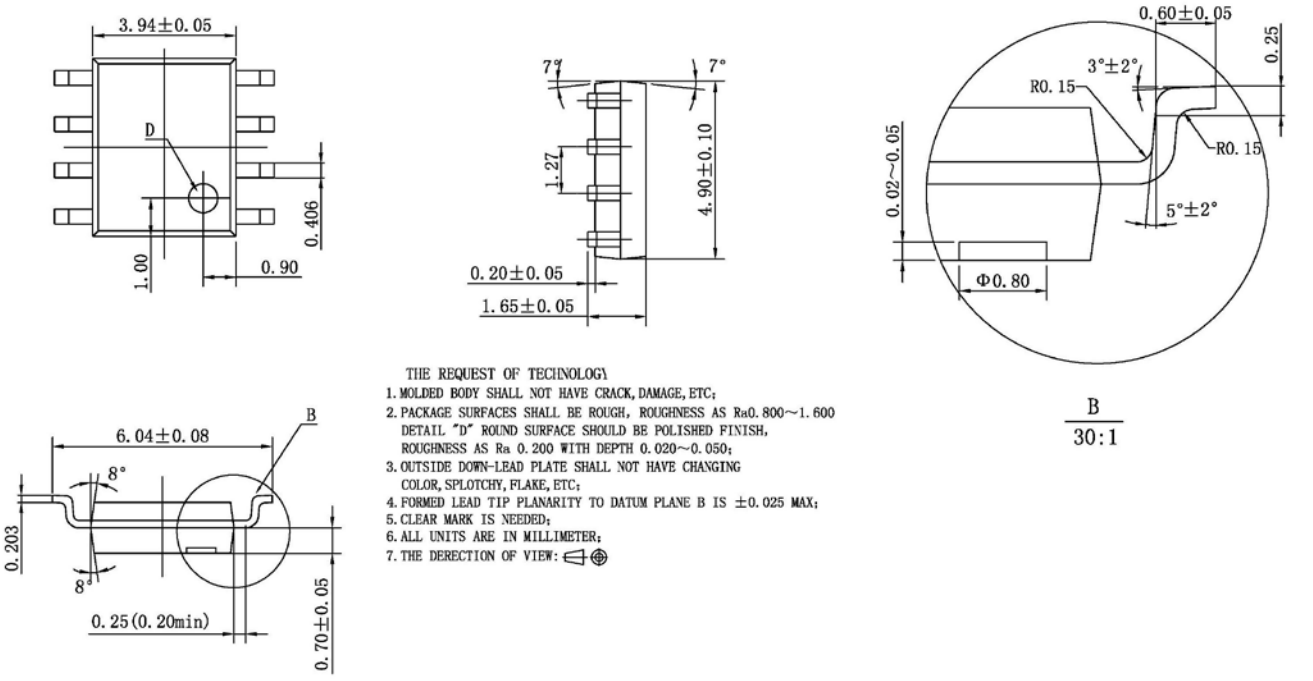
Tape and Reel Information



NOTES:

1.CARRIER TAPE COLOR: BLACK
2.COVER TAPE WIDTH:9.50± 0.10
3.COVER TAPE COLOR:TRANSPARENT
4. SURFACE ANTISTATIC COATED 10^{5} ~ 10^{11} OHMS/SQ.
5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.20MAX.
6. IN A REEL CARRIER THE THICKNESS CUMULATIVE TOLERANCE ± 0.05MAX.
7.CAMBER NOT TO EXCEED 1 MM IN 100 MM【载带直线弯曲度：≤1mm/100mm.】
8.MOLD# SOP8
9.ALL DIMS IN mm.
10.THE DERECTION OF VIEW:

Package Information



THE REQUEST OF TECHNOLOG\

1. MOLDED BODY SHALL NOT HAVE CRACK, DAMAGE, ETC;
2. PACKAGE SURFACES SHALL BE ROUGH, ROUGHNESS AS Ra0.800~1.600 DETAIL "D" ROUND SURFACE SHOULD BE POLISHED FINISH, ROUGHNESS AS Ra 0.200 WITH DEPTH 0.020~0.050;
3. OUTSIDE DOWN-LEAD PLATE SHALL NOT HAVE CHANGING COLOR, SPLOTCHY, FLAKE, ETC;
4. FORMED LEAD TIP PLANARITY TO DATUM PLANE B IS ±0.025 MAX;
5. CLEAR MARK IS NEEDED;
6. ALL UNITS ARE IN MILLIMETER;
7. THE DERECTION OF VIEW: