

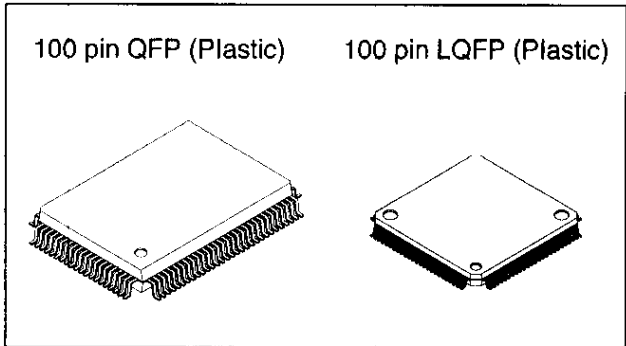
CXP81720A/81724A

CMOS 8-bit Single Chip Microcomputer

Description

The CXP81720A/81724A is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, 32kHz timer/event counter, remote control receiving circuit, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP81720A/81724A provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.



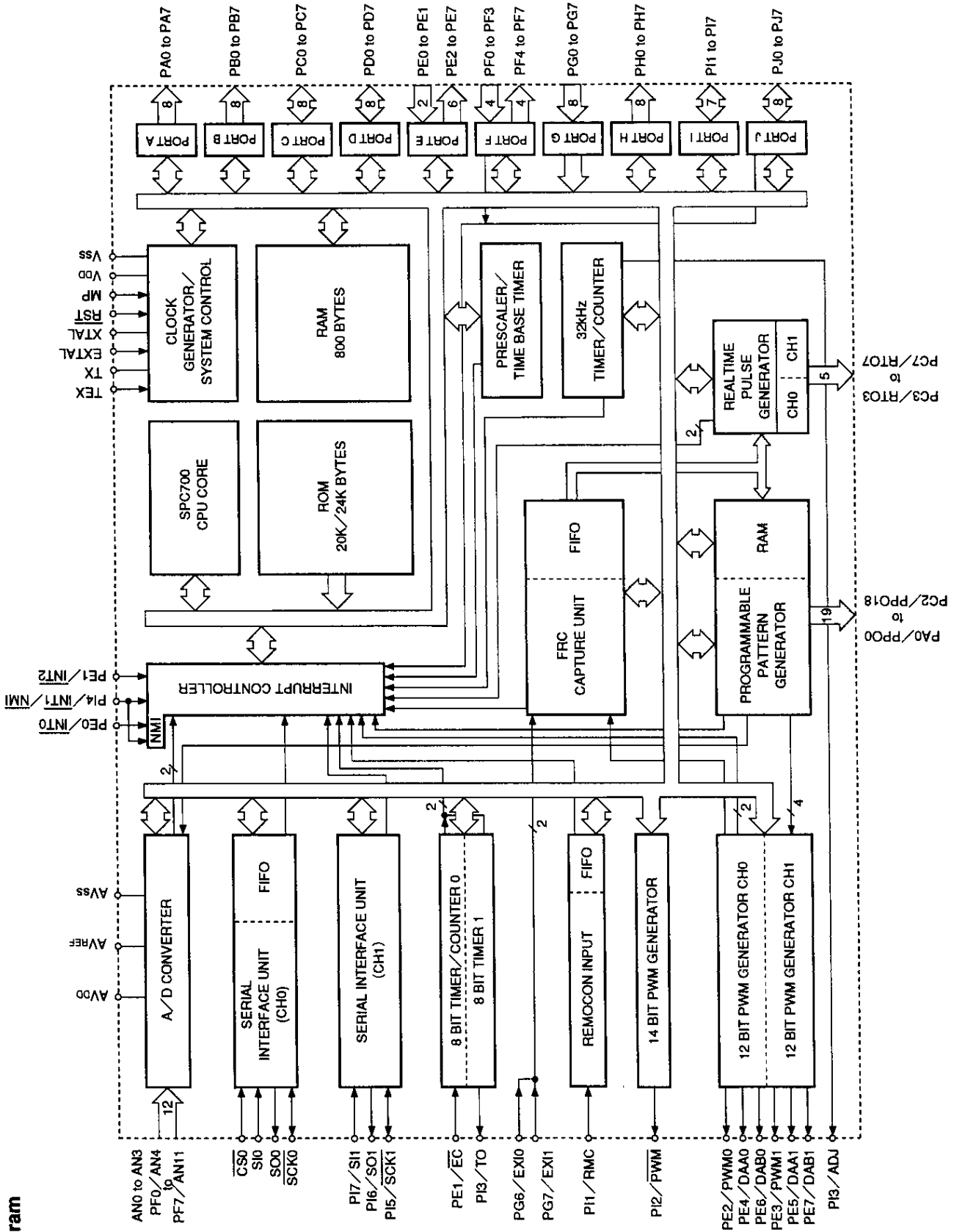
Structure

Silicon gate CMOS IC

Features

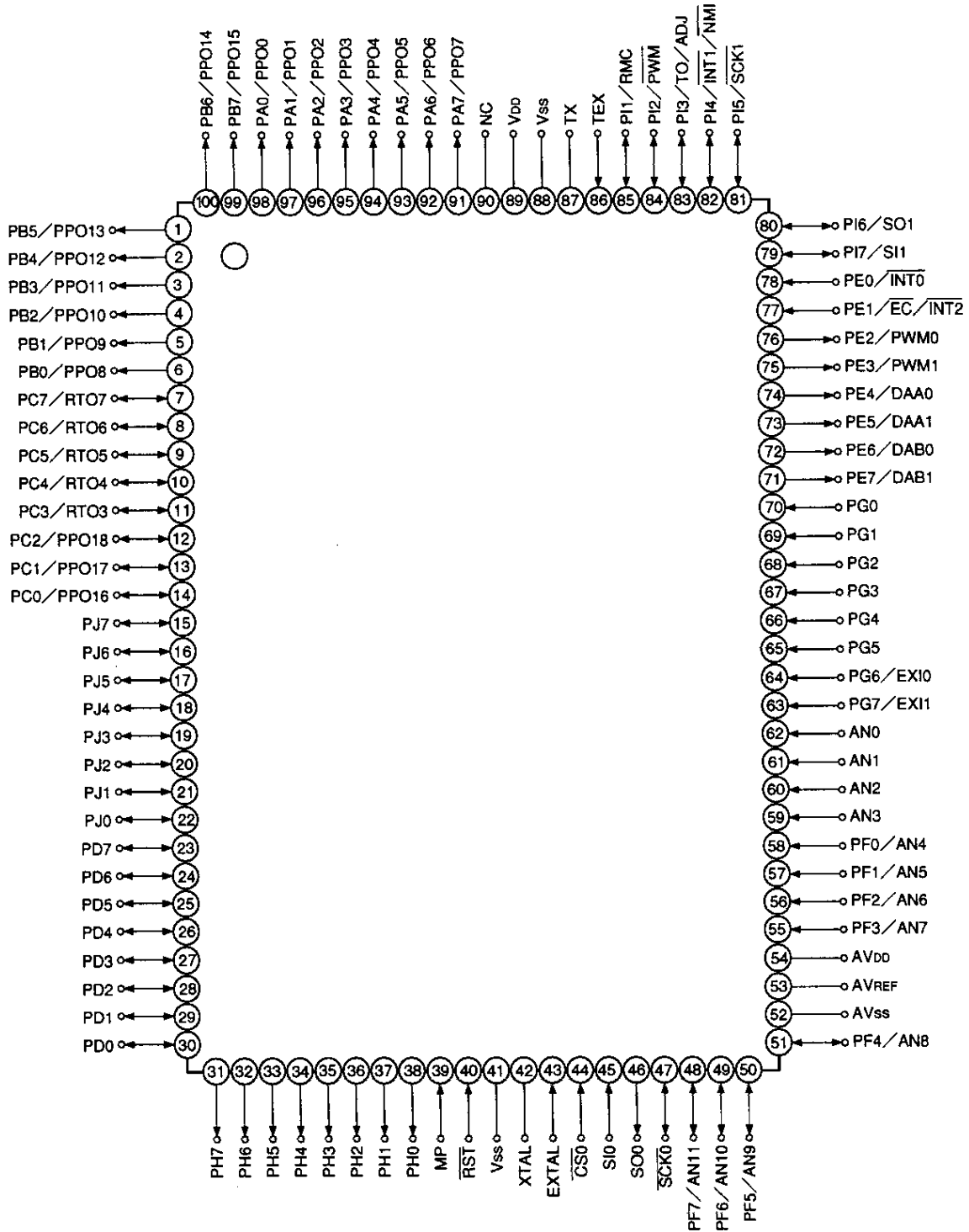
- A wide instruction set (213 instructions) which cover various types of data
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle During operation 250ns/16MHz (Supply voltage 4.5 to 5.5V)
 During operation 122µs/32kHz
- Incorporated ROM capacity 20K bytes (CXP81720A)
 24K bytes (CXP81724A)
- Incorporated RAM capacity 800 bytes
- Peripheral functions
 - A/D converter 8-bit, 12-channel, successive approximation system
 (Conversion time 20.0µs/16MHz)
 - Serial interface Incorporated 8-bit and 8-stage FIFO, 1-channel
 (1 to 8 bytes auto transfer)
 8-bit serial I/O, 1-channel
 - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer
 32kHz timer/counter
 - High precision timing pattern generator PPG 19 pins 32-stage programmable
 RTG 5-pins 2-channel
 - PWM/DA gate output 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)
 - FRC capture unit Incorporated 26-bit and 8-stage FIFO
 - PWM output 14-bit, 1-channel
 - Remote control receiving circuit 8-bit pulse measuring counter, 6-stage FIFO
- Interruption 20 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin plastic QFP/LQFP
- Piggyback/evaluation chip CXP81800 100-pin ceramic QFP/LQFP

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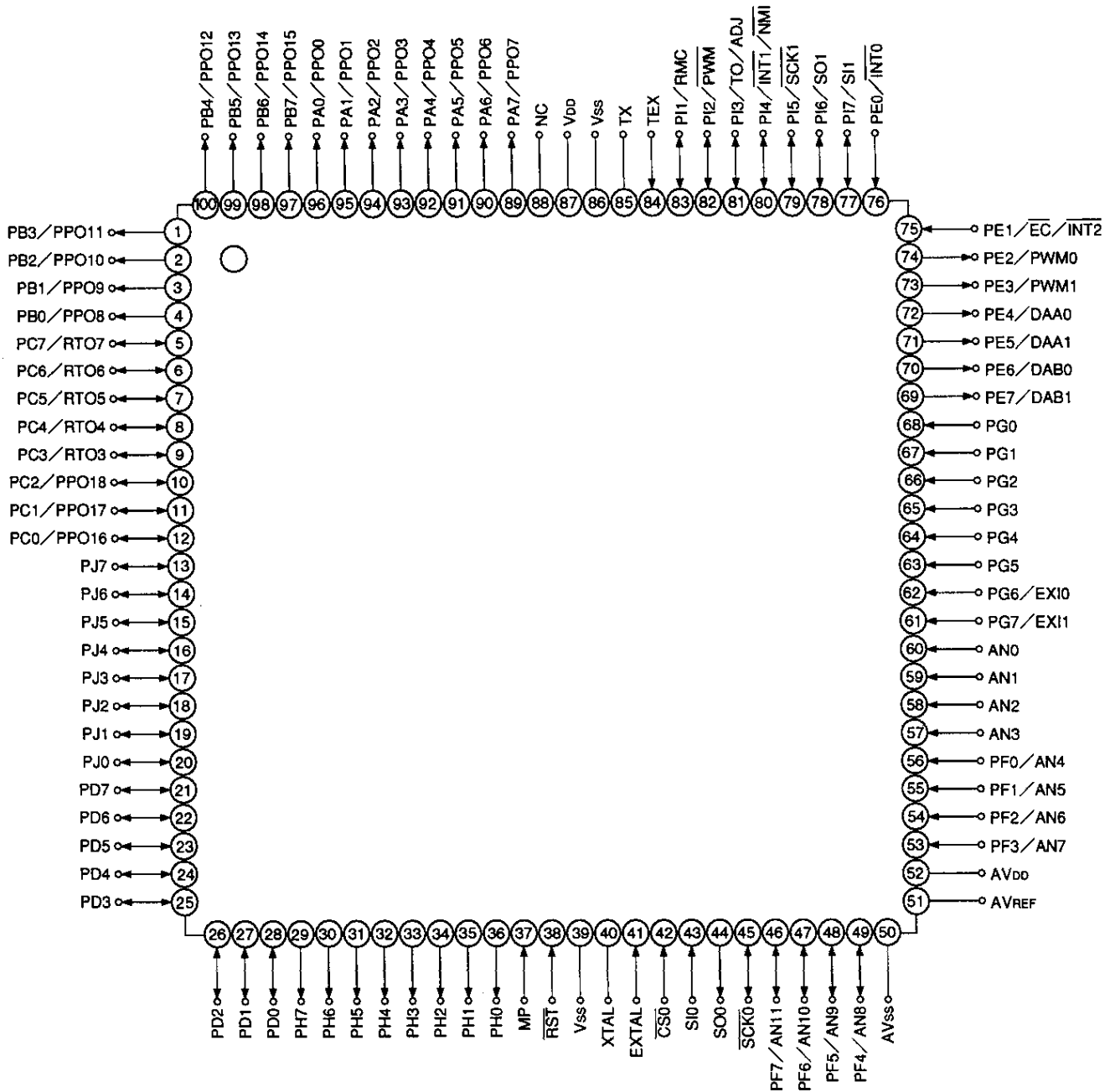
Block Diagram

Pin Configuration 1 (Top View) 100 pin QFP package



- Note)** 1. NC (Pin 90) is always connected to VDD.
 2. VSS (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100 pin LQFP package



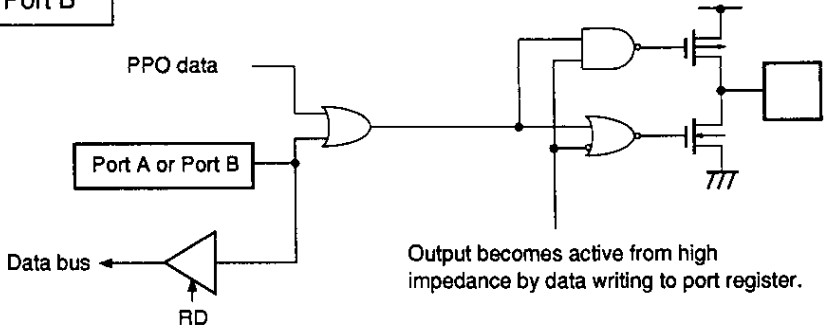
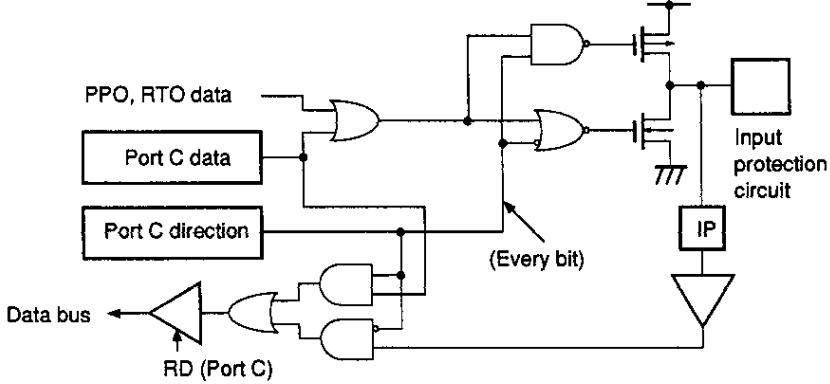
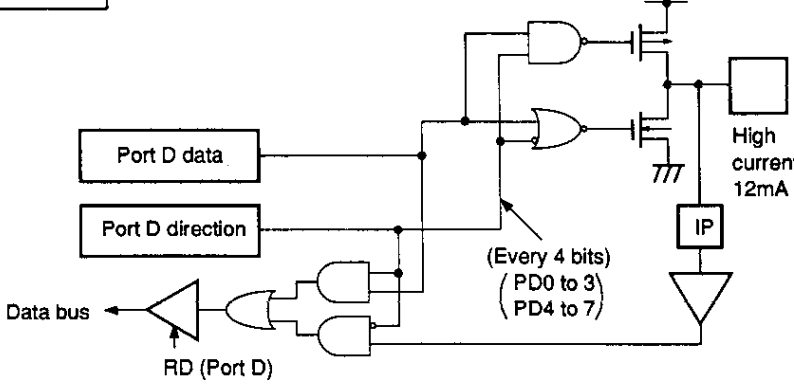
- Note)**
1. NC (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 86) are both connected to GND.

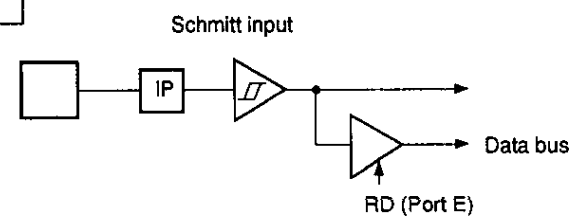
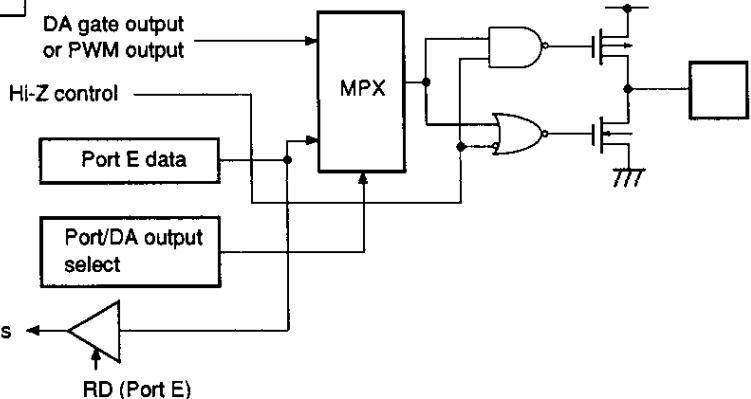
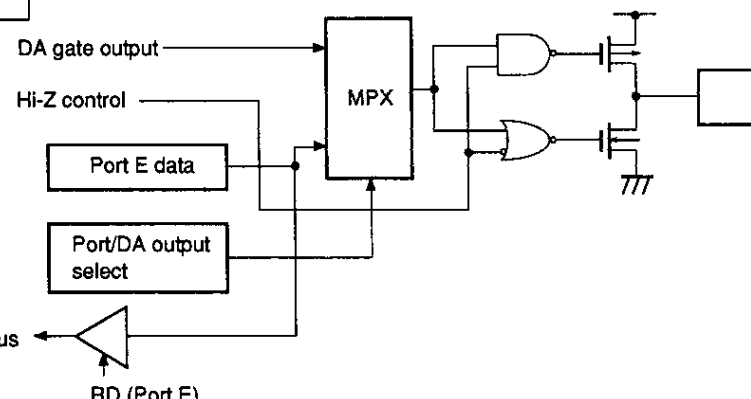
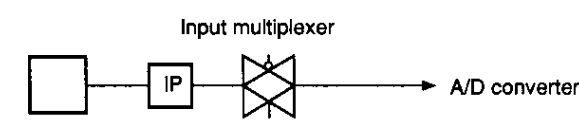
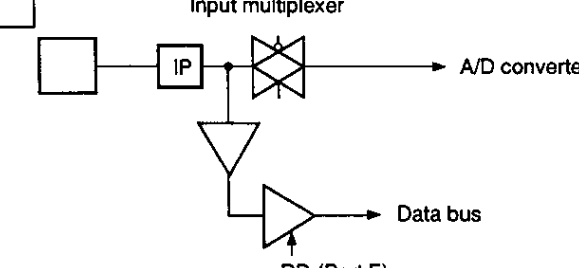
Pin Description

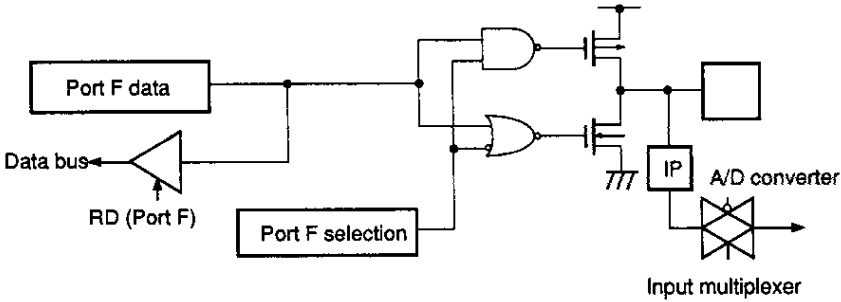
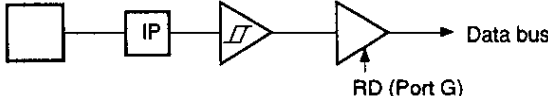
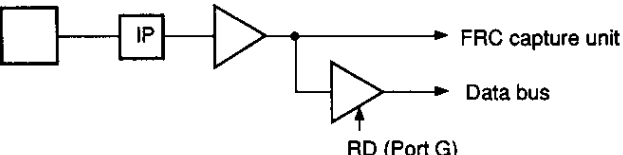
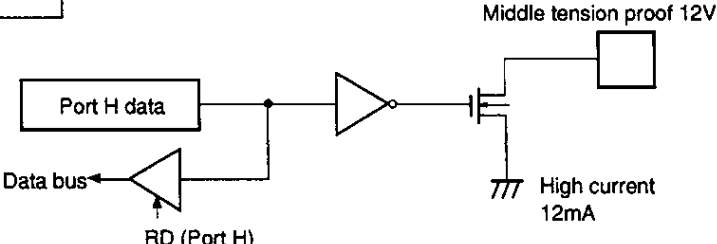
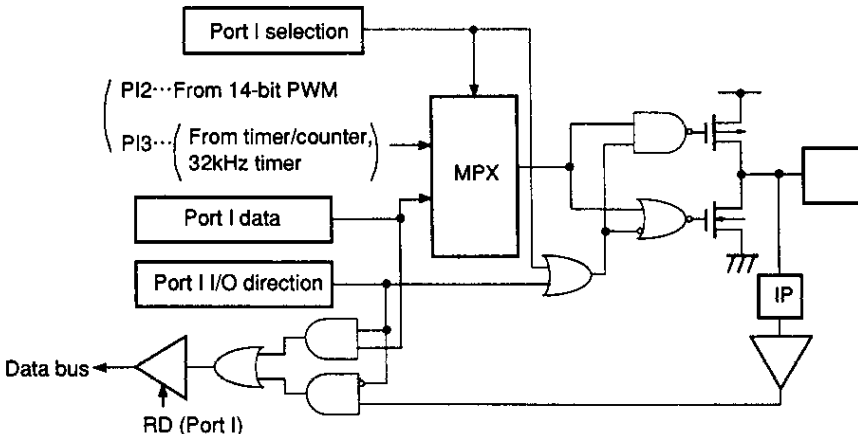
Symbol	I/O	Description	
PA0/PPO0 to PA7/PPO7	Output/ Real time Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)
PB0/PPO8 to PB7/PPO15	Output/ Real time Output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	
PC0/PPO16 to PC2/PPO18	I/O/ Real time Output	(Port C) 8-bit I/O port, enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)	
PC3/RTO3 to PC7/RTO7	I/O/ Real time Output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (8 pins)	
PE0/ $\overline{\text{INT0}}$	Input/input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$	Input/input/input		External event input pin for timer/counter. Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/output		PWM output pins. (2 pins)
PE3/PWM1	Output/output		
PE4/DAA0	Output/output		DA gate pulse output pins. (4 pins)
PE5/DAA1	Output/output		
PE6/DAB0	Output/output		
PE7/DAB1	Output/output		
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)	
PF0/AN4 to PF3/AN7	Input/input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)	
PF4/AN8 to PF7/AN11	Output/input		
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.	
SO0	Output	Serial data (CH0) output pin.	
SI0	Input	Serial data (CH0) input pin.	
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.	

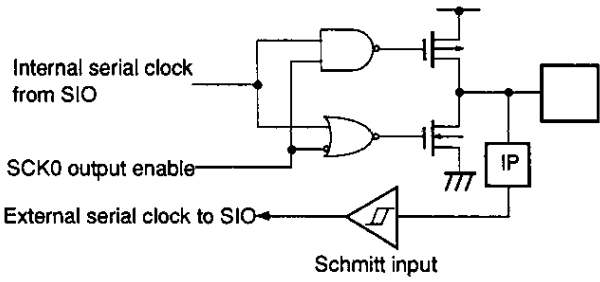
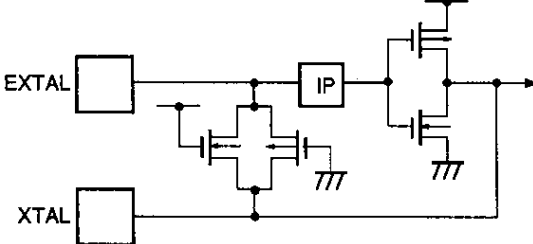
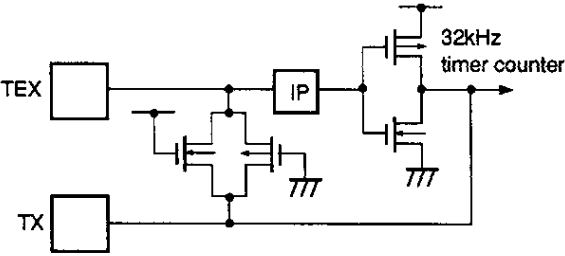
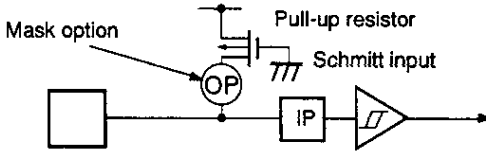
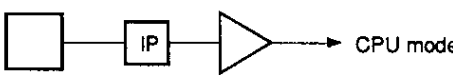
Symbol	I/O	Description	
PG0 to PG5	Input	(Port G) 8-bit input port. (8 pins)	External input pin to FRC capture unit.
PG6/EXI0	Input/input		
PG7/EXI1	Input/input		
PH0 to PH7	Output	(Port H) N-ch open drain output of middle tension proof (12V) and high current (12mA). (8 pins)	
PI1/RMC	I/O/input	(Port I) 7-bit I/O port. I/O port can be specified by the bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/PWM	I/O/output		14-bit PWM output pin.
PI3/TO/ADJ	I/O/output/output		Timer/counter, 32kHz oscillation adjustment output pin.
PI4/ $\overline{\text{INT1}}$ / NMI	I/O/input/input		Input pin to request external interruption and non maskable interruption. Active when falling edge.
PI5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/output		Serial data (CH1) output pin.
PI7/SI1	I/O/input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by the bit unit. I/O can be specified by the bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active "Low" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AVDD		Positive power supply pin of A/D converter.	
AVREF	Input	Reference voltage input pin of A/D converter.	
AVSS		GND pin of A/D converter.	
VDD		Positive power supply pin.	
VSS		GND pin. Connect both Vss pins to GND.	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15</p> <p>16 pins</p>	 <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>Port C</p> <p>PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7</p> <p>8 pins</p>	 <p>(Every bit)</p>	<p>Hi-Z</p>
<p>Port D</p> <p>PD0 to PD7</p> <p>8 pins</p>	 <p>(Every 4 bits) (PD0 to 3) (PD4 to 7)</p> <p>High current 12mA</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{EC}}/\overline{\text{INT2}}$</p> <p>2 pins</p>	<p>Port E</p>  <p>Schmitt input</p> <p>IP</p> <p>RD (Port E)</p> <p>Data bus</p>	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p>  <p>DA gate output or PWM output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output select</p> <p>MPX</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p>  <p>DA gate output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output select</p> <p>MPX</p> <p>Data bus</p> <p>RD (Port E)</p>	<p>H level</p>
<p>AN0 to AN3</p> <p>4 pins</p>	 <p>Input multiplexer</p> <p>IP</p> <p>A/D converter</p>	<p>Hi-Z</p>
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p>  <p>Input multiplexer</p> <p>IP</p> <p>A/D converter</p> <p>Data bus</p> <p>RD (Port F)</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>Port F data</p> <p>Data bus</p> <p>RD (Port F)</p> <p>Port F selection</p> <p>IP</p> <p>A/D converter</p> <p>Input multiplexer</p>	<p>Hi-Z</p>
<p>PG0 to PG5</p> <p>6 pins</p>	<p>Port G</p>  <p>Schmitt input</p> <p>IP</p> <p>Data bus</p> <p>RD (Port G)</p> <p>Note) For PG4 and PG5, CMOS schmitt input or TTL schmitt input can be selected with the mask option.</p>	<p>Hi-Z</p>
<p>PG6/EXI0 PG7/EXI1</p> <p>2 pins</p>	<p>Port G</p>  <p>IP</p> <p>FRC capture unit</p> <p>Data bus</p> <p>RD (Port G)</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Port H data</p> <p>Data bus</p> <p>RD (Port H)</p> <p>Middle tension proof 12V</p> <p>High current 12mA</p>	<p>Hi-Z</p>
<p>PI2/PWM PI3/TO/ADJ</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I selection</p> <p>PI2...From 14-bit PWM</p> <p>PI3...From timer/counter, 32kHz timer</p> <p>MPX</p> <p>Port I data</p> <p>Port I I/O direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>$\overline{\text{SCK0}}$</p> <p>1 pin</p>	 <p>Internal serial clock from SIO</p> <p>SCK0 output enable</p> <p>External serial clock to SIO</p> <p>Schmitt input</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL becomes "H" level. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>L level</p>
<p>MP</p> <p>1 pin</p>	 <p>CPU mode</p>	<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Medium withstand output voltage	V _{OUTP}	-0.3 to +15.0	V	PH pin
High level output current	I _{OH}	-5	mA	
High level total output current	Σ I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than high current output pins: per pin
	I _{OLC}	20	mA	High current port pin* ³ : per pin
Low level total output current	Σ I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package type
		380		LQFP package type

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD}+0.3V.

*3) The high current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS}=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input*4
	V _{IHEX}	V _{DD} -0.4	V _{DD} +0.3	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3
	V _{ILTS}	0	0.8	V	TTL schmitt input*4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	Topr	-20	+75	°C	

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) Normal input port (each pin of PC, PD, PE0, PE1, PF0 to PF3, PG, PI and PJ), MP pin.

*3) Each pin of CS0, SI0, SCK0, RST, PE0/INT0, PE1/EC/INT2, PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option), PI1/RMC, PI4/INT1/NMI, PI5/SCK1 and PI7/SI1.

*4) Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5) It specifies only when the external clock is input.

*6) It specifies only when the event count clock is input.

Electrical Characteristics

DC Characteristics (V_{DD}=4.5 to 5.5V)

(T_a=-20 to +75°C, V_{SS}=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V _{OL} only)	V _{DD} =4.5V, I _{OH} =-0.5mA	4.0			V
			V _{DD} =4.5V, I _{OH} =-1.2mA	3.5			V
Low level output voltage	V _{OL}	PI1 to PI7, PJ, SO0, SCK0	V _{DD} =4.5V, I _{OL} =1.8mA			0.4	V
			V _{DD} =4.5V, I _{OL} =3.6mA			0.6	V
		PD, PH	V _{DD} =4.5V, I _{OL} =12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} =5.5V, V _{IH} =5.5V	0.5		40	μA
	I _{ILE}		V _{DD} =5.5V, V _{IL} =0.4V	-0.5		-40	μA
	I _{IHT}	TEX	V _{DD} =5.5V, V _{IH} =5.5V	0.1		10	μA
	I _{ILT}		V _{DD} =5.5V, V _{IL} =0.4V	-0.1		-10	μA
	I _{ILR}		RST*1	-1.5		-400	μA
I/O leakage current	I _{Iz}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, RST*1	V _{DD} =5.5V, V _I =0, 5.5V			±10	μA
Open drain output leakage current (N-CH Tr OFF in state)	I _{LOH}	PH	V _{DD} =5.5V, V _{OH} =12V			50	μA
Supply current*2	I _{DD1}	V _{DD}	16MHz crystal oscillation (C ₁ =C ₂ =15pF)		22	45	mA
			V _{DD} =5V±0.5V*3				
	I _{DDs1}		SLEEP mode		1.1	8	mA
			V _{DD} =5V±0.5V				
	I _{DD2}		32kHz crystal oscillation (C ₁ =C ₂ =47pF)		35	100	μA
			V _{DD} =3V±0.3V				
	I _{DDs2}		SLEEP mode		9	30	μA
V _{DD} =3V±0.3V							
I _{DDs3}	STOP mode (EXTAL and TEX pins oscillation stop)			10	μA		
		V _{DD} =5V±0.5V					
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) RST pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2) When entire output pins are open.

*3) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta=-20 to +75°C, VDD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1	16	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	28		ns
System clock input rise and fall times	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	t _{EH} , t _{EL}	\overline{EC}	Fig. 3	t _{sys} x 4*		ns
Event count clock input rise and fall times	t _{ER} , t _{EF}	\overline{EC}	Fig. 3		20	ns
System clock frequency	fc	TEX TX	Fig. 2 VDD=2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz
Event count clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10		μs
Event count clock input rise and fall times	t _{TR} , t _{TF}	TEX	Fig. 3		20	ms

* t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns]=2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

Fig. 1. Clock timing

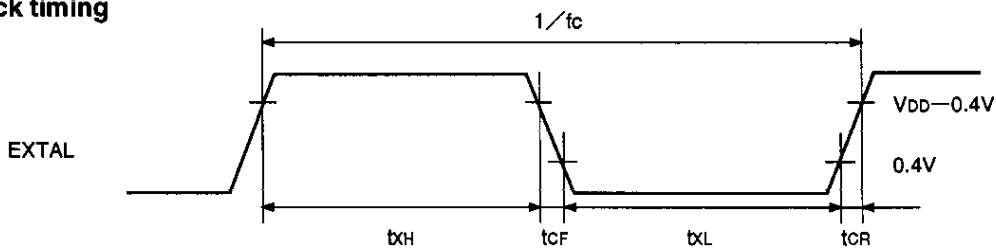


Fig. 2. Clock applied condition

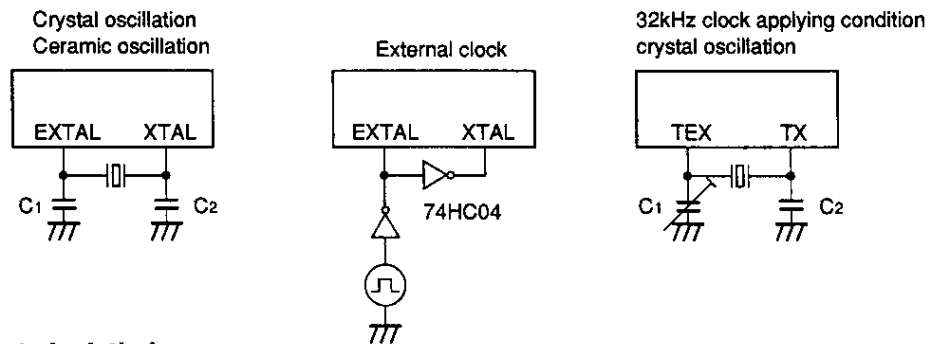
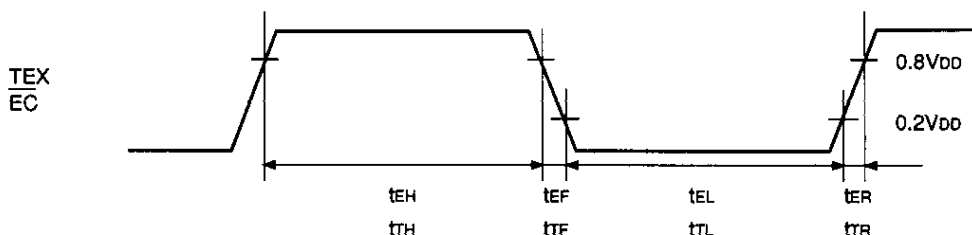


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta=-20 to +75°C, VDD=4.5 to 5.5V, VSS=0V)

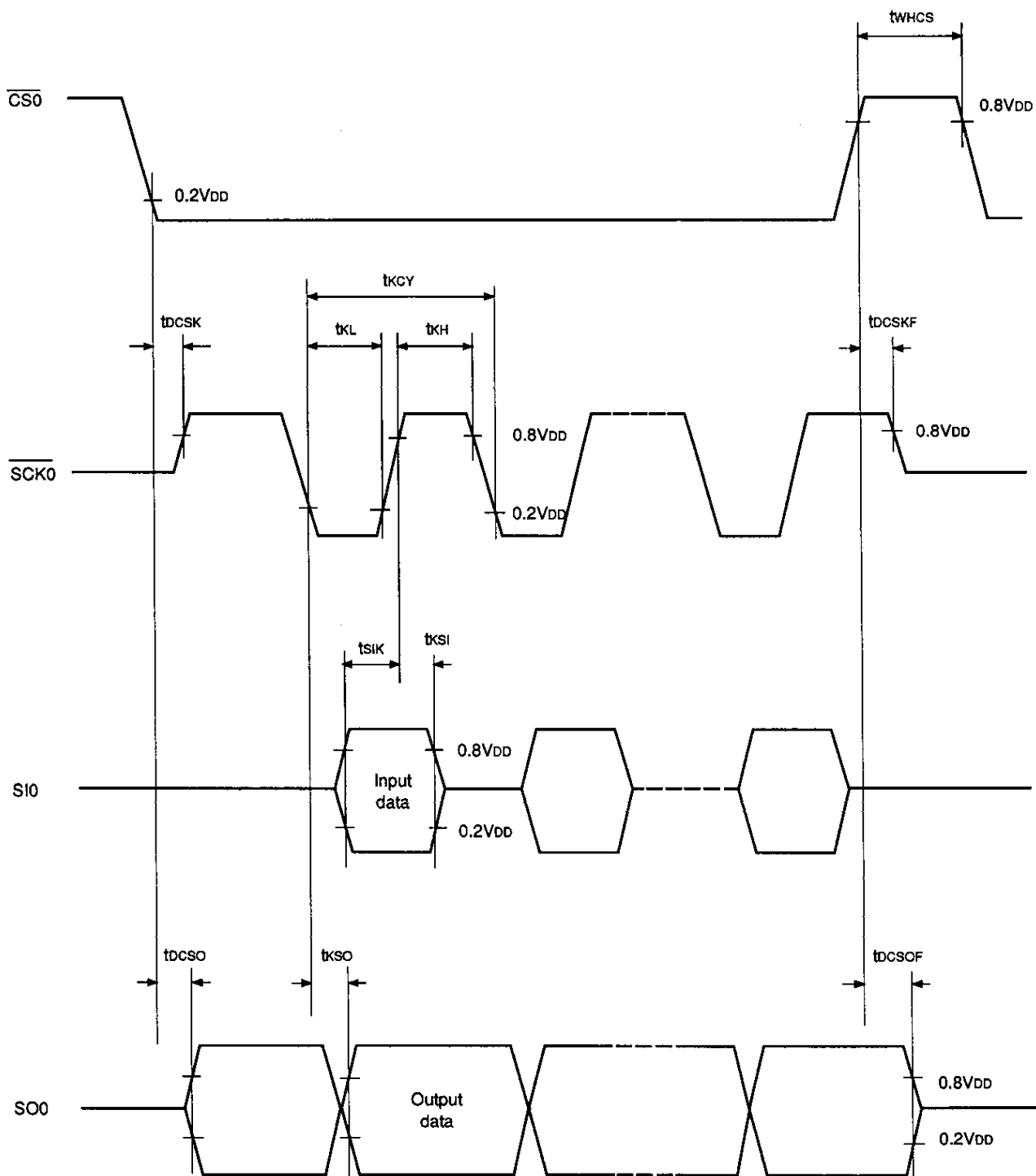
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ =output mode)		t _{sys} +200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ =output mode)		t _{sys} +200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} +200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} +200	ns
$\overline{\text{CS0}}$ high level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} +200		ns
$\overline{\text{SCK0}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} +200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ high and low level widths	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} +100		ns
			Output mode	8000/fc-50		ns
SIO input setup time (against $\overline{\text{SCK0}} \uparrow$)	t _{SIK}	SIO	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SIO input hold time (against $\overline{\text{SCK0}} \uparrow$)	t _{SI}	SIO	$\overline{\text{SCK0}}$ input mode	t _{sys} +200		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		t _{sys} +200	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns]=2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is 50pF+1TTL.

Fig. 4. Serial transfer CH0 timing



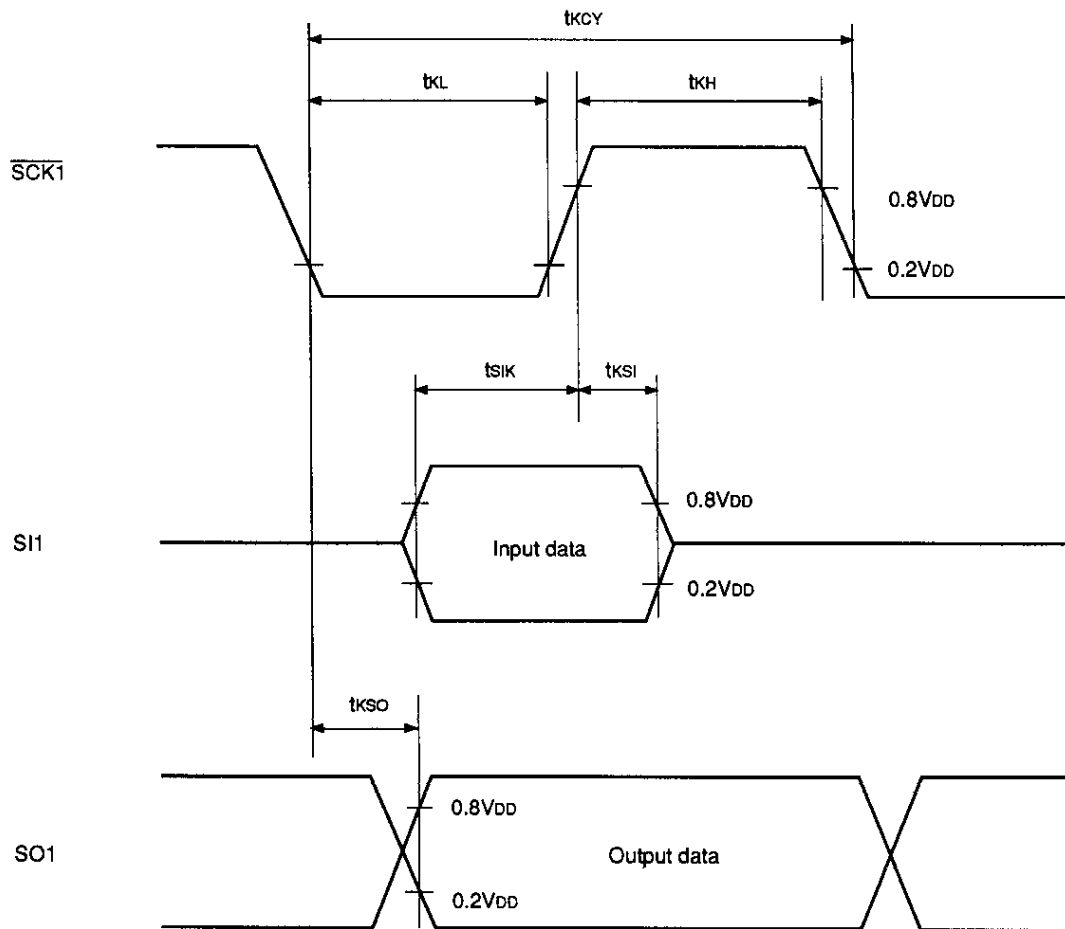
Serial transfer (CH1)

(Ta=-20 to +75°C, VDD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{CY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	8000/fc-50		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ \uparrow)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ \uparrow)	t_{SIL}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ \downarrow \rightarrow SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF+1TTL.

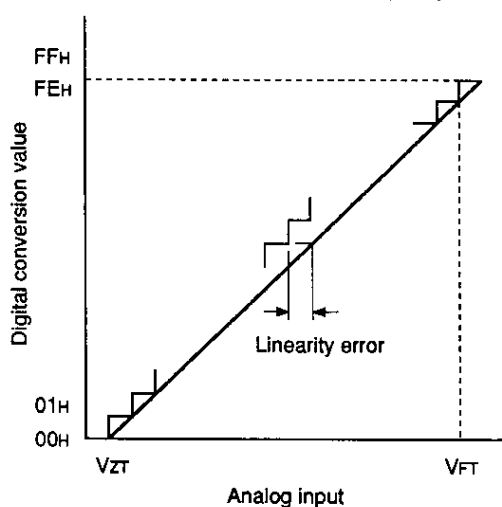
Fig. 5. Serial transfer CH1 timing



(3) A/D converter characteristics (Ta=-20 to +75°C, VDD=AVDD=4.5 to 5.5V, AVREF=4.0 to AVDD, VSS=AVSS=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta=25°C VDD=AVDD=AVREF=5.0V VSS=AVSS=0V			±1	LSB
Absolute error						±2	LSB
Conversion time	tCONV			160/fADC*			µs
Sampling time	tSAMP			12/fADC*			µs
Reference input voltage	VREF	AVREF	VDD=AVDD=4.5 to 5.5V	AVDD-0.5		AVDD	V
Analog input voltage	VIAN	AN0 to AN11		0			V
AVREF current	IREF	AVREF	Operating mode		0.6	1.0	mA
	IREFS		SLEEP mode STOP mode 32kHz operating mode			10	µA

Fig. 6. Definitions of A/D converter terms



* The value of fADC is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
 When PS2 is selected, fADC=fc/2
 When PS1 is selected, fADC=fc

(4) Interruption, reset input

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$ PJ0 to PJ7		1		μs
	t_{IL}					
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 7. Interruption input timing

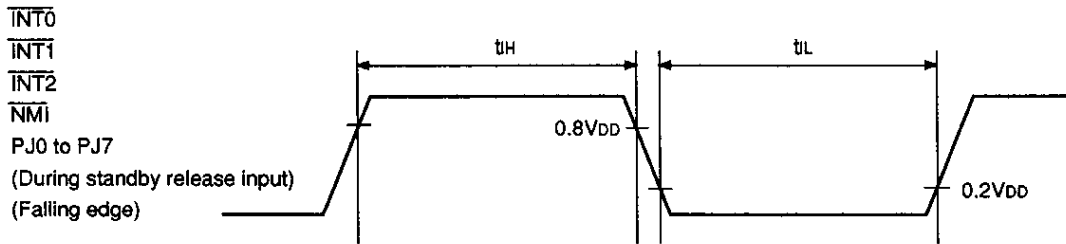
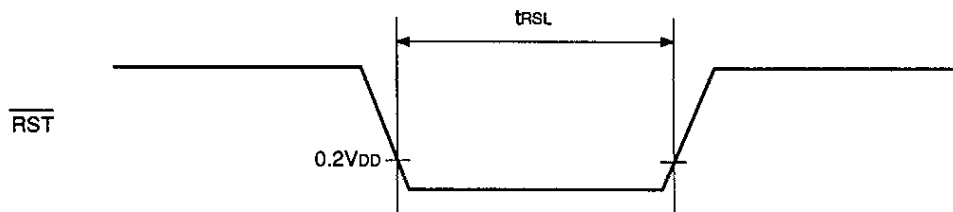


Fig. 8. Reset input timing



(5) Others

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

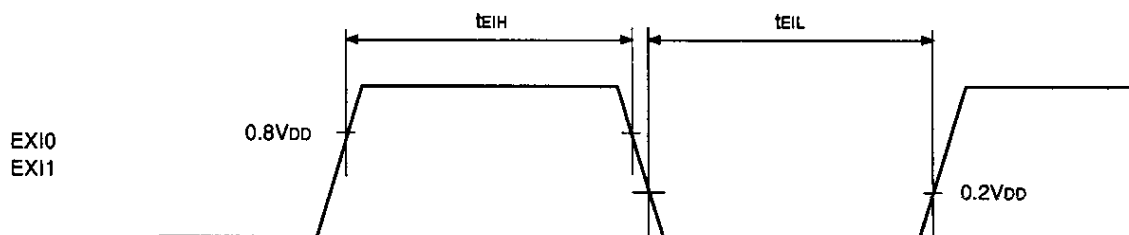
Item	Symbol	Pin	Condition	Min.	Max.	Unit
EX1 input high and low level width	t_{EIH}	EX10	$t_{\text{sys}} = 2000/f_c$	$t_{\text{sys}} + 200$		ns
	t_{EIL}	EX11				

Note t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2-bit="00"), 4000/ f_c (Upper 2-bit="01"), 16000/ f_c (Upper 2-bit="11")

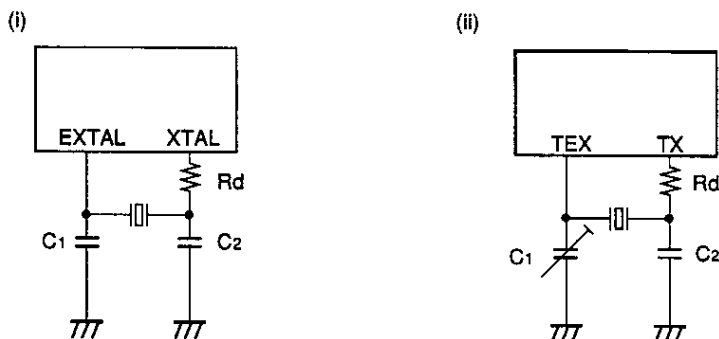
t_{FRC} [ns] = 1000/ f_c

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16	12	0	(i)
		10.00	16	12		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

Mask option table

Item	Content	
	Reset pin pull-up resistor	Non-existent
Input circuit format*	CMOS schmitt	TTL schmitt

* The input circuit format can be selected each for PG4 pin and PG5 pin.

Characteristics Curve

