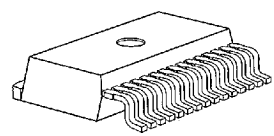
SIEMENS

TrilithIC™ **BTS 780**

Target Data

Overview



P-TO263-15-1

Features

- Quad switch driver
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Ultra low $R_{DS\,ON}$ @ 25 °C:
  High-side switch: typ. 35 mΩ,
  Low-side switch: typ. 15 mΩ
- Very high peak current capability
- Very low quiescent current
- Space- and thermal optimized SMD-Power-Package
- Load and GND-short-circuit-protected
- Operates up to 40 V
- 2-Bit status flag diagnosis
- Overtemperature shut down with hysteresis
- Short-circuit detection and diagnosis
- Open-load detection and diagnosis
- C-MOS compatible inputs
- Internal clamp diodes
- Isolated sources for external current sensing
- Over- and under-voltage detection with hysteresis

Type	Ordering Code	Package
BTS 780	on request	P-TO263-15-1

Description

The **BTS 780** is a **TrilithIC** contains one double high-side switch and two low-side switches in **one P-TO263-15-1**.

"Silicon instead of heatsink"
becomes true

The ultra low $R_{DS\,ON}$ of this device avoids powerdissipation. It saves costs in mechanical construction and mounting and increases the efficiency.

The high-side switches are produced in the **SIEMENS SMART SIPMOS®** technology. It is fully protected and contains the signal conditioning circuitry for diagnosis (the comparable standard high-side product is the **BTS 734L1**).

For minimized $R_{DS\,ON}$ the two low-side switches are produced in the **SIEMENS S-Fet** logic level technology (the comparable standard product is the **BUZ 100SL**).

Each drain of these three chips is mounted on separated leadframes (see pin configuration). The sources of all four power transistors are connected to separate pins.

So the **BTS 780** can be used in H-Bridge configuration as well as in any other switch configuration.

Moreover, it is possible to add current sense resistors.

All these features open a broad range of automotive and industrial applications.

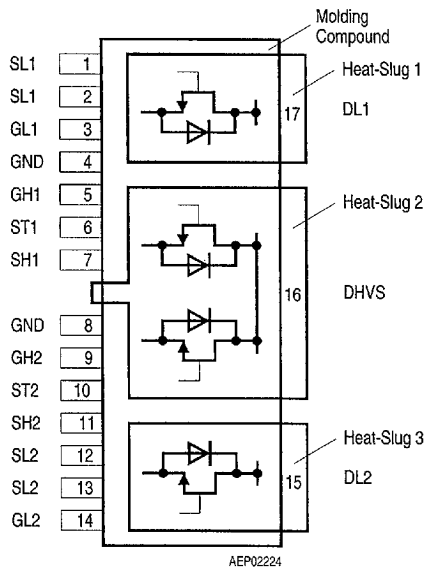


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1, 2	**SL1**	**Source of low-side switch 1**
3	GL1	Gate of low-side switch 1
4, 8	GND	Ground
5	GH1	Gate of high-side switch 1
6	ST1	Status of high-side switch 1; open Drain output
7	**SH1**	**Source of high-side switch 1**
9	GH2	Gate of high-side switch 2
10	ST2	Status of high-side switch 2; open Drain output
11	**SH2**	**Source of high-side switch 2**
12, 13	**SL2**	**Source of low-side switch 2**
14	GL2	Gate of low-side switch 2
15	**DL2**	**Drain of low-side switch 2** **Heat-Slug 3 or Heat-Dissipator**
16	**DHVS**	**Drain of high-side switches and power supply voltage** **Heat-Slug 2 or Heat-Dissipator**
17	**DL1**	**Drain of low-side switch 1** **Heat-Slug 1 or Heat-Dissipator**

Bold type: Pin needs power wiring

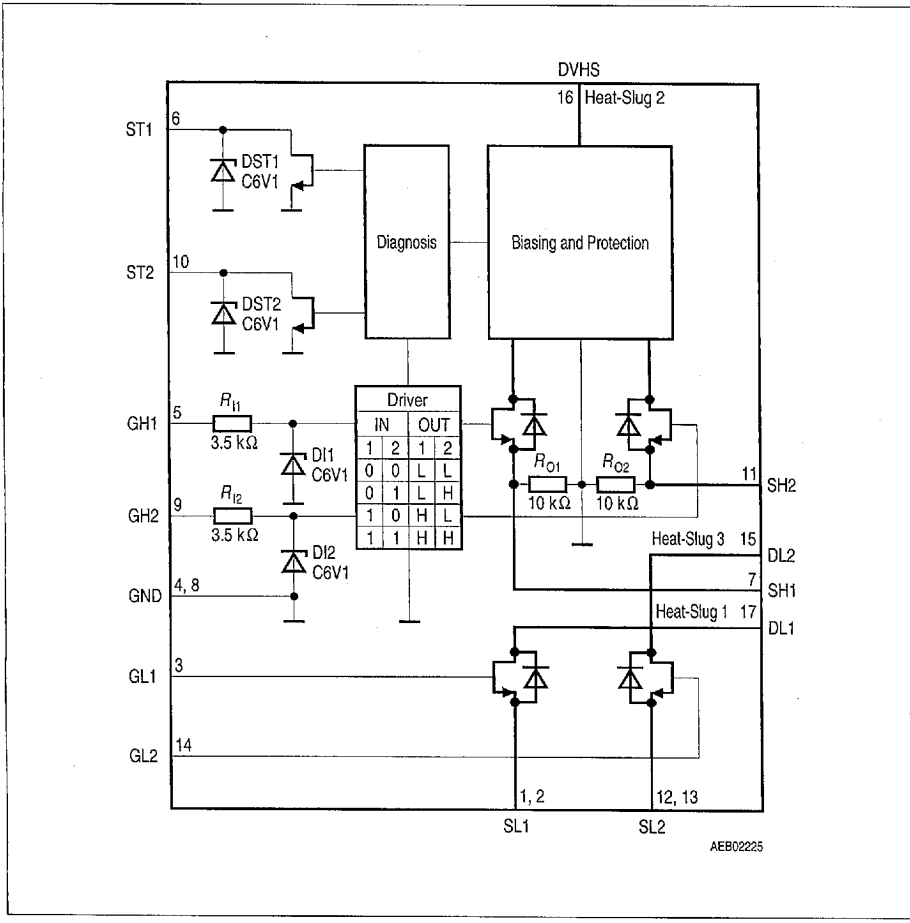


Figure 2 Block Diagram

Circuit Description

Input Circuit

The control inputs GH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages.

The inputs GH1 and GH2 are connected to a standard N-channel logic level power-MOS gate.

Output Stages

The output stages consist of an ultra low $R_{DS\,ON}$ Power-MOS H-Bridge. Protective circuits make the outputs short-circuit proof to ground and load short-circuit proof. Positive and negative voltage spikes, which occur when driving inductive loads, are limited by integrated power clamp diodes.

Short-Circuit Protection (valid only for the high-side switches)

The outputs are protected against

- output short circuit to ground, and
- overload (load short circuit).

An internal OP-Amp controls the Drain-Source-Voltage of the HS-Switches by comparing the DS-Voltage-Drop with an internal reference voltage. Above this trippoint the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

In the case of an overloaded high-side switch the corresponding status output is set to low.

If the HS-Switches are in OFF-state-Condition internal resistors $R_{O1,2}$ from SH1,2 to GND pull the voltage at SH1,2 to low values. On each output pin SH1 and SH2 an output examiner circuit compares the output voltages with the internal reference voltage VEO. This results in switching the corresponding status output to low if the source voltage in OFF-Condition is higher then VEO. In H-Bridge condition this feature can be used to protect the low-side switches against short circuit during the OFF-period.

Overtemperature Protection (valid only for the high-side-switches)

The chip also incorporates an overtemperature protection circuit with hysteresis which switches off the output transistors and sets the status output to low.

Under-Voltage-Lockout (UVLO)

When V_S reaches the switch-on voltage $V_{UV\,ON}$ the IC becomes active with a hysteresis. The High-Side output transistors are switched off if the supply voltage V_S drops below the switch off value $V_{UV\,OFF}$.

Over-Voltage-Lockout (OVLO)

When V_S reaches the switch-off voltage $V_{OV\,OFF}$ the High-Side output transistors are switched off with a hysteresis. The IC becomes active if the supply voltage V_S drops below the switch-on value $V_{OV\,ON}$.

Open Load Detection

Open load is detected by current measurement. If the output current drops below an internal fixed level the error flag is set with a delay.

Status Flag

Various errors as listed in the table "Diagnosis" are detected by switching the open drain outputs ST1 or ST2 to low.

Truthtable and Diagnosis (valid only for the High-Side-Switches)

Flag	GH1	GH2	SH1	SH2	ST1	ST2	Remarks
	Inputs		Outputs				
	0	0	L	L	1	1	stand-by mode
Normal operation;	0	1	L	H	1	1	switch1 active
identical with functional truth table	1	0	H	L	1	1	switch2 active
	1	1	H	H	1	1	both switches active
Open load at high-side switch1	0	0	Z	L	1	1	
	0	1	Z	H	1	1	
	1	X	H	X	0	1	detected
Open load at high-side switch2	0	0	L	Z	1	1	
	1	0	H	Z	1	1	
	X	1	X	H	1	0	detected
Short circuit to DHVS at high-side switch1	0	0	H	L	0	1	detected
	0	1	H	H	1	1	
	1	X	H	X	1	1	
Short circuit to DHVS at high-side switch2	0	0	L	H	1	0	detected
	1	0	H	H	1	1	
	X	1	X	H	1	1	
Overtemperature high-side switch1	0	X	L	X	1	1	
	1	X	L	X	0	1	detected
Overtemperature high-side switch2	X	0	X	L	1	1	
	X	1	X	L	1	0	detected
Overtemperature both high-side switch	0	0	L	L	1	1	
	X	1	L	L	0	0	detected
	1	X	L	L	0	0	detected
Over- and Under-Voltage	X	X	L	L	1	1	not detected

Inputs:
0 = Logic LOW
1 = Logic HIGH
X = don't care

Outputs:
Z = Output in tristate condition
L = Output in sink condition
H = Output in source condition
X = Voltage level undefined

Status:
1 = No error
0 = Error

Electrical Characteristics

Absolute Maximum Ratings

$-40\ °C < T_j < 150\ °C$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
High-Side-Switches (Pins DHVS, GH1,2 and SH1,2)					
Supply voltage	V_S	– 0.3	43	V	–
HS-drain current	I_{DHS}	– 30	*	A	* internally limited
HS-input current	I_{GH}	– 2	2	mA	Pin GH1 and GH2
HS-input voltage	V_{GH}	– 10	16	V	Pin GH1 and GH2
Status Output ST					
Status Output current	I_{ST}	– 5	5	mA	Pin ST1 and ST2
Low-Side-Switches (Pins DL1,2, GL1,2 and SL1,2)					
Break-down voltage	$V_{(BR)DSS}$	50	–	V	$V_{GS} = 0$ V; $I_D \leq 1$ mA
LS-drain current	I_{DLS}	–	30	A	–
LS-drain current	I_{DLS}	–	50	A	$t < 1$ ms; v < 0.1
IS-input voltage	V_{GL}	– 10	14	V	Pin GL1 and GL2
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Thermal Resistances (one HS-LS-Path active)					
LS-junction case	R_{thjCLS}	–	tbd	K/W	measured to pin 15 or 17
HS-junction case	R_{thjCHS}	–	tbd	K/W	measured to pin 16
Junction ambient	R_{thja}	–	50	K/W	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\,OFF}$	34	V	After V_S rising above $V_{UV\,ON}$
Input voltages	V_{GH}	– 0.3	15	V	–
Input voltages	V_{GL}	– 9	13	V	–
Status output current	I_{ST}	0	2	mA	Pin ST1 or ST2
HS-junction temperature	T_{jHS}	– 40	150	°C	–
LS-junction temperature	T_{jLS}	– 40	150	°C	–

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; -40 °C $< T_j <$ 150 °C; 8 V $> V_S >$ 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
Quiescent current	I_S	–	15	40	µA	GH1 = GH2 = L V_S = 13.2 V T_j = 25 °C
Quiescent current	I_S	–	–	50	µA	GH1 = GH2 = L V_S = 13.2 V
Supply current	I_S	–	2	4	mA	GH1 or GH2 = H
Supply current	I_S	–	4	8	mA	GH1 and GH2 = H
Under-Voltage-Lockout (UVLO)						
Switch-ON voltage	$V_{UV\,ON}$	–	–	7	V	V_S increasing
Switch-OFF voltage	$V_{UV\,OFF}$	3.5	–	–	V	V_S decreasing
Switch ON/OFF hysteresis	$V_{UV\,HY}$	–	0.2	–	V	$V_{UV\,ON} - V_{UV\,OFF}$
Over-Voltage-Lockout (OVLO)						
Switch-OFF voltage	$V_{OV\,OFF}$	34	–	43	V	V_S increasing
Switch-ON voltage	$V_{OV\,ON}$	33	–	–	V	V_S decreasing
Switch OFF/ON hysteresis	$V_{OV\,HY}$	–	0.5	–	V	$V_{OV\,OFF} - V_{OV\,ON}$

Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; -40 °C $< T_j <$ 150 °C; 8 V $> V_S >$ 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High-Side-Switches1, 2						
Static drain-source on-resistance	$R_{DS\ ON\ H}$	–	35	40	mΩ	$I_{SH} = 10$ A $T_j = 25$ °C
Static drain-source on-resistance	$R_{DS\ ON\ H}$	–	–	75	mΩ	$I_{SH} = 10$ A
Leakage current	I_{HSLK}	–	–	30	µA	$V_{GH} = V_{SH} = 0$ V
Clamp-diode forward-voltage	V_{FH}	–	0.8	1.5	V	$I_{FH} = 10$ A
Clamp-diode leakage-current ($I_{FH} + I_{SH}$)	I_{LKCL}	–	–	10	mA	$I_{FH} = 10$ A
Short Circuit to GND						
Initial peak SC current	I_{SCP}	47	55	66	A	$T_j = -40$ °C
Initial peak SC current	I_{SCP}	35	44	54	A	$T_j = 25$ °C
Initial peak SC current	I_{SCP}	28	35	44	A	$T_j = 85$ °C
Initial peak SC current	I_{SCP}	21	26	34	A	$T_j = 150$ °C
Short Circuit to V_S						
OFF-state examiner-voltage	V_{EO}	2	3	4	V	$V_{GH} = 0$ V
Output pull-down-resistor	R_O	4	10	30	kΩ	–
Open Circuit						
Detection current	I_{OCD}	0.01	–	1.2	A	–

Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; -40 °C $< T_j <$ 150 °C; 8 V $> V_S >$ 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching Times						
Switch-ON-time; to 90% V_{SH}	t_{ON}	–	–	0.5	ms	resistive load $I_{SH} = 10$ A; $V_S = 12$ V
Switch-OFF-time; to 10% V_{SH}	t_{OFF}	–	–	0.5	ms	resistive load $I_{SH} = 10$ A; $V_S = 12$ V
Control Inputs GH 1, 2						
H-input voltage threshold	V_{GHH}	–	–	3.5	V	–
L-input voltage threshold	V_{GHL}	1.5	–	–	V	–
Input voltage hysterese	V_{GHHY}	–	0.5	–	V	–
H-input current	I_{GHH}	20	50	90	µA	$V_{GH} = 5$ V
L-input current	I_{GHL}	1	–	50	µA	$V_{GH} = 0.4$ V
Input series resistance	R_I	2.5	3.5	6	kΩ	–
Zener limit voltage	V_{GHZ}	5.4	–	–	V	$I_{GH} = 1.6$ mA
Low-Side-Switches 1, 2						
Static drain-source on-resistance	$R_{DS\ ON\ L}$	–	15	18	mΩ	$I_{SL} = 10$ A; $V_{GL} = 5$ V $T_j = 25$ °C
Static drain-source on-resistance	$R_{DS\ ON\ L}$	–	–	35	mΩ	$I_{SH} = 10$ A
Leakage current	I_{LKL}	–	–	100	µA	$V_{GL} = 0$ V $V_{DS} = 18$ V
Clamp-diode forward-voltage	V_{FL}	–	0.8	1.5	V	$I_{FL} = 10$ A

Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; -40 °C $< T_j <$ 150 °C; 8 V $> V_S >$ 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Control Inputs GL1, 2						
Gate-threshold-voltage	$V_{GL(th)}$	0.6	1.6	2	V	$V_{GL} = V_{DSL}$; $I_{DL} = 100$ µA
Transconductance	g_{fs}	–	5	–	S	$V_{DSL} = 20$ V; $I_{DL} = 20$ A
Status Flag Output ST						
Low output voltage	V_{STL}	–	0.2	0.6	V	$I_{ST} = 1.6$ mA
Leakage current	I_{STLK}	–	–	10	µA	$V_{ST} = 5$ V
Zener-limit-voltage	V_{STZ}	5.4	–	–	V	$I_{ST} = 1.6$ mA
Thermal Shutdown						
Thermal shutdown junction temperature	T_{jSD}	150	–	190	°C	–
Thermal switch-on junction temperature	T_{jSO}	140	–	180	°C	–
Temperature hysteresis	ΔT	–	10	–	°C	$\Delta T = T_{jSD} - T_{jSO}$

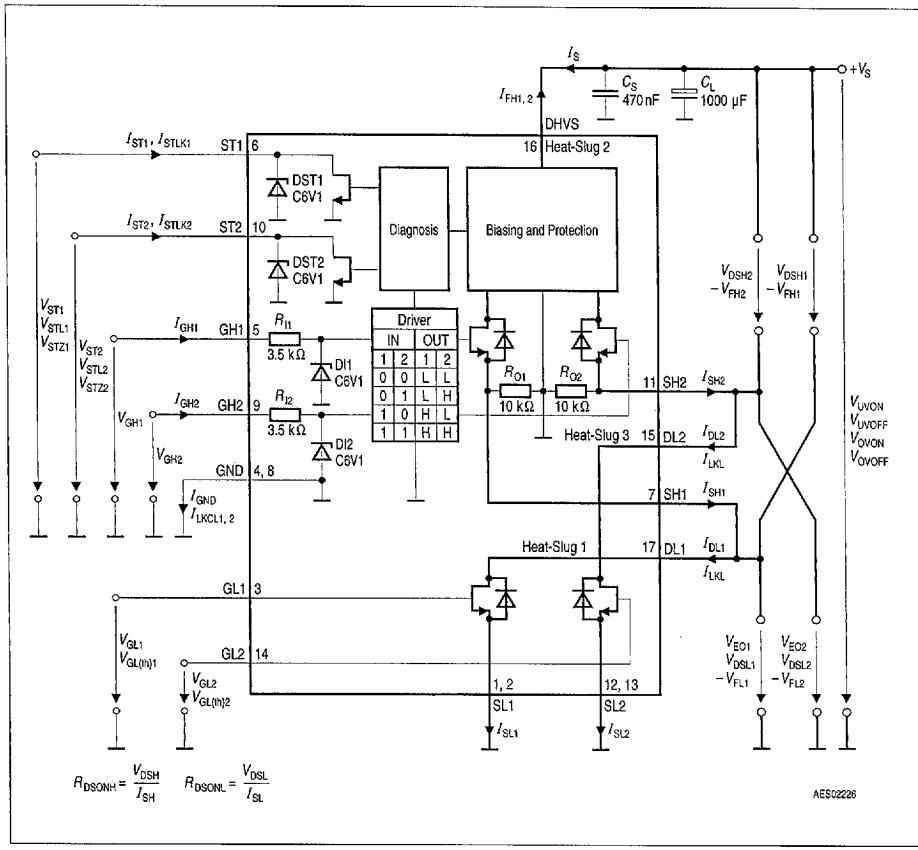


Figure 3 Test Circuit

HS-Source-Current	Named during Short Circuit	Named during Open Circuit	Named during Leakage-Cond.
$I_{SH1,2}$	I_{SCP}	I_{OCD}	I_{HSLK}

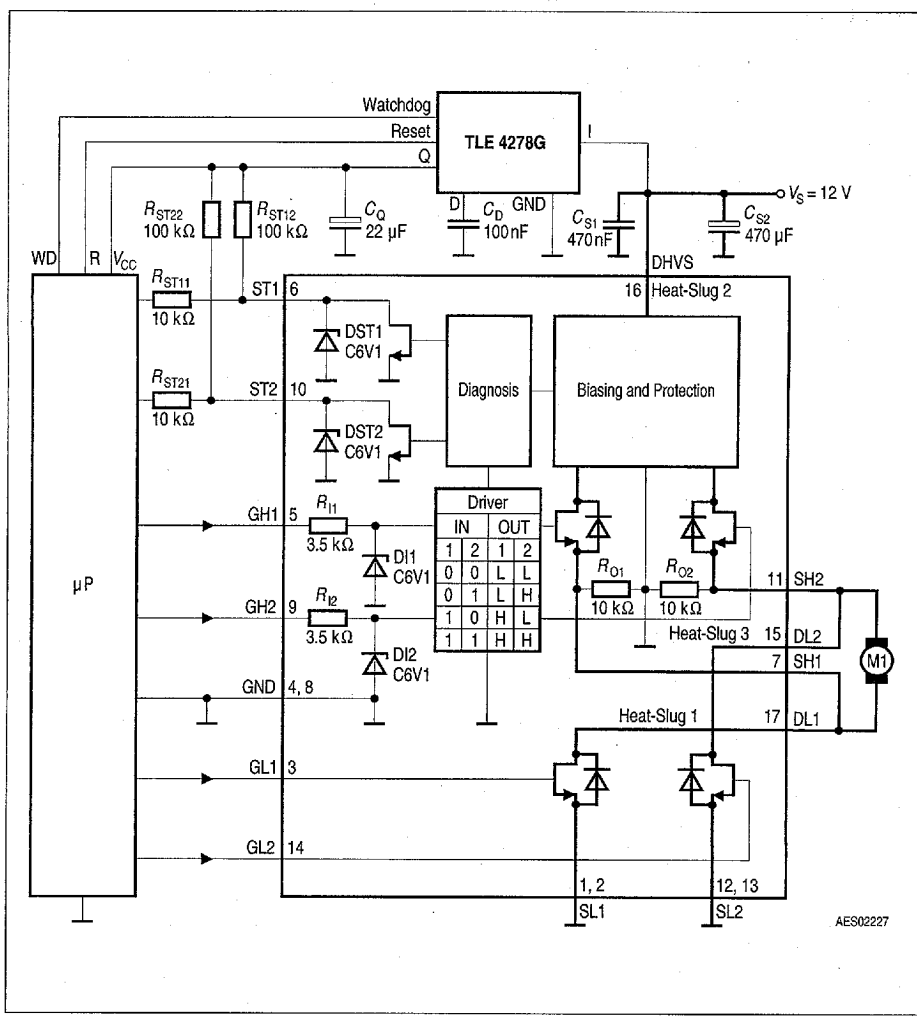
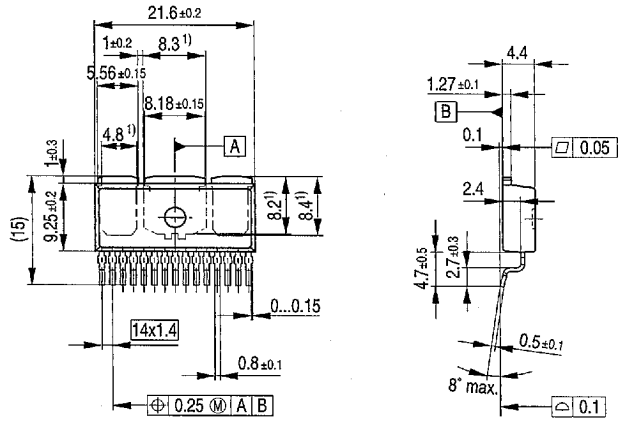


Figure 4 Application Circuit

Package Outlines

P-TO263-15-1
(Plastic Transistor Single Outline Package)



1) Typical
All metal surfaces tin plated, except area of cut.

GPT09151

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm