# AF9013/13S/13A/13AS/15/15A

## DVB-T COFDM DEMODULATOR

### Features

- Complete COFDM DVB-T demodulator single chip IC compliant with **ETSI EN 300 744** and **Nordig Unified 1.0.2**
- Superior dynamic multipath performance in **pre/post-echo,** and **long echo** environments
- Joint common phase error correction and channel estimation for low cost tuner support
- Integrated 10-bit ADC and PLL
- Dual AGC (RF and IF) control with 1-bit $\Sigma\Delta$ output
- Fully programmable RF/IF AGC **Take-Over-Point** (TOP) to work with any **Silicon/Can-tuner**
- Digital carrier frequency offset **±500KHz** correction
- Digital crystal frequency jitter **±100ppm** compensation
- All-digital time and frequency synchronization tracking loop
- Adaptive FFT window position tracking in mobile/portable environments
- Two-dimensional time-frequency channel estimation, tracking, and filtering for excellent fixed and mobile reception
- All-digital adjacent channel interference (ACI) filter for supporting 6/7/8MHz bandwidth with a single 8MHz SAW filter
- Adaptive co-channel interference (CCI) filter for PAL/SECAM/NICAM rejection
- Configurable IF sampling (high or low IF) from a single crystal frequency
- Comprehensive performance monitoring parameters available through register access
- Embedded **high-speed USB 2.0** interface compatible with USB1.1
- Supports USB **suspend** and **selective suspend** modes capable of entering **C3 mode** for notebook power-saving applications
- Complete **API C source code** for easy integration with most backend host processors
- Microsoft Broadcast Driver Architecture (**BDA**) driver support with **WHQL/MCE** certified and compliant for USB applications
- **IR** (Infrared) interface compliant with MCE RC6 protocol is supported for remote control using **HID** class
- Integrated transport stream **de-multiplexer** (32-entry **PID filtering**)
- Serial and parallel **MPEG2-TS interface output**
- Support **second MPEG2-TS input** for **PIP/PVR** applications
- Support **dual display** transport stream output from MPEG-TS and USB interfaces
- **Low power** consumption
- 56-pin QFN and 64-pin LQFP packages

### Applications

- Digital DVB-T **set-top boxes**
- Integrated digital DVB-T **televisions**
- **USB** bus-powered portable DVB-T receivers for PC desktops/notebooks
- **DVD recorders** with DVB-T receivers
- **PMC** (Personal Multimedia Center) or **PVR** (Personal Video Recorder) with DVB-T receivers

### Mobile Performance

- Doppler Tolerance for QEF at 8MHz with C/N=25dB (*AF9013/13A* and *AF9015/15A* only)

| | | | | |
|---|---|---|---|---|
| 2K | QPSK | CR1/2 | GI1/32 | 480Hz |
| 2K | 64QAM | CR1/2 | GI1/32 | 120Hz |
| 8K | 16QAM | CR2/3 | GI1/4 | 50Hz |

# Revision History

| Revision | Date | Description |
|---|---|---|
| 0.9 | 3/27/2006 | First Draft |
| 0.95 | 3/29/2006 | First Preliminary Release |
| 0.96 | 5/2/2006 | Editorial |
| 1.0 | 6/5/2006 | Filled in TBD items |
| 1.1 | 3/7/2007 | Add 9013A/9013AS/9015A |
| 1.2 | 12/19/2007 | Add Model No. AF9013S-N1* |
| 1.3 | 2/18/2008 | Remove asterisk (*) from model numbers |

# Ordering Information

| Model Number | Description | Package |
|---|---|---|
| AF9013-L2 | DVB-T COFDM Demodulator with MPEG interface | 64-pin LQFP, Pb-free |
| AF9013-N1 | DVB-T COFDM Demodulator with MPEG interface | 56-pin QFN, Pb free |
| AF9013S-N1 | DVB-T COFDM Demodulator with MPEG interface | 56-pin QFN, Pb free |
| AF9013S-L2 | DVB-T COFDM Demodulator with MPEG interface | 64-pin LQFP, Pb-free |
| AF9015-N1 | DVB-T COFDM Demodulator with USB interface | 56-pin QFN, Pb-free |
| AF9013A-L2 | DVB-T COFDM Demodulator with MPEG interface | 64-pin LQFP, Pb-free |
| AF9013A-N1 | DVB-T COFDM Demodulator with MPEG interface | 56-pin QFN, Pb free |
| AF9013AS-L2 | DVB-T COFDM Demodulator with MPEG interface | 64-pin LQFP, Pb-free |
| AF9015A-N1 | DVB-T COFDM Demodulator with USB interface | 56-pin QFN, Pb-free |

Unless otherwise specified, in the following context the description for AF9013 applies for AF9013A, the description for AF9013S applies for AF9013AS, and description for AF9015 applies to AF9015A.

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# 1 Description

The *AF9013/13S/15* DVB-T COFDM demodulator is a versatile second-generation single-chip IC that supports multiple interfaces including serial and parallel MPEG2-TS and embedded USB 2.0 interface with built-in de-multiplexer. It is compliant with both ETSI EN 300 744 and Nordig Unified 1.0.2, and it can operate at 2K or 8K mode with 6, 7, or 8MHz bandwidth. All modulations (QPSK, 16QAM, 64QAM), code rates (1/2, 2/3, 3/4, 5/6, 7/8), and guard intervals (1/4, 1/8, 1/16, 1/32) are supported and automatically detected from the TPS parameters.

*AF9013/13S/15* integrates a 10-bit analog-to-digital converter (ADC) capable of delivering the performance required for all modulations and code rates of DVB-T. It supports direct sampling of IF (*e.g.*, 36.125 MHz or 43.75 MHz) or low IF (*e.g.*, 4.57MHz) signals.

The device uses the most advanced digital signal processing techniques to combat various impairments encountered in fixed, portable, and mobile DVB-T channels.

*AF9013/13S/15* provides single AGC or dual RF/IF AGC control options for maximal flexibility in tuner selections. The AGC control loop bandwidth is designed to track a wide dynamic range of the received signal levels for slow or fast channel variations.

In *AF9013/13S/15,* an active impulse noise rejection algorithm removes the detrimental effects of the impulse noise and significantly improves the robustness of TV reception against interference from vehicles and electrical appliances.

Co-channel interference is actively searched and rejected by a digital notch filter in *AF9013/13S/15*. The digital notch filter is enabled only when the interference is present to avoid any unnecessary signal loss. Adjacent channel interference is rejected by precisely controlled digital filters for 6, 7, and 8MHz bandwidth. This makes it possible to use a single 8MHz SAW filter independent of the bandwidth used.

The all-digital synchronization tracking loops of *AF9013/13S/15* are capable of recovering carrier frequency offsets as large as ±500 kHz and tolerating crystal jitters as large as ±100ppm. The adaptive FFT window position tracking loop in *AF9013/13S/15* accurately identifies pre-echo or post-echo multipath channels even in highly mobile environments. Therefore, inter-symbol interference (ISI) and inter-carrier interference (ICI) is greatly reduced.

In *AF9013/13S/15*, the common phase error caused by tuner phase noise is corrected by a joint channel estimation and phase noise tracking algorithm, thus enabling the use of low cost tuners. Besides, the multi-dimensional channel estimation and tracking scheme in *AF9013* and *AF9015* adaptively adjusts its internal parameters to reflect the different requirements in fixed, portable, or mobile channels. Hence, optimal performance can be achieved for all DVB-T applications. *AF9013S*, on the other hand, is optimized for performance in stationary environments.

*AF9013/13S/15* provides a comprehensive set of performance monitoring parameters accessible through the 2-wire bus. These parameters include signal strength and signal quality indicators, post-Viterbi bit error rate, Reed-Solomon packet error rate, TPS lock and MPEG Sync lock indicators, carrier and crystal offsets, and many more.

*AF9015* also includes a serial input interface for accepting a secondary MPEG2 transport stream (TS) input, thus enabling applications such as picture-in-picture (PIP) and personal video recorder (PVR). It also provides a serial interface for concurrent MPEG2 TS output, and can be easily incorporated into devices with dual display.

A complete set of application programming interface (API) is available for *AF9013/13S/15*, facilitating fast and easy integration into products. Furthermore, a complete set of Microsoft BDA (Broadcast Driver Architecture) and MCE compliant drivers are provided for *AF9015*. Together with the built-in USB and IR (infrared) interfaces, *AF9015* provides a complete and low cost solution for a DVB-T USB portable receiver.

# 2 Block Diagram

Figure 1 shows the block diagram of *AF9013/13S/15* DVB-T COFDM demodulator.

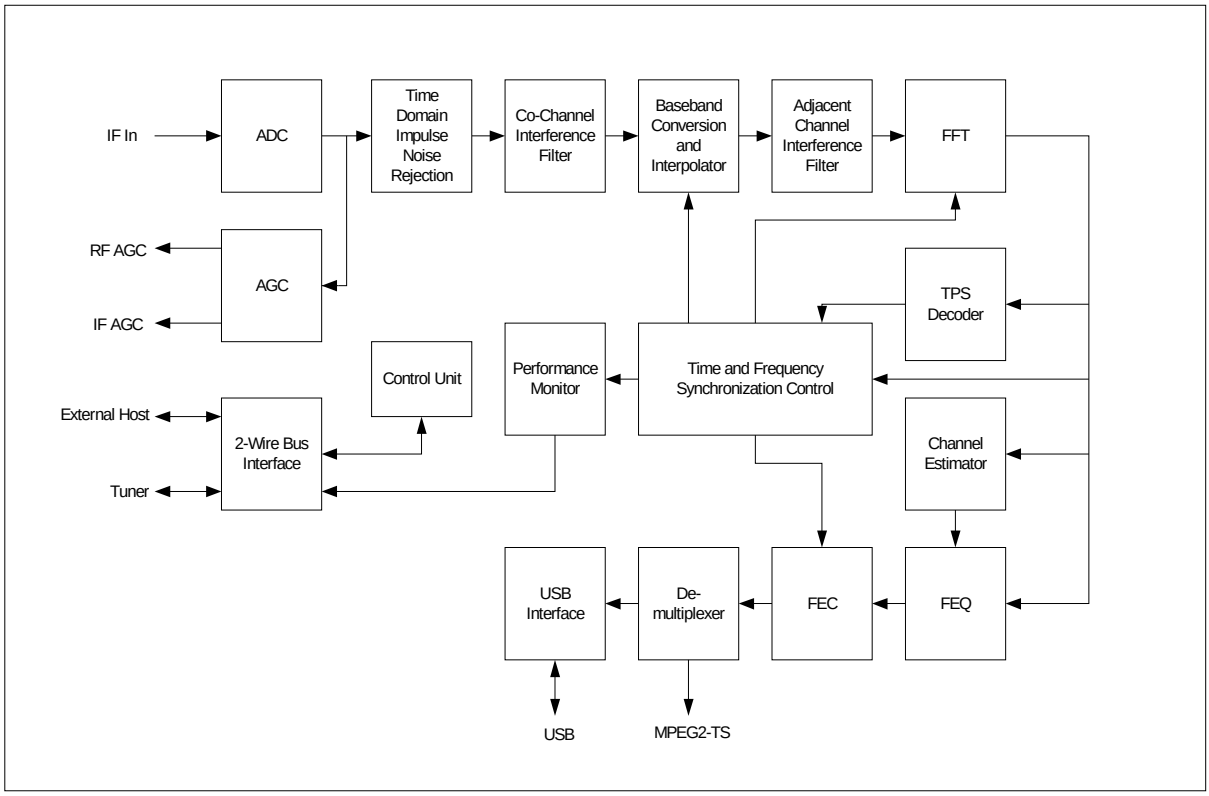


Figure 1: Block diagram of *AF9013/13S/15*.

# 3 Pin Description

## 3.1 Pin Diagrams

### 3.1.1 56-pin USB Mode (*AF9015-N1* / *AF9015A-N1*)

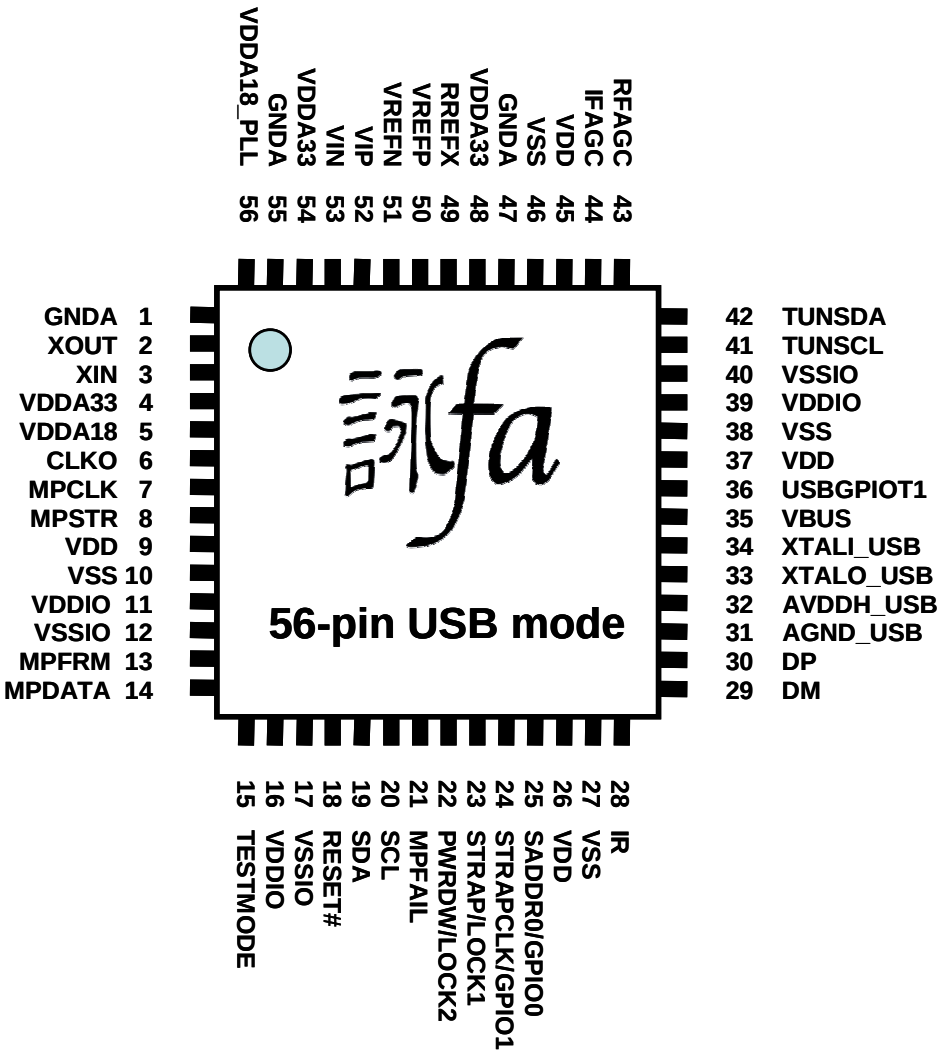


Figure 2: *AF9015 56-pin* USB mode pin diagram.

### 3.1.2 64-pin MPEG Mode (*AF9013-L2* / *AF9013A-L2*)

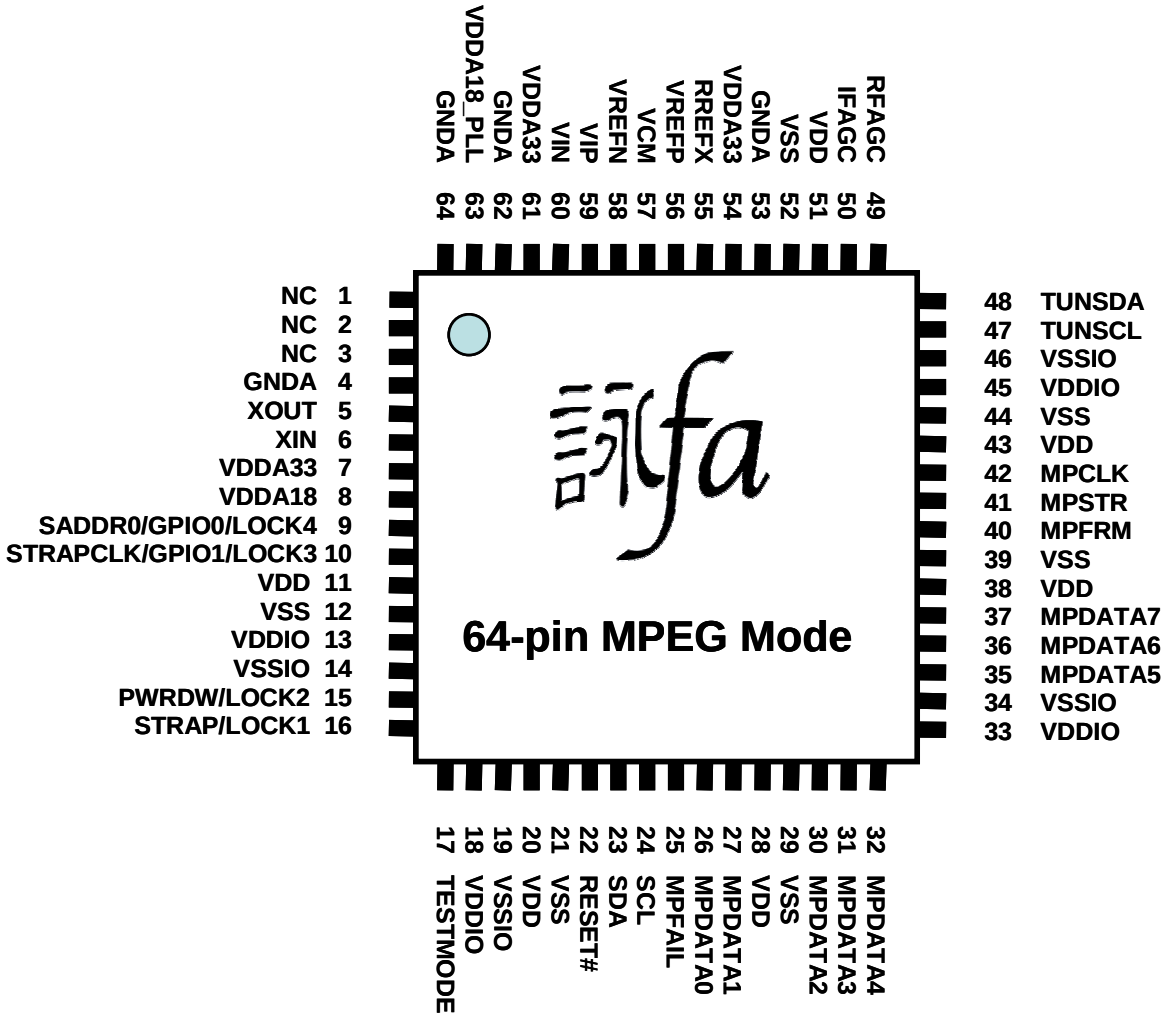


Figure 3: *AF9013* 64-pin MPEG mode pin diagram.

### 3.1.3 64-pin MPEG Mode (*AF9013S-L2* / *AF9013AS-L2*)

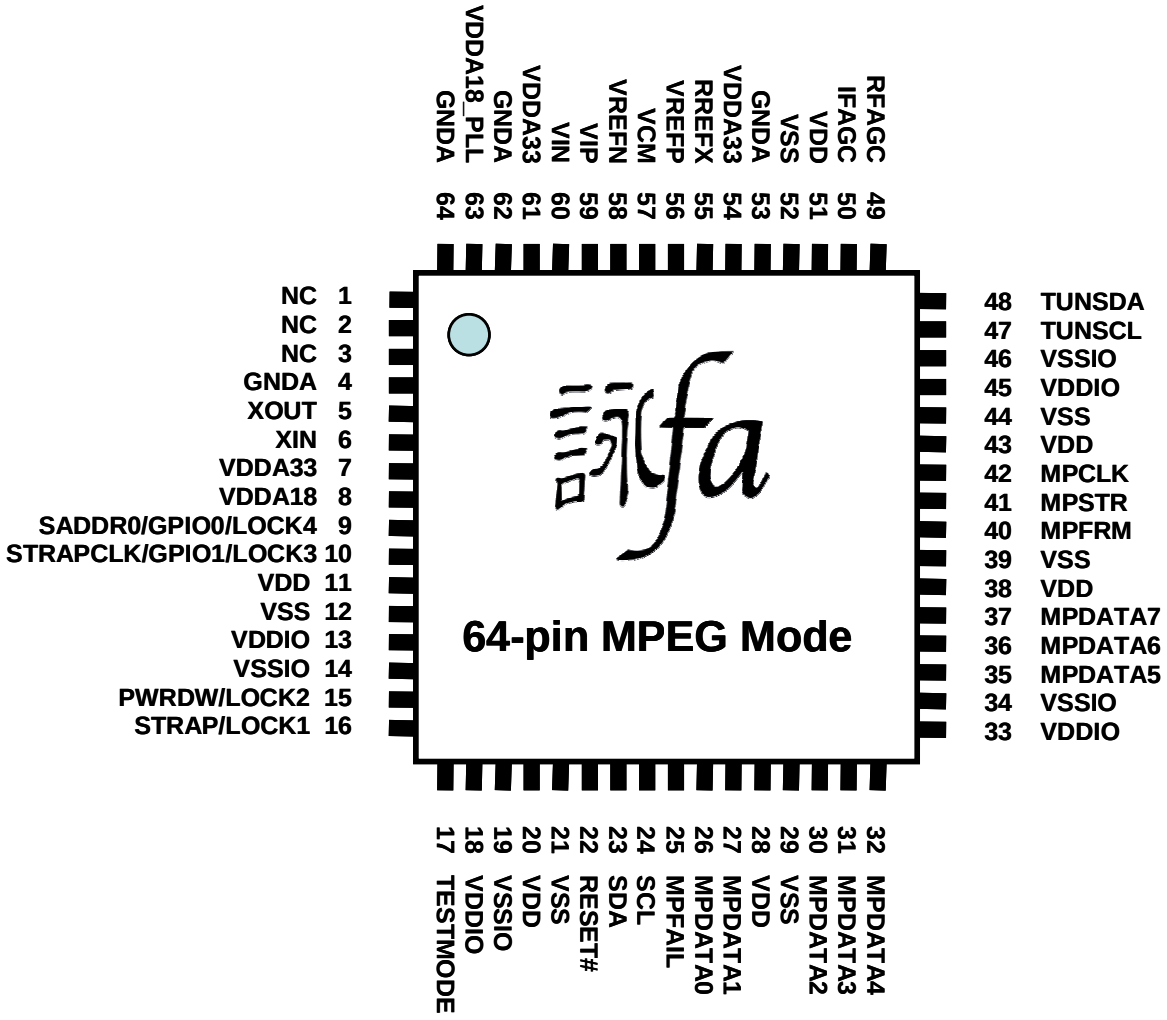


Figure 4: *AF9013S* 64-pin MPEG mode pin diagram.

### 3.1.4 56-pin MPEG Mode (*AF9013-N1* / *AF9013S-N1* / *AF9013A-N1*)

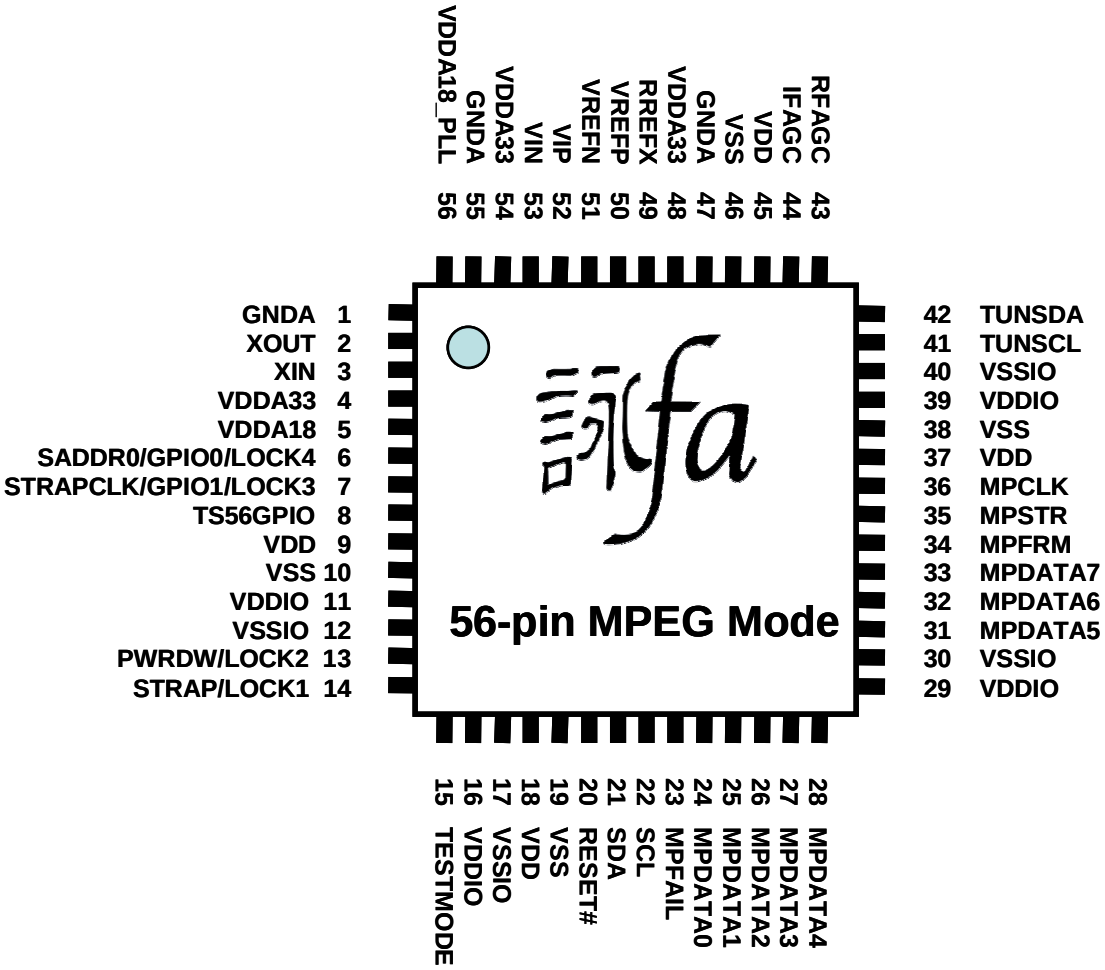


Figure 5: *AF9013* 56-pin MPEG mode pin diagram.

## 3.2 Pin List

Table 1: *AF9013/13S/15* pin list.

| Pin No. | AF9015/15A 56-pin USB mode Pin Name | AF9013/13S/13A/13AS 64-pin MPEG mode Pin Name | AF9013/13S/13A 56-pin MPEG mode Pin Name |
|---|---|---|---|
| 1 | GNDA | NC | GNDA |
| 2 | XOUT | NC | XOUT |
| 3 | XIN | NC | XIN |
| 4 | VDDA33 | GNDA | VDDA33 |
| 5 | VDDA18 | XOUT | VDDA18 |
| 6 | CLKO | XIN | SADDR0/GPIO0/LOCK4 |
| 7 | MPCLK | VDDA33 | STRAPCLK/GPIO1/LOCK3 |
| 8 | MPSTR | VDDA18 | TS56GPIO |
| 9 | VDD | SADDR0/GPIO0/LOCK4 | VDD |
| 10 | VSS | STRAPCLK/GPIO1/LOCK3 | VSS |
| 11 | VDDIO | VDD | VDDIO |
| 12 | VSSIO | VSS | VSSIO |
| 13 | MPFRM | VDDIO | PWRDW/LOCK2 |
| 14 | MPDATA | VSSIO | STRAP/LOCK1 |
| 15 | TESTMODE | PWRDW/LOCK2 | TESTMODE |
| 16 | VDDIO | STRAP/LOCK1 | VDDIO |
| 17 | VSSIO | TESTMODE | VSSIO |
| 18 | RESET# | VDDIO | VDD |
| 19 | SDA | VSSIO | VSS |
| 20 | SCL | VDD | RESET# |
| 21 | MPFAIL | VSS | SDA |
| 22 | PWRDW/LOCK2 | RESET# | SCL |
| 23 | STRAP/LOCK1 | SDA | MPFAIL |
| 24 | STRAPCLK/GPIO1 | SCL | MPDATA0 |
| 25 | SADDR0/GPIO0 | MPFAIL | MPDATA1 |
| 26 | VDD | MPDATA0 | MPDATA2 |
| 27 | VSS | MPDATA1 | MPDATA3 |
| 28 | IR | VDD | MPDATA4 |
| 29 | DM | VSS | VDDIO |
| 30 | DP | MPDATA2 | VSSIO |
| 31 | AGND_USB | MPDATA3 | MPDATA5 |
| 32 | AVDDH_USB | MPDATA4 | MPDATA6 |
| 33 | XTALO_USB | VDDIO | MPDATA7 |

| | | | |
|---|---|---|---|
| 34 | XTALI_USB | VSSIO | MPFRM |
| 35 | VBUS | MPDATA5 | MPSTR |
| 36 | USBGPIOT1 | MPDATA6 | MPCLK |
| 37 | VDD | MPDATA7 | VDD |
| 38 | VSS | VDD | VSS |
| 39 | VDDIO | VSS | VDDIO |
| 40 | VSSIO | MPFRM | VSSIO |
| 41 | TUNSCL | MPSTR | TUNSCL |
| 42 | TUNSDA | MPCLK | TUNSDA |
| 43 | RFAGC | VDD | RFAGC |
| 44 | IFAGC | VSS | IFAGC |
| 45 | VDD | VDDIO | VDD |
| 46 | VSS | VSSIO | VSS |
| 47 | GNDA | TUNSCL | GNDA |
| 48 | VDDA33 | TUNSDA | VDDA33 |
| 49 | RREFX | RFAGC | RREFX |
| 50 | VREFP | IFAGC | VREFP |
| 51 | VREFN | VDD | VREFN |
| 52 | VIP | VSS | VIP |
| 53 | VIN | GNDA | VIN |
| 54 | VDDA33 | VDDA33 | VDDA33 |
| 55 | GNDA | RREFX | GNDA |
| 56 | VDDA18_PLL | VREFP | VDDA18_PLL |
| 57 | | VCM | |
| 58 | | VREFN | |
| 59 | | VIP | |
| 60 | | VIN | |
| 61 | | VDDA33 | |
| 62 | | GNDA | |
| 63 | | VDDA18_PLL | |
| 64 | | GNDA | |

## 3.3 Detailed Pin Descriptions

Table 2: Digital I/O pin detailed description.

| Pin Name | Pin Description | I/O | Type | Integrated Pull-Up/Down | State Immediately After RESET |
|---|---|---|---|---|---|
| SADDR0/GPIO0, SADDR0/GPIO0/LOCK4 | 2-wire bus address strapping; or GPO pin | I/O | CMOS | Pull-down | LOW |
| STRAPCLK/GPIO1, STRAPCLK/GPIO1/LOCK3 | Crystal frequency strapping; or GPO pin | I/O | CMOS | Pull-up | HIGH |
| PWRDW/LOCK2 | Crystal frequency strapping; power down signal; or GPIO pin | I/O | CMOS | Pull-up | High-Z |
| STRAP/LOCK1 | strap select: needs to be pulled down for normal mode; or GPIO pin | I/O | CMOS | Pull-down | High-Z |
| TS56GPIO USBGPIOT1 | GPIO pins | I/O | CMOS | Pull-down Pull-up | High-Z |
| TESTMODE | test mode select: needs to be pulled down for normal mode | I/O | CMOS | Pull-down | High-Z |
| RESET# | reset signal, active low | I/O | CMOS | Pull-up | High-Z |
| SDA, SCL | primarily 2-wire bus | I/O | Open drain | Pull-up | High-Z |
| MPDATA0-7 | MPEG2 data bus | I/O | CMOS | None | High-Z |
| MPFAIL | MPEG2 frame uncorrectable | I/O | CMOS | None | High-Z |
| MPCLK | MPEG2 clock | I/O | CMOS | None | High-Z |
| MPFRM | MPEG2 frame valid | I/O | CMOS | None | High-Z |
| MPSTR | MPEG2 frame start | I/O | CMOS | None | High-Z |
| MPDATA | MPEG2 data pin (serial mode) | I/O | CMOS | None | High-Z |
| IR | infrared input for USB2.0 mode | I/O | CMOS | None | High-Z |
| TUNSDA,TUNSCL | 2-wire bus for tuner | I/O | Open drain | Pull-up | High-Z |
| IFAGC,RFAGC | AGC control for RF and IF | I/O | Open drain | Pull-up | High-Z |
| VBUS | VBUS pin for USB 2.0 | I/O | CMOS | Pull-up | High-Z |
| CLKO | clock out for second TS | I/O | CMOS | None | Clock |

Table 3: Analog I/O pin detailed description.

| Pin Name | Pin description | Type |
|---|---|---|
| DP/DM | DP/DM pins for USB2.0 | Analog I/O |
| XTALI_USB/ XTALO_USB | Crystal pins for USB2.0. | Analog I/O |
| XIN, XOUT | Crystal pins for chip clock. | Analog I/O |
| RREFX | Reference bias pin. Please connect 20k resistor to ground. | Analog I/O |
| VREFP, VREFN, VCM | Reference voltages for ADC. | Analog I/O |
| VIP/VIN | Differential analog input. | Analog I/O |

Table 4: Power/Ground pin detailed description.

| Pin Name | Pin description | Nominal voltage |
|---|---|---|
| VDD | Digital core power | 1.8v |
| VSS | Digital core ground | 0v |
| VDDIO | Digital I/O power | 3.3v |
| VSSIO | Digital I/O ground | 0v |
| AVDDH_USB | Power for USB2.0 | 3.3v |
| VDDA33 | Power for Analog 3.3v | 3.3v |
| VDDA18 | Power for Analog 1.8v | 1.8v |
| VDDA18_PLL | Power for Clocking | 1.8v |
| GNDA/AGND_USB | Analog ground | 0v |

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Table 5: Strapping pins sampled at the rising edge of the RESET signal.

| Pin Name | Strapping Usage | Normal Usage |
|---|---|---|
| SADDR0/GPIO0, SADDR0/GPIO0/LOCK4 | Determine the 2-wire bus address. See Table 7 of Section 4.6.1 | GPIO |
| STRAPCLK/GPIO1, STRAPCLK/GPIO1/LOCK3 | Main crystal frequency information. | GPIO |
| PWRDW/LOCK2 | Main crystal frequency information. | Power down control or GPIO (register programmed) |
| STRAP/LOCK1 | Test mode select. Pull-down for normal mode. Pull-up for test mode. | GPIO |

# 4 Functional Description

## 4.1 Operation Modes

*AF9013/13S/15* operates in several modes, including the MPEG2 TS mode for *AF9013/13S*, and the standard USB2.0 and MPEG2/USB concurrent modes for *AF9015.* The operation mode of *AF9015* is chosen by appropriately setting the 2-wire bus address using the strapping pin SADDR0 according to Table 6. Details of the 2-wire bus interface are given in Section 4.6.

Table 6: AF9015 operation mode selection.

| Strapping Logic Level of SADDR0 | *AF9015* Operation Mode |
|---|---|
| LOW | Standard USB 2.0 |
| HIGH | Concurrent |

### 4.1.1 MPEG TS Mode (*AF9013/13S* Only)

In the MPEG TS mode, *AF9013/13S* outputs MPEG2 Transport Stream through either the parallel or serial MPEG2 transport stream interface. A backend MPEG2 decoder is used to interface with *AF9013/13S* using the 2-wire bus and the MPEG2 TS interface signals. More detailed signal and timing descriptions of the 2-wire bus and MPEG2 transport stream interface can be found in Sections 4.6 and 4.7, respectively.

### 4.1.2 Standard USB2.0 Mode (*AF9015* Only)

In the standard USB 2.0 mode, *AF9015* communicates with a PC through the embedded USB 2.0 interface. The MPEG-2 transport stream decoded by *AF9015* and control/status signals are all encapsulated in the USB frames. In the standard USB 2.0 mode *AF9015* also accepts a secondary MPEG2 transport stream input from the MPEG-2 serial interface and delivers it to the PC through the embedded USB 2.0 interface. This secondary transport stream can, for example, come from an *AF9013/13S*, thus enabling the PC to simultaneously receive and display two transport streams transmitted on different RF frequencies. More detailed description of the *AF9015* MPEG2 transport stream interface and USB 2.0 interface can be found in Sections 4.7 and 4.8, respectively.

### 4.1.3 Concurrent Mode (*AF9015* Only)

In the MPEG/USB concurrent mode, *AF9015* chip outputs MPEG2 transport stream through the serial MPEG2 interface. A backend MPEG2 decoder is used to interface with *AF9015* using the 2-wire bus and MPEG2 TS serial interface. Concurrently, *AF9015* outputs the same MPEG transport stream to a PC through the USB port. More detailed signal and timing descriptions of the 2-wire bus and MPEG2 transport stream interface can be found in Sections 4.6 and 4.7, respectively. More detailed description of the *AF9015* USB 2.0 interface can be found in Section 4.8.

## 4.2 Analog Interface

### 4.2.1 Crystal Oscillator

*AF9013/13S/15* has an on-chip crystal amplifier for clock generation. This amplifier's normal operation current is less than 0.5mA when generating a 28MHz clock. No extra resistor is necessary between XIN and XOUT since it is already embedded.

AF9015 also needs an additional 12MHz XTALI/XTALO pair for 12MHz clock generation for the embedded USB 2.0 interface.

The *AF9013/13S/15* clocking circuit requires a stable reference clock. It can be provided by either of the following two methods:

1. Connect a crystal across the oscillator pins (XIN and XOUT), or

2. Connect an external clock source to pin XIN, and leave XOUT open.

The selection of the crystal clock frequency for ADC depends on the IF frequency, DVB-T channel bandwidth, and ADC sampling frequency. An example for the 8MHz bandwidth is to use a 20.48MHz crystal for 36.17 or 4.57MHz IF frequencies.

*AF9015* also provides a buffered clock output which, for example, can be used to drive a second *AF9013/13S/15*.

### 4.2.2 Analog-to-Digital Converter (ADC)

A 10-bit analog-to-digital converter is used in the front-end of *AF9013/13S/15*. The ADC supports direct sampling of 36.17 MHz or 43.75MHz and near-zero 4.57 MHz IF signals, as well as 6, 7, 8 MHZ OFDM channel bandwidth. Its maximum differential input is 2 volt peak-to-peak.

The ADC clock input is directly from crystal output or from internal PLL.

### 4.2.3 Automatic Gain Control (AGC)

The *AF9013/13S/15* AGC monitors the ADC output samples and generates two pulse-density-modulated (PDM) control signals for the RF and IF voltage gain amplifiers (VGA's) as shown in Figure 6. A single-bit interface is used to reduce the number of connection pins. The amplifier gain is increased or decreased to maintain the ADC output at a target level. The dual AGC mechanism combined with the take-over-point (TOP) operation permit optimal control of both gain amplifiers to minimize noise. Figure 7 shows an example of the TOP operation.

The *AF9013/13S/15* AGC is fully programmable to meet the needs of different tuners or applications. Specifically, the target ADC output level is programmable. The VGA control voltage range can be digitally controlled to avoid nonlinear regions of the gain amplifiers. The loop bandwidth of both RF and IF AGC's can be independently adjusted. Also, VGA's with inverted or non-inverted voltage-gain curve can be supported.

The RF AGC control can be disabled for tuners with built-in RF AGC control. Disabling the RF AGC control is done by register programming.

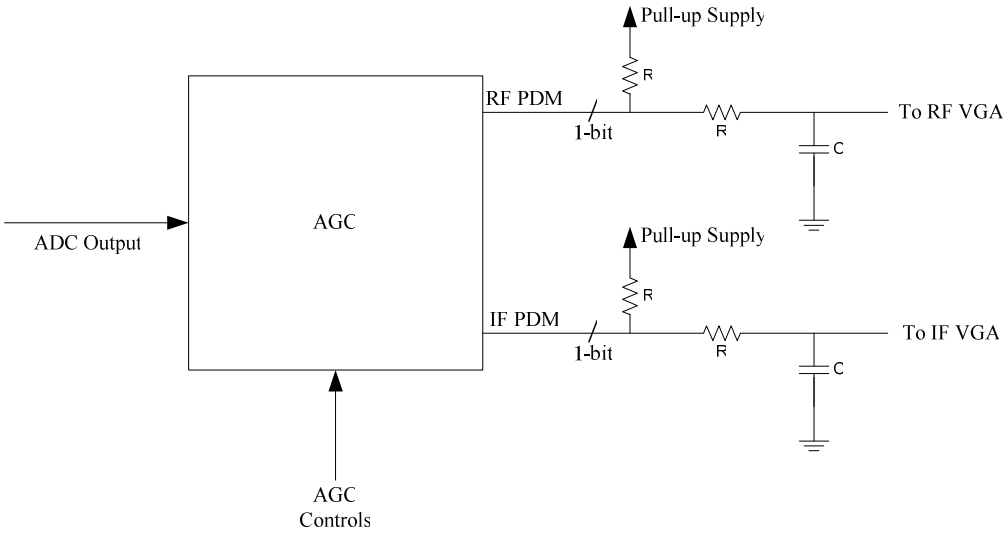



Figure 6: Dual AGC control.

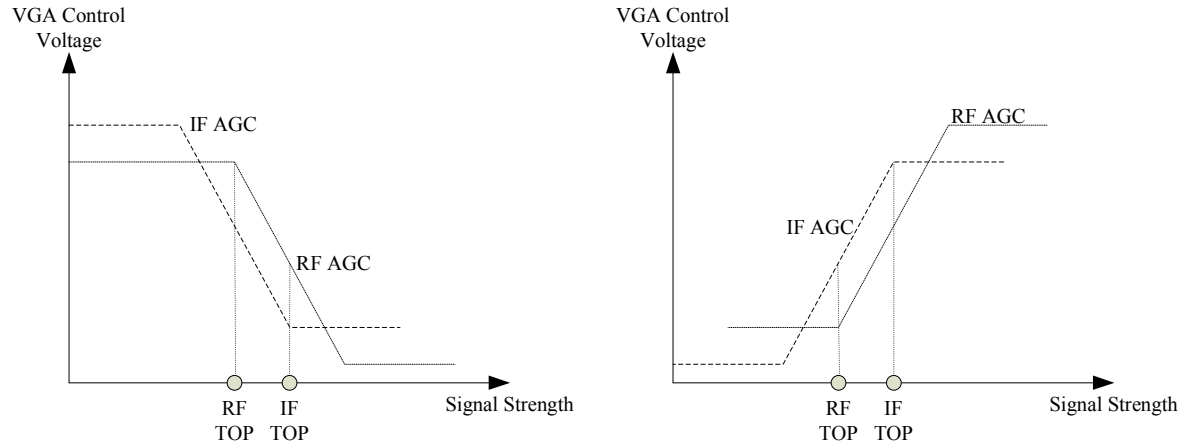



Figure 7: TOP Operations for inverted (left) and non-inverted (right) voltage-gain Curves.

## 4.3 COFDM Digital Signal Processing

### 4.3.1 Initialization

Several important system parameters need to be programmed correctly in order to insure proper operations of *AF9013/13S/15*. These include the ADC sampling frequency, tuner IF frequency, whether the tuner introduces spectral inversion, and the DVB-T channel bandwidth, which can be 6, 7, or 8 MHz.

### 4.3.2 Time-Domain Signal Processing

Before the received signals are converted to the frequency domain via Fast Fourier Transform (FFT), several complicated digital signal processing algorithms are implemented to handle different impairments encountered in the transmission environment.

An automatic gain control (AGC) module measures the received signal strength to determine the correct tuner gain-control signal values. Based on different characteristics of different tuners used, the AGC module can be programmed to accommodate any specific tuner gain-control curve and also the best take-over-point (TOP).

Impulse noise is also actively searched and eliminated.

Co-channel interference (CCI) due to PAL, NICAM, or any other source is adaptively detected and notched out if necessary. No prior knowledge of the CCI location is needed, and the activation of the CCI cancellation filter is automatic.

The IF signal sampled by *AF9013/13S/15* ADC is digitally converted to a complex signal in the baseband at the elementary period, which is 7/64us for 8MHz channels, 1/8us for 7MHz channels, and 7/48us for 6MHz channels.

Adjacent channel interference (ACI) is removed by a very sharp digital filter whose bandwidth is independent of the DVB-T channel bandwidth. Therefore, a signal 8MHz SAW filter is sufficient for 6, 7 or 8 MHz channels.

### 4.3.3 Frequency-Domain Signal Processing

In the frequency domain, a Transmission Parameter Signaling (TPS) decoder is implemented to extract system parameters, including the constellation, hierarchy information, code rate, FFT mode, and guard interval.

The channel estimator estimates and the amplitude and phase distortion caused by the transmission channel and radio frequency (RF) front-end. The common phase error introduced by the RF front-end is also estimated. These distortions are then compensated by the frequency domain equalizer (FEQ). The equalized output of FEQ is then used to generate the input to forward-error-correction (FEC) for further processing.

### 4.3.4 Synchronization Loop

An all-digital synchronization loop is implemented in *AF9013/13S/15* to determine and track the correct FFT window position, track and compensate for the carrier frequency offset caused by the front-end tuner, and track and compensate for the clock jitter introduced by the local crystal. Since the synchronization loop is entirely digital, no analog VCXO is necessary. The *AF9013/13S/15* synchronization loop is capable of correcting carrier frequency offsets of up to ±500 kHz and clock offsets of up to ±100ppm.

## 4.4 Forward Error Correction

The symbol and bit de-interleavers compliant with ETSI EN 300 744 are implemented in the *AF9013/13S/15* forward error correction (FEC). A Viterbi decoder with de-puncturing is used to decode the punctured convolutional code. A shortened (204, 188) Read-Solomon decoder that corrects up to eight byte-errors in a 204 byte frame follows the Viterbi decoder to extract the MPEG2 transport stream packets. A fail signal is alerted when the number of error bytes exceeds eight, and the same input is bypassed to the output in this case. Finally, de-scrambler reverses the scrambling process, and the 0x47 to 0xB8 sync byte inversion is removed after the de-scrambler.

## 4.5 Performance Monitoring

*AF9013/13S/15* provides a complete set of registers for monitoring the performance and status of the demodulator. The parameters that can be monitored and derived include the sampling clock and carrier frequency offsets, TPS and MPEG-2 lock signals, TPS parameters, bit error rates and packet error rates, signal quality, and signal strength. Details on performance monitoring can be found in *AF9013/13S/15 Design Manual*.

## 4.6 2-Wire Interface

*AF9013/13S/15* provides two independent 2-wire interfaces for communicating with the external host and tuner.

### 4.6.1 Host Interface

The *AF9013/13S/15* host 2-wire interface uses, respectively, pins SDA for the serial data and SCL for the serial clock. The bus address of the *AF9013/13S/15* 2-wire host interface is determined by the strapping pin SADDR0. When *AF9013/13S/15* is first powered up, the RESET pin should be held low. As the RESET pin transitions from low to high, the logic level of the strapping pin SADDR0 is latched to determine the 2-wire bus address, as shown in Table 7. For *AF9015*, the logic level of the strapping pin SADDR0 also determines its operation mode, as described in Section 4.1.

Table 7: *AF9013/13S/15* 2-wire bus address mapping table.

| SADDR0 at strapping | 2-Wire Bus Address | Remarks |
|---|---|---|
| LOW | 0x38 | *AF9015* works in the standard USB2.0 mode |
| HIGH | 0x3A | *AF9015* works in the concurrent USB2.0 mode |

The *AF9013/13S/15* host 2-wire interface supports both read and write operations. The circuit works as a slave transmitter in the read operation mode and slave receiver in the write operation mode.

Details on using the 2-wire host interface can be found in *AF9013/13S/15 Design Manual.*

### 4.6.2 Tuner Interface

*AF9013/13S/15* also provides a secondary 2-wire interface for communicating with the external tuner. It uses pins TUNSDA for serial data and TUNSCL for serial clock. The circuit works as a master transmitter in the write operation mode and master receiver in the read operation mode. Details on using the 2-wire tuner interface can be found in *AF9013/13S/15 Design Manual.*

## 4.7 MPEG-2 Transport Stream Interface

The *AF9013/13S/15* MPEG-2 transport stream interface pins and their meanings are listed in Table 8.

The MPEG-2 transport stream interface of *AF9013/13S/15* offers both parallel and serial outputs, as well as serial input in the *AF9015* standard USB2.0 mode. For *AF9013/13S* operating in the MPEG-2 TS mode, the MPEG-2 transport stream interface can operate in the parallel output mode, serial output mode, or be disabled. An example timing diagram of the parallel output mode is shown in Figure 8. For the serial output mode the MPEG-2 TS data can be configured to be output on pins MPDATA7 or MPDATA0. On the other hand, for *AF9015* operating in the standard USB2.0 mode, the MPEG-2 transport stream interface is an *input* interface that accepts MPEG-2 transport streams in a serial fashion. The MPEG-2 TS data pin is MPDATA. Finally, for *AF9015* operating in the concurrent mode, the MPEG-2 transport stream interface is a serial output interface. A table of *AF9013/13S/15* MPEG-2 TS interface modes is given in Table 9.

The *AF9013/13S/15* MPEG-2 transport stream interface is fully configurable. The list of configurable parameters is shown in Table 10. Details on configuring the *AF9013/13S/15* MPEG-2 TS interface are available in *AF9013/13S/15 Design Manual.*

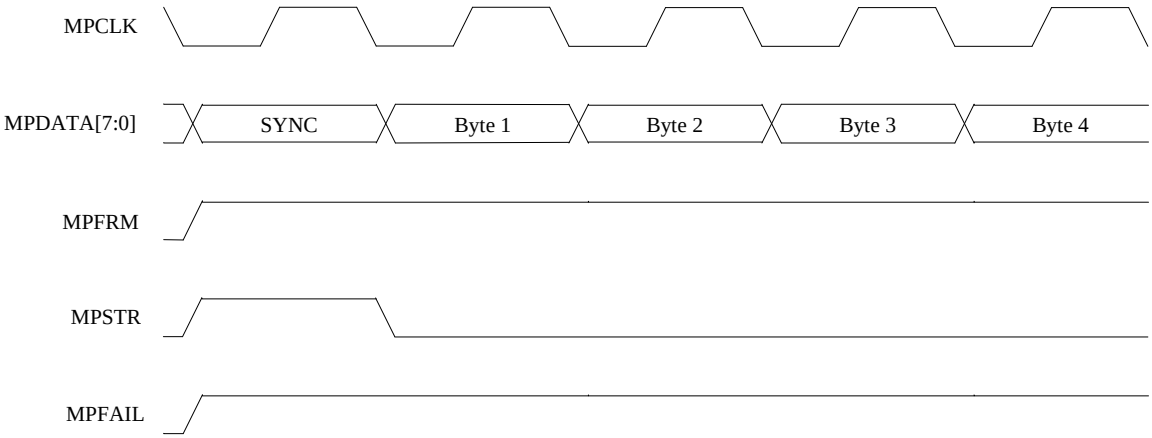



Figure 8: An example of MPEG2 parallel interface timing diagram.

Table 8: *AF9013/13S/15* MPEG-2 TS interface pins.

| Pin Name | I/O | Description |
|---|---|---|
| MPCLK | In/Out | MPEG clock |
| MPDATA7, MPDATA6, MPDATA5, MPDATA4, MPDATA3, MPDTAT2, MPDATA1, MPDATA0 | Out | MPEG transport stream data for *AF9013/13S*.<br><br>8-bit in the parallel mode and 1-bit in the serial mode.<br><br>MPDATA0 or MPDATA7 can be the output pin in the serial mode. |
| MPDATA | In/Out | MPEG transport stream data (serial input or output) for *AF9015*. |
| MPFRM | In/Out | MPEG data valid |
| MPSTR | In/Out | MPEG packet sync pulse |
| MPFAIL | In/Out | MPEG uncorrectable packet |

Table 9: The *AF9013/13S/15* MPEG-2 TS interface mode selection.

| Part Number | Operation Mode | MPEG-2 transport stream interface operation modes |
|---|---|---|
| *AF9013/13S* | MPEG-2 TS mode | Serial Output. Data is on pins MPDATA7 or MPDATA0. |
| | | Parallel Output |
| | | Disabled |
| *AF9015* | Standard USB2.0 mode | Serial Input. Data is on pin MPDATA. |
| | Concurrent Mode | Serial Output Data is on pin MPDATA |

Table 10: Configurable parameters of the *AF9013/13S/15* MPEG-2 TS interface.

| Parameter | Selections |
|---|---|

| | |
|---|---|
| **Input/Output Mode** | **Parallel Output**<br>**Serial Output**<br>**Serial Input (*AF9015* only)** |
| **Output data pin of serial mode.** | **MPDATA7 or MPDATA0 (*AF9013/13S* only)** |
| **Bit-Order** | For Parallel Mode:<br>**MPDATA7 can be MSB or LSB**<br>For Serial Input and Output Modes:<br>**Can be MSB first or LSB first.** |
| **Style of the MPEG-2 sync byte** | **MPEG-2 style or DVB-T style.** |
| **Signal polarity** | **MPCLK, MPFRM, MPSTR, and MPFAIL can be independently configured to be active high or low.** |
| **The style of MPFRM** | **Continuous or gapped.** |
| **The gap between consecutive 188-byte payloads in units of byte times.** | **0 ~ 31** |
| **MPSTR assertion for the serial output mode, select whether MPSTR is asserted only for the first bit or for all bits of the first byte.** | **Asserted for all bits of the first byte or for the first bi t only.** |
| **MPCLK frequency** | **Configurable** |
| **MPSTR pin for the serial input mode For the serial input mode** | **Can be used or wired to ground.** |
| **Output driving capability** | **Configurable with optional slew-rate control** |

### 4.7.1 Parallel Output Interface

For *AF9013/13S*, when the MPEG-2 TS interface is programmed to be the parallel output mode, each byte of the payload of the MPEG-2 transport stream will be output to MPDATA7~MPDATA0 in parallel. MPFRM is asserted when a payload byte is being output on MPDATA7~MPDATA0. MPSTR is asserted at the first payload byte of each transport stream packet. MPFAIL is asserted throughout the entire duration of any erroneous transport stream packet.

Note that there can be gaps between bytes in MPFRM. Example timing diagrams with continuous and gapped MPFRM are shown in Figure 9 and Figure 10, respectively.

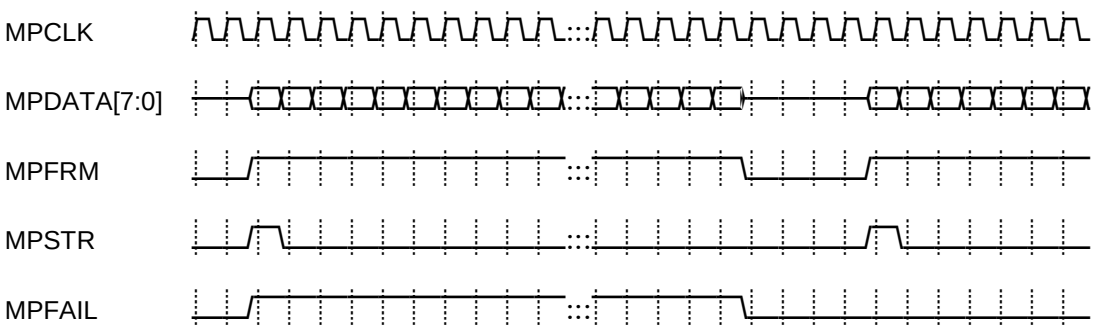



Figure 9: Timing diagram with continuous MPFRM in parallel mode.

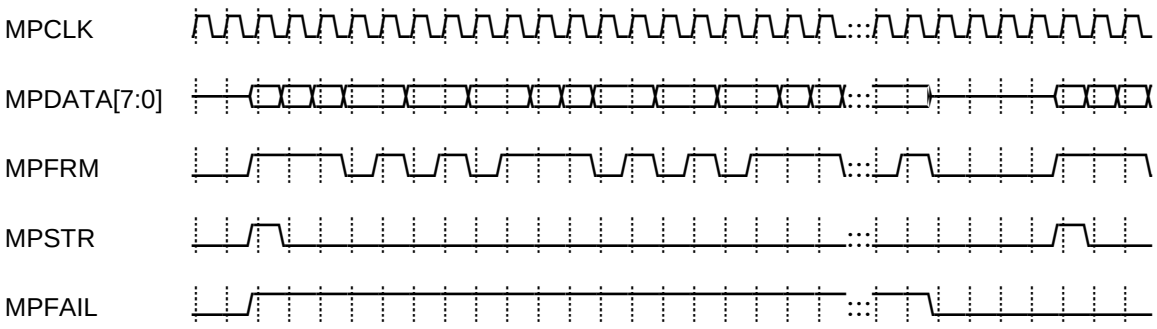



Figure 10: Timing diagram with gapped MPFRM in parallel mode.

### 4.7.2 Serial Output Interface

In the serial output mode, the payloads of MPEG-2 transport stream will be serially output on MPDATA7 or MPDATA0 for *AF9013/13S* or on MPDATA for *AF9015*. In this mode, MPSTR can be asserted at the first bit or first 8 bits of the payload of the transport stream. Furthermore, there can be gaps in MPFRM, but there can be no gaps within the 8 bits of a byte. Example timing diagrams of MPFRM without and with gaps are shown in Figure 11 and Figure 12, respectively. Finally, same as in the parallel mode, for any error packet, MPFAIL is asserted throughout the entire duration of any erroneous transport stream packet.

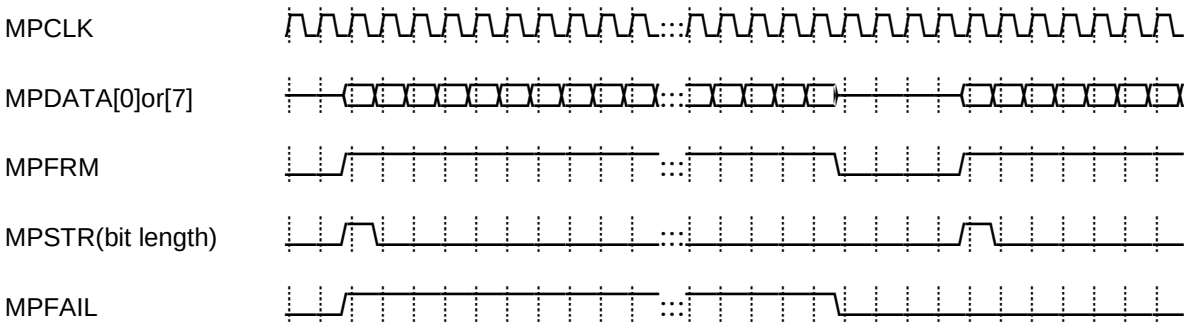



Figure 11: Timing diagram of continuous MPFRM signal in serial mode.

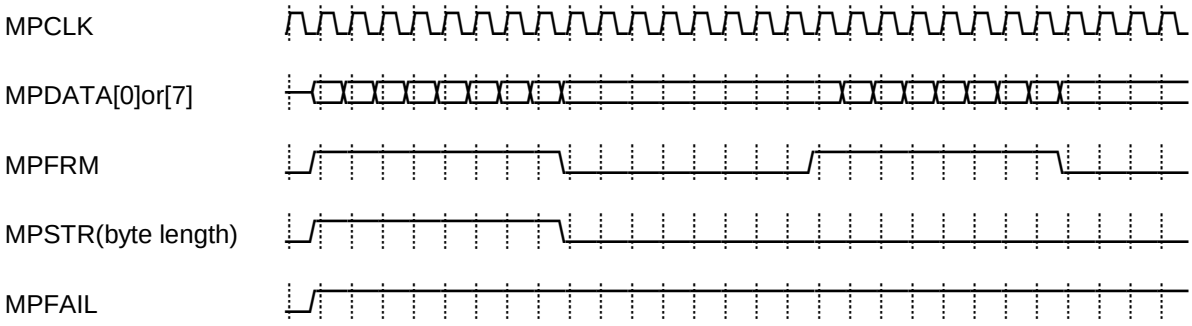



Figure 12: Timing diagram of gapped MPFRM signal in serial mode.

### 4.7.3 Serial Input Interface (AF9015 Only)

The MPEG2 TS interface of *AF9015* can also become an input interface for accepting a secondary MPEG2 TS stream and forwarding to the PC through the USB2.0 interface. Only serial data is supported for receiving the secondary MPEG2 TS stream. An example timing diagram for the *AF9015* MPEG2 TS input interface is shown in Figure 13.

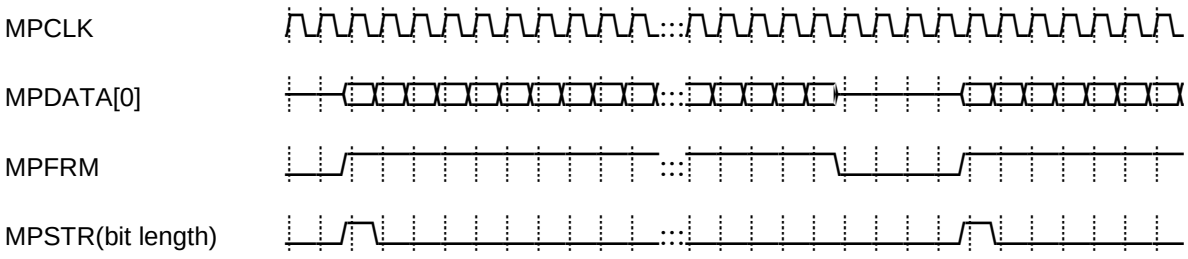



Figure 13: Timing diagram of the *AF9015* MPEG-2 TS serial input interface.

MPSTR of *AF9015* can be wired to the ground if MPSTR is not available from the MPEG TS stream provider.

## 4.8 USB Interface (*AF9015* Only)

*AF9015* supports USB 2.0 standard with many configurable parameters in the Endpoint 0 descriptors.

### 4.8.1 USB Descriptors

Most strings and parameters in the descriptors are configurable in the external EEPROM, including:

- Device descriptors: vender ID, product ID, device release number, manufacturer string index, product string index, serial number string index, configuration characteristics (self-powered, remote wake-up, …etc.), max power consumption, and interrupt endpoint (Endpoint 3) polling interval; and
- Strings: the string description of the manufacturer and the product and the serial number. These strings are defined in USB 2.0 standard.

See *AF9013/13S/15 Design Manual* for details on the external EEPROM.

### 4.8.2 USB Control Protocol

#### 4.8.2.1 Default Endpoint (Endpoint 0)

Endpoint 0 is the same as defined in USB 2.0 standard.

#### 4.8.2.2 Control Messages

Control messages are sent through a request-and-reply model. Any request packet corresponds to a reply packet, unless the communication is malfunctioning. A sequence number field is employed in each control packet to resolve the late reply and duplicate request/reply problems.

The available control messages include those for getting the current configuration, downloading the firmware, computing firmware checksum, booting *AF9015*, copying the firmware to a slave device, reading and writing the *AF9015* memory, as well as 2-wire bus control messages, software reset control messages, and Control Unit command control messages.

#### 4.8.2.3 Data Messages

Data messages convey the MPEG2 transport streams received by *AF9015*.

## 4.9 Infrared (IR) Interface (*AF9015* Only)

*AF9015* supports two IR protocols: NEC and RC6. The IR function can be enabled or disabled and the IR protocol can be selected by appropriately setting the corresponding fields in the external EEPROM. If the IR function is enabled, *AF9015* is considered as a USB composite device with HID. Otherwise *AF9015* is a USB single device. More details on EEPROM settings are available in *AF9013/13S/15 Design Manual*. The *AF9015* IR decoder decodes raw signals received from the IR photo-receiver. Then the demodulated signals are converted to HID (Human Interface Devices) format according to a translation table that is downloaded from the driver via the memory write protocol (See Section 4.8.2.2 for more details on USB control protocols). At last the USB host receives IR messages via USB Endpoint 3.

More details of the *AF9015* IR interface are available in *AF9013/13S/15 Design Manual.*

### 4.9.1 The Function Key and Alternative Keys

The function key (FN) is used to create alternative key sequences for a remote control. When FN of a remote control is pressed, an alternative key sequence is initiated, and any keys pressed are considered “alternative” if they are pressed within a predefined expiration time after the previous key press. This design enables a remote control with fewer keys (buttons) to almost double its “effective” number of keys. *AF9015* will *not* send any key when only the function key is pressed

Alternative keys are supported in *AF9015* as mentioned in *AF9013/13S/15 Design Manual.*

## 4.10 The External EEPROM

An external EEPROM can be used for storing USB related information, firmware, and possibly other hardware related information in systems using *AF9015*. The content and format of the external *EEPROM* is given in great detail in *AF9013/13S/15 Design Manual.*

## 4.11 Boot Scheme

*AF9013/13S/15* operates in the MPEG2 TS, standard USB2.0, or MPEG/USB concurrent modes, each with its own booting scheme. Details of the operation modes are available in Section 4.1. In the MPEG-2 TS mode for *AF9013/13S* and concurrent mode of *AF9015*, the booting process is a simplex process, in the sense that information only flows from the host to *AF9013/13S*. *AF9013/13S/15* does not send any information to the host. However, *AF9013/13S/15* does make the download status available to the host by writing the status to an internal register for the host to poll. On the other hand, the booting scheme of the standard USB2.0 download mode is a duplex process in which requests from the host is responded by replies from *AF9015*. Furthermore, the *AF9015* USB firmware is also involved in this scheme to inform the host that the USB firmware is running.

Details of the boot schemes are available in *AF9013/13S/15 Design Manual*.

# 5 Electrical Characteristics

## 5.1 Absolute Maximum Ratings

Table 11: *AF9013/13S/15* absolute maximum ratings.

| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
|---|---|---|---|---|
| I/O Power Voltage | VDDIO | -0.3 | 3.6 | V |
| Digital Core Power Voltage | VDD | -0.3 | 2.0 | V |
| Analog 3.3V Power Voltage | VDDA33 | -0.3 | 3.6 | V |
| Analog 1.8V Power Voltage | VDDA18 | -0.3 | 2.0 | V |
| Voltage on input pins | VI | -0.3 | VDDIO+0.3 | V |
| Voltage on output pins | VO | -0.3 | VDDIO+0.3 | V |
| Storage Temperature | Tstg | -40 | 150 | ºC |
| Junction Temperature | Tj | | 125 | ºC |
| Ambient Operating Temperature (Commercial) | Ta | 0 | 70 | ºC |

| Junction-Ambient Thermal Resistance for 64-pin chip and 4-layers PCB | Rth(j-a) | 0(m/s) | 1(m/s) | 2(m/s) | ºC/W |
|---|---|---|---|---|---|
| | | 37 | 35 | 32.6 | |
| Junction-Ambient Thermal Resistance for 56-pin chip and 4-layers PCB | Rth(j-a) | 0(m/s) | 1(m/s) | 2(m/s) | ºC/W |
| | | 21.5 | 18.9 | 17.1 | |

## 5.2 DC Electrical Characteristics

Table 12: *AF9013/13S/15* DC electrical characteristics (not applicable for *9013A/13AS/15A*).

Note: VDD=1.8V, VDDIO=3.3V and Ta=25C unless otherwise specified.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital Core Power Voltage | VDD | | 1.6 | 1.8 | 2.0 | V |
| I/O Power Voltage | VDDIO | | 3.0 | 3.3 | 3.6 | V |
| Analog 1.8V Power Voltage | VDDA18 | | 1.6 | 1.8 | 2.0 | V |
| Analog 3.3V Power Voltage | VDDA33 | | 3.0 | 3.3 | 3.6 | V |
| Digital Core Power Supply Current | $I_{VDD}$ | *AF9013/13S* Typical Air Reception* | | 103 | | mA |
| I/O Power Supply Current | $I_{VDDIO}$ | *AF9013/13S* Typical Air Reception* | | 3 | | mA |
| Analog 1.8V Power Supply Current | $I_{VDDA18}$ | *AF9013/13S* Typical Air Reception* | | 5 | | mA |
| Analog 3.3V Power Supply Current | $I_{VDDA33}$ | *AF9013/13S* Typical Air Reception* | | 27 | | mA |
| Power Consumption (Operating) | $P_{OP}$ | *AF9013/13S* Typical Air Reception* | | 293 | | mW |
| Digital Core Power Supply Current | $I_{VDD}$ | *AF9015* Typical Air Reception* | | 107 | | mA |
| I/O Power Supply Current | $I_{VDDIO}$ | *AF9015* Typical Air Reception* | | 27 | | mA |
| Analog 1.8V Power Supply Current | $I_{VDDA18}$ | *AF9015* Typical Air Reception* | | 5 | | mA |
| Analog 3.3V Power Supply Current | $I_{VDDA33}$ | *AF9015* Typical Air Reception* | | 27 | | mA |
| Power Consumption (Operating) | $P_{OP}$ | *AF9015* Typical Air Reception* | | 380 | | mW |
| Current Consumption (Suspend Mode) | $I_{SUS}$ | | | 290 | | uA |
| High Level Input Voltage | VIH | | 2.0 | | | V |
| Low Level Input Voltage | VIL | | | | 0.8 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Capacitance | Cin | | | 3 | | pF |
| High Level Output Voltage | VOH | | 3.0 | | | V |
| Low Level Output Voltage | VOL | | | | 0.4 | V |
| High/Low Level Output Current | IOH/IOL | Digital Output Pins | 0 | | 4 | mA |
| High/Low Level Output Current | IOH/IOL | 5V tolerant Open-Drain | 0 | | 2 | mA |

* The air signal being received uses 8K, 16QAM, CR=2/3, GI=1/4, and 6MHz. The ADC sampling clock is 20.48MHz.

Table 13: *AF9013A/13AS/15A* DC electrical characteristics (not applicable for *9013/13S/15*).

Note: VDD=1.8V, VDDIO=3.3V and Ta=25C unless otherwise specified.

| **Parameter** | **Symbol** | **Test Condition** | **Min** | **Typ** | **Max** | **Unit** |
|---|---|---|---|---|---|---|
| Digital Core Power Voltage | VDD | | 1.6 | 1.8 | 2.0 | V |
| I/O Power Voltage | VDDIO | | 3.0 | 3.3 | 3.6 | V |
| Analog 1.8V Power Voltage | VDDA18 | | 1.6 | 1.8 | 2.0 | V |
| Analog 3.3V Power Voltage | VDDA33 | | 3.0 | 3.3 | 3.6 | V |
| Digital Core Power Supply Current | $I_{VDD}$ | *AF9013A/13AS* Typical Air Reception* | | **83** | | mA |
| I/O Power Supply Current | $I_{VDDIO}$ | *AF9013A/13AS* Typical Air Reception* | | **2** | | mA |
| Analog 1.8V Power Supply Current | $I_{VDDA18}$ | *AF9013A/13AS* Typical Air Reception* | | **4** | | mA |
| Analog 3.3V Power Supply Current | $I_{VDDA33}$ | *AF9013A/13AS* Typical Air Reception* | | **27** | | mA |
| Power Consumption (Operating) | $P_{OP}$ | *AF9013A/13AS* Typical Air Reception* | | **253** | | mW |
| Digital Core Power Supply Current | $I_{VDD}$ | *AF9015A* Typical Air Reception* | | **90** | | mA |
| I/O Power Supply Current | $I_{VDDIO}$ | *AF9015A* Typical Air Reception* | | **27** | | mA |
| Analog 1.8V Power Supply Current | $I_{VDDA18}$ | *AF9015A* Typical Air Reception* | | **5** | | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| Analog 3.3V Power Supply Current | $I_{VDDA33}$ | *AF9015A* Typical Air Reception* | | **27** | | mA |
| Power Consumption (Operating) | $P_{OP}$ | *AF9015A* Typical Air Reception* | | **349** | | mW |
| Current Consumption (Suspend Mode) | $I_{SUS}$ | | | **7** | | uA |
| High Level Input Voltage | VIH | | 2.0 | | | V |
| Low Level Input Voltage | VIL | | | | 0.8 | V |
| Input Capacitance | Cin | | | 3 | | pF |
| High Level Output Voltage | VOH | | 3.0 | | | V |
| Low Level Output Voltage | VOL | | | | 0.4 | V |
| High/Low Level Output Current | IOH/IOL | Digital Output Pins | 0 | | 4 | mA |
| High/Low Level Output Current | IOH/IOL | 5V tolerant Open-Drain | 0 | | 2 | mA |

## 5.3 Analog Characteristics

Table 14: *AF9013/13S/15* Analog electrical characteristics.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ADC resolution | | | | 10 | | bit |
| ADC input range, register programmable | Vinpp | | 1 | | 2 | V |
| ADC VREFP voltage | Vrefp | | 1.6 | | 2.2 | V |
| ADC VREFN voltage | Vrefp | | 0.9 | 1 | 1.4 | V |
| ADC VCM voltage | Vcm | | 1.35 | 1.5 | 1.65 | V |
| Differential input bandwidth | fin | | 50 | | | MHz |
| Crystal input capacitance | Ccry | | | | 2 | pF |

## 5.4 AC Electrical Characteristics

### 5.4.1 MPEG-2 TS Output

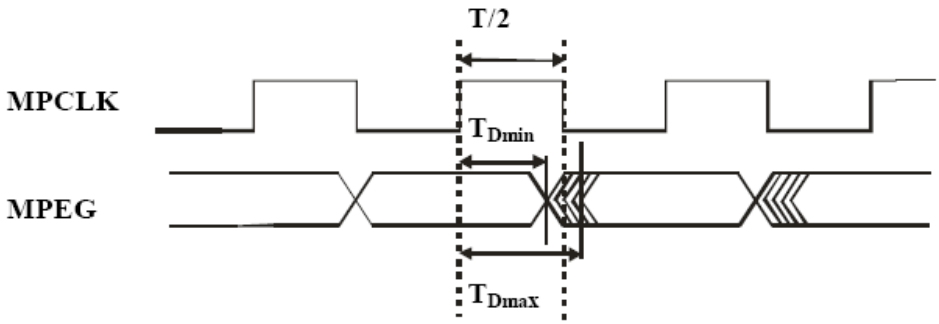



Figure 14: *AF9013/13S/15* MPEG-2 TS output timing diagram.

Table 15: *AF9013/13S/15* MPEG-2 TS output timing.

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| T/2 | a half MPCLK (40MHz) clock cycle | | | ns |
| $T_{Dmin}$ | Minimum valid delay | T/2 - 3 | | ns |
| $T_{Dmax}$ | Maximum valid delay | | T/2 + 3 | ns |

### 5.4.2 MPEG-2 TS Input (*AF9015* Only)

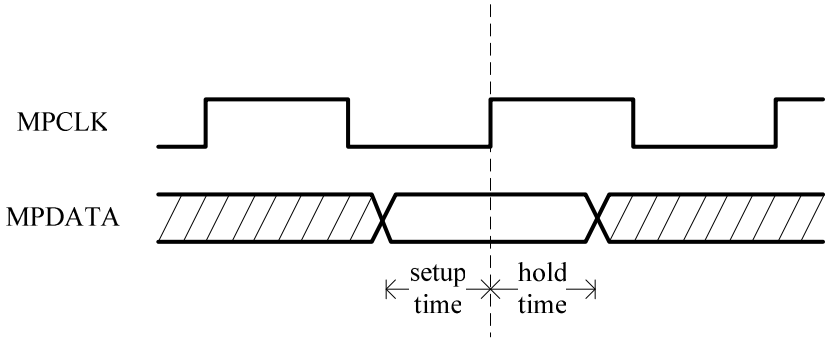



Figure 15: *AF9015* MPEG-2 TS input timing diagram.

Table 16: *AF9015* MPEG-2 TS input timing

| Parameter | Requirement | Unit |
|---|---|---|
| Input Set-up Time | 0 | ns |
| Input Hold Time | 6.26 | ns |

### 5.4.3 2-Wire Bus Output

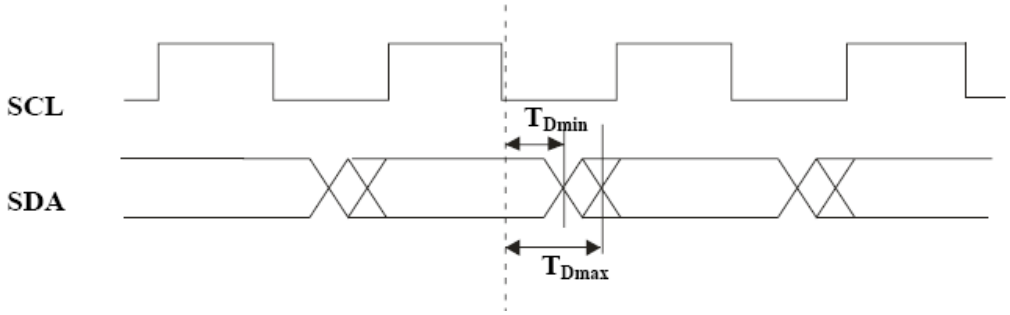



Figure 16: *AF9013/13S/15* 2-wire bus output timing diagram.

Table 17: *AF9013/13S/15* 2-wire bus output timing.

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{Dmin}$ | Minimum valid delay of 2-wire bus output | 317 | | ns |
| $T_{Dmax}$ | Maximum valid delay of 2-wire bus output | | 334 | ns |

### 5.4.4 2-Wire Bus Input

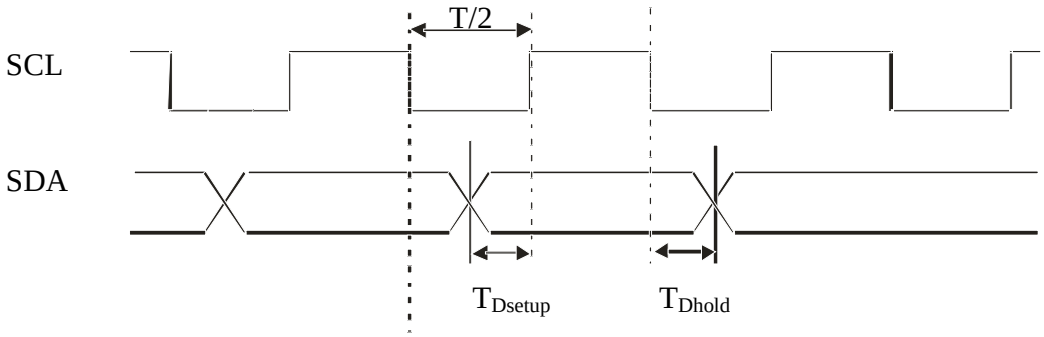


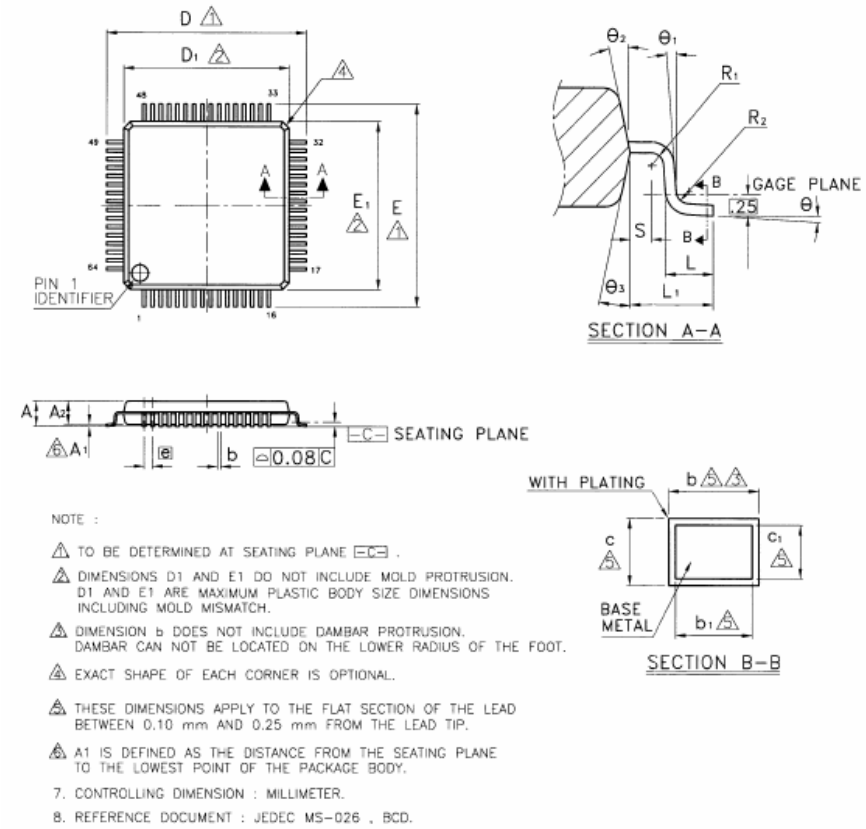

Figure 17: *AF9013/13S/15* 2-wire bus input timing diagram.

Table 18: *AF9013/13S/15* 2-wire bus input timing.

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{Dsetup}$ | 2-wire bus input setup time | 2 | T/2 -2 | ns |
| $T_{Dhold}$ | 2-wire bus input hold time | 2 | T/2 -2 | ns |

# 6 Mechanical Specification

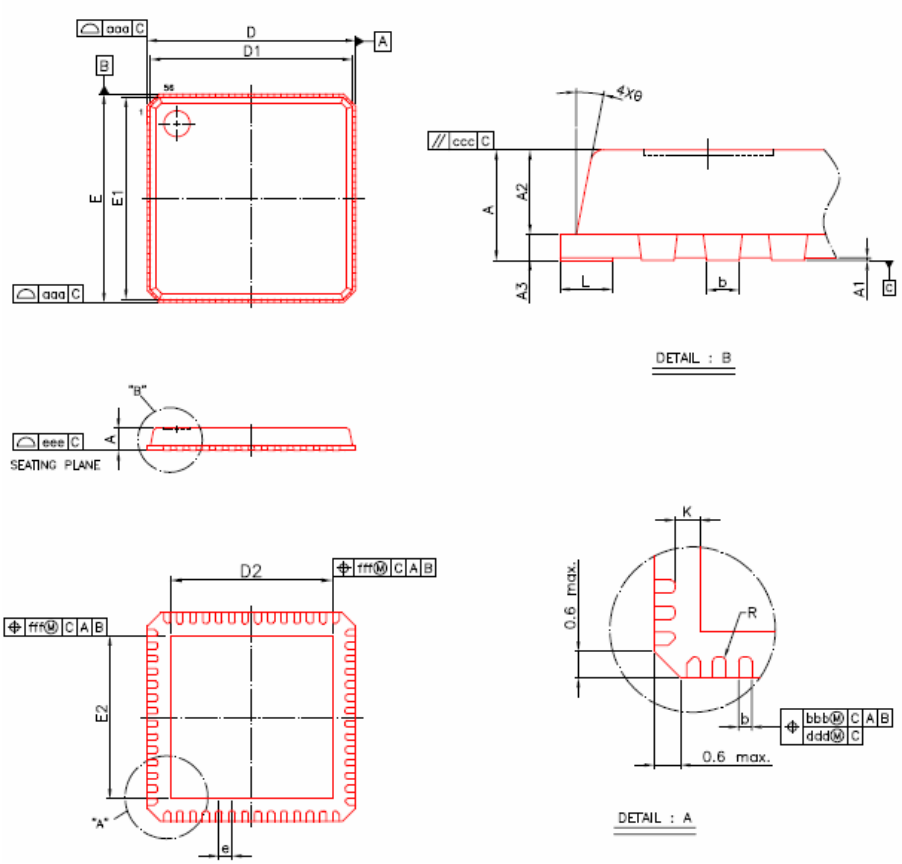
## 6.1 LQFP-64 Outline Dimensions




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.60 | — | — | 0.063 |
| $A_1$ | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| $b_1$ | 0.17 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| $c_1$ | 0.09 | — | 0.16 | 0.004 | — | 0.006 |
| D | 12.00 BSC | | | 0.472 BSC | | |
| $D_1$ | 10.00 BSC | | | 0.394 BSC | | |
| E | 12.00 BSC | | | 0.472 BSC | | |
| $E_1$ | 10.00 BSC | | | 0.394 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | 1.00 REF | | | 0.039 REF | | |
| $R_1$ | 0.08 | — | — | 0.003 | — | — |
| $R_2$ | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| S | 0.20 | — | — | 0.008 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $θ_1$ | 0° | — | — | 0° | — | — |
| $θ_2$ | 12°TYP | | | 12°TYP | | |
| $θ_3$ | 12°TYP | | | 12°TYP | | |

Figure 18: LQFP-64 outline dimensions.

## 6.2 QFN-56 Outline Dimensions




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 1.00 | 0.031 | 0.033 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A2 | 0.60 | 0.65 | 0.80 | 0.024 | 0.026 | 0.031 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D/E | 8.00 BSC | | | 0.315 BSC | | |
| D1/E1 | 7.75 BSC | | | 0.305 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| θ | 0° | --- | 14° | 0° | --- | 14° |
| R | 0.09 | --- | --- | 0.004 | --- | --- |
| K | 0.20 | --- | --- | 0.008 | --- | --- |
| aaa | --- | --- | 0.15 | --- | --- | 0.006 |
| bbb | --- | --- | 0.10 | --- | --- | 0.004 |
| ccc | --- | --- | 0.10 | --- | --- | 0.004 |
| ddd | --- | --- | 0.05 | --- | --- | 0.002 |
| eee | --- | --- | 0.08 | --- | --- | 0.003 |
| fff | --- | --- | 0.10 | --- | --- | 0.004 |

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

| L/F | Exposed Pad Size | | | | | |
|---|---|---|---|---|---|---|
| | D2/E2 (mm) | | | D2/E2 (inch) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| ① | 4.22 | 4.37 | 4.52 | 0.166 | 0.172 | 0.178 |
| ② | 5.90 | 6.05 | 6.20 | 0.232 | 0.238 | 0.244 |

Figure 19: QFN-56 outline dimensions.

# 7 Register List

Table 19: *AF9013/13S/15* register list.

| Register Name | Address | Bits | Access | Register Description | Default |
|---|---|---|---|---|---|
| | 0xD07C | | | | |
| reg_aagc_rf_gain[7:0] | | 7:0 | rs | Return AGC RF gain value | 8'h0 |
| | 0xD07D | | | | |
| reg_aagc_if_gain[7:0] | | 7:0 | rs | Return AGC IF gain value | 8'h0 |
| | 0xD140 | | | | |
| reg_bfs_fcw[7:0] | | 7:0 | rw | BFS Frequency Control Word | 8'h0 |
| | 0xD141 | | | | |
| reg_bfs_fcw[15:8] | | 7:0 | rw | BFS Frequency Control Word | 8'h0 |
| | 0xD142 | | | | |
| reg_bfs_fcw[22:16] | | 6:0 | rw | BFS Frequency Control Word | 7'h0 |
| | 0xD150 | | | | |
| fcw_q[7:0] | | 7:0 | rs | Carrier frequency offset value | 8'h0 |
| | 0xD151 | | | | |
| fcw_q[15:8] | | 7:0 | rs | Carrier frequency offset value | 8'h0 |
| | 0xD152 | | | | |
| fcw_q[22:16] | | 6:0 | rs | Carrier frequency offset value | 7'h0 |
| | 0xD180 | | | | |
| reg_f_adc[7:0] | | 7:0 | rw | ADC frequency | 8'h0 |
| | 0xD181 | | | | |
| reg_f_adc[15:8] | | 7:0 | rw | ADC frequency | 8'h0 |
| | 0xD182 | | | | |
| reg_f_adc[23:16] | | 7:0 | rw | ADC frequency | 8'h0 |
| | 0xD190 | | | | |
| intp_mu[7:0] | | 7:0 | rs | Sampling Frequency Offset. | 8'h0 |
| | 0xD191 | | | | |
| intp_mu[15:8] | | 7:0 | rs | Sampling Frequency Offset. | 8'h0 |
| | 0xD192 | | | | |
| intp_mu[23:16] | | 7:0 | rs | Sampling Frequency Offset. | 8'h0 |
| | 0xD1A0 | | | | |
| reg_agc_rst | | 0 | rws | Reset RF AGC | 1'h0 |
| rf_agc_en | | 1 | rw | Enable RF AGC | 1'h0 |
| agc_lock | | 6 | rws | Indicate AGC lock | 1'h0 |
| | 0xD2C0 | | | | |

| | | | | | |
|---|---|---|---|---|---|
| fpcc_cp_corr_signn[7:0] | | 7:0 | rs | Pilot error count | 8'h0 |
| | 0xD2E1 | | | | |
| reg_qnt_vbc_rdy | | 3 | rws | vbc ready indicator | 1'h0 |
| | 0xD2E2 | | | | |
| reg_qnt_vbc_sframe_num[7:0] | | 7:0 | rw | vbc count (unit: super-frames) | 8'h1 |
| | 0xD2E3 | | | | |
| reg_qnt_vbc_err[7:0] | | 7:0 | rs | vbc error count | 8'h0 |
| | 0xD2E4 | | | | |
| reg_qnt_vbc_err[15:8] | | 7:0 | rs | vbc error count | 8'h0 |
| | 0xD2E5 | | | | |
| reg_qnt_vbc_err[23:16] | | 7:0 | rs | vbc error count | 8'h0 |
| | 0xD2E6 | | | | |
| reg_qnt_vbc_ccid_mode | | 0 | rw | Busy status of 0xD2E3, 0xD2E4, 0xD2E5.<br>0: Available (not busy)<br>1: Unavailable (busy) | 1'h0 |
| | 0xD330 | | | | |
| tpsd_lock | | 3 | rws | To declare whether TPS is lock or not. NOTE: OFSM should "read clear" this register. | 1'h0 |
| tpsd_s19 | | 4 | rs | S19 of Length indicator.<br>0: Cell_id is not supported<br>1: Cell_id is supported. | 1'h0 |
| tpsd_s17 | | 5 | rs | S17 of Length indicator.<br>0: Reserved Bits are not used<br>1: Reserved Bits are used | 1'h0 |
| | 0xD385 | | | | |
| rsd_packet_unit[7:0] | | 7:0 | rw | RBC packet number per unit for error count | 8'h0 |
| | 0xD386 | | | | |
| rsd_packet_unit[15:8] | | 7:0 | rw | RBC packet number per unit for error count | 8'h1 |
| | 0xD387 | | | | |
| reg_rsd_bit_err_cnt[7:0] | | 7:0 | rs | RBC error bit counter | 8'h0 |
| . | 0xD388 | | | | |
| reg_rsd_bit_err_cnt[15:8] | | 7:0 | rs | RBC error bit counter | 8'h0 |
| . | 0xD389 | | | | |
| reg_rsd_bit_err_cnt[23:16] | | 7:0 | rs | RBC error bit counter | 8'h0 |
| | 0xD38A | | | | |
| reg_rsd_abort_packet_cnt[7:0] | | 7:0 | rs | RBC abort packet counter | 8'h0 |
| . | 0xD38B | | | | |
| reg_rsd_abort_packet_cnt[15:8] | | 7:0 | rs | RBC abort packet counter | 8'h0 |
| | 0xD3C0 | | | | |

| | | | | | |
|---|---|---|---|---|---|
| reg_tpsd_txmod[1:0] | | 1:0 | rw | s38~s39 Transmission mode | 2'h0 |
| reg_tpsd_gi[1:0] | | 3:2 | rw | s36~s37 Guard interval | 2'h0 |
| reg_tpsd_hier[2:0] | | 6:4 | rw | s27~s29 Hierarchy information | 3'h0 |
| | 0xD3C1 | | | | |
| reg_bw[1:0] | | 3:2 | rw | channel bandwidth | 2'h0 |
| reg_dec_pri | | 4 | rw | Decode Priority | 1'h0 |
| reg_tpsd_const[1:0] | | 7:6 | rw | s25~s26 Constellation | 2'h0 |
| | 0xD3C2 | | | | |
| reg_tpsd_hpcr[2:0] | | 2:0 | rw | Code Rate, HP stream s30~s32 | 3'h0 |
| reg_tpsd_lpcr[2:0] | | 5:3 | rw | Code Rate, LP stream s33~s35 | 3'h0 |
| | 0xD400 | | | | |
| i2c_m_slave_addr[7:0] | | 7:0 | rw | 2-wire bus master slave address | 8'h0 |
| | 0xD401 | | | | |
| i2c_m_data1[7:0] | | 7:0 | rw | 2-wire bus master mail box data1 | 8'h0 |
| | 0xD402 | | | | |
| i2c_m_data2[7:0] | | 7:0 | rw | 2-wire bus master mail box data2 | 8'h0 |
| | 0xD403 | | | | |
| i2c_m_data3[7:0] | | 7:0 | rw | 2-wire bus master mail box data3 | 8'h0 |
| | 0xD404 | | | | |
| i2c_m_data4[7:0] | | 7:0 | rw | 2-wire bus master mail box data4 | 8'h0 |
| | 0xD405 | | | | |
| i2c_m_data5[7:0] | | 7:0 | rw | 2-wire bus master mail box data5 | 8'h0 |
| | 0xD406 | | | | |
| i2c_m_data6[7:0] | | 7:0 | rw | 2-wire bus master mail box data6 | 8'h0 |
| | 0xD407 | | | | |
| i2c_m_data7[7:0] | | 7:0 | rw | 2-wire bus master mail box data7 | 8'h0 |
| | 0xD408 | | | | |
| i2c_m_data8[7:0] | | 7:0 | rw | 2-wire bus master mail box data8 | 8'h0 |
| | 0xD409 | | | | |
| i2c_m_data9[7:0] | | 7:0 | rw | 2-wire bus master mail box data9 | 8'h0 |
| | 0xD40A | | | | |
| i2c_m_data10[7:0] | | 7:0 | rw | 2-wire bus master mail box data10 | 8'h0 |
| | 0xD40B | | | | |
| i2c_m_data11[7:0] | | 7:0 | rw | 2-wire bus master mail box data11 | 8'h0 |
| | 0xD40C | | | | |
| i2c_m_data12[7:0] | | 7:0 | rw | 2-wire bus master mail box data12 | 8'h0 |
| | 0xD40D | | | | |
| i2c_m_data13[7:0] | | 7:0 | rw | 2-wire bus master mail box data13 | 8'h0 |

| | | | | | |
|---|---|---|---|---|---|
| | 0xD40E | | | | |
| i2c_m_data14[7:0] | | 7:0 | rw | 2-wire bus master mail box data14 | 8'h0 |
| | 0xD40F | | | | |
| i2c_m_data15[7:0] | | 7:0 | rw | 2-wire bus master mail box data15 | 8'h0 |
| | 0xD410 | | | | |
| i2c_m_data16[7:0] | | 7:0 | rw | 2-wire bus master mail box data16 | 8'h0 |
| | 0xD411 | | | | |
| i2c_m_data17[7:0] | | 7:0 | rw | 2-wire bus master mail box data17 | 8'h0 |
| | 0xD412 | | | | |
| i2c_m_data18[7:0] | | 7:0 | rw | 2-wire bus master mail box data18 | 8'h0 |
| | 0xD413 | | | | |
| i2c_m_data19[7:0] | | 7:0 | rw | 2-wire bus master mail box data19 | 8'h0 |
| | 0xD414 | | | | |
| i2c_m_cmd_rw | | 0 | rw | 2-wire bus master command byte read/write specification | 1'h0 |
| i2c_m_cmd_rwlen[3:0] | | 6:3 | rw | 2-wire bus master command byte read/write length specification | 4'h0 |
| | 0xD415 | | | | |
| i2c_m_status_cmd_exe | | 0 | rw | 2-wire bus master status execution indicator | 1'h0 |
| i2c_m_status_wdat_done | | 1 | rws | 2-wire bus master write done indicator | 1'h0 |
| i2c_m_status_wdat_fail | | 2 | rws | 2-wire bus master write fail indicator | 1'h0 |
| i2c_m_status_rdat_rdy | | 3 | rws | 2-wire bus master read data ready | 1'h0 |
| | 0xD416 | | | | |
| i2c_m_period[7:0] | | 7:0 | rw | 2-wire bus master period setting. | 8'h0 |
| | 0xD417 | | | | |
| i2c_m_reg_msb_lsb | | 0 | rw | 2-wire bus master register: MSB/LSB selector | 1'h1 |
| reg_sample_period_on_tuner | | 2 | rw | sample period on tuner | 1'h0 |
| reg_sel_tuner | | 3 | rw | 2-wire bus master register: 2-wire bus traffic selector for tuner | 1'h0 |
| | 0xD500 | | | | |
| mpeg_par_mode | | 1 | rw | MPEG-2 output is parallel | 1'h0 |
| mpeg_ser_mode | | 2 | rw | MPEG-2 output is serial | 1'h0 |
| mpeg_ser_do7 | | 3 | rw | MPEG-2 serial output pin number. 0: output from DATA0, 1: output from DATA1 | 1'h0 |
| data_access_disable | | 4 | rw | disable MPEG-2 data access | 1'h0 |
| keep_sf_sync_byte | | 5 | rw | keep super frame sync byte | 1'h0 |
| no_modify_tei_bit | | 6 | rw | disable modification of TEI | 1'h0 |
| | 0xD501 | | | | |
| mpeg_clk_pol | | 0 | rw | The polarity of MPCLK signal | 1'h0 |

| | | | | | |
|---|---|---|---|---|---|
| | | | | 0: Data changed after positive edge of MPCLK<br>1: Data changed after negative edge of MPCLK | |
| mpeg_vld_pol | | 1 | rw | The polarity of MPFRM signal<br>0: active high (set to 1 to indicate valid data)<br>1: active low | 1'h0 |
| mpeg_sync_pol | | 2 | rw | The polarity of MPSTR signal<br>0: active high (set to 1 to indicate frame sync)<br>1: active low | 1'h0 |
| mpeg_err_pol | | 3 | rw | The polarity of MPFAIL signal<br>0: active high (set to 1 to indicate error)<br>1: active low | 1'h0 |
| mpeg_clk_gated | | 4 | rw | The style of MPCLK signal<br>0: free running MPCLK<br>1: gated MPCLK<br>When gated clock is selected, there is no clock running when no valid data is available. | 1'h0 |
| msdo_msb | | 5 | rw | MSB or LSB first on the MPEG data output<br>0: LSB first<br>1: MSB first | 1'h1 |
| mssync_len | | 6 | rw | MPSTR is asserted for the first bit or byte<br>0: asserted for whole bits of first byte<br>1: asserted for first bit only | 1'h0 |
| | 0xD502 | | | | |
| reg_mpeg_full_speed | | 4 | rw | full speed in mpeg interface | 1'h0 |
| | 0xD503 | | | | |
| pid_en | | 0 | rw | pid_en | 1'h0 |
| pid_rst | | 1 | rws | Reset PID table | 1'h0 |
| pid_complement | | 2 | rw | PID table complement; 0: pid out if table hit, 1: pid out if table not hit. | 1'h0 |
| | 0xD504 | | | | |
| pid_index[4:0] | | 4:0 | rws | PID index | 5'h0 |
| pid_index_en | | 5 | rws | Enable current PID index | 1'h0 |
| | 0xD505 | | | | |
| pid_dat_l[7:0] | | 7:0 | rw | PID data register (bit 7-0) | 8'h0 |
| | 0xD506 | | | | |
| pid_dat_h[4:0] | | 4:0 | rw | PID data register (bit 12-8) | 5'h0 |
| | 0xD507 | | | | |
| reg_mp2_sw_rst | | 2 | rw | Software reset | 1'h1 |
| reg_mpeg_vld_tgl | | 3 | rw | MPFRM toggle select | 1'h0 |
| sync_byte_locked | | 6 | rs | indicate sync_byte_locked | 1'h0 |
| reg_mp2_sw_rst2 | | 3 | rw | Software reset | 1'h1 |

| | | | | | |
|---|---|---|---|---|---|
| | 0xD50C | | | | |
| reg_tpsd_bw_mp2if[1:0] | | 1:0 | rw | programmed bw | 2'h0 |
| reg_tpsd_gi_mp2if[1:0] | | 3:2 | rw | programmed gi | 2'h0 |
| reg_tpsd_cr_mp2if[2:0] | | 6:4 | rw | programmed cr | 3'h0 |
| | 0xD50D | | | | |
| reg_tpsd_cons_mp2if[1:0] | | 1:0 | rw | programmed constellation | 2'h0 |
| reg_fw_table_en | | 2 | rw | programmed tpsd enable | 1'h0 |
| | 0xD510 | | | | |
| reg_packet_gap[4:0] | | 4:0 | rw | size of the gap between 188 packets | 5'h10 |
| | 0xD520 | | | | |
| reg_ts_clk_inv | | 0 | rw | Invert the input clock of 2nd TS. | 1'h0 |
| reg_ts_dat_inv | | 1 | rw | Invert the input data of 2nd TS. | 1'h0 |
| reg_ts_lsb_1st | | 2 | rw | 0: the input serial data of 2nd TS is MSB first; 1: the input serial data of 2nd TS is LSB first. | 1'h0 |
| reg_ts_capt_bg_sel | | 3 | rw | 0: the 2nd TS input sync signal is not used to sync data; 1: the 2nd TS input sync signal is used to sync data | 1'h1 |
| reg_mp2if_stop_en | | 4 | rw | 0: back pressure scheme is not applied; 1: enable back pressure to do flow control of the 2nd TS. | 1'h0 |
| reg_mp2if2_pes_base | | 5 | rw | 0: the 2nd TS data can be dropped anytime when the buffer is full; 1: the 2nd TS data will be dropped by the unit of 188 bytes. | 1'h0 |
| reg_ts_sync_inv | | 6 | rw | Invert the input signal "sync" of 2nd TS. | 1'h0 |
| reg_ts_vld_inv | | 7 | rw | Invert the input signal "valid" of 2nd TS. | 1'h0 |
| | 0xD607 | | | | |
| reg_bypass_host2tuner | | 2 | rw | 0:disable 1:enable, create bypass path from host to tuner 2-wire bus | 1'h0 |
| | 0xD730 | | | | |
| reg_top_lock1out | | 0 | rw | lock1 direct output tpsd/mepg_lock enable | 1'h0 |
| reg_top_lock1_tpsd | | 1 | rw | lock1 output, 1: tpsd_lock, 0: mpeg_lock | 1'h0 |
| reg_top_lock2out | | 2 | rw | lock2 direct output tpsd/mepg_lock enable | 1'h0 |
| reg_top_lock2_tpsd | | 3 | rw | lock2 output, 1: tpsd_lock, 0: mpeg_lock | 1'h0 |
| reg_top_lock3out | | 4 | rw | lock3 direct output tpsd/mepg_lock enable | 1'h0 |
| reg_top_lock3_tpsd | | 5 | rw | lock3 output, 1: tpsd_lock, 0: mpeg_lock | 1'h0 |
| reg_top_lock4out | | 6 | rw | lock4 direct output tpsd/mepg_lock enable | 1'h0 |
| reg_top_lock4_tpsd | | 7 | rw | lock4 output, 1: tpsd_lock, 0: mpeg_lock | 1'h0 |
| | 0xD731 | | | | |
| reg_top_pwrdw_hwen | | 0 | rw | Shut down clock without interrupting control unit. | 1'h0 |
| reg_top_pwrdw | | 6 | rw | turn on pwrdw function | 1'h0 |

| | | | | | |
|---|---|---|---|---|---|
| reg_top_pwrdw_inv | | 7 | rw | turn on pwrdw inverse function | 1'h0 |
| | 0xD734 | | | | |
| reg_top_lock1on | | 0 | rw | gpio on | 1'h0 |
| reg_top_lock1en | | 1 | rw | gpio on | 1'h0 |
| reg_top_lock1o | | 2 | rw | gpio on | 1'h0 |
| reg_top_lock1i | | 3 | rs | gpio on | 1'h0 |
| reg_top_lock2on | | 4 | rw | gpio on | 1'h0 |
| reg_top_lock2en | | 5 | rw | gpio on | 1'h0 |
| reg_top_lock2o | | 6 | rw | gpio on | 1'h0 |
| reg_top_lock2i | | 7 | rs | gpio on | 1'h0 |
| | 0xD735 | | | | |
| reg_top_gpio0on | | 0 | rw | gpio output | 1'h1 |
| reg_top_gpio0en | | 1 | rw | gpio output | 1'h1 |
| reg_top_gpio0o | | 2 | rw | gpio output | 1'h0 |
| reg_top_gpio0i | | 3 | rs | gpio output | 1'h0 |
| reg_top_gpio1on | | 4 | rw | gpio output | 1'h1 |
| reg_top_gpio1en | | 5 | rw | gpio output | 1'h1 |
| reg_top_gpio1o | | 6 | rw | gpio output | 1'h1 |
| reg_top_gpio1i | | 7 | rs | gpio output | 1'h0 |
| | 0xD736 | | | | |
| reg_top_gpio2on | | 0 | rw | gpio output | 1'h0 |
| reg_top_gpio2en | | 1 | rw | gpio output | 1'h0 |
| reg_top_gpio2o | | 2 | rw | gpio output | 1'h0 |
| reg_top_gpio2i | | 3 | rs | gpio output | 1'h0 |
| reg_top_gpio3on | | 4 | rw | gpio output | 1'h0 |
| reg_top_gpio3en | | 5 | rw | gpio output | 1'h0 |
| reg_top_gpio3o | | 6 | rw | gpio output | 1'h0 |
| reg_top_gpio3i | | 7 | rs | gpio output | 1'h0 |
| | 0xD737 | | | | |
| reg_top_gpio4on | | 0 | rw | gpio output | 1'h0 |
| reg_top_gpio4en | | 1 | rw | gpio output | 1'h0 |
| reg_top_gpio4o | | 2 | rw | gpio output | 1'h0 |
| reg_top_gpio4i | | 3 | rs | gpio output | 1'h0 |
| | 0xD73B | | | | |
| reg_afe_mem1[3] | | 3 | rws | 1: ADC input range is 2V peak-to-peak<br>0: ADC input range is 1V peak-to-peak | 1'h0 |
| | 0xD740 | | | | |
| reg_top_padmpdr2 | | 0 | rw | pads driving strength | 1'h0 |

| | | | | | |
|---|---|---|---|---|---|
| reg_top_padmpdr4 | | 1 | rw | pads driving strength | 1'h1 |
| reg_top_padmpdr8 | | 2 | rw | pads driving strength | 1'h0 |
| reg_top_padmpdrsr | | 3 | rw | pads driving strength | 1'h0 |
| | 0xD742 | | | | |
| reg_rst_i2cs | | 0 | rw | reset of 2-wire slave | 1'h0 |
| reg_rst_i2cm | | 1 | rw | reset of 2-wire master | 1'h0 |
| | 0xD743 | | | | |
| reg_top_gpiosdaon | | 0 | rw | gpio output | 1'h0 |
| reg_top_gpiosdaen | | 1 | rw | gpio output | 1'h0 |
| reg_top_gpiosdao | | 2 | rw | gpio output | 1'h1 |
| reg_top_gpiosdai | | 3 | rs | gpio output | 1'h0 |
| reg_top_gpiosclon | | 4 | rw | gpio output | 1'h0 |
| reg_top_gpiosclen | | 5 | rw | gpio output | 1'h0 |
| reg_top_gpiosclo | | 6 | rw | gpio output | 1'h1 |
| reg_top_gpioscli | | 7 | rs | gpio output | 1'h0 |