AMIC

A82DL16x4T(U) Series

Stacked Multi-Chip Package (MCP) Flash Memory and SRAM, A82DL16x4T(U) 16 Megabit (2Mx8 Bit/1Mx16 Bit) CMOS 3.3 Volt-only, Simultaneous Operation Flash Memory and 4M (256Kx16 Bit) Static RAM

Preliminary

Document Title

Stacked Multi-Chip Package (MCP) Flash Memory and SRAM, A82DL16x4T(U) 16 Megabit (2Mx8 Bit/1Mx16 Bit) CMOS 3.3 Volt-only, Simultaneous Operation Flash Memory and 4M (256Kx16 Bit) Static RAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	August 15, 2005	Preliminary

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DISTINCTIVE CHARACTERISTICS

MCP Features

- Single power supply operation 2.7 to 3.6 volt
- High Performance
  - Access time as fast as 70ns
- Package 69-Ball TFBGA (8x11x1.4 mm)
- Industrial operating temperature range: -40°C to 85°C for –U; -25°C to 85°C for –I

Flash Features

ARCHITECTURAL ADVANTAGES

- Simultaneous Read/Write operations
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- Multiple bank architectures
  - Three devices available with different bank sizes (refer to Table 2)
- Package
  - 69-Ball TFBGA (8x11x1.4 mm)
- Top or bottom boot block
- Manufactured on 0.18 µm process technology
  - Compatible with AM42DL16x4D devices
- Compatible with JEDEC standards
  - Pinout and software compatible with single-power-supply flash standard

PERFORMANCE CHARACTERISTICS

- High performance
  - Access time as fast as 70ns
  - Program time: 7µs/word typical utilizing Accelerate function
- Ultra low power consumption (typical values)
  - 2mA active read current at 1MHz
  - 10mA active read current at 5MHz
  - 200nA in standby or automatic sleep mode
- Minimum 1 million write cycles guaranteed per sector
- 20 Year data retention at 125°C
  - Reliable operation for the life of the system

SOFTWARE FEATURES

- Supports Common Flash Memory Interface (CFI)
- Erase Suspend/Erase Resume
  - Suspends erase operations to allow programming in same bank
- $\overline{\text{Data}}$ Polling and Toggle Bit
  - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- Any combination of sectors can be erased
- Ready/$\overline{\text{Busy}}$ output (RY/$\overline{\text{BY}}$)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin ($\overline{\text{RESET}}$)
  - Hardware method of resetting the internal state machine to reading array data
- $\overline{\text{WP}}$ /ACC input pin
  - Write protect ($\overline{\text{WP}}$) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- Sector protection
  - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

LP SRAM Features

- Power supply range: 2.7V to 3.6V
- Access times: 70 ns (max.)
- Current:
  Very low power version: Operating: 35mA(max.)
  Standby: 10uA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Output enable and two chips enable inputs for easy application
- Data retention voltage: 2.0V (min.)

GENERAL DESCRIPTION

The A82DL16x2T(U) family consists of 16 megabit, 3.0 volt-only flash memory devices, organized as 1,048,576 words of 16 bits each or 2,097,152 bytes of 8 bits each. Word mode data appears on I/O_0–I/O_{15}; byte mode data appears on I/O_0–I/O_7. The device is designed to be programmed in-system with the standard 3.0 volt VCC supply, and can also be programmed in standard EPROM programmers.

The device is available with an access time of 70ns. The devices are offered in 69-ball Fine-pitch BGA. Standard control pins—chip enable ($\overline{CE\_F}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$)—control normal read and write operations, and avoid bus contention issues.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into two banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The A82DL16x4T(U) devices uses multiple bank architectures to provide flexibility for different applications. Three devices are available with these bank sizes:

Device	Bank 1	Bank 2
DL1624	2 Mb	14 Mb
DL1634	4 Mb	12 Mb
DL1644	8 Mb	8 Mb

A82DL16x4T(U) Features

The device offers complete compatibility with the **JEDEC single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bits:** RY/$\overline{BY}$ pin, I/O_7 ($\overline{Data}$ Polling) and I/O_6/I/O_2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

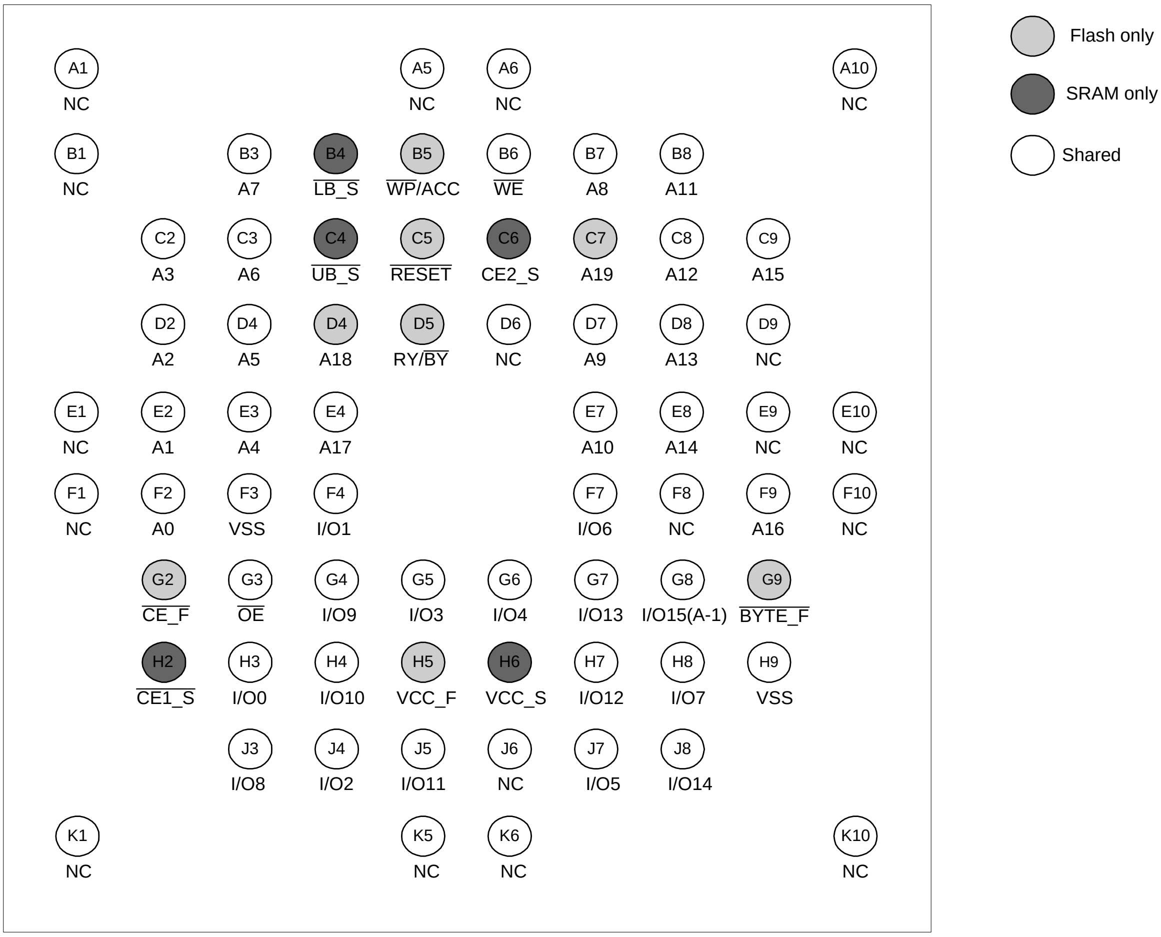
The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low VCC detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-s y s t e m or via programming equipment.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Pin Configurations

■ **69-Ball TFBGA**
Top View



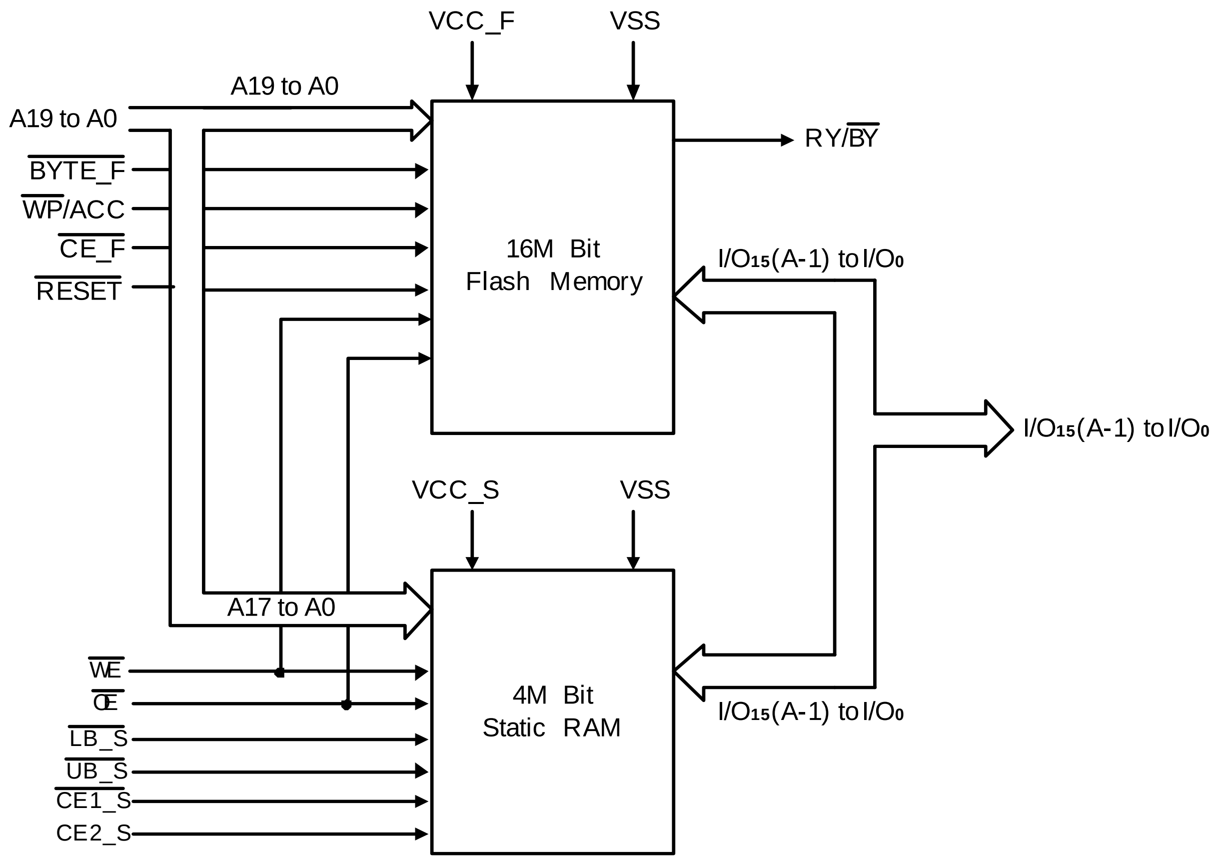
Special Handling Instructions for TFBGA Package

Special handling is required for Flash Memory products in TFBGA packages.
Flash memory devices in TFBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time

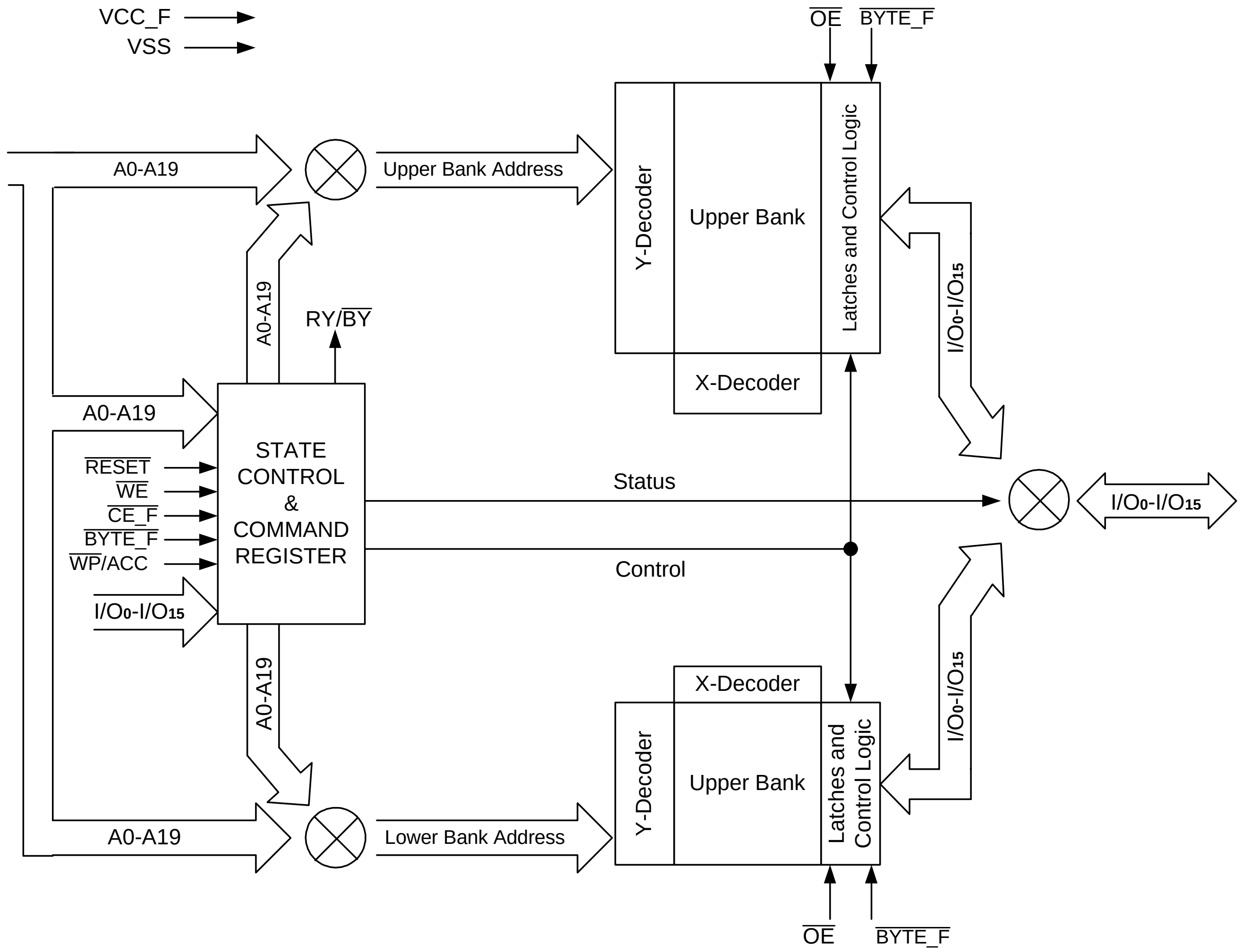
Product Information Guide

Part Number		A82DL16x4T(U)
Speed Options	Standard Voltage Range: VCC_F/VCC_S=2.7-3.6V	70
Max Access Time (ns)		70
$\overline{CE\_F}$ / $\overline{CE\_S}$ Access (ns)		70
$\overline{OE}$ Access (ns)		40

MCP Block Diagram



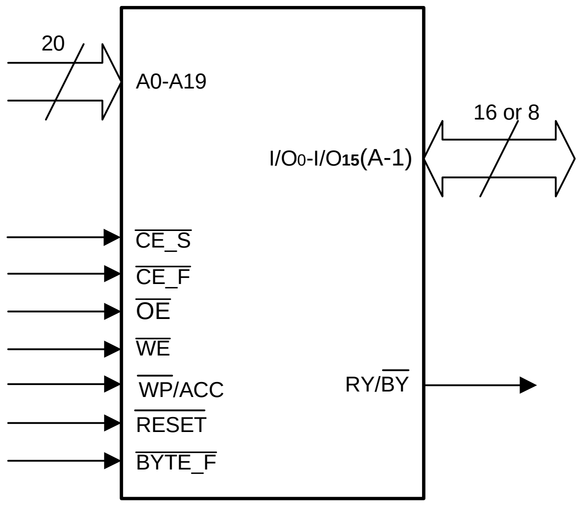
Flash Block Diagram



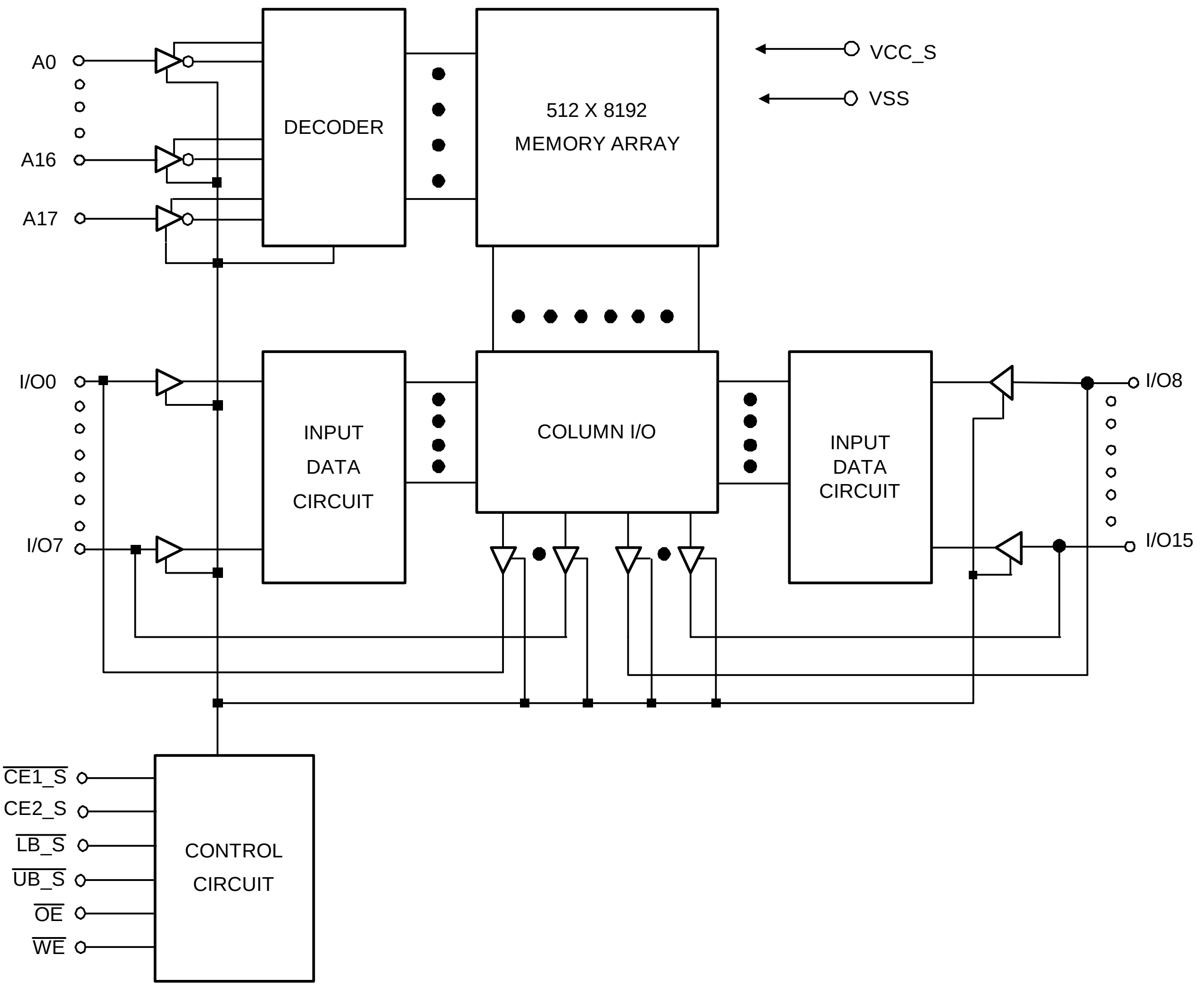
Pin Descriptions

Pin No.		Description
A0 - A19		Address Inputs
I/O_0 - I/O_{14}		Data Inputs/Outputs
I/O_{15} (A-1)	I/O_{15}	Data Input/Output, Word Mode
	A-1	LSB Address Input, Byte Mode
$\overline{\text{CE\_F}}$		Chip Enable
$\overline{\text{CE\_S}}$		Chip Enable (SRAM)
$\overline{\text{WE}}$		Write Enable
$\overline{\text{OE}}$		Output Enable
$\overline{\text{WP}}$ /ACC		Hardware Write Protect/Acceleration Pin
$\overline{\text{RESET}}$		Hardware Reset Pin, Active Low
$\overline{\text{BYTE\_F}}$		Selects 8-bit or 16-bit Mode
RY/$\overline{\text{BY}}$		Ready/$\overline{\text{BUSY}}$ Output
VSS		Ground
VCC_F		Power Supply (Flash)
VCC_S		Power Supply (SRAM)
NC		Pin Not Connected Internally

Logic Symbol



SRAM Block Diagram



DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1-1. Device Bus Operations – Flash Byte Mode ($\overline{BYTE\_F}$ = V_{IH})

Operation (Notes 1, 2)	$\overline{CE\_F}$	$\overline{CE1\_S}$	CE2_S	$\overline{OE}$	$\overline{WE}$	A0-A19	$\overline{LB\_S}$ (Note3)	$\overline{UB\_S}$ (Note3)	$\overline{RESET}$	$\overline{WP}$/ACC (Note 4)	I/O7–I/O0	I/O15–I/O0
Read from Flash	L	H	X	L	H	AIN	X	X	H	L/H	IOUT	IOUT
		X	L									
Write to Flash	L	H	X	H	L	AIN	X	X	H	(Note 4)	IIN	IIN
		X	L									
Standby	VCC ± 0.3 V	H	X	X	X	X	X	X	VCC ± 0.3 V	H	High-Z	High-Z
		X	L									
Output Disable	L	L	H	H	H	X	L	X	H	L/H	High-Z	High-Z
							X	L				
Flash Hardware Reset	X	H	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L									
		H	X									
Sector Protect (Notes)	L	X	L	H	L	SA, A6 = L, A1 = H, A0 = L	X	X	VID	L/H	IIN	X
		H	X									
Sector Unprotect (Note 5)	L	X	L	H	L	SA, A6 = H, A1 = H, A0 = L	X	X	VID	(Note 6)	IIN	X
Temporary Sector Unprotect	X	H	X	X	X	AIN	X	X	VID	(Note 6)	IIN	High-Z
		X	L								IOUT	IOUT
Read from SRAM	H	L	H	L	H	AIN	H	L	H	X	High-Z	IOUT
							L	H			IOUT	High-Z
							L	L			IIN	IIN
Write to SRAM	H	L	H	X	L	AIN	H	L	H	X	High-Z	IIN
							L	H			IIN	High-Z

Legend: L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 8.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, I_{IN} = Data In, I_{OUT} = Data Out

Notes:

1. Other operations except for those indicated in this column are inhibited.
2. Do not apply $\overline{CE\_F}$ = V_{IL}, $\overline{CE1\_S}$ = V_{IL} and CE2_S = V_{IH} at the same time.
3. Don't care or open $\overline{LB\_S}$ or $\overline{UB\_S}$.
4. The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.
5. If $\overline{WP}$/ACC = V_{IL}, the two outermost boot sectors remain protected. If $\overline{WP}$/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If $\overline{WP}$/ACC = V_{HH}, all sectors will be unprotected.

Table 1-2. Device Bus Operations – Flash Byte Mode ($\overline{\text{BYTE\_F}}$ = V_{IL})

Operation (Notes 1, 2)	$\overline{\text{CE\_F}}$	$\overline{\text{CE1\_S}}$	CE2_S	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0-A19	$\overline{\text{LB\_S}}$ (Note3)	$\overline{\text{UB\_S}}$ (Note3)	$\overline{\text{RESET}}$	$\overline{\text{WP}}$/ACC (Note 4)	I/O$_7$–I/O$_0$	I/O$_{15}$–I/O$_8$
Read from Flash	L	H	X	L	H	A_{IN}	X	X	H	L/H	I_{OUT}	High-Z
		X	L									
Write to Flash	L	H	X	H	L	A_{IN}	X	X	H	(Note 3)	I_{IN}	I/O$_{14-8}$ =Hi-Z; I/O$_{15}$=A-1
		X	L									
Standby	VCC ± 0.3 V	H	X	X	X	X	X	X	VCC_F ± 0.3 V	H	High-Z	High-Z
		X	L									
Output Disable	L	L	H	H	H	X	L	X	H	L/H	High-Z	High-Z
				H	X	X	X	L				
Flash Hardware Reset	X	H	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L									
Sector Protect (Notes)	L	H	X	H	L	SA, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	I_{IN}	X
		X	L									
Sector Unprotect (Note 5)	L	H	X	H	L	SA, A6 = H, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	I_{IN}	X
		X	L									
Temporary Sector Unprotect	X	H	X	X	X	A_{IN}	X	X	V_{ID}	(Note 6)	I_{IN}	High-Z
		X	L									
Read from SRAM	H	L	H	L	H	A_{IN}	H	L	H	X	I_{OUT}	I_{OUT}
							H	L			High-Z	I_{OUT}
							L	H			I_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	A_{IN}	H	L	H	X	I_{IN}	I_{IN}
							L	H			High-Z	I_{IN}
							L	H			I_{IN}	High-Z

Legend: L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 8.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In (for Flash Byte Mode, I/O$_{15}$=A-1), I_{IN} = Data In, I_{OUT} = Data Out

Notes:

1.Other operations except for those indicated in this column are inhibited.

2.Do not apply $\overline{\text{CE\_F}}$ = V_{IL}, $\overline{\text{CE1\_S}}$ = V_{IL} and CE2_S = V_{IH} at the same time.

3.Don't care or open $\overline{\text{LB\_S}}$ or $\overline{\text{UB\_S}}$.

4.The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.

5. If $\overline{\text{WP}}$/ACC = V_{IL}, the two outermost boot sectors remain protected. If $\overline{\text{WP}}$/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If $\overline{\text{WP}}$/ACC = V_{HH}, all sectors will be unprotected.

Word/Byte Configuration

The BYTE_F pin determines whether the I/O pins I/O15-I/O0 operate in the byte or word configuration. If the BYTE_F pin is set at logic "1", the device is in word configuration, I/O15-I/O0 are active and controlled by CE_F and OE.

If the BYTE_F pin is set at logic "0", the device is in byte configuration, and only I/O0-I/O7 are active and controlled by CE_F and OE. I/O8-I/O14 are tri-stated, and I/O15 pin is used as an input for the LSB(A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE_F and OE pins to VIL. CE_F is the power control and selects the device. OE is the output control and gates array data to the output pins. WE should remain at VIH. The BYTE_F pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

See "Requirements for Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 11 for the timing waveform, ICC1_F in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE and CE_F to VIL, and OE to VIH.

For program operations, the BYTE_F pin determines whether the device accepts program data in bytes or words, Refer to "Word/Byte Configuration" for more information.

The device features an Unlock Bypass mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word / Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequence.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables 3-4 indicate the address range that each sector occupies. The device address space is divided into two banks: Bank 1 contains the boot/parameter sectors, and Bank 2 contains the larger, code sectors of uniform size. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" is the address bits required to uniquely select a sector.

ICC2_F in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP /ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts VHH on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing VHH from the WP /ACC pin returns the device to normal operation. Note that the WP /ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result. In addition, the WP /ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on I/O7-I/O0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 18 shows how read and write cycles may be initiated for simultaneous operation with zero latency. ICC6_F and ICC7_F in the DC Characteristics table represent the current specifications for read-while-program and read-while-erase, respectively.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE input.

The device enters the CMOS standby mode when the CE_F & RESET pins are both held at VCC_F ± 0.3V. (Note that this is a more restricted voltage range than VIH.) If CE_F and RESET are held at VIH, but not within VCC_F ± 0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires the standard access time (tCE) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

ICC3_F in the DC Characteristics tables represent the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} +30ns. The automatic sleep mode is independent of the $\overline{CE\_F}$, $\overline{WE}$ and $\overline{OE}$ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4_F} in the DC Characteristics table represents the automatic sleep mode current specification.

$\overline{RESET}$: Hardware Reset Pin

The $\overline{RESET}$ pin provides a hardware method of resetting the device to reading array data. When the system drives the $\overline{RESET}$ pin low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the $\overline{RESET}$ pulse. When $\overline{RESET}$ is held at VSS ± 0.3V, the device draws CMOS standby current (I_{CC4_F}). If $\overline{RESET}$ is held at V_{IL} but not within VSS ± 0.3V, the standby current will be greater.

The $\overline{RESET}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If $\overline{RESET}$ is asserted during a program or erase operation, the RY/$\overline{BY}$ pin remains a "0" (busy) until the internal reset operation is complete, which requires a time t_{READY} (during Embedded Algorithms). The system can thus monitor RY/$\overline{BY}$ to determine whether the reset operation is complete. If $\overline{RESET}$ is asserted when a program or erase operation is not executing (RY/$\overline{BY}$ pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the $\overline{RESET}$ pin return to V_{IH}.

Refer to the AC Characteristics tables for $\overline{RESET}$ parameters and diagram.

Output Disable Mode

When the $\overline{OE}$ input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. A82DL16x4T(U) Device Bank Divisions

Device Part Number	Bank 1		Bank 2	
	Megabits	Sector Sizes	Megabits	Sector Sizes
A82DL1624	2 Mbit	Eight 8 Kbyte/4 Kword, three 64 Kbyte/32 Kword	14 Mbit	Twenty-eight 64 Kbyte/32 Kword
A82DL1634	4 Mbit	Eight 8 Kbyte/4 Kword, seven 64 Kbyte/32 Kword	12 Mbit	Twenty-four 64 Kbyte/32 Kword
A82DL1644	8 Mbit	Eight 8 Kbyte/4 Kword, fifteen 64 Kbyte/32 Kword	8 Mbit	Sixteen 64 Kbyte/32 Kword

Table 3. Sector Addresses for Top Boot Sector Devices

A82DL1644T	A82DL1634T	A82DL1624T	Sector	Sector Address A19–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
Bank 2	Bank 2	Bank 2	SA0	00000xxx	64/32	000000h-00FFFFh	00000h–07FFFh
			SA1	00001xxx	64/32	010000h-01FFFFh	08000h–0FFFFh
			SA2	00010xxx	64/32	020000h-02FFFFh	10000h–17FFFh
			SA3	00011xxx	64/32	030000h-03FFFFh	18000h–1FFFFh
			SA4	00100xxx	64/32	040000h-04FFFFh	20000h–27FFFh
			SA5	00101xxx	64/32	050000h-05FFFFh	28000h–2FFFFh
			SA6	00110xxx	64/32	060000h-06FFFFh	30000h–37FFFh
			SA7	00111xxx	64/32	070000h-07FFFFh	38000h–3FFFFh
			SA8	01000xxx	64/32	080000h-08FFFFh	40000h–47FFFh
			SA9	01001xxx	64/32	090000h-09FFFFh	48000h–4FFFFh
			SA10	01010xxx	64/32	0A0000h-0AFFFFh	50000h–57FFFh
			SA11	01011xxx	64/32	0B0000h-0BFFFFh	58000h–5FFFFh
			SA12	01100xxx	64/32	0C0000h-0CFFFFh	60000h–67FFFh
			SA13	01101xxx	64/32	0D0000h-0DFFFFh	68000h–6FFFFh
			SA14	01110xxx	64/32	0E0000h-0EFFFFh	70000h–77FFFh
			SA15	01111xxx	64/32	0F0000h-0FFFFFh	78000h–7FFFFh
Bank 1			SA16	10000xxx	64/32	100000h-10FFFFh	80000h–87FFFh
			SA17	10001xxx	64/32	110000h-11FFFFh	88000h–8FFFFh
			SA18	10010xxx	64/32	120000h-12FFFFh	90000h–97FFFh
			SA19	10011xxx	64/32	130000h-13FFFFh	98000h–9FFFFh
			SA20	10100xxx	64/32	140000h-14FFFFh	A0000h–A7FFFh
			SA21	10101xxx	64/32	150000h-15FFFFh	A8000h–AFFFFh
			SA22	10110xxx	64/32	160000h-16FFFFh	B0000h–B7FFFh
			SA23	10111xxx	64/32	170000h-17FFFFh	B8000h–BFFFFh
	Bank 1		SA24	11000xxx	64/32	180000h-18FFFFh	C0000h–C7FFFh
			SA25	11001xxx	64/32	190000h-19FFFFh	C8000h–CFFFFh
			SA26	11010xxx	64/32	1A0000h-1AFFFFh	D0000h–D7FFFh
			SA27	11011xxx	64/32	1B0000h-1BFFFFh	D8000h–DFFFFh
		Bank 1	SA28	11100xxx	64/32	1C0000h-1CFFFFh	E0000h–E7FFFh
			SA29	11101xxx	64/32	1D0000h-1DFFFFh	E8000h–EFFFFh
			SA30	11110xxx	64/32	1E0000h-1EFFFFh	F0000h–F7FFFh
			SA31	11111000	8/4	1F0000h-1F1FFFh	F8000h–F8FFFh
			SA32	11111001	8/4	1F2000h-1F3FFFh	F9000h–F9FFFh
			SA33	11111010	8/4	1F4000h-1F5FFFh	FA000h–FAFFFh
			SA34	11111011	8/4	1F6000h-1F7FFFh	FB000h–FBFFFh
			SA35	11111100	8/4	1F8000h-1F9FFFh	FC000h–FCFFFh
			SA36	11111101	8/4	1FA000h-1FBFFFh	FD000h–FDFFFh
			SA37	11111110	8/4	1FC000h-1FDFFFh	FE000h–FEFFFh
			SA38	11111111	8/4	1FE000h-1FFFFFh	FF000h–FFFFFh

Note:
The address range is A19: A-1in byte mode ($\overline{BYTE\_F}$=V_{IL}) or A19:A0 in word mode ($\overline{BYTE\_F}$=V_{IH}). The bank address bits are A19-A17 for A82DL1624T, A19 and A18 for A82DL1634T, and A19 for A82DL1644T.

Table 4. Sector Addresses for Bottom Boot Sector Devices

A82DL1644U	A82DL1634U	A82DL1624U	Sector	Sector Address A19–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
Bank 1	Bank 1	Bank 1	SA0	00000000	8/4	000000h-001FFFh	00000h-00FFFh
			SA1	00000001	8/4	002000h-003FFFh	01000h-01FFFh
			SA2	00000010	8/4	004000h-005FFFh	02000h-02FFFh
			SA3	00000011	8/4	006000h-007FFFh	03000h-03FFFh
			SA4	00000100	8/4	008000h-009FFFh	04000h-04FFFh
			SA5	00000101	8/4	00A000h-00BFFFh	05000h-05FFFh
			SA6	00000110	8/4	00C000h-00DFFFh	06000h-06FFFh
			SA7	00000111	8/4	00E000h-00FFFFh	07000h-07FFFh
			SA8	00001XXX	64/32	010000h-01FFFFh	08000h-0FFFFh
			SA9	00010XXX	64/32	020000h-02FFFFh	10000h-17FFFh
			SA10	00011XXX	64/32	030000h-03FFFFh	18000h-1FFFFh
		Bank 2	SA11	00100XXX	64/32	040000h-04FFFFh	20000h-27FFFh
			SA12	00101XXX	64/32	050000h-05FFFFh	28000h-2FFFFh
			SA13	00110XXX	64/32	060000h-06FFFFh	30000h-37FFFh
			SA14	00111XXX	64/32	070000h-07FFFFh	38000h-3FFFFh
	Bank 2		SA15	01000XXX	64/32	080000h-08FFFFh	40000h-47FFFh
			SA16	01001XXX	64/32	090000h-09FFFFh	48000h-4FFFFh
			SA17	01010XXX	64/32	0A0000h-0AFFFFh	50000h-57FFFh
			SA18	01011XXX	64/32	0B0000h-0BFFFFh	58000h-5FFFFh
			SA19	01100XXX	64/32	0C0000h-0CFFFFh	60000h-67FFFh
			SA20	01101XXX	64/32	0D0000h-0DFFFFh	68000h-6FFFFh
			SA21	01110XXX	64/32	0E0000h-0EFFFFh	70000h-77FFFh
			SA22	01111XXX	64/32	0F0000h-0FFFFFh	78000h-7FFFFh
Bank 2			SA23	10000XXX	64/32	100000h-10FFFFh	80000h-87FFFh
			SA24	10001XXX	64/32	110000h-11FFFFh	88000h-8FFFFh
			SA25	10010XXX	64/32	120000h-12FFFFh	90000h-97FFFh
			SA26	10011XXX	64/32	130000h-13FFFFh	98000h-9FFFFh
			SA27	10100XXX	64/32	140000h-14FFFFh	A0000h-A7FFFh
			SA28	10101XXX	64/32	150000h-15FFFFh	A8000h-AFFFFh
			SA29	10110XXX	64/32	160000h-16FFFFh	B0000h-B7FFFh
			SA30	10111XXX	64/32	170000h-17FFFFh	B8000h-BFFFFh
			SA31	11000XXX	64/32	180000h-18FFFFh	C0000h-C7FFFh
			SA32	11001XXX	64/32	190000h-19FFFFh	C8000h-CFFFFh
			SA33	11010XXX	64/32	1A0000h-1AFFFFh	D0000h-D7FFFh
			SA34	11011XXX	64/32	1B0000h-1BFFFFh	D8000h-DFFFFh
			SA35	11100XXX	64/32	1C0000h-1CFFFFh	E0000h-E7FFFh
			SA36	11101XXX	64/32	1D0000h-1DFFFFh	E8000h-EFFFFh
			SA37	11110XXX	64/32	1E0000h-1EFFFFh	F0000h-F7FFFh
			SA38	11111XXX	64/32	1F0000h-1FFFFFh	F8000h-FFFFFh

Note:

The address range is A19: A-1in byte mode ($\overline{BYTE\_F}$=V_{IL}) or A19:A0 in word mode ($\overline{BYTE\_F}$=V_{IH}). The bank address bits are A19-A17 for A82DL1624U, A19 and A18 for A82DL1634U, and A19 for A82DL1644U.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on I/O_7 - I/O_0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (8.5V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 5. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. (see Table 3-4). Table 5 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on I/O_7 - I/O_0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 12. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 5. A82DL16x4T(U) Autoselect Codes (High Voltage Method)

Description	$\overline{CE\_F}$	$\overline{OE}$	$\overline{WE}$	A19 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	I/O_8 to I/O_{15}		I/O_7 to I/O_0
												$\overline{BYTE\_F}$ = V_{IH}	$\overline{BYTE\_F}$ = V_{IL}	
Manufacturer ID: AMIC	L	L	H	BA	X	V_{ID}	X	L	X	L	L	X	X	37h
Device ID: A82DL1624	L	L	H	BA	X	V_{ID}	X	L	X	L	H	22h	X	2Dh (T), 2Eh (U)
Device ID: A82DL1634	L	L	H	BA	X	V_{ID}	X	L	X	L	H	22h	X	28h (T), 2Bh (U)
Device ID: A82DL1644	L	L	H	BA	X	V_{ID}	X	L	X	L	H	22h	X	33h (T), 35h (B)
Continuation ID	L	L	H	X	X	V_{ID}	X	L	X	H	H	X	X	7Fh
Read Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	X	01h (protected), 00h (unprotected)

L=Logic Low= V_{IL}, H=Logic High=V_{IH}, SA=Sector Address, X=Don't Care, BA=Bank Address

Note: The autoselect codes may also be accessed in-system via command sequences.

Sector/Sector Block Protection and Unprotection

(Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Tables 6 and 7).

Table 6. Top Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector / Sector Block	A19–A12	Sector / Sector Block Size
SA0	00000XXX	64 Kbytes
SA1-SA3	00001XXX, 00010XXX, 00011XXX	192 (3x64) Kbytes
SA4-SA7	001XXXXX	256 (4x64) Kbytes
SA8-SA11	010XXXXX	256 (4x64) Kbytes
SA12-SA15	011XXXXX	256 (4x64) Kbytes
SA16-SA19	100XXXXX	256 (4x64) Kbytes
SA20-SA23	101XXXXX	256 (4x64) Kbytes
SA24-SA27	110XXXXX	256 (4x64) Kbytes
SA28-SA30	11100XXX, 11101XXX, 11110XXX	192 (3x64) Kbytes
SA31	11111000	8 Kbytes
SA32	11111001	8 Kbytes
SA33	11111010	8 Kbytes
SA34	11111011	8 Kbytes
SA35	11111100	8 Kbytes
SA36	11111101	8 Kbytes
SA37	11111110	8 Kbytes
SA38	11111111	8 Kbytes

Table 7. Bottom Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector / Sector Block	A19–A12	Sector / Sector Block Size
SA38	11111XXX	64 Kbytes
SA37-SA35	11110XXX, 11101XXX, 11100XXX	192 (3x64) Kbytes
SA34-SA31	110XXXXX	256 (4x64) Kbytes
SA30-SA27	101XXXXX	256 (4x64) Kbytes
SA26-SA23	100XXXXX	256 (4x64) Kbytes
SA22-SA19	011XXXXX	256 (4x64) Kbytes
SA18-SA15	010XXXXX	256 (4x64) Kbytes
SA14-SA11	001XXXXX	256 (4x64) Kbytes
SA10-SA8	00001XXX, 00010XXX, 00011XXX	192 (3x64) Kbytes
SA7	00000111	8 Kbytes
SA6	00000110	8 Kbytes
SA5	00000101	8 Kbytes
SA4	00000100	8 Kbytes
SA3	00000011	8 Kbytes
SA2	00000010	8 Kbytes
SA1	00000001	8 Kbytes
SA0	00000000	8 Kbytes

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection and unprotection can be implemented via two methods.

The primary method requires V_{ID} on the $\overline{RESET}$ pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 23 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The sector unprotect algorithm unprotects all sectors in parallel. All previously protected sectors must be individually re-protected. To change data in protected sectors efficiently, the temporary sector unprotect function is available. See "Temporary Sector/Sector Block Unprotect".

The alternate method for protection and unprotection is by software temporary sector /sector block unprotect command. See Figure 2 for Command Flow.

The device is shipped with all sectors unprotected.

It is possible to determine whether a sector is protected or unprotected. See the Autoselect Mode section for details.

Write Protect ($\overline{WP}$/ACC)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the $\overline{WP}$ /ACC pin.

If the system asserts V_{IL} on the $\overline{WP}$ /ACC pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

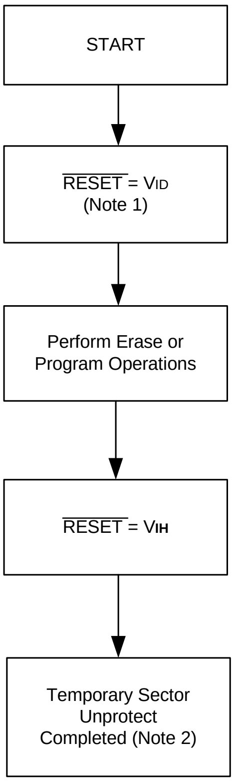
If the system asserts V_{IH} on the $\overline{WP}$ /ACC pin, the device reverts to whether the two outermost 8 Kbyte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection".

Note that the $\overline{WP}$ /ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Temporary Sector/Sector Block Unprotect

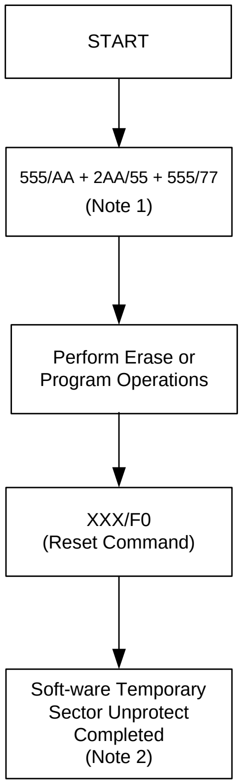
(Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Tables 6 and 7).

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to V_{ID} (8.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the $\overline{RESET}$ pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 22 shows the timing diagrams, for this feature.



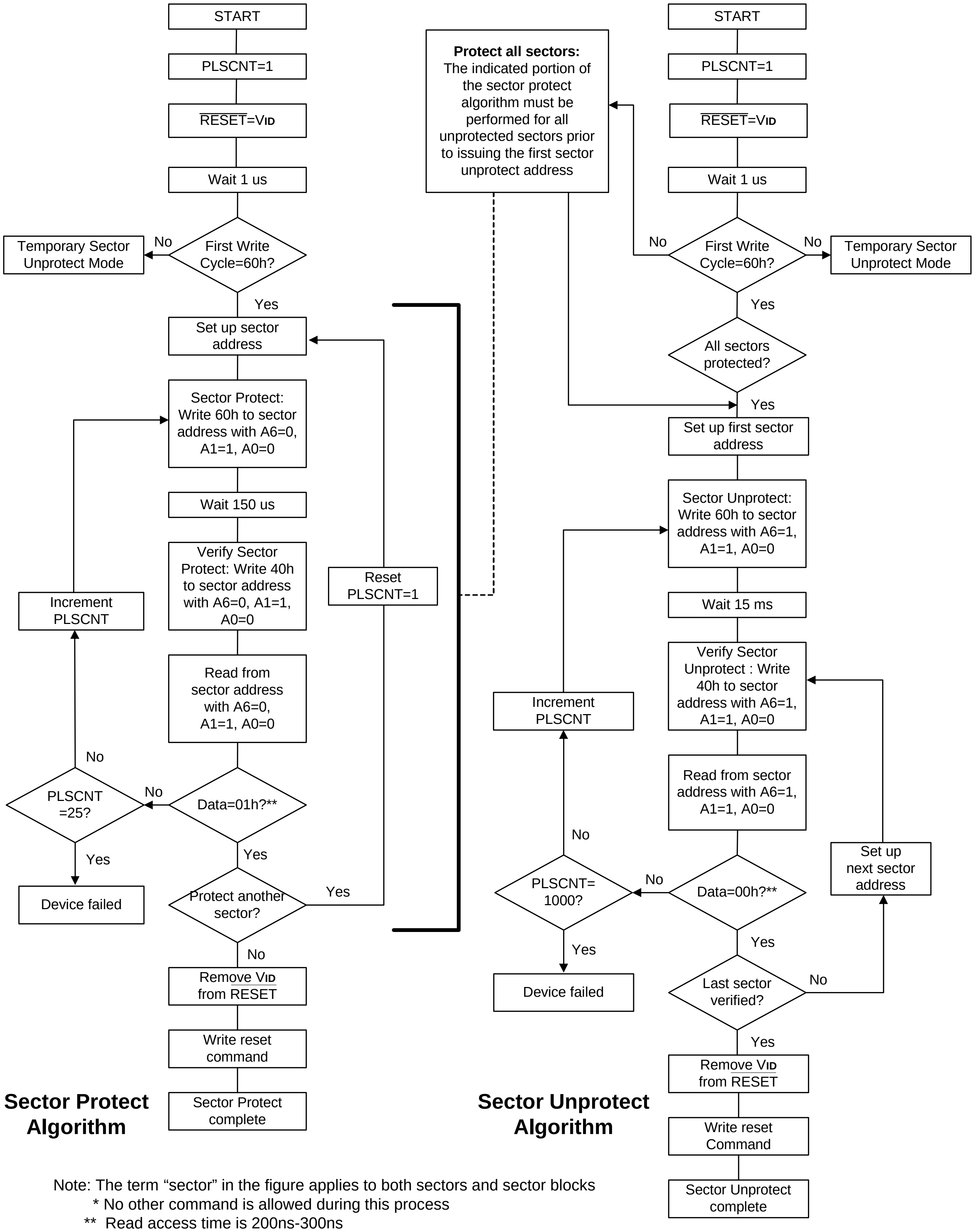
Notes:
1. All protected sectors unprotected (If $\overline{WP}$/ACC=V_{IL}, outermost boot sectors will remain protected).
2. All previously protected sectors are protected once again.

Figure 1-1. Temporary Sector Unprotect Operation by $\overline{RESET}$ Mode



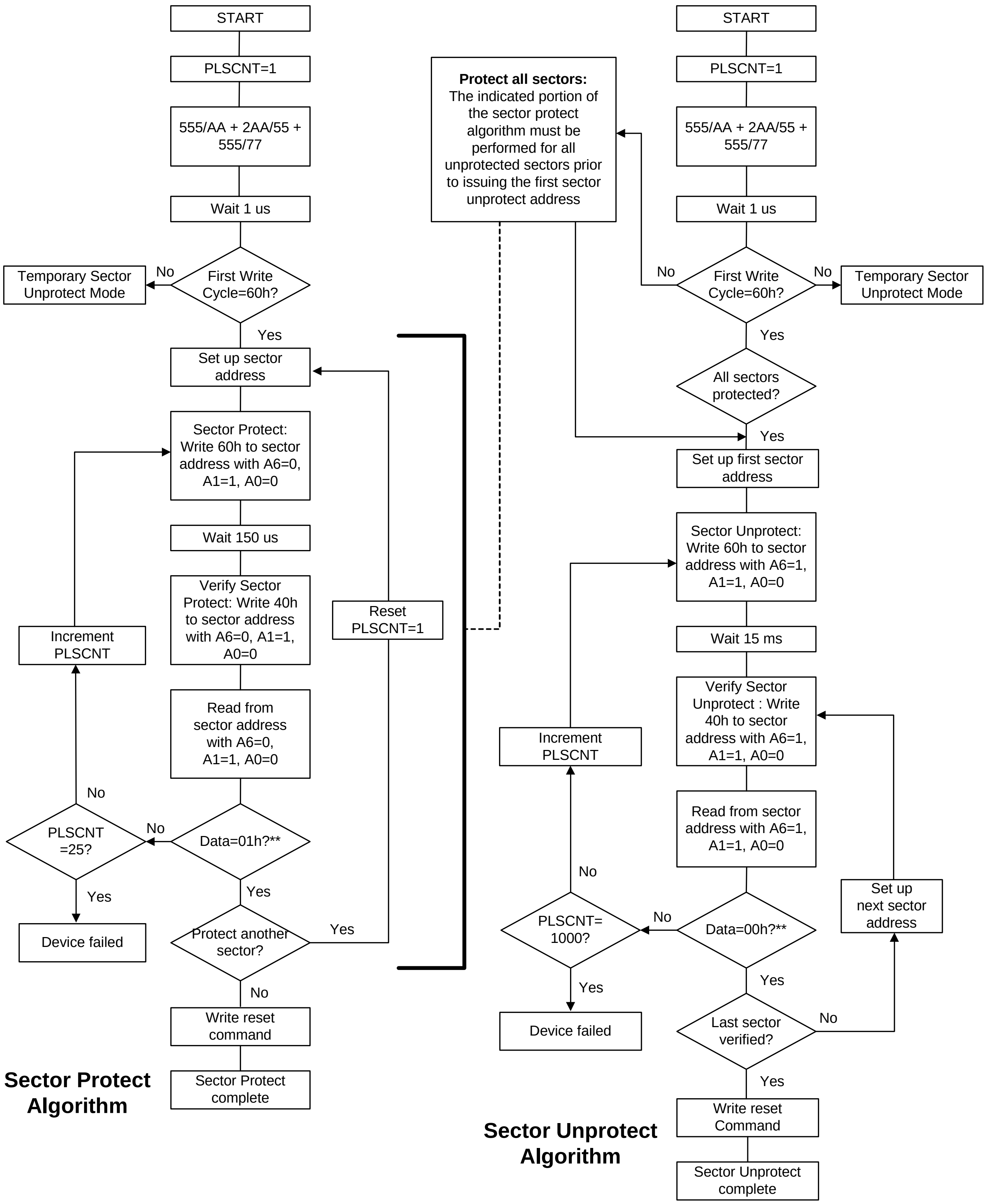
Notes:
1. All protected sectors unprotected (If $\overline{WP}$/ACC=V_{IL}, outermost boot sectors will remain protected).
2. All previously protected sectors are protected once again.

Figure 1-2. Temporary Sector Unprotect Operation by Software Mode



Note: The term “sector” in the figure applies to both sectors and sector blocks
* No other command is allowed during this process
** Read access time is 200ns-300ns

Figure 2-1. High Voltage Sector/Sector Block Protection and Unprotection Algorithms



Note: The term “sector” in the figure applies to both sectors and sector blocks
* No other command is allowed during this process
** Access time is 200ns-300ns

Figure 2-2. Software Sector/Sector Block Protection and Unprotection Algorithms

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 12 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during VCC_F power-up and power-down transitions, or from system noise.

Low VCC Write Inhibit

When VCC_F is less than V_{LKO}, the device does not accept any write cycles. This protects data during VCC_F power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until VCC_F is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when VCC_F is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE\_F}$ or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE\_F}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE\_F}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

If $\overline{WE}$ = $\overline{CE\_F}$ = V_{IL} and $\overline{OE}$ = V_{IH} during power up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to reading array data on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8-11. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8-11. The system must write the reset command to return the device to the autoselect mode.

Table 8. CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	VCC Min. (write/erase) I/O_7- I/O_4 : volt, I/O_3- I/O_0: 100 millivolt
1Ch	38h	0036h	VCC Max. (write/erase) I/O_7- I/O_4: volt, I/O_3- I/O_0: 100 millivolt
1Dh	3Ah	0000h	Vpp Min. voltage (00h = no Vpp pin present)
1Eh	3Ch	0000h	Vpp Max. voltage (00h = no Vpp pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N μs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N μs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 10 Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0015h	Device Size = 2^N byte
28h	50h	0002h	Flash Device Interface description
29h	52h	0000h	
2Ah	54h	0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Bh	56h	0000h	
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh	5Ah	0007h	Erase Block Region 1 Information (refer to the CFI specification)
2Eh	5Ch	0000h	
2Fh	5Eh	0020h	
30h	60h	0000h	
31h	62h	001Eh	Erase Block Region 2 Information
32h	64h	0000h	
33h	66h	0000h	
34h	68h	0001h	
35h	6Ah	0000h	Erase Block Region 3 Information
36h	6Ch	0000h	
37h	6Eh	0000h	
38h	40h	0000h	
39h	72h	0000h	Erase Block Region 4 Information
3Ah	74h	0000h	
3BH	76h	0000h	
3Ch	78h	0000h	

Table 11. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0032h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 04 = A29L800 mode
4Ah	94h	00XXh (See Note)	Simultaneous Operation 00 = Not Supported, X = Number of Sectors (excluding Bank 1)
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	000Xh	Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device

Note:
The number of sectors in Bank 2 is device dependent.
A82DL1624 = 1Ch
A82DL1634 = 18h
A82DL1644 = 10h

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 12 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE\_F}$, whichever happens later. All data is latched on the rising edge of $\overline{WE}$ or $\overline{CE\_F}$, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if I/O_5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 11 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to reading array data. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If I/O_5 goes high during a program or erase operation, writing the reset command returns the banks to reading array data (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 12 shows the address and data requirements. This method is an alternative to that shown in Table 5, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address wit h in a bank that is either in t he read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. T he bank then enter s the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence:

- A read cycle at address (BA)XX00h (where BA is the bank address) returns the manufacturer code.
- A read cycle at address (BA)XX01h in word mode (or (BA)XX02h in byte mode) returns the device code.
- A read cycle to an address containing a sector address (SA) within the same bank, and the address 02h on A7-A0 in word mode (or the address 04h on A6-A-1 in byte mode) returns 01h if the sector is protected, or 00h if it is unprotected. (Refer to Tables 3-4 for valid sector addresses).

The system must write the reset command to return to reading array data (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Byte/Word Program Command Sequence

The system may program the device by word or byte, depending on the state of the $\overline{BYTE\_F}$ pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 12 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using I/O_7, I/O_6, or RY/$\overline{BY}$. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from "0" back to a "1." Attempting to do so may cause that bank to set I/O_5 = 1, or cause the I/O_7 and I/O_6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

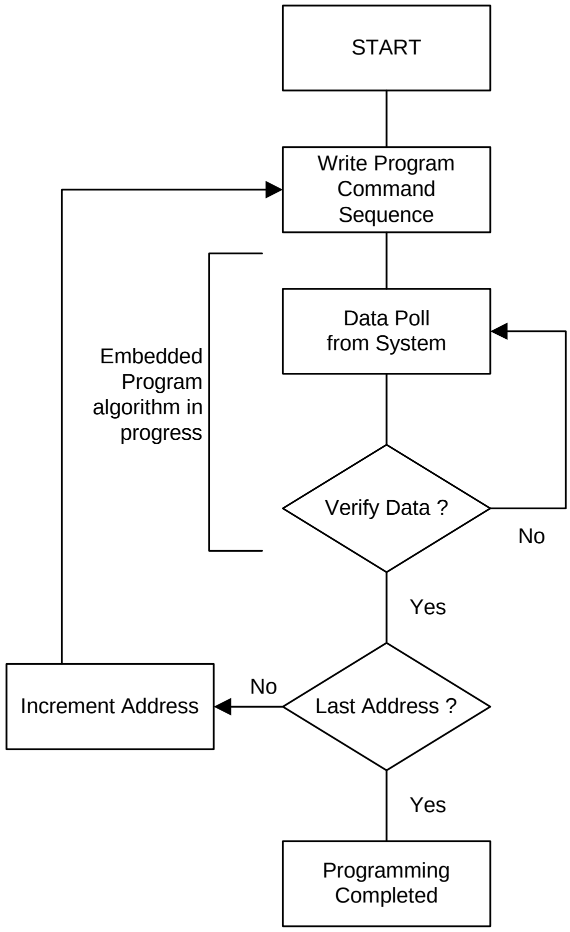
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 12 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The device then returns to reading array data.

The device offers accelerated program operations through the $\overline{WP}$ /ACC pin. When the system asserts V_{HH} on the $\overline{WP}$ /ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the $\overline{WP}$ /ACC pin to accelerate the operation. Note that the $\overline{WP}$ /ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the $\overline{WP}$ /ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 15 for timing diagrams.



Note : See Table 14 for program command sequnce.

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 12 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using I/O_7, I/O_6, I/O_2, or RY/$\overline{BY}$. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 17 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 12 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands within the bank may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to reading array data. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor I/O_3 to determine if the sector erase timer has timed out (See the section on I/O_3: Sector Erase Timer.). The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading I/O_7, I/O_6, I/O_2, or RY/$\overline{BY}$ in the erasing bank.

Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 17 section for timing diagrams

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

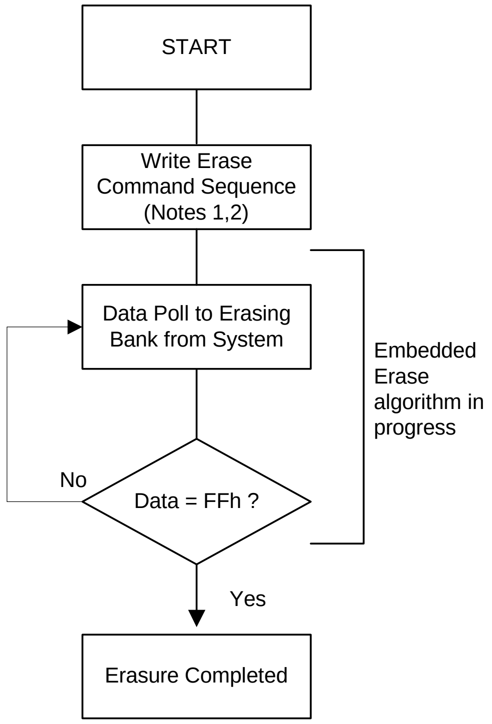
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on I/O_7–I/O_0. The system can use I/O_7, or I/O_6 and I/O_2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the I/O_7 or I/O_6 status bits, just as in the standard Byte Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is ignored when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Note :
1. See Table 14 for erase command sequence.
2. See the section on I/O3 for information on the sector erase timer.

Figure 4. Erase Operation

Command Definitions

Table 12. A82DL16x4T(U) Command Definitions

Command Sequence (Note 1)		Cycle	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8): Manufacturer ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X00	37				
	Byte		AAA		555		(BA)AAA							
Autoselect (Note 8): Device ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X01	(see Table5)				
	Byte		AAA		555		(BA)AAA		(BA)X02					
Autoselect (Note 8): Continuation ID	Word	4	555	AA	2AA	55	555	90	X03	7F				
	Byte		AAA		555		AAA		X06					
Autoselect (Note 8): Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	(BA)555	90	(SA)	00/01				
	Byte		AAA		555		(BA)AAA		(SA)X04					
Command Temporary Sector Unprotect(Note 15)	Word	3	555	AA	2AA	55	555	77						
	Byte		AAA		555		AAA							
Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte		AAA		555		AAA							
Unlock Bypass	Word	3	555	AA	2AA	55	555	20						
	Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)		2	XXX	90	XXX	00								
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AA A		555		AAA	
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)		1	XXX	B0										
Erase Resume (Note 13)		1	XXX	30										
CFI Query (Note 14)	Word	1	55	98										
	Byte		AA											

Legend:
X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the $\overline{WE}$ or $\overline{CE\_F}$ pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of $\overline{WE}$ or $\overline{CE\_F}$ pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19 - A12 select a unique sector.
BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased.
Note:
1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.
3. Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.
4. Data bits I/O$_{15}$-I/O$_8$ are don't care in command sequences. Except for RD and PD.
5. Unless otherwise noted, address bits A19-A11 are don't cares.
6. No unlock or command cycles required when bank is reading array data.
7. The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if I/O$_5$ goes high (while the bank is providing status information).
8. The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacture ID, or device ID information. Data bits I/O$_{15}$-I/O$_8$ are don't care. See the Autoselect Command Sequence section for more information.
9. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
10. The Unlock Bypass command is required prior to the Unlock Bypass Program Command.
11. The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.
12. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and require the bank address.
13. The Erase Resume command is valid only during the Erase.
14. Command is valid when device is ready to read array data or when device is in autoselect mode.
15. Once reset command is applied, software temporary unprotect is exit to return read array data. But under erase suspend condition, this command is still effective even a reset command has been applied. The reset command which can deactivate the software temporary unprotect command is useful only after the erase command is complete.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: I/O$_2$, I/O$_3$, I/O$_5$, I/O$_6$, and I/O$_7$. Table 13 and the following subsections describe the function of these bits. I/O$_7$ and I/O$_6$ each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/$\overline{\text{BY}}$, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

I/O$_7$: $\overline{\text{Data}}$ Polling

The $\overline{\text{Data}}$ Polling bit, I/O$_7$, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. $\overline{\text{Data}}$ Polling is valid after the rising edge of the final $\overline{\text{WE}}$ pulse in the program or erase command sequence.

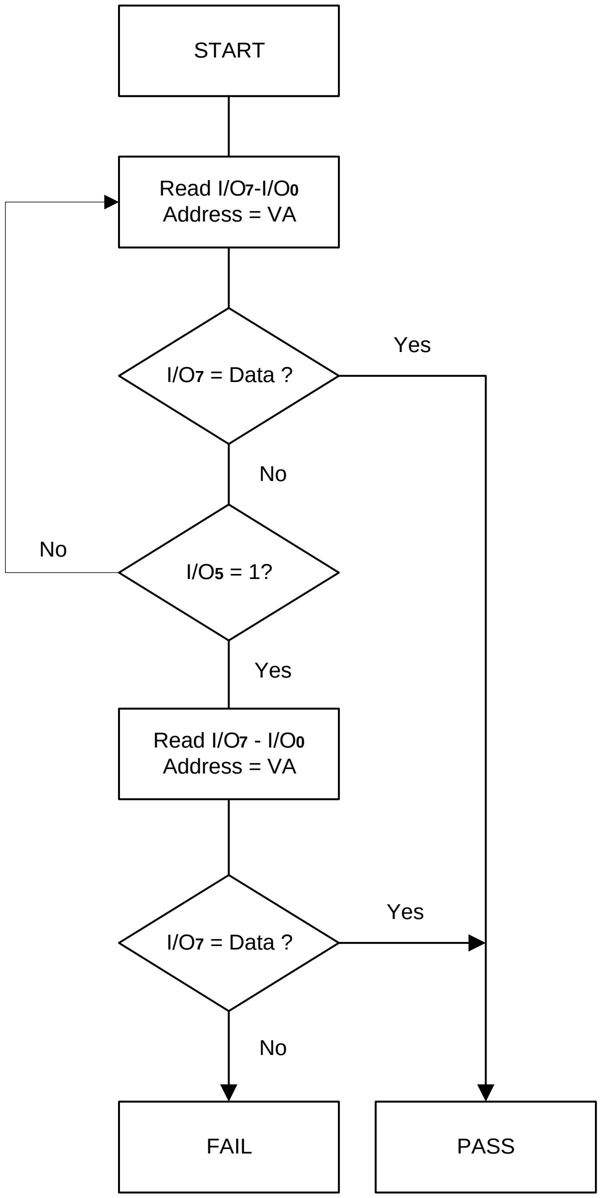
During the Embedded Program algorithm, the device outputs on I/O$_7$ the complement of the datum programmed to I/O$_7$. This I/O$_7$ status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to I/O$_7$. The system must provide the program address to read valid status information on I/O$_7$. If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on I/O$_7$ is active for approximately 1μs, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{\text{Data}}$ Polling produces a "0" on I/O$_7$. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{\text{Data}}$ Polling produces a "1" on I/O$_7$. The system must provide an address within any of the sectors selected for erasure to read valid status information on I/O$_7$.

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on I/O$_7$ is active for approximately 100μs, then the bank returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads I/O$_7$ at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, I/O$_7$ may change asynchronously with I/O$_0$–I/O$_6$ while Output Enable ($\overline{\text{OE}}$) is asserted low. That is, the device may change from providing status information to valid data on I/O$_7$. Depending on when the system samples the I/O$_7$ output, it may read the status or valid data. Even if the device has completed the program or erase operation and I/O7 has valid data, the data outputs on I/O$_0$-I/O$_6$ may be still invalid. Valid data on I/O$_0$-I/O$_7$ will appear on successive read cycles.

Table 13 shows the outputs for $\overline{\text{Data}}$ Polling on I/O$_7$. Figure 5 shows the $\overline{\text{Data}}$ Polling algorithm. Figure 19 in the AC Characteristics section shows the $\overline{\text{Data}}$ Polling timing diagram.



Note :

1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. I/O$_7$ should be rechecked even if I/O$_5$ = "1" because I/O$_7$ may change simultaneously with I/O$_5$.

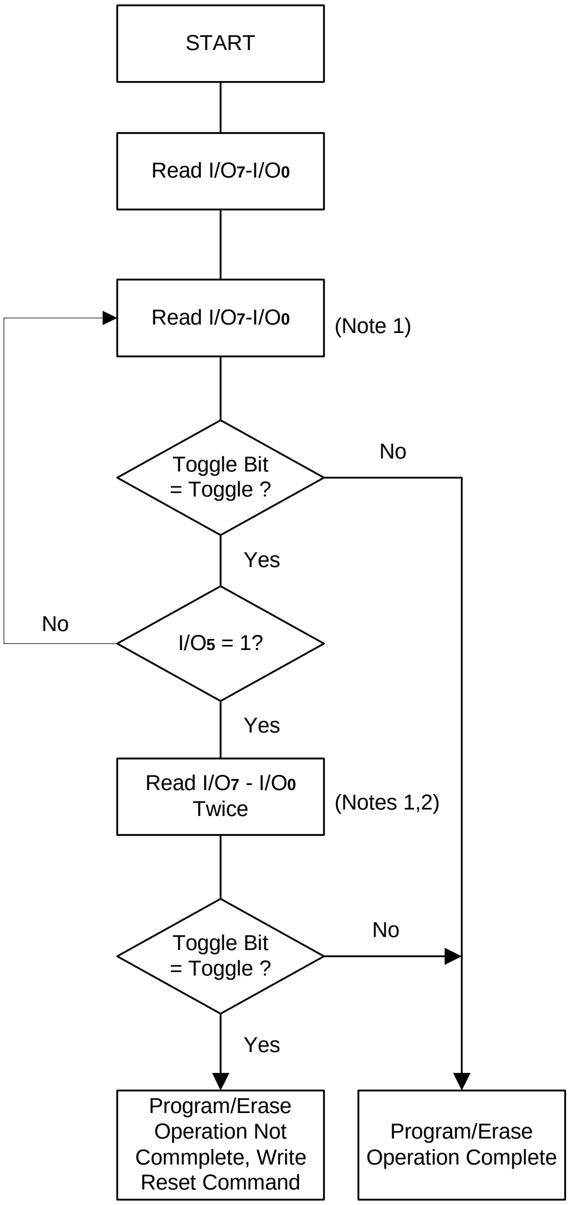
Figure 5. $\overline{\text{Data}}$ Polling Algorithm

RY/$\overline{BY}$: Ready/$\overline{Busy}$

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Embedded algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to VCC_F.
If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.
Table 13 shows the outputs for RY/$\overline{BY}$.

I/O$_6$: Toggle Bit I

Toggle Bit I on I/O$_6$ indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.
During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause I/O$_6$ to toggle. The system may use either $\overline{OE}$ or $\overline{CE\_F}$ to control the read cycles. When the operation is complete, I/O$_6$ stops toggling.
After an erase command sequence is written, if all sectors selected for erasing are protected, I/O$_6$ toggles for approximately 100μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.
The system can use I/O$_6$ and I/O$_2$ together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), I/O$_6$ toggles. When the device enters the Erase Suspend mode, I/O$_6$ stops toggling. However, the system must also use I/O$_2$ to determine which sectors are erasing or erase-suspended. Alternatively, the system can use I/O$_7$ (see the subsection on " I/O$_7$: $\overline{Data}$ Polling").
If a program address falls within a protected sector, I/O$_6$ toggles for approximately 1μs after the program command sequence is written, then returns to reading array data.
I/O$_6$ also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.
Table 13 shows the outputs for Toggle Bit I on I/O$_6$. Figure 6 shows the toggle bit algorithm. Figure 20 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 23 shows the differences between I/O$_2$ and I/O$_6$ in graphical form. See also the subsection on I/O$_2$: Toggle Bit II.



Note:
The system should recheck the toggle bit even if I/O$_5$="1" because the toggle bit may stop toggling as I/O$_5$ changes to "1". See the subsections on I/O$_6$ and I/O$_2$ for more information.

Figure 6. Toggle Bit Algorithm

I/O2: Toggle Bit II

The "Toggle Bit II" on I/O_2, when used with I/O_6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.
I/O_2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE\_F}$ to control the read cycles.) But I/O_2 cannot distinguish whether the sector is actively erasing or is erase-suspended. I/O_6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 8 to compare outputs for I/O_2 and I/O_6.
Figure 6 shows the toggle bit algorithm in flowchart form, and the section " I/O_2: Toggle Bit II" explains the algorithm. See also the " I/O_6: Toggle Bit I" subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between I/O_2 and I/O_6 in graphical form.

Reading Toggle Bits I/O6, I/O2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read I/O_7-I/O_0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on I/O_7-I/O_0 on the following read cycle.
However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of I/O_5 is high (see the section on I/O_5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as I/O_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.
The remaining scenario is that the system initially determines that the toggle bit is toggling and I/O_5 has not gone high. The system may continue to monitor the toggle bit and I/O_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

I/O5: Exceeded Timing Limits

I/O_5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions I/O_5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.
The device may output a “1” on I/O_5 if the system tries to program a “1” to a location that was previously programmed to “0.” Only an erase operation can change a “0” back to a “1.” Under this condition, the device halts the operation, and when the timing limit has been exceeded, I/O_5 produces a “1.” .
Under both these conditions, the system must write the reset command to return to reading array data (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

I/O3: Sector Erase Timer

After writing a sector erase command sequence, the system may read I/O_3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, I/O_3 switches from "0" to "1." The system may ignore I/O_3 if the system can guarantee that the time between additional sector erase commands will always be less than 50μs. See also the "Sector Erase Command Sequence" section.
After the sector erase command sequence is written, the system should read the status on I/O_7 ($\overline{Data}$ Polling) or I/O_6 (Toggle Bit 1) to ensure the device has accepted the command sequence, and then read I/O_3. If I/O_3 is "1", the internally controlled erase cycle has begun; all further commands (Except Erase Suspend) are ignored until the erase operation is complete. If I/O_3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of I/O_3 prior to and following each subsequent sector erase command. If I/O_3 is high on the second status check, the last command might not have been accepted.
Table 13 shows the status of I/O_3 relative to the other status bits.

Table 13. Write Operation Status

Status			I/O_7 (Note 2)	I/O_6	I/O_5 (Note 1)	I/O_3	I/O_2 (Note 2)	RY/$\overline{BY}$
Standard Mode	Embedded Program Algorithm		$\overline{I/O_7}$	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspend Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		$\overline{I/O_7}$	Toggle	0	N/A	N/A	0

Notes:

1. I/O_5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on I/O_5 for more information.
2. I/O_7 and I/O_2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature Plastic Packages. . . -55°C to +125°C
Ambient Temperature, ……………………...-65°C to + 125°C
Voltage with Respect to Ground (Note 1)
VCC_F/VCC_S ………. . . . . ….... . -0.5V to +4.0V
A9, $\overline{\text{OE}}$ & $\overline{\text{RESET}}$ (Note 2) . . . . -0.5V to +12.5V
$\overline{\text{WP}}$ /ACC . . . . -0.5V to +10.5V
All other pins (Note 1) . . . . . . -0.5V to VCC_F/VCC_S + 0.5V
Output Short Circuit Current (Note 3) 200mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is VCC_F/VCC_F +0.5V. See Figure 7. During voltage transitions, input or I/O pins may overshoot to VCC_F/VCC_S +2.0V for periods up to 20ns. See Figure 8.
2. Minimum DC input voltage on A9, $\overline{\text{OE}}$, $\overline{\text{RESET}}$ and $\overline{\text{WP}}$ /ACC is -0.5V. During voltage transitions, A9, $\overline{\text{OE}}$, $\overline{\text{WP}}$ /ACC and $\overline{\text{RESET}}$ may overshoot VSS to -2.0V for periods of up to 20ns. See Figure 7. Maximum DC input voltage on A9 is +12.5V which may overshoot to 14.0V for periods up to 20ns. Maximum DC input voltage on $\overline{\text{WP}}$ /ACC is +9.5V which may overshoot to +12.0V for period up to 20ns.
3. No more than one output is shorted to ground at a time. Duration of the short circuit should not be greater than one second.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Industrial (U) Devices

Ambient Temperature (T_A) . . . . -40°C to +85°C

VCC Supply Voltages

VCC_F/VCC_S for all devices . .. .+2.7V to +3.6V

Operating ranges define those limits between which the functionally of the device is guaranteed.

Figure 7. Maximum Negative Overshoot Waveform

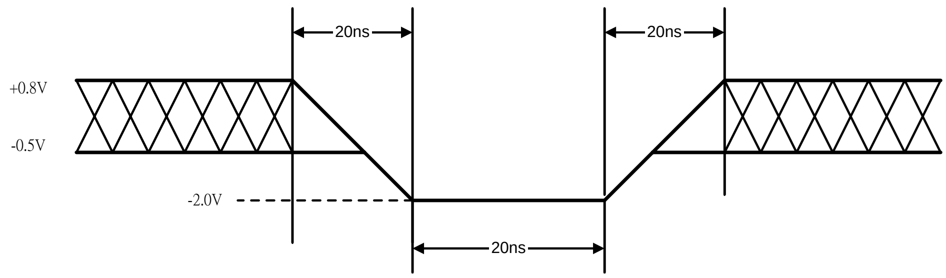
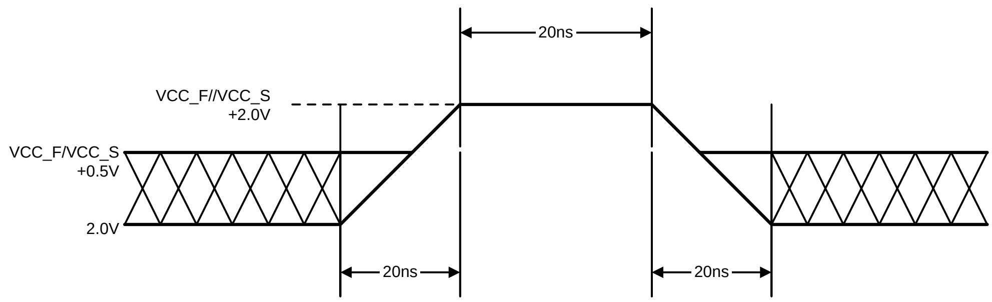


Figure 8. Maximum Positive Overshoot Waveform



DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description	Test Description		Min.	Typ.	Max.	Unit
I_{LI}	Input Load Current	V_{IN} = VSS to VCC_F. VCC_F= VCC_F Max				±1.0	µA
I_{LIT}	A9 Input Load Current	VCC = VCC Max, A9 =12.5V				35	µA
I_{LO}	Output Leakage Current	VOUT = VSS to VCC_F. VCC = VCC_F Max				±1.0	µA
I_{CC1_F}	VCC_F Active Read Current (Notes 1, 2)	$\overline{CE\_F}$ = V_{IL}, $\overline{OE}$ = V_{IH} Byte Mode	5 MHz		10	16	mA
			1 MHz		2	4	
		$\overline{CE\_F}$ = V_{IL}, $\overline{OE}$ = V_{IH} Word Mode	5 MHz		10	16	
			1 MHz		2	4	
I_{CC2_F}	VCC_F Active Write Current (Notes 2, 3)	$\overline{CE\_F}$ = V_{IL}, $\overline{OE}$ = V_{IH}			20	30	mA
I_{CC3_F}	VCC_F Standby Current (Note 2)	$\overline{CE\_F}$ = V_{IH}, $\overline{RESET}$ = VCC_F ± 0.3V			0.2	5	µA
I_{CC4_F}	VCC_F Reset Current (Note 2)	$\overline{RESET}$ = VSS ± 0.3V			0.2	5	µA
I_{CC5_F}	Automatic Sleep Mode (Note 2, 4)	V_{IH} = VCC_F ± 0.3V; V_{IL} = VSS ± 0.3V			0.2	5	µA
I_{CC6_F}	VCC_F Active Read-While-Program Current (Notes 1, 2)	$\overline{CE\_F}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte		21	45	mA
			Word		21	45	
I_{CC7_F}	VCC_F Active Read-While-Erase Current (Notes 1, 2)	$\overline{CE\_F}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte		21	45	mA
			Word		21	45	
I_{CC8_F}	VCC_F Active Program-While-Erase-Suspended Current (Notes 2, 5)	$\overline{CE\_F}$ = V_{IL}, $\overline{OE}$ = V_{IH}			17	35	mA
I_{ACC}	ACC Accelerated Program Current, Word or Byte	$\overline{CE\_F}$ = V_{IL}, $\overline{OE}$ = V_{IH}	ACC pin		5	10	mA
			VCC_F pin		15	30	
V_{IL}	Input Low Level			-0.5		0.8	V
V_{IH}	Input High Level			0.7 x VCC_F		VCC_F + 0.3	V
V_{HH}	Voltage for $\overline{WP}$ /ACC Sector Protect/Unprotect and Program Acceleration	VCC_F = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Unprotect Sector	VCC_F = 3.0 V ± 10%		8.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0mA, VCC_F = VCC_F Min				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, VCC_F = VCC_F Min		0.85x VCC_F			V
V_{OH2}		I_{OH} = -100 µA, VCC_F = VCC Min		VCC_F - 0.4			V
V_{LKO}	Low VCC_F Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:
1. The I_{CC} current listed is typically less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Maximum I_{CC} specifications are tested with VCC_F = VCC_F max.
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC_F} + 30ns. Typical sleep mode current is 200nA.
5. Not 100% tested.

TEST CONDITIONS

Table 14. Test Specifications

Test Condition	-70	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L(including jig capacitance)	35	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0 - 3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

Figure 9. Test Setup

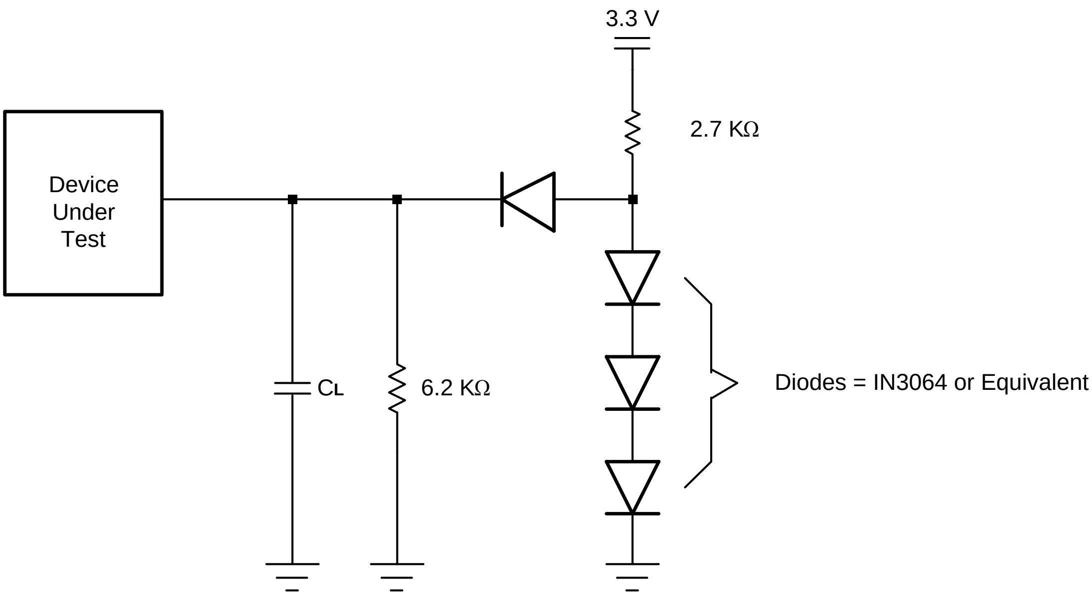
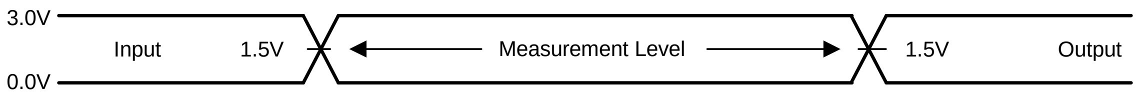


Figure 10. Input Waveforms and Measurement Levels



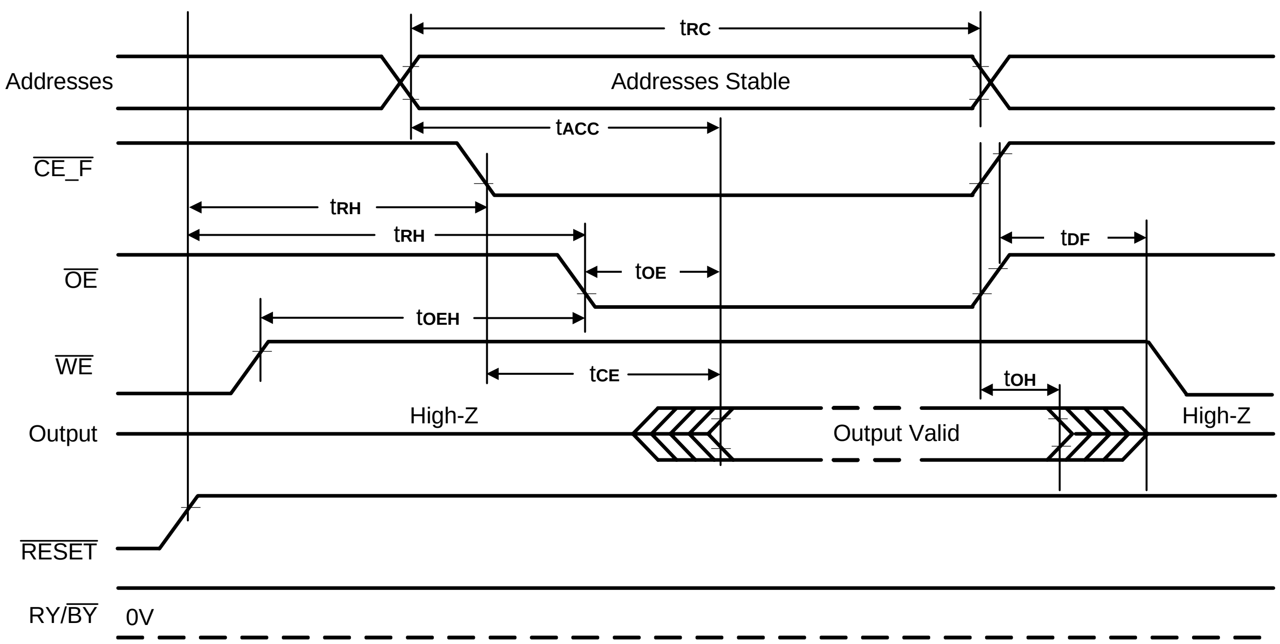
AC CHARACTERISTICS

Read Only Operations

Parameter JEDEC	Parameter Std	Description	Test Setup		Speed -70	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)		Min.	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE\_F} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max.	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1,3)		Max.	16	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1,3)		Max.	16	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min.	0	ns
	t_{OEH}	Output Enable Hold Time (Note 1) — Read		Min.	0	ns
	t_{OEH}	Output Enable Hold Time (Note 1) — Toggle and $\overline{Data}$ Polling		Min.	10	ns

Notes:
1. Not 100% tested.
2. See Figure 9 and Table 14 for test specifications.
3. Measurements performed by placing a 50-ohm termination on the data pin with a bias of (VCC_F)/2. The time from $\overline{OE}$ high to the data bus driven to (VCC_F)/2 is taken as t_{DF}.

Figure 11. Read Operation Timings



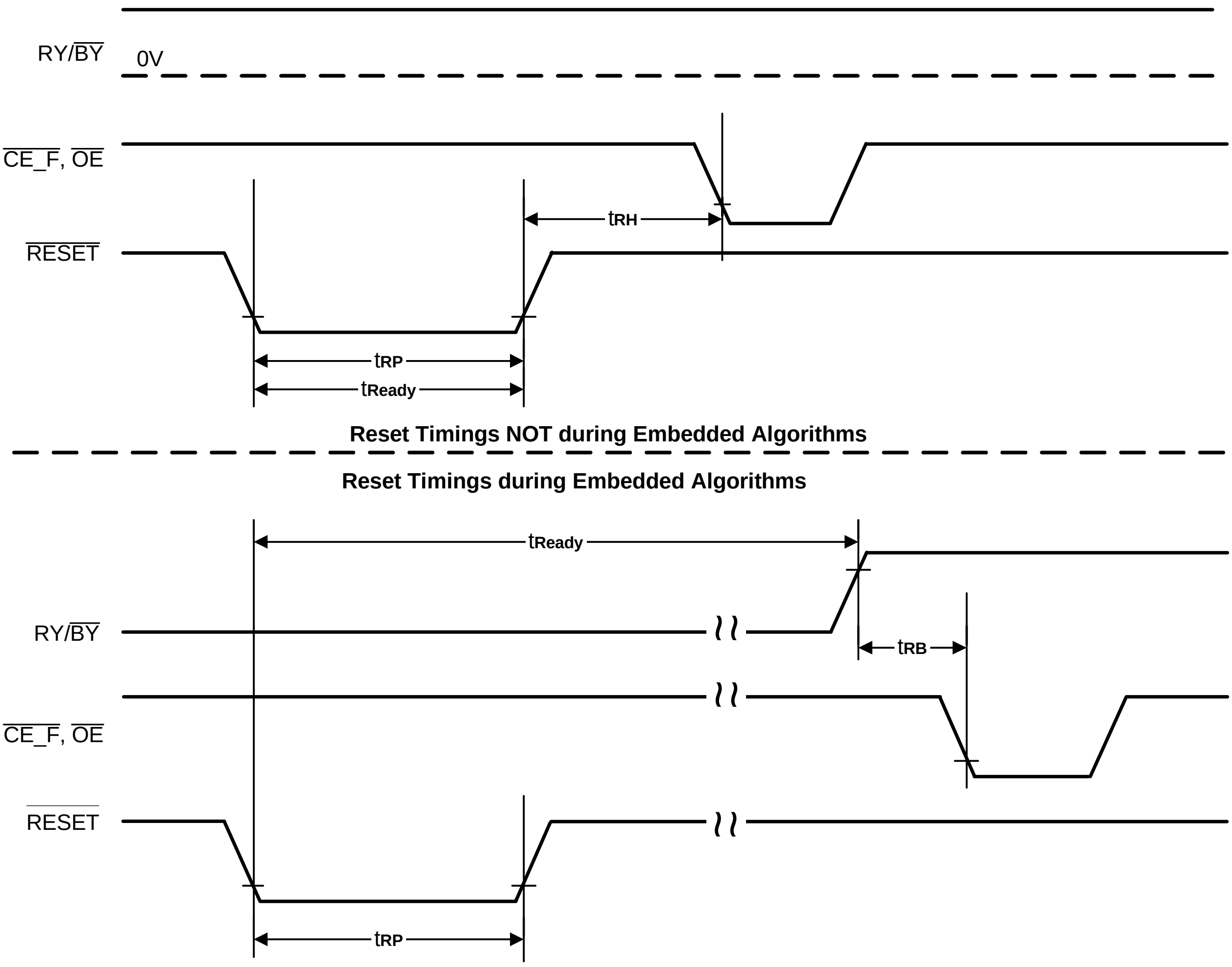
AC CHARACTERISTICS

Hardware Reset ($\overline{\text{RESET}}$)

Parameter JEDEC	Parameter Std	Description	Test Setup		All Speed Options	Unit
	t_{READY}	$\overline{\text{RESET}}$ Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	$\overline{\text{RESET}}$ Pin Low (Not During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	$\overline{\text{RESET}}$ Pulse Width		Min	500	ns
	t_{RH}	$\overline{\text{RESET}}$ High Time Before Read (See Note)		Min	50	ns
	t_{RB}	RY/$\overline{\text{BY}}$ Recovery Time		Min	0	ns
	t_{RPD}	$\overline{\text{RESET}}$ Low to Standby Mode		Min	20	µs

Note: Not 100% tested.

Figure 12. $\overline{\text{RESET}}$ Timings



AC CHARACTERISTICS

Word/Byte Configuration (BYTE_F)

Parameter		Description		Speed Option	Unit
JEDEC	Std			-70	
	tELFL/tELFH	CE_F to BYTE_F Switching Low or High	Max	5	ns
	tFLQZ	BYTE_F Switching Low to Output High-Z	Max	25	ns
	tHQV	BYTE_F Switching High to Output Active	Min	70	ns

Figure 13. BYTE_F Timings for Read Operations

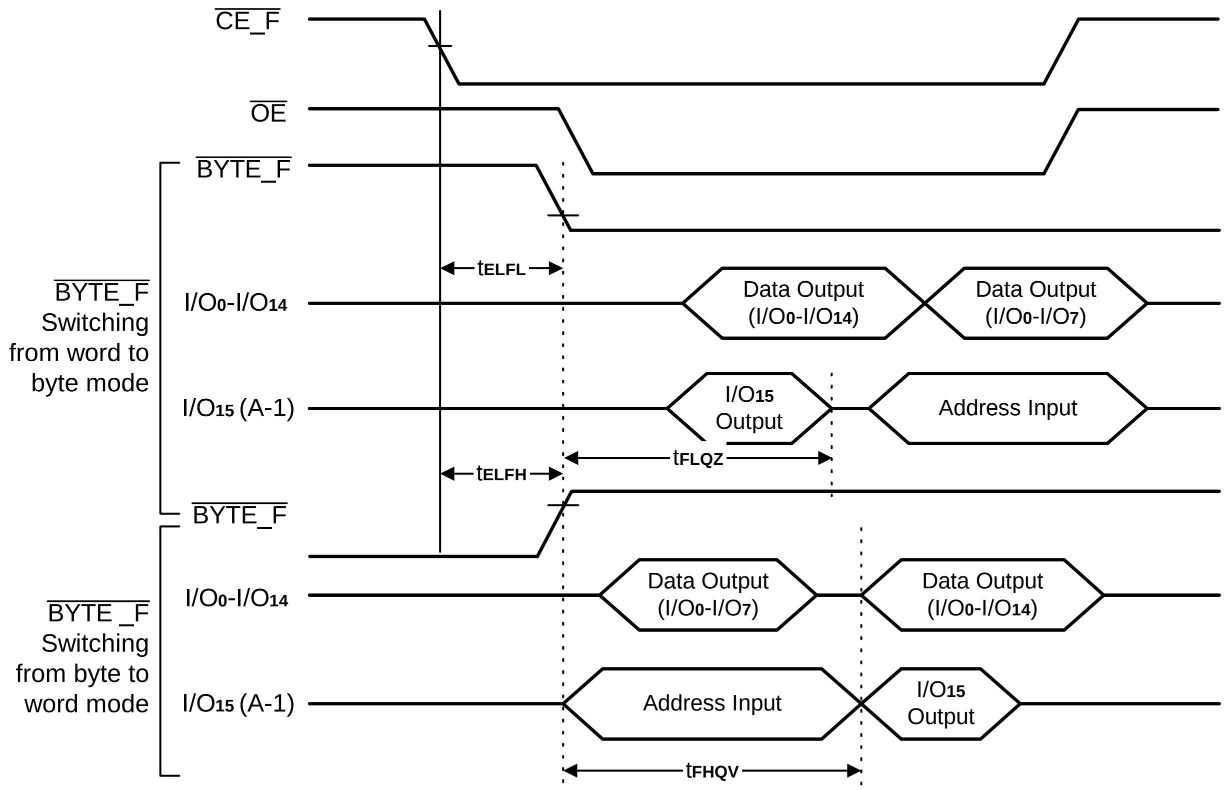
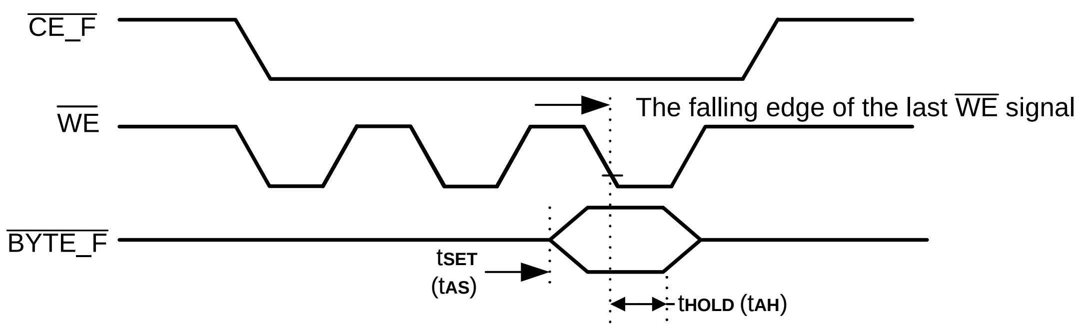


Figure 14. BYTE_F Timings for Write Operations



Note:
Refer to the Erase/Program Operations table for tAS and tAH specifications.

AC CHARACTERISTICS

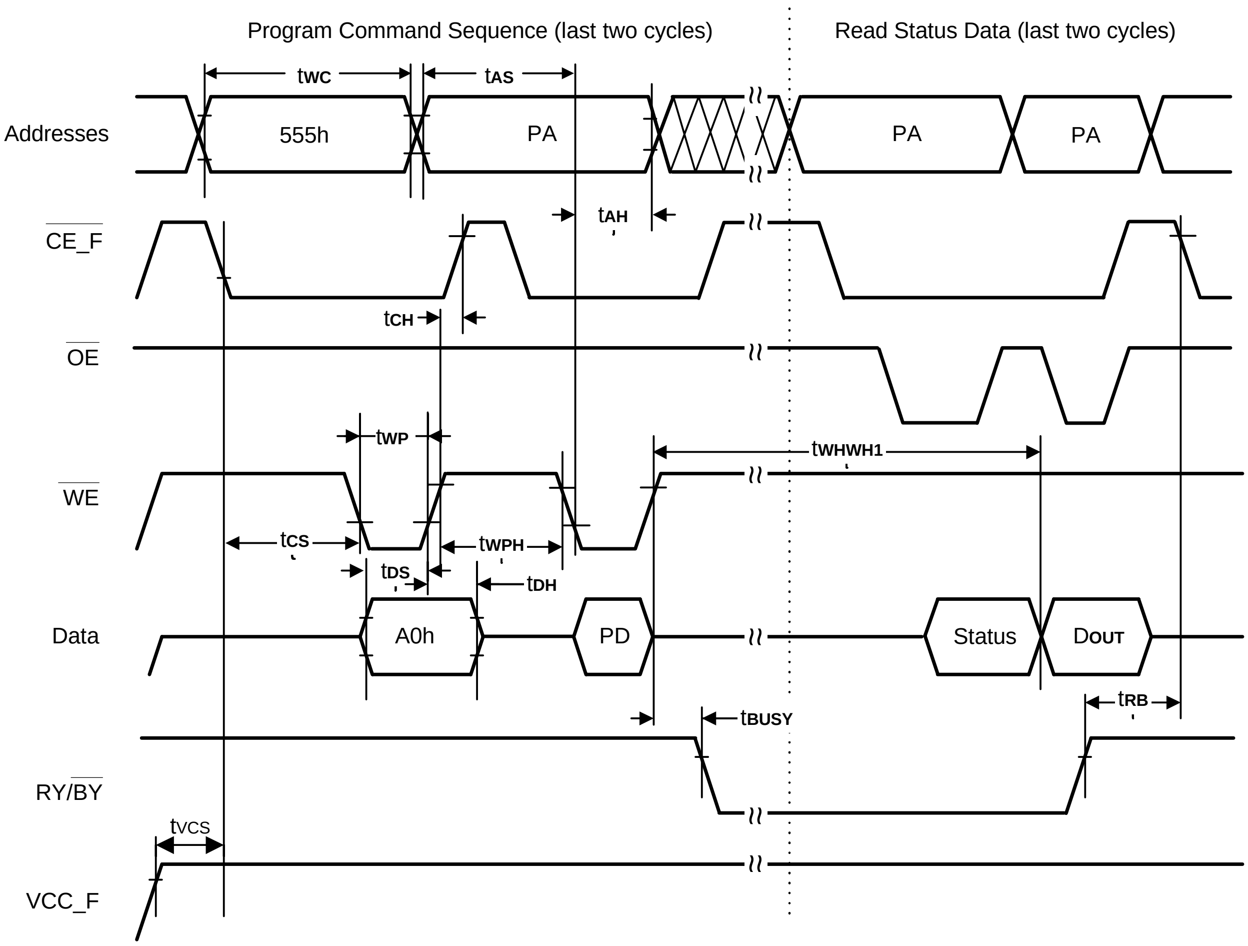
Erase and Program Operations

Parameter JEDEC	Parameter Std	Description		Speed -70	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min.	70	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min.	0	ns
	t_{ASO}	Address Setup Time to $\overline{OE}$ low during toggle bit polling		15	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min.	45	ns
	t_{AHT}	Address Hold Time From $\overline{CE\_F}$ or $\overline{OE}$ high during toggle bit polling		0	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min.	35	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min.	0	ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min.	20	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ high to $\overline{WE}$ low)	Min.	0	ns
t_{ELWL}	t_{CS}	$\overline{CE\_F}$ Setup Time	Min.	0	ns
t_{WHEH}	t_{CH}	$\overline{CE\_F}$ Hold Time	Min.	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min.	30	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min.	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min.	0	
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 2) — Byte	Typ.	5	µs
		Byte Programming Operation (Note 2) — Word	Typ.	7	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)	Typ.	4	sec
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ.	0.7	sec
	t_{VCS}	VCC_F Set Up Time (Note 1)	Min.	50	µs
	t_{RB}	Recovery Time from RY/$\overline{BY}$	Min	0	ns
	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	Min	90	ns

Notes:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

AC CHARACTERISTICS

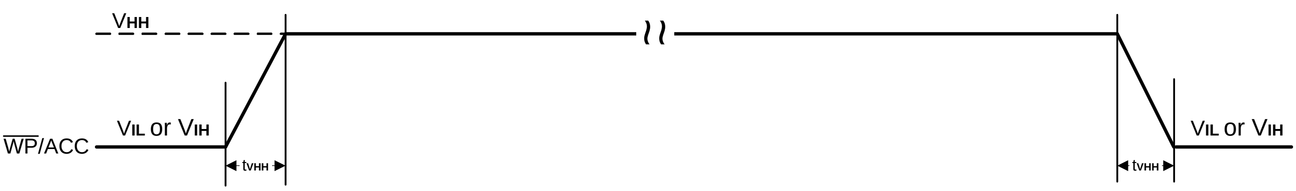
Figure 15. Program Operation Timings



Note :

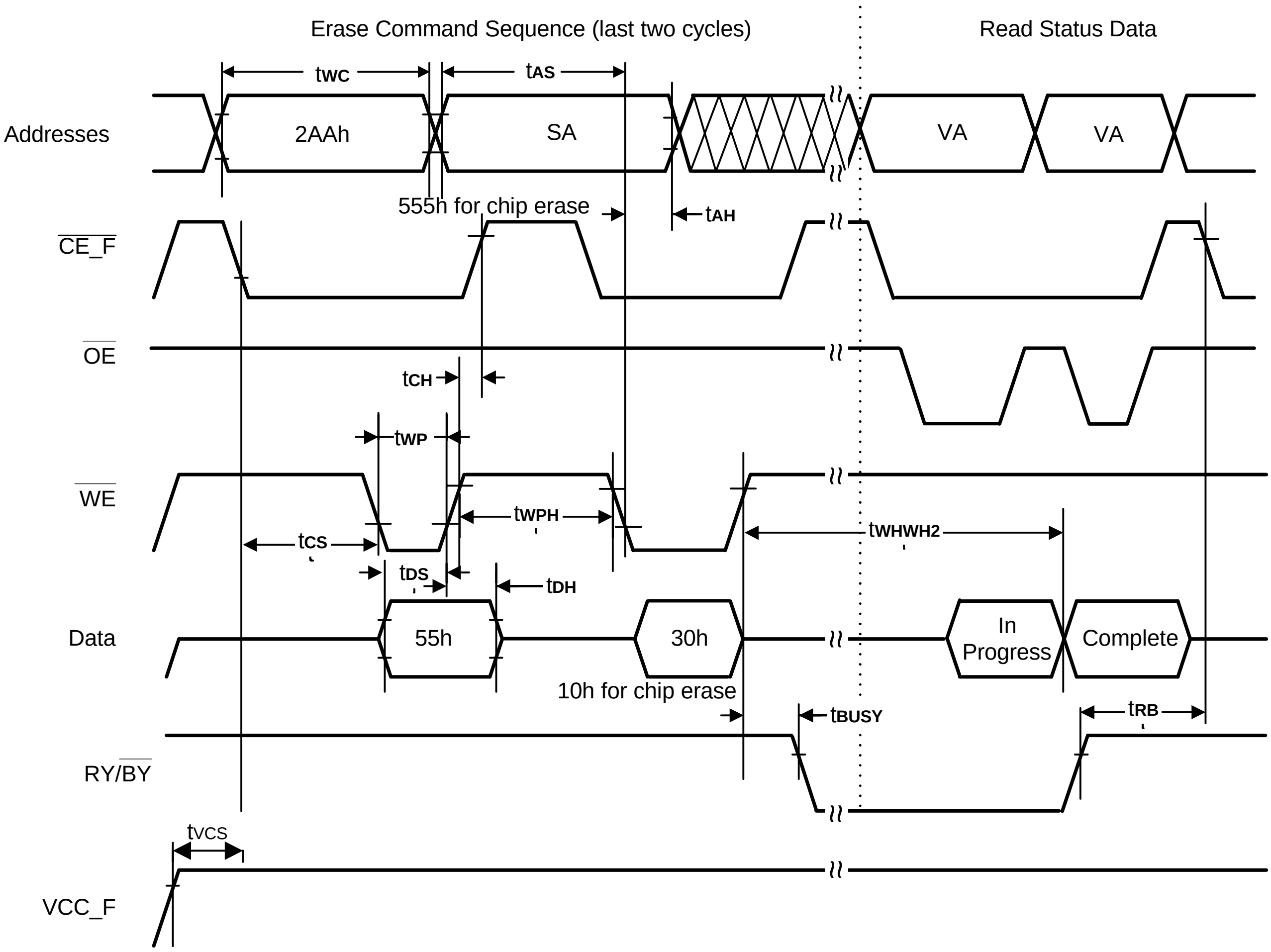
1. PA = program address, PD = program data, Dout is the true data at the program address.
2. Illustration shows device in word mode.

Figure 16. Accelerated Program Timing Diagram



AC CHARACTERISTICS

Figure 17. Chip/Sector Erase Operation Timings



Note :
1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operaion Ststus").
2. Illustration shows device in word mode.

AC CHARACTERISTICS

Figure 18. Back-to-back Read/Write Cycle Timings

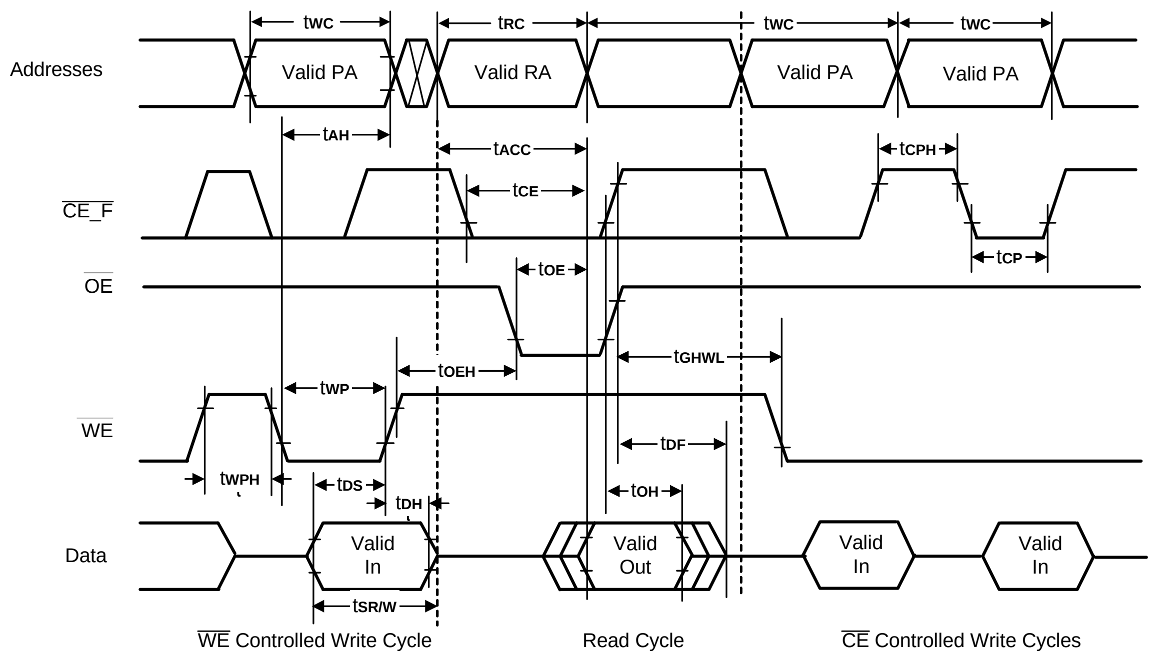
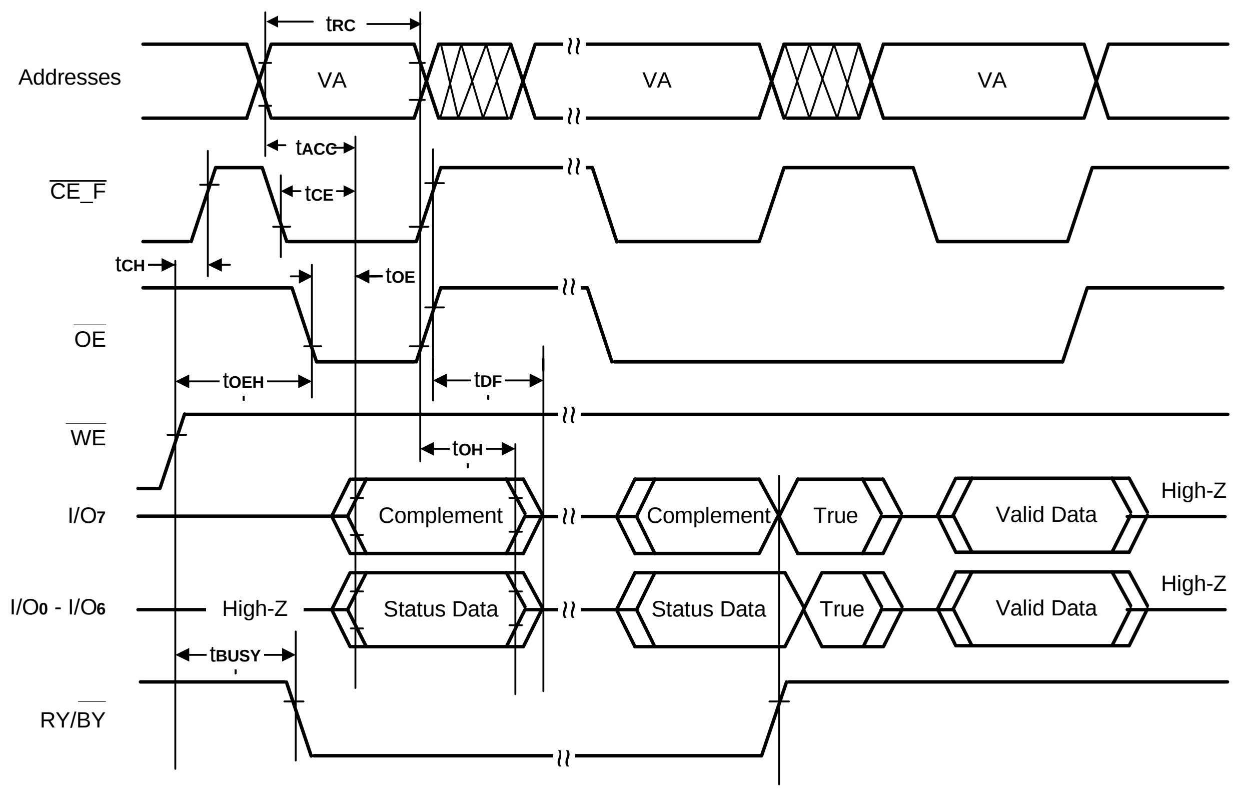


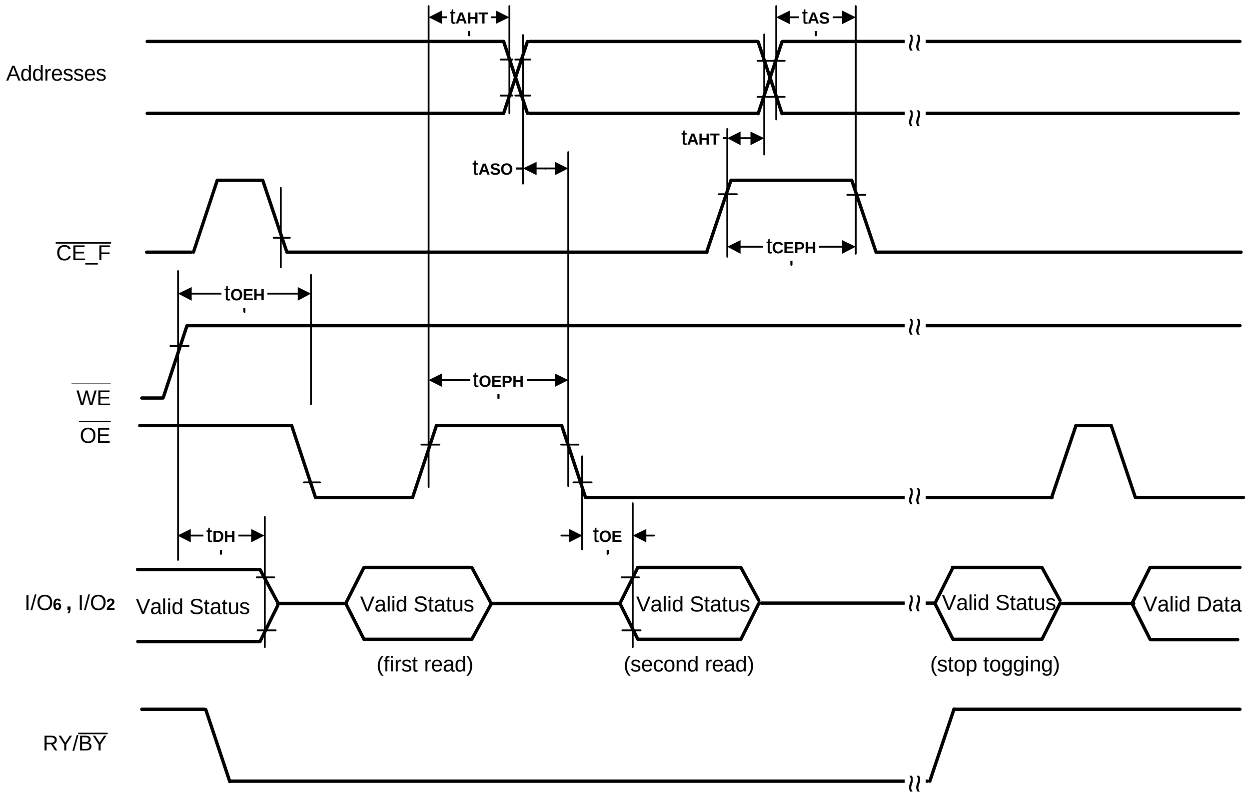
Figure 19. Data Polling Timings (During Embedded Algorithms)



Note : VA = Valid Address. Illustation shows first status cycle after command sequence, last status read cycle, and array data read cycle.

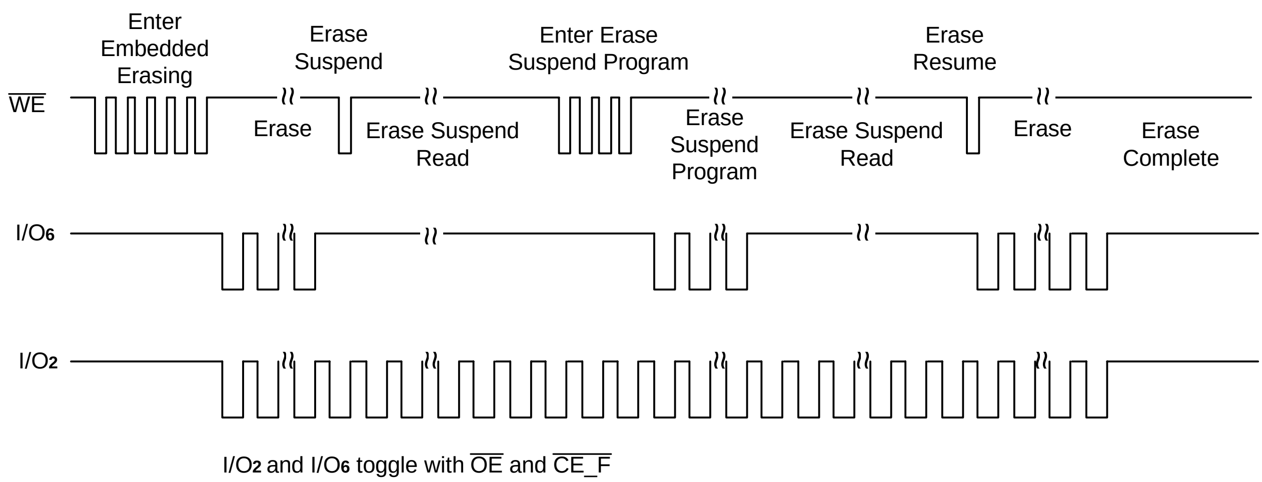
AC CHARACTERISTICS

Figure 20. Toggle Bit Timings (During Embedded Algorithms)



Note: VA = Valid Address; not required for I/O6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 21. I/O2 vs. I/O6



Note : Both I/O6 and I/O2 toggle with OE or CE_F. See the text on I/O6 and I/O2 in the section "Write Operation Status" for more information.

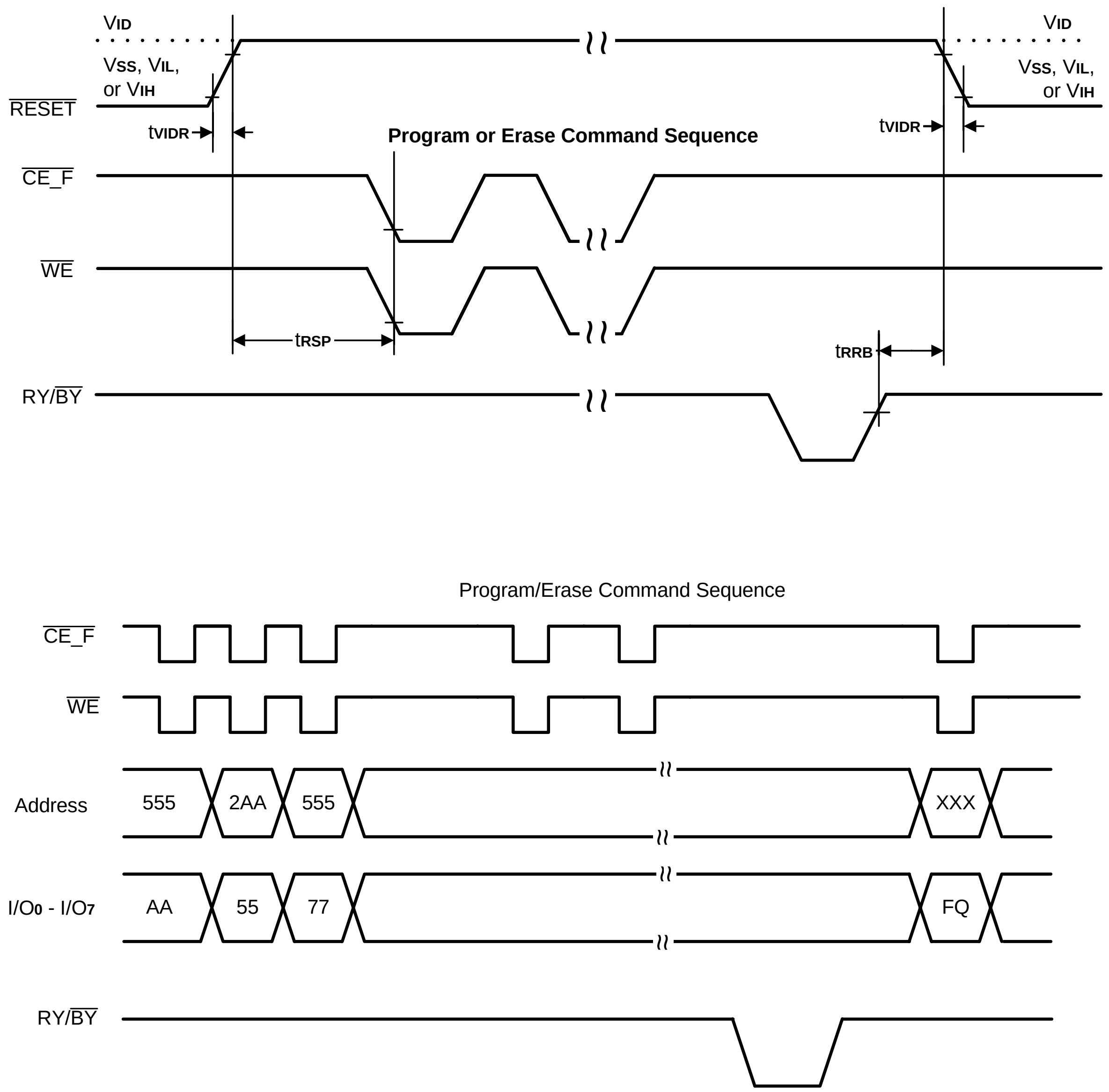
AC CHARACTERISTICS

Temporary Sector/Sector Block Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	μs
	t_{RSP}	RESET Setup Time for Temporary Sector/Sector Block Unprotect	Min	4	μs
	t_{RRB}	RESET Hold Time from RY/BY High for Temporary Sector/Sector Block Unprotect	Min	4	μs

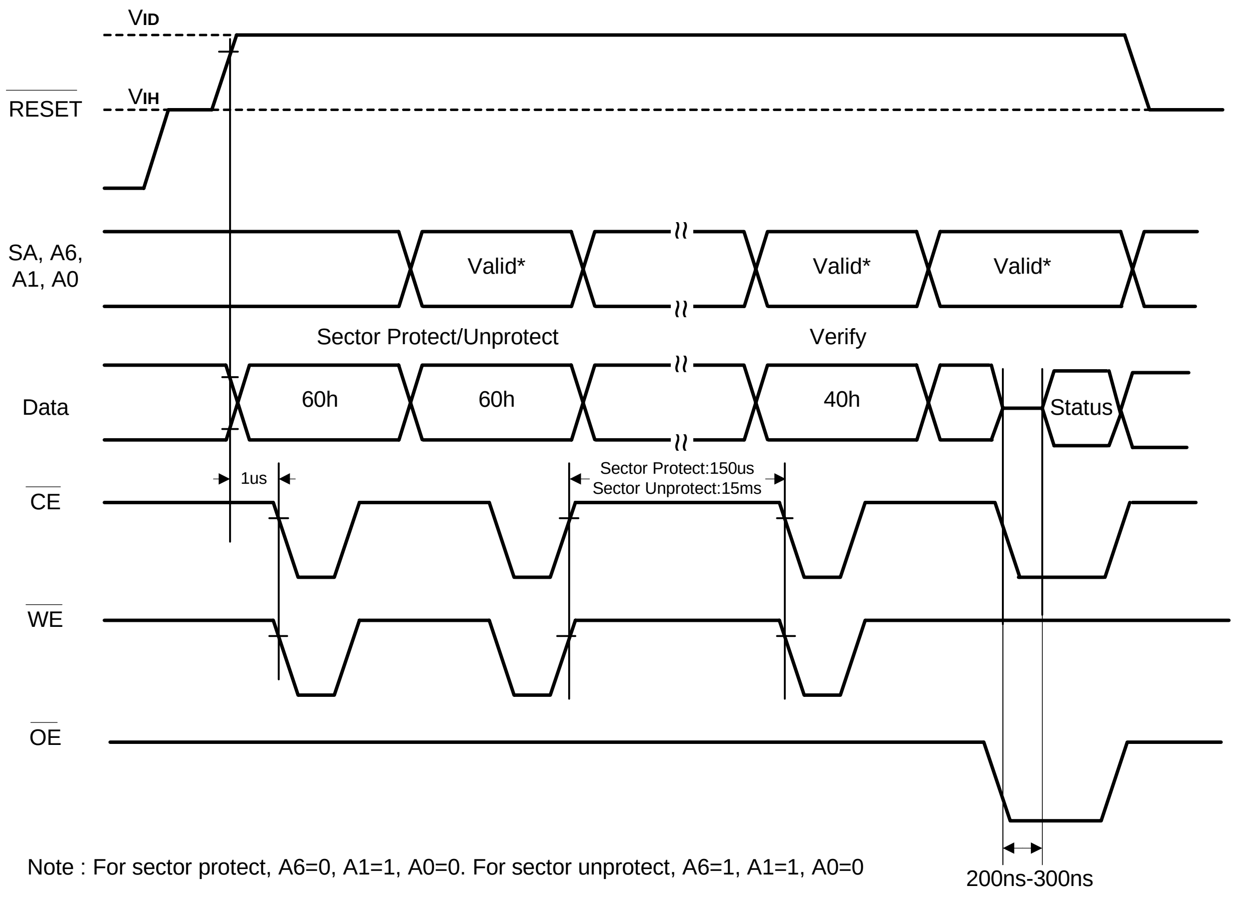
Note: Not 100% tested.

Figure 22. Temporary Sector/Sector Block Unprotect Timing Diagram



AC CHARACTERISTICS

Figure 23. Sector/Sector Block Protect and Unprotect Timing Diagram



Note : For sector protect, A6=0, A1=1, A0=0. For sector unprotect, A6=1, A1=1, A0=0

AC CHARACTERISTICS

Alternate $\overline{CE\_F}$ Controlled Erase and Program Operations

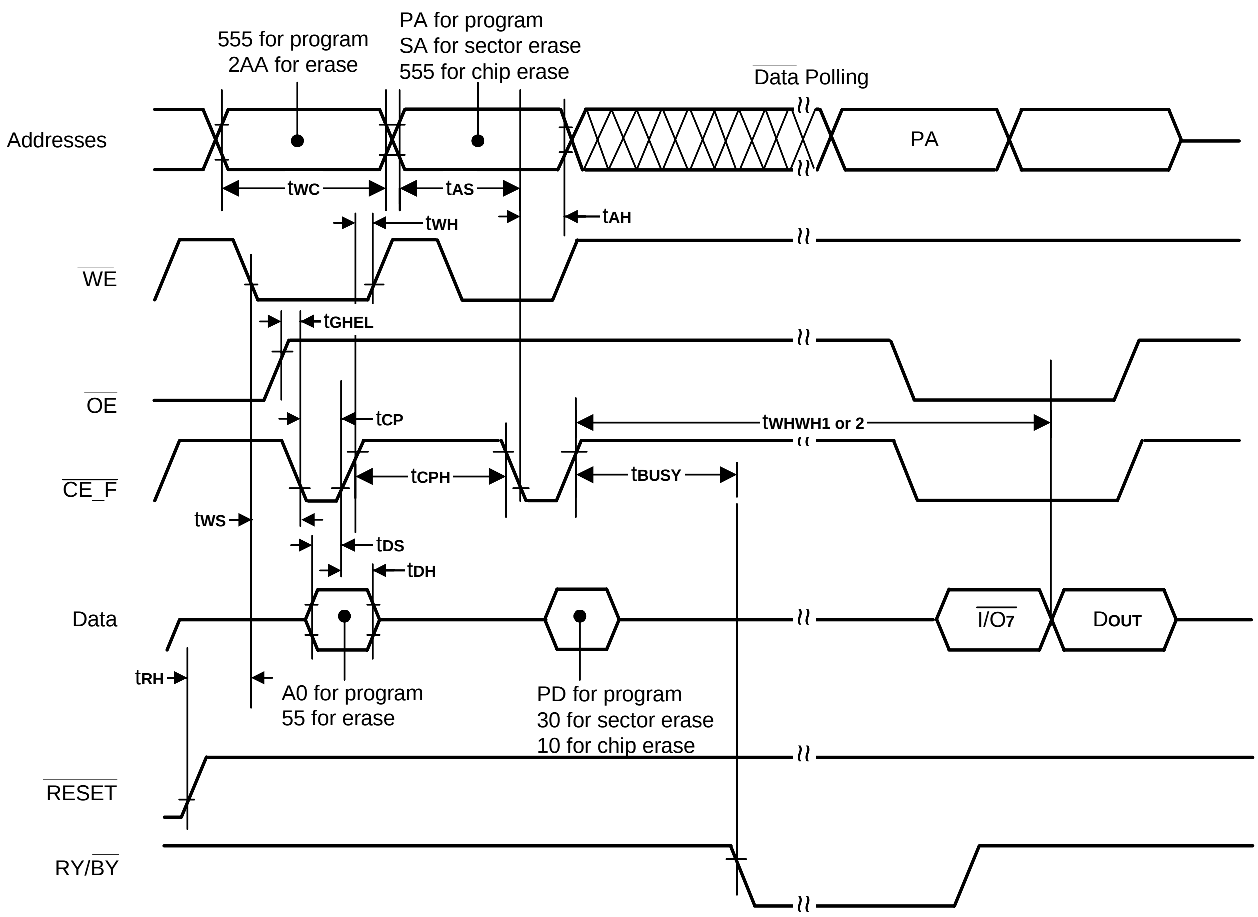
Parameter		Description			Speed	Unit
JEDEC	Std				-70	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min.	70	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min.	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min.	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min.	35	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min.	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min.	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	ns
t_{ELEH}	t_{CP}	$\overline{CE\_F}$ Pulse Width		Min.	30	ns
t_{EHEL}	t_{CPH}	$\overline{CE\_F}$ Pulse Width High		Min.	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ.	5	µs
			Word	Typ.	7	
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ.	4	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ.	0.7	sec

Notes:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

AC CHARACTERISTICS

Figure 24. Alternate $\overline{CE\_F}$ Controlled Write (Erase/Program) Operation Timings



Notes:

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. $\overline{I/O_7}$ is the complement of the data written to the device. DOUT is the data written to the device.
4. Waveforms are for the word mode.

SRAM

DC Electrical Characteristics (T_A = -40°C to +85°C, VCC_S = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	- 70 ns		Unit	Conditions
		Min.	Max.		
$\vert I_{LI} \vert$	Input Leakage Current	-	1	μA	V_{IN} = GND to VCC_S
$\vert I_{LO} \vert$	Output Leakage Current	-	1	μA	$\overline{CE1\_S}$ = V_{IH} or CE2_S = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC_S}	Active Power Supply Current	-	3	mA	$\overline{CE1\_S}$ = V_{IL}, CE2_S = V_{IH} $I_{I/O}$ = 0mA
I_{CC1_S}	Dynamic Operating Current	-	30	mA	Min. Cycle, Duty = 100% $\overline{CE1\_S}$ = V_{IL}, CE2_S = V_{IH} $I_{I/O}$ = 0mA
I_{CC2_S}		-	3	mA	$\overline{CE1\_S}$ = V_{IL}, CE2_S = V_{IH} V_{IH} = VCC_S, V_{IL} = 0V f = 1 MHz, $I_{I/O}$ = 0mA
I_{SB_S}	Standby Power Supply Current	-	0.5	mA	VCC_S ≤ 3.3V, $\overline{CE1\_S}$ = V_{IH} or CE2_S = V_{IL}
I_{SB1_S}		-	5	μA	VCC ≤ 3.3V, $\overline{CE1\_S}$ ≥ VCC - 0.2V or CE2_S ≤ 0.2V, V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.2	-	V	I_{OH} = -1.0mA

Truth Table

Mode	$\overline{CE1\_S}$	CE2_S	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

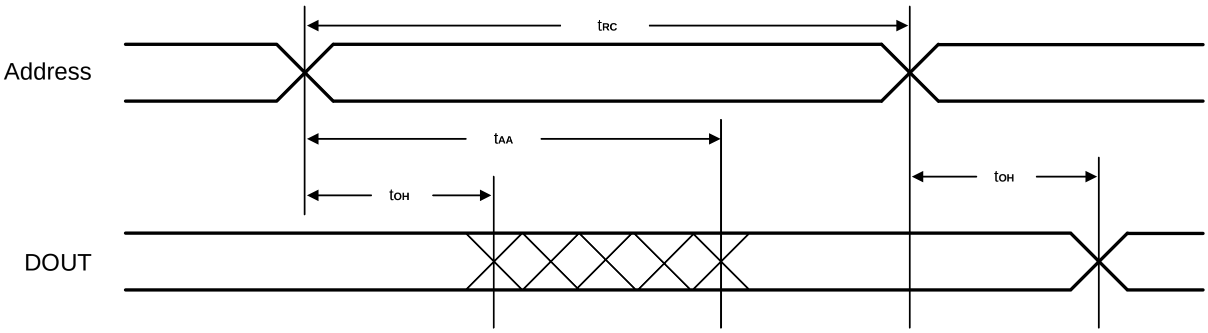
AC Characteristics (T_A = -40°C to +85°C, VCC_S = 2.7V to 3.6V)

Symbol	Parameter		-70 ns		Unit
			Min.	Max.	
Read Cycle					
t_{RC}	Read Cycle Time		70	-	ns
t_{AA}	Address Access Time		-	70	ns
t_{ACE1}	Chip Enable Access Time	$\overline{CE1\_S}$	-	70	ns
t_{ACE2}		CE2_S	-	70	ns
t_{OE}	Output Enable to Output Valid		-	35	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1\_S}$	10	-	ns
t_{CLZ2}		CE2_S	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z		5	-	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1\_S}$	0	25	ns
t_{CHZ2}		CE2_S	0	25	ns
t_{OHZ}	Output Disable to Output in High Z		0	25	ns
t_{OH}	Output Hold from Address Change		10	-	ns
Write Cycle					
t_{WC}	Write Cycle Time		70	-	ns
t_{CW}	Chip Enable to End of Write		60	-	ns
t_{AS}	Address Setup Time		0	-	ns
t_{AW}	Address Valid to End of Write		60	-	ns
t_{WP}	Write Pulse Width		50	-	ns
t_{WR}	Write Recovery Time		0	-	ns
t_{WHZ}	Write to Output in High Z		0	25	ns
t_{DW}	Data to Write Time Overlap		30	-	ns
t_{DH}	Data Hold from Write Time		0	-	ns
t_{OW}	Output Active from End of Write		5	-	ns

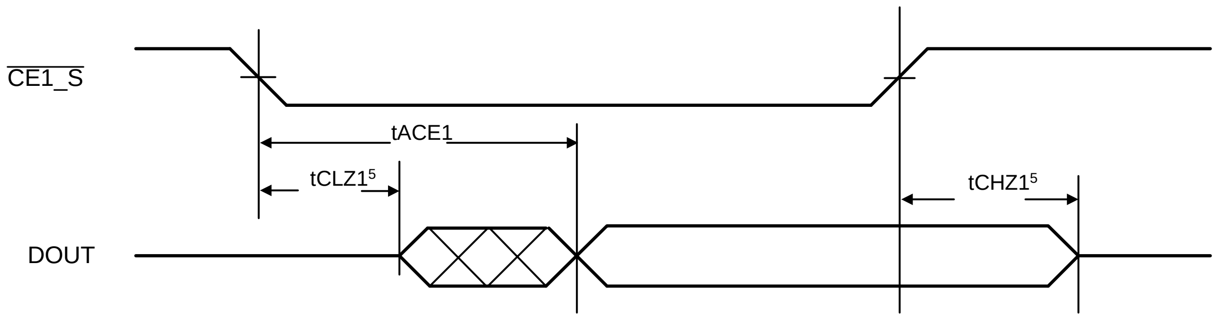
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ}, and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

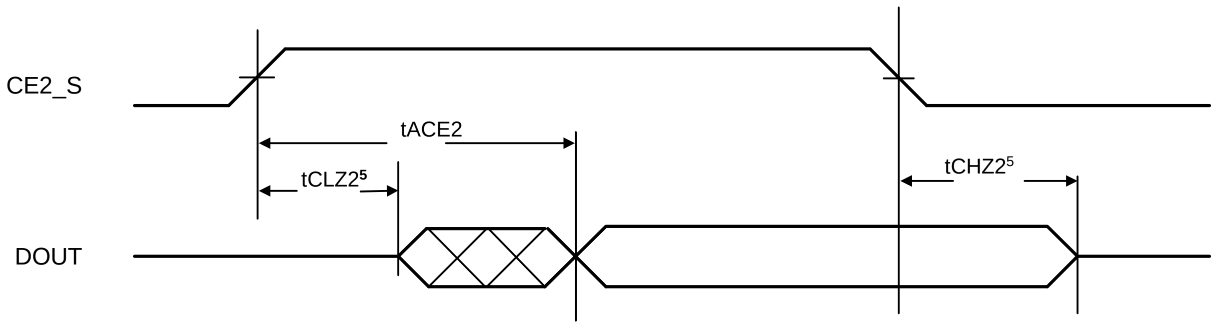
Read Cycle 1 (1, 2, 4)



Read Cycle 2 (1, 3, 4, 6)

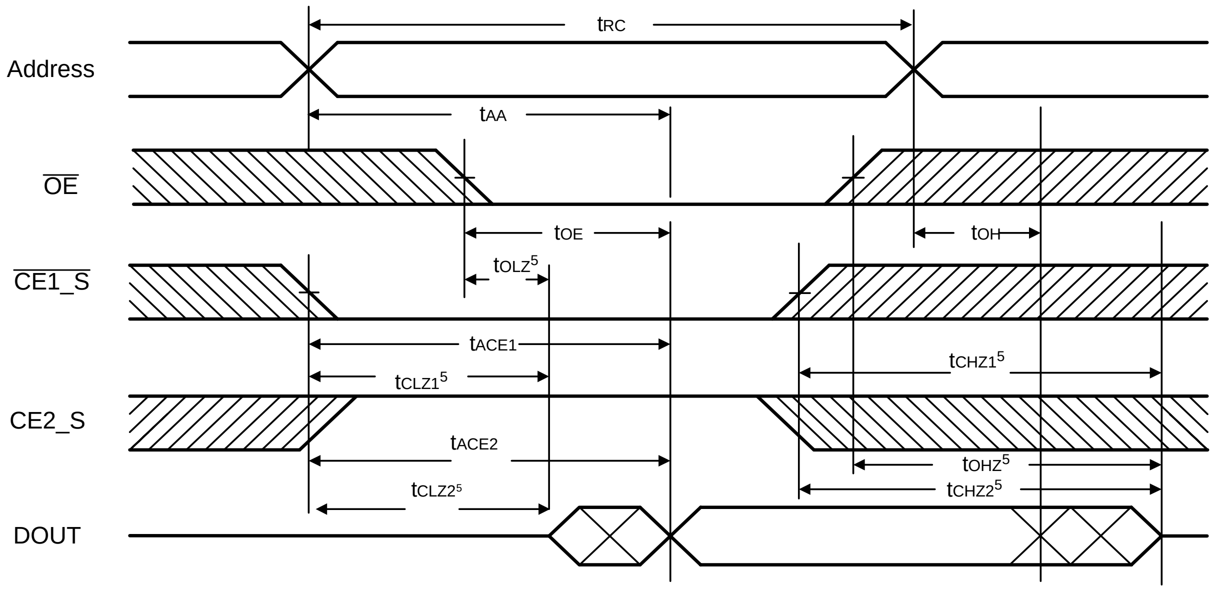


Read Cycle 3 (1, 4, 7, 8)



Timing Waveforms (continued)

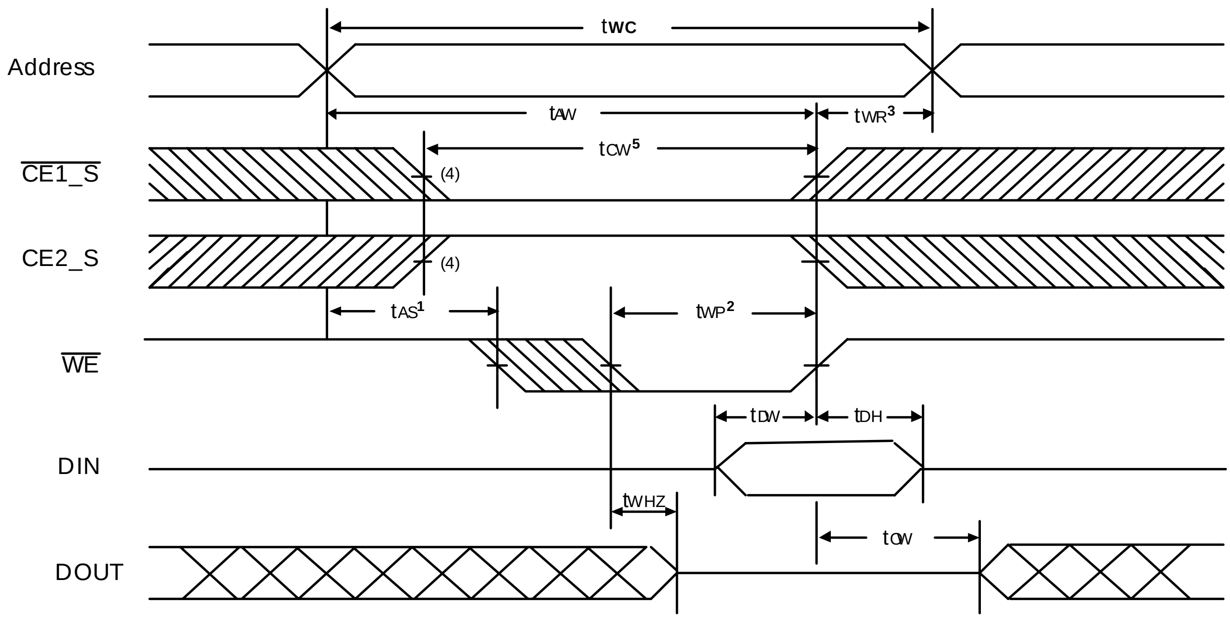
Read Cycle 4 (1)



Notes: 1. $\overline{\text{WE}}$ is high for Read Cycle.

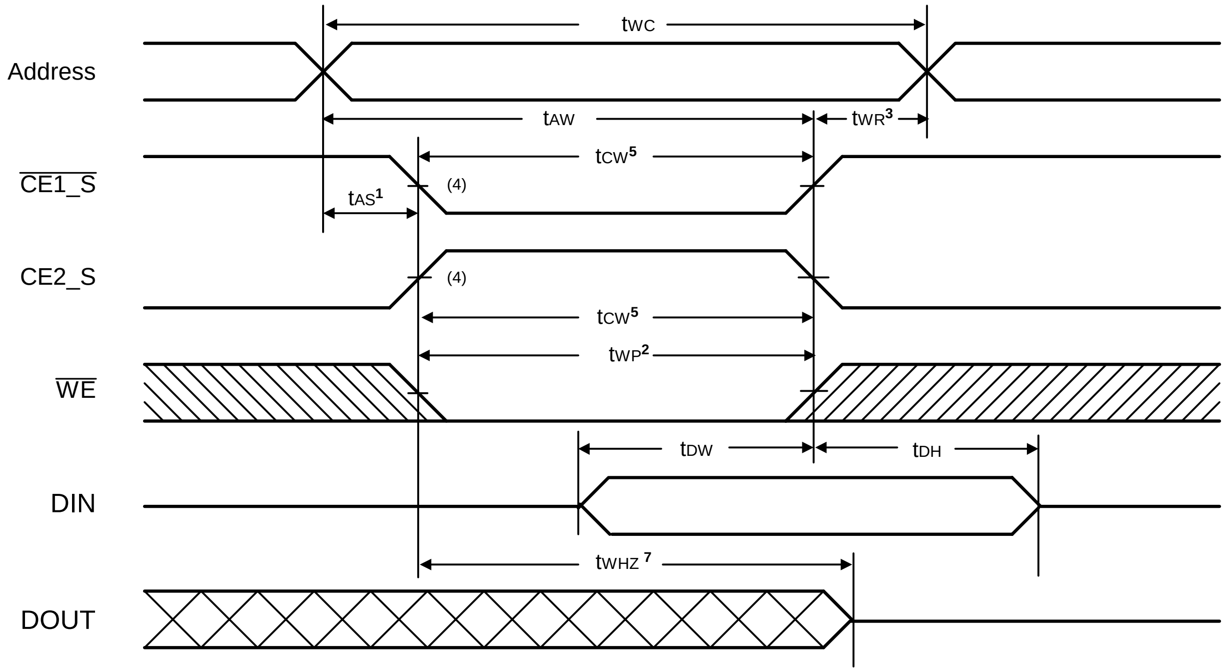
2. Device is continuously enabled $\overline{\text{CE1\_S}}$ = V_{IL} and CE2_S = V_{IH}.
3. Address valid prior to or coincident with $\overline{\text{CE1\_S}}$ transition low.
4. $\overline{\text{OE}}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2_S is high.
7. $\overline{\text{CE1\_S}}$ is low.
8. Address valid prior to or coincident with CE2_S transition high.

Write Cycle 1 (6)
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.

2. A Write occurs during the overlap (t_{WP}) of a low $\overline{\text{CE1\_S}}$, a high CE2_S and a low $\overline{\text{WE}}$.
3. t_{WR} is measured from the earliest of $\overline{\text{CE1\_S}}$ or $\overline{\text{WE}}$ going high or CE2_S going low to the end of the Write cycle.
4. If the $\overline{\text{CE1\_S}}$ low transition or the CE2_S high transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{\text{CE1\_S}}$ going low or CE2_S going high to the end of Write.
6. $\overline{\text{OE}}$ is continuously low. ($\overline{\text{OE}}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

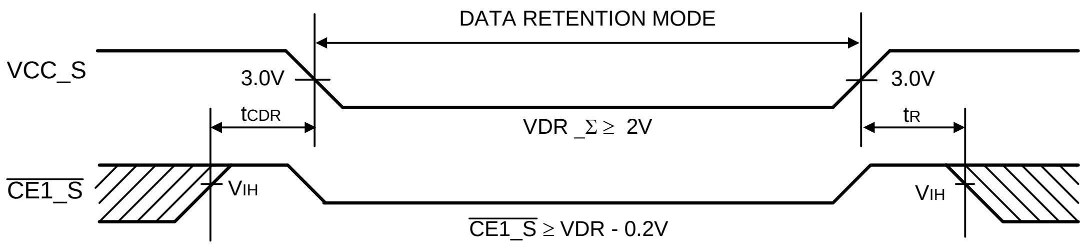
SRAM

Data Retention Characteristics (T$_A$ = -40°C to 85°C)

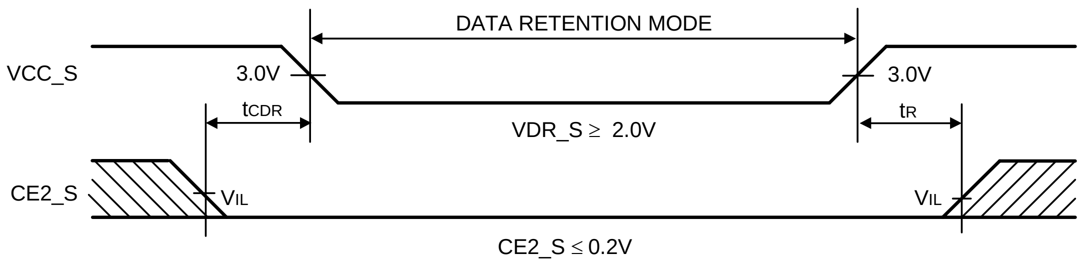
Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention	2.0	3.6	V	$\overline{\text{CE1\_S}} \geq$ VCC - 0.2V
V_{DR2}		2.0	3.6	V	CE2_S $\leq$ 0.2V,
I_{CCDR1_S}	Data Retention Current	-	1*	µA	VCC_S = 2V, $\overline{\text{CE1\_S}} \geq$ VCC_S - 0.2V, $V_{IN} \geq$ 0V
I_{CCDR2_S}		-	1*	µA	VCC_S = 2V, CE2_S $\leq$ 0.2V, $V_{IN} \geq$ 0V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	5	-	ms	

* I_{CCDR_S}: max. 1µA at T$_A$ = 0°C to + 40°C

Low VCC Data Retention Waveform (1) ($\overline{\text{CE1\_S}}$ Controlled)



Low VCC Data Retention Waveform (2) (CE2_S Controlled)



ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ. (Note 1)	Max. (Note 2)	Unit	Comments
Sector Erase Time		0.7	15	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		27		sec	
Byte Programming Time		5	150	µs	Excludes system-level overhead (Note 5)
Word Programming Time		7	210	µs	
Accelerated Word/Byte Programming Time		4	120	µs	
Chip Programming Time (Note 3)	Byte Mode	9	27	sec	
	Word Mode	6	18	sec	

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC_F, 10,000 cycles. Additionally, programming typically assumes checkerboard pattern.
2. Under worst case conditions of 90°C, VCC_F = 2.7V, 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 12 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 10,000 cycles.

FLASH LATCH-UP CHARACTERISTICS

Description	Min.	Max.
Input Voltage with respect to VSS on all I/O pins	-1.0V	VCC+1.0V
VCC_F Current	-100 mA	+100 mA
Input voltage with respect to VSS on all pins except I/O pins (including A9, $\overline{OE}$ and $\overline{RESET}$)	-1.0V	12.5V

Includes all pins except VCC_F. Test conditions: VCC_F = 3.0V, one pin at time.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Ordering Information

Top Boot Sector Flash & SRAM

Part No.	Access Time (ns)	Bank 1	Bank 2	Package
A82DL1624TG-70	70	2M	14M	69-ball TFBGA
A82DL1624TG-70F				69-ball Pb-Free TFBGA
A82DL1624TG-70I				69-ball TFBGA
A82DL1624TG-70IF				69-ball Pb-Free TFBGA
A82DL1624TG-70U				69-ball TFBGA
A82DL1624TG-70UF				69-ball Pb-Free TFBGA
A82DL1634TG-70	70	4M	12M	69-ball TFBGA
A82DL1634TG-70F				69-ball Pb-Free TFBGA
A82DL1634TG-70I				69-ball TFBGA
A82DL1634TG-70IF				69-ball Pb-Free TFBGA
A82DL1634TG-70U				69-ball TFBGA
A82DL1634TG-70UF				69-ball Pb-Free TFBGA
A82DL1644TG-70	70	8M	8M	69-ball TFBGA
A82DL1644TG-70F				69-ball Pb-Free TFBGA
A82DL1644TG-70I				69-ball TFBGA
A82DL1644TG-70IF				69-ball Pb-Free TFBGA
A82DL1644TG-70U				69-ball TFBGA
A82DL1644TG-70UF				69-ball Pb-Free TFBGA

Note: Industrial operating temperature range: -40°C to 85°C for –U; -25°C to 85°C for –I

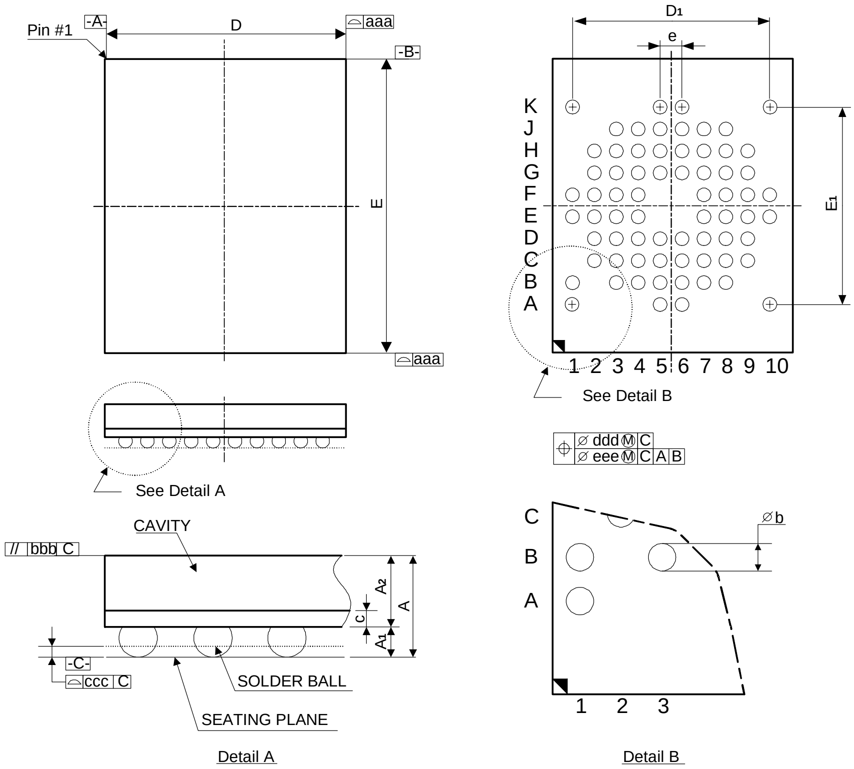
Bottom Boot Sector Flash & SRAM

Part No.	Access Time (ns)	Bank 1	Bank 2	Package
A82DL1624UG-70	70	2M	14M	69-ball TFBGA
A82DL1624UG-70F				69-ball Pb-Free TFBGA
A82DL1624UG-70I				69-ball TFBGA
A82DL1624UG-70IF				69-ball Pb-Free TFBGA
A82DL1624UG-70U				69-ball TFBGA
A82DL1624UG-70UF				69-ball Pb-Free TFBGA
A82DL1634UG-70	70	4M	12M	69-ball TFBGA
A82DL1634UG-70F				69-ball Pb-Free TFBGA
A82DL1634UG-70I				69-ball TFBGA
A82DL1634UG-70IF				69-ball Pb-Free TFBGA
A82DL1634UG-70U				69-ball TFBGA
A82DL1634UG-70UF				69-ball Pb-Free TFBGA
A82DL1644UG-70	70	8M	8M	69-ball TFBGA
A82DL1644UG-70F				69-ball Pb-Free TFBGA
A82DL1644UG-70I				69-ball TFBGA
A82DL1644UG-70IF				69-ball Pb-Free TFBGA
A82DL1644UG-70U				69-ball TFBGA
A82DL1644UG-70UF				69-ball Pb-Free TFBGA

Note: Industrial operating temperature range: -40°C to 85°C for –U; -25°C to 85°C for –I

Package Information

69LD STF BGA (8 x 11mm) Outline Dimensions unit: mm



Symbol	Dimensions in mm			Dimensions in inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.40	-	-	0.055
A_1	0.25	0.30	0.35	0.010	0.012	0.014
A_2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	7.90	8.00	8.10	0.311	0.315	0.319
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	-	7.20	-	-	0.283	-
E1	-	7.20	-	-	0.283	-
e	-	0.80	-	-	0.031	-
b	0.35	0.40	0.45	0.14	0.16	0.18
aaa	0.15			0.006		
bbb	0.20			0.008		
ccc	0.12			0.005		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	10/10			10/10		

Notes:

1. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. REFERENCE DOCUMENT : JEDEC MO-219
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.