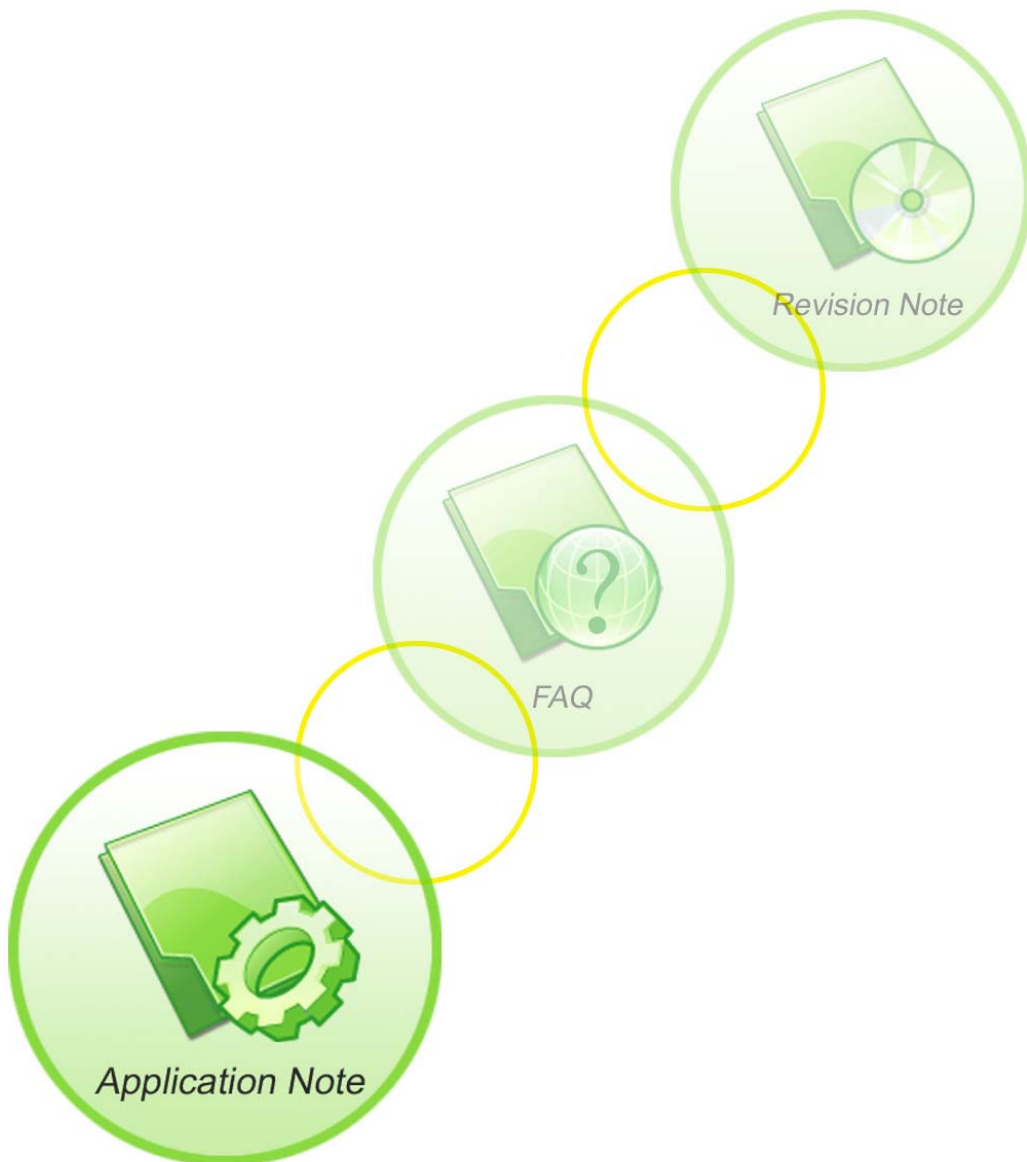




# SIM900D-TE\_PCB Layout & Schematic for Reference\_Application Note\_V1.00



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## Version History

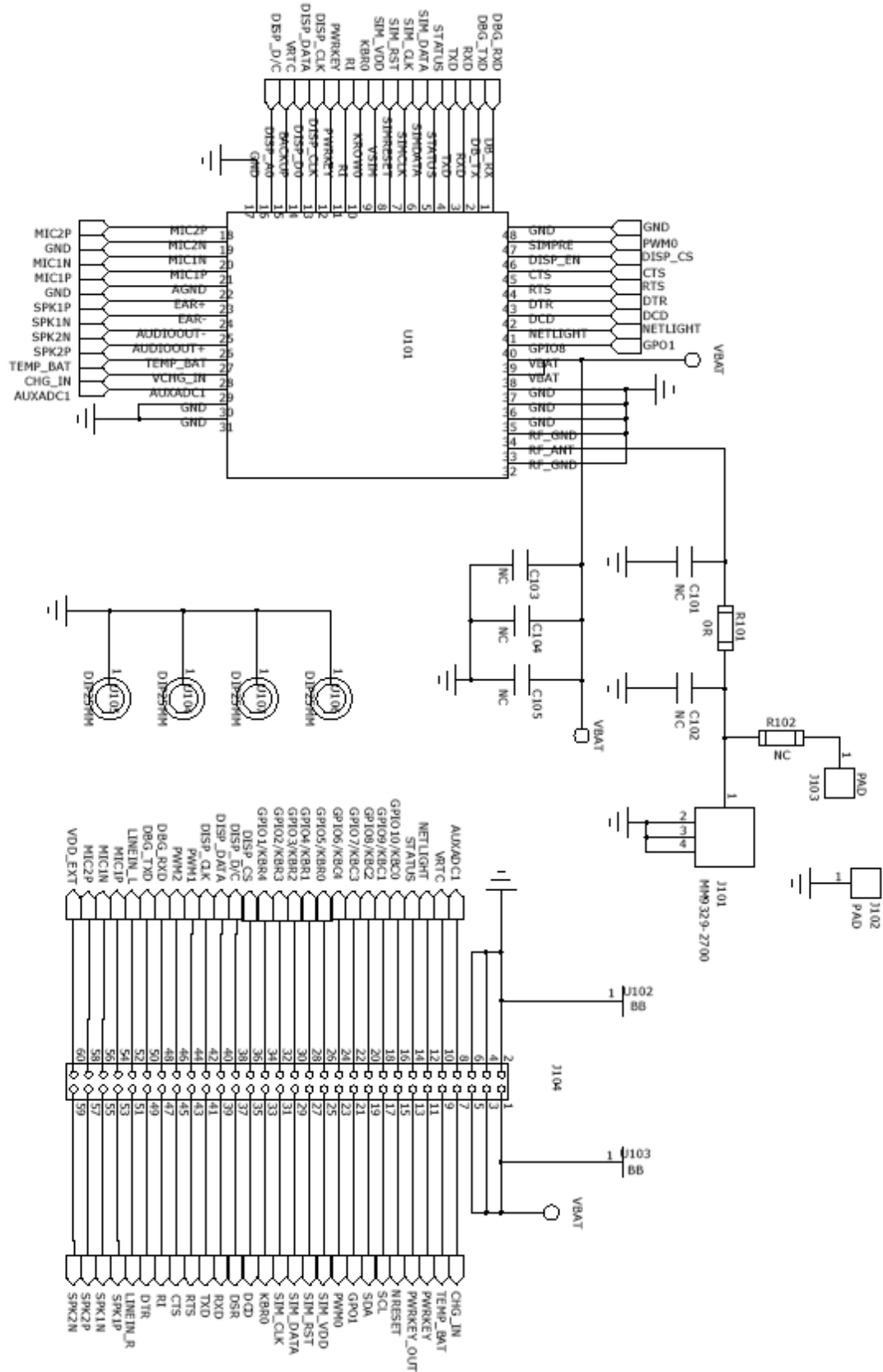
Data	Version	Description of change	Author
2010-8-27	V1.00	Origin	liya Wang Guoqiang

# 1 Introduction

This document shows the detailed information about SIM900D-TE PCB Layout and Schematic. It is only an illustration for customer. Users should modify the PCB layout based on different cases.

## 2 Schematic

**SIM900D-TE PCB Layout for Reference**



*Note: In this schematic, the resistor R102 is a option for choosing either a GSC type coaxial RF*

**SIM900D-TE PCB Layout for Reference**

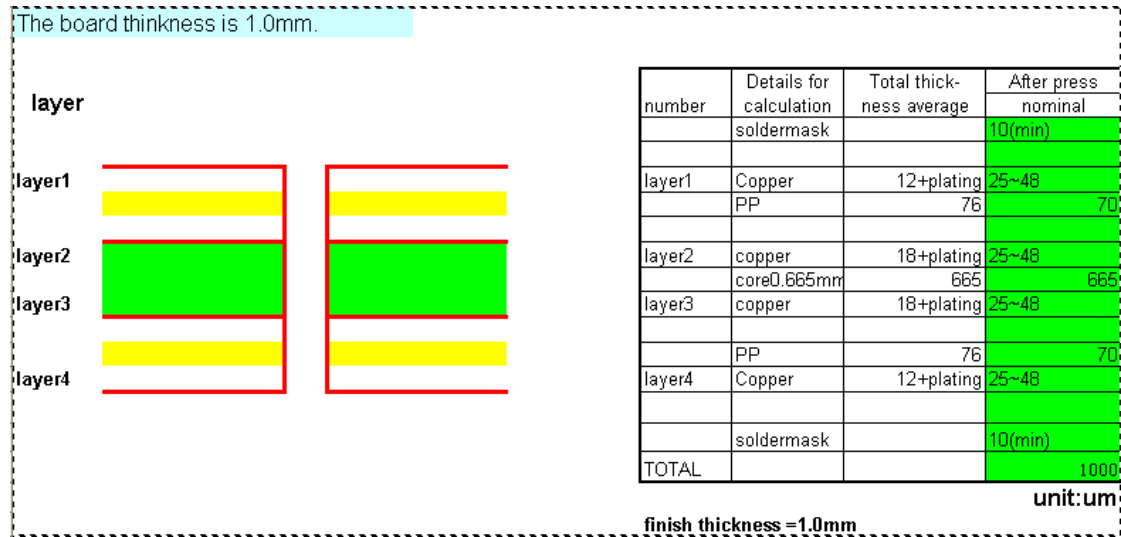
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*cable (MXTK series, vended by Murata) or a soldered coaxial RF cable. The R102 is mounted with a 0ohm resistor, a soldered coaxial RF cable can be chose for antenna connection, and if the R102 is not mounted, the antenna should be connected via a **GSC** type coaxial RF cable.*



### 3 PCB Layout

#### 3.1 The SIM900D-TE PCB's stack up



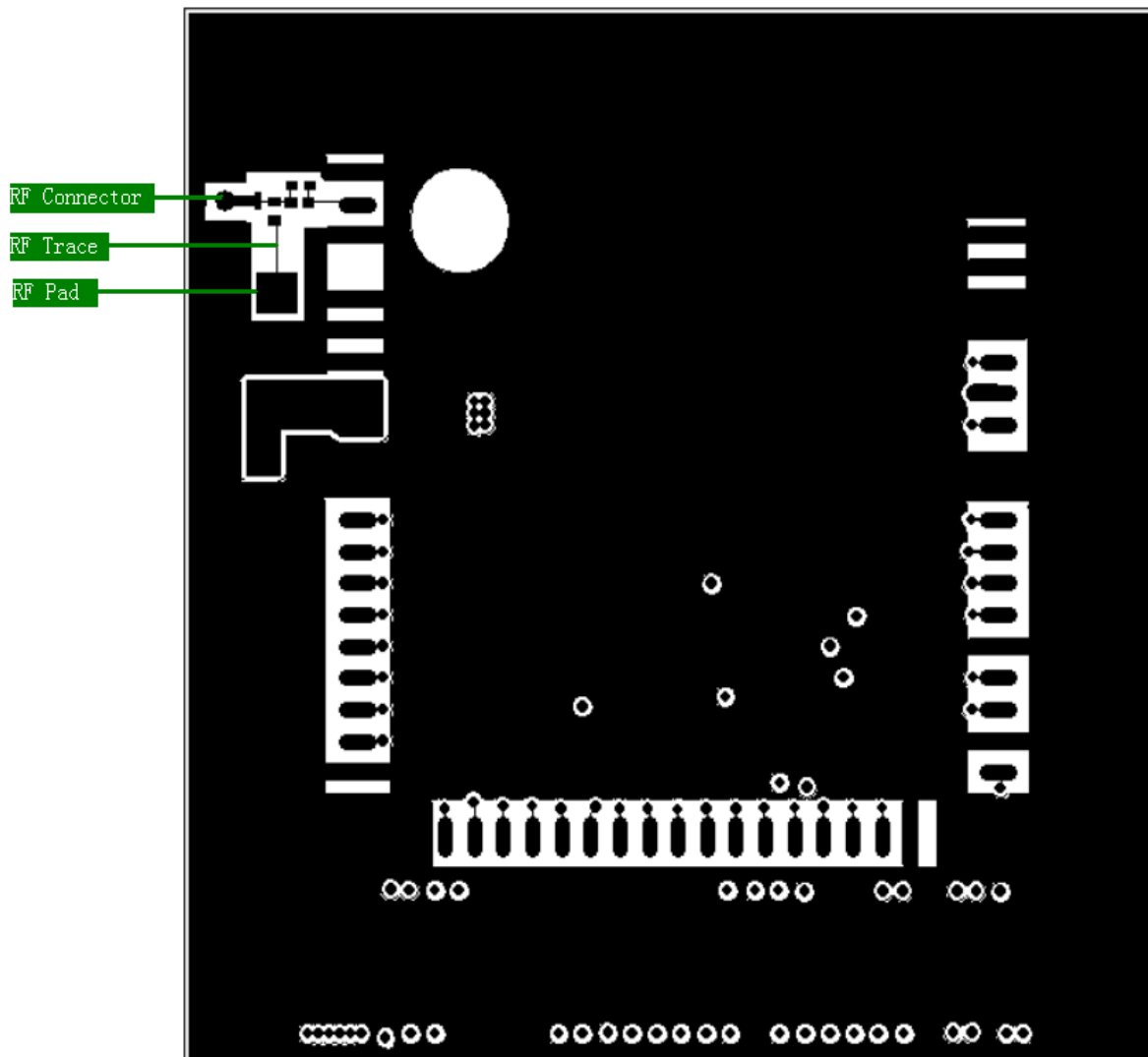
The SIM900D-TE is a four layer PCB, the PCB's total thickness is 1.0mm, the clearance between the first layer and the second layer is 0.076mm, the clearance between the second layer and the third layer is 0.665mm.

The RF trace is routed on the top layer, and the second layer is the reference ground layer, For the Thickness between the top layer and the second layer is only 0.076mm, so the width of the RF trace on the top layer is 0.11mm.

#### 3.2 The SIM900D-TE's PCB layout

The following picture are the detailed PCB layout of SIM900D-TE.

## Top Layer



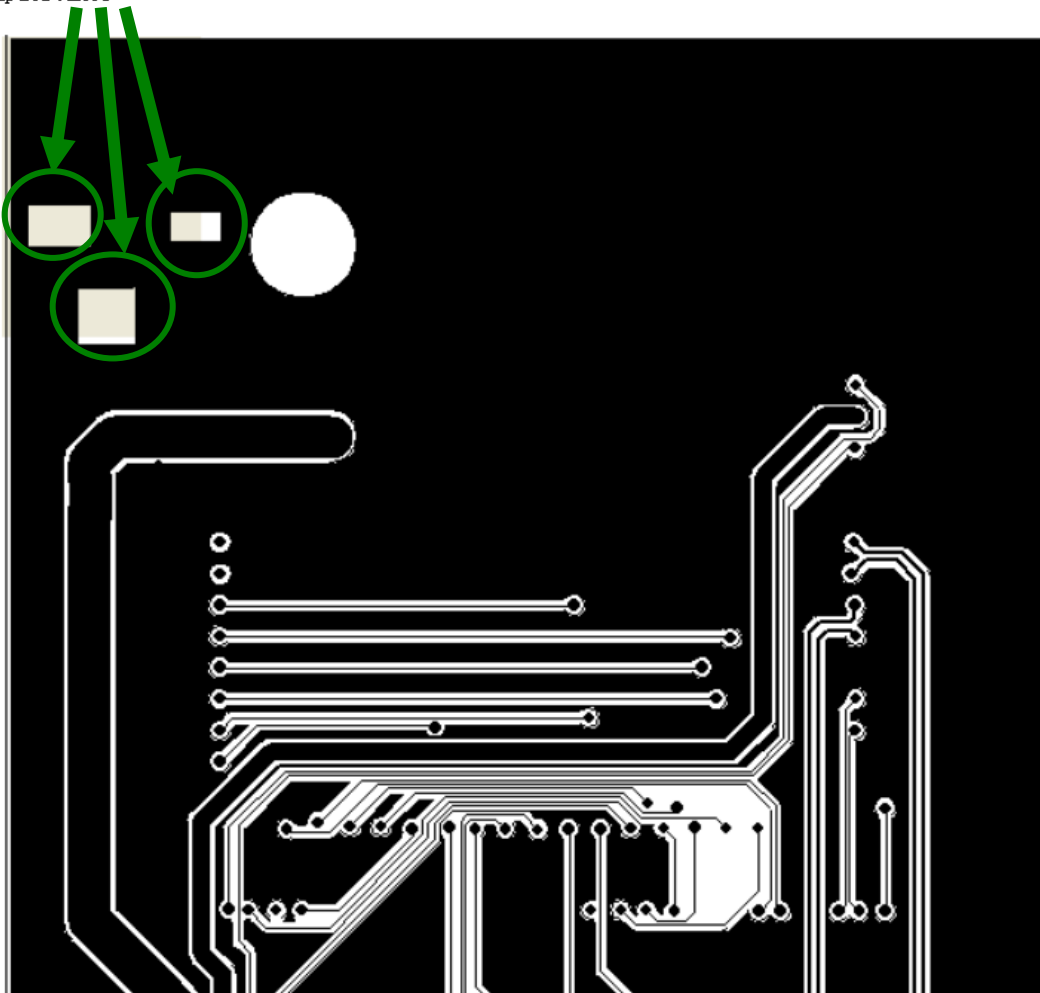
1 the RF traces are 50ohm impedance controlled.

RF connector is matched the GSC coaxial cable assembly, the RF cable should be 50ohm impedance controlled coaxial cable.

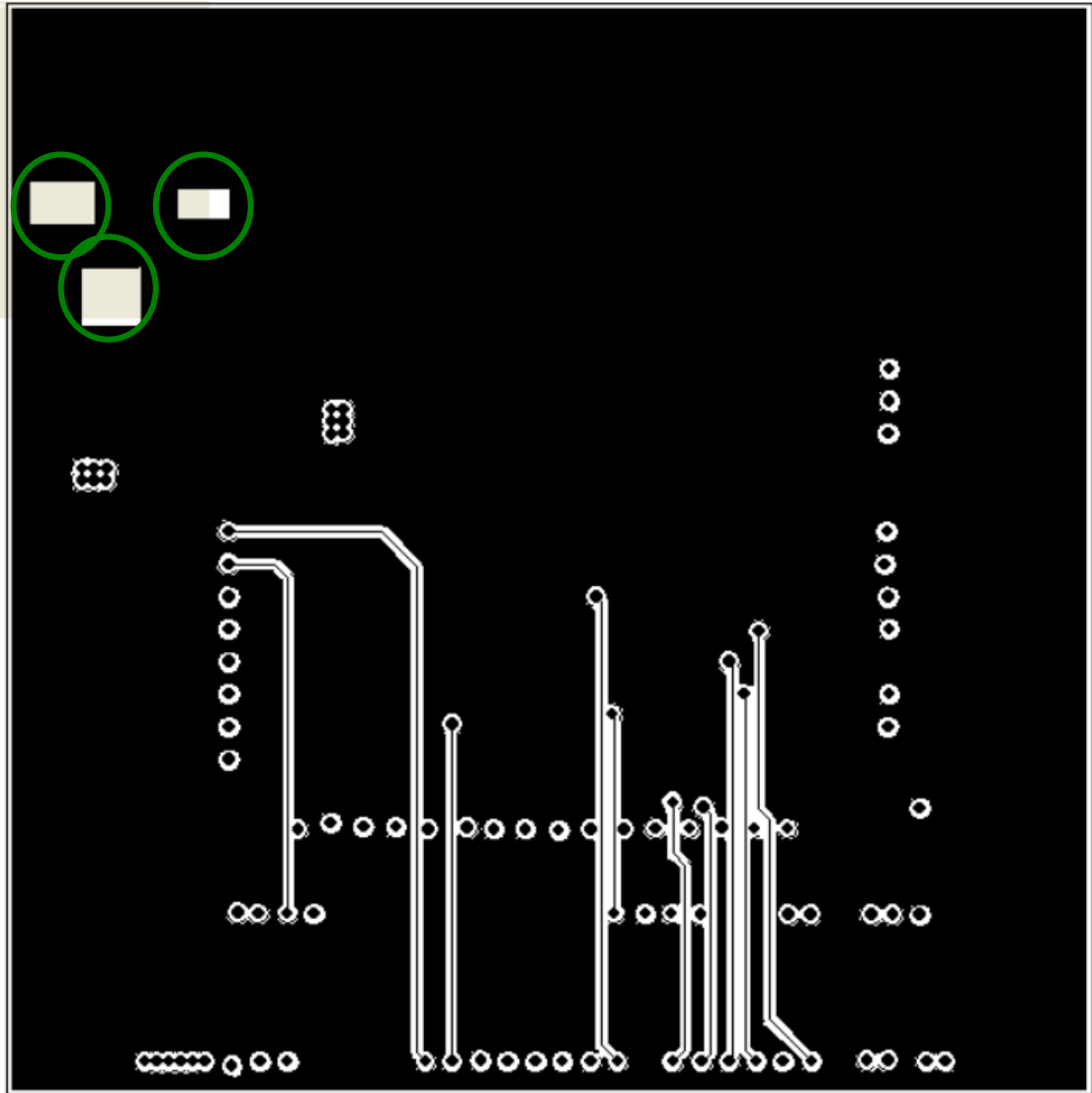
RF PAD is used for connect with solderable RF coaxial cable assembly, the RF cable is also should be 50ohm impedance controlled.

Layer 2

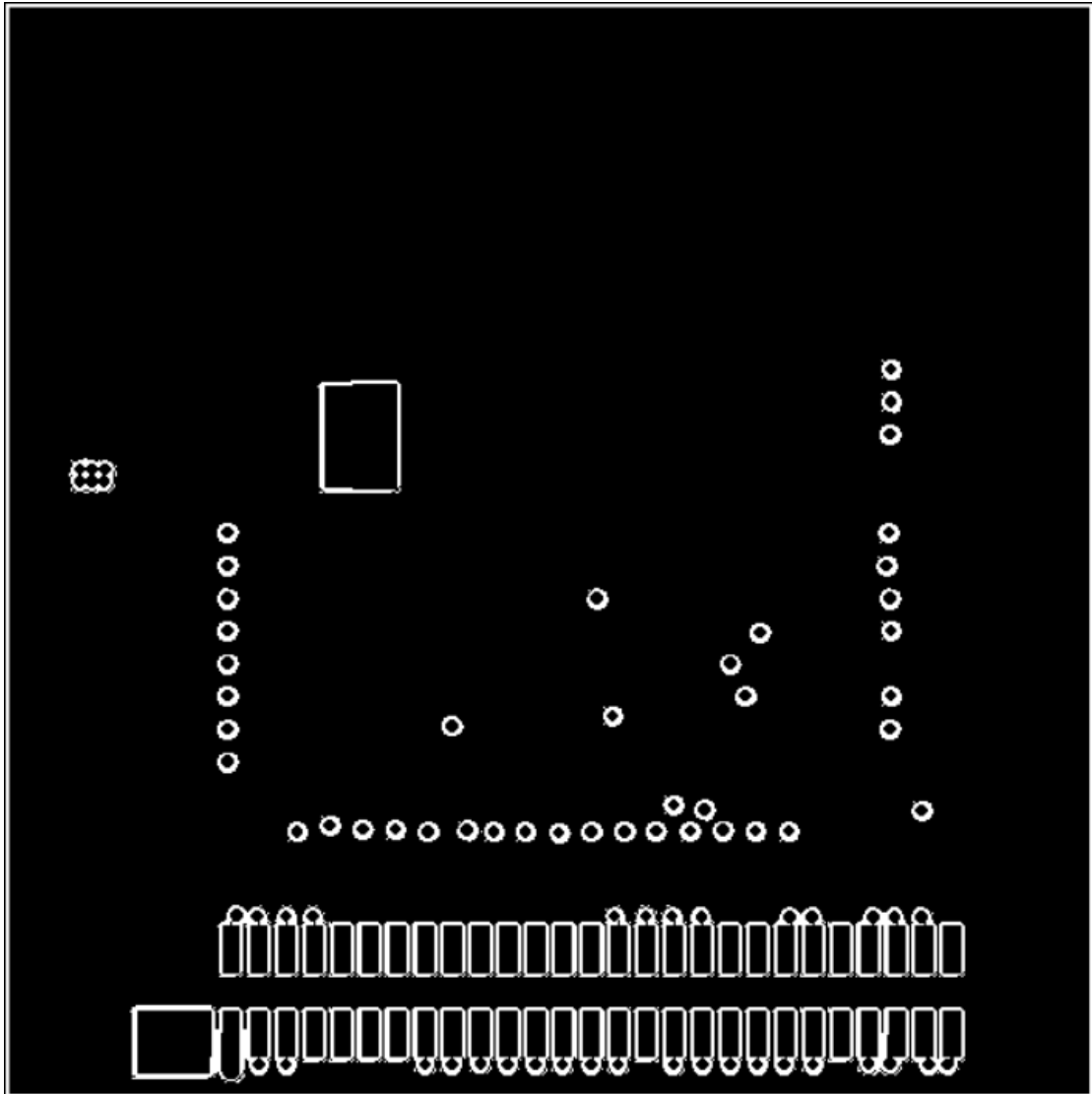
Copper in these area  
should be keep out to  
reduce the parasitic  
capacitance



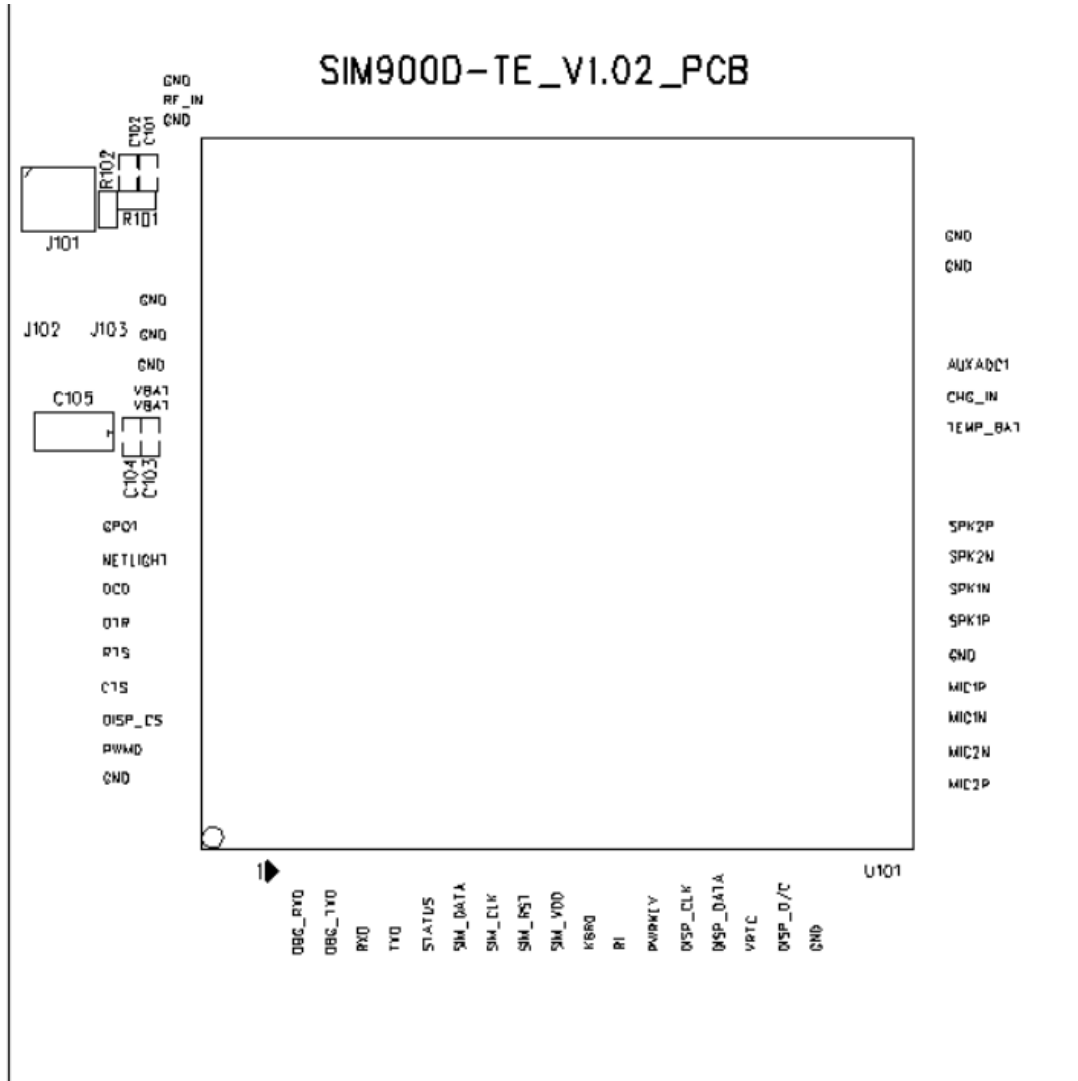
Layer 3



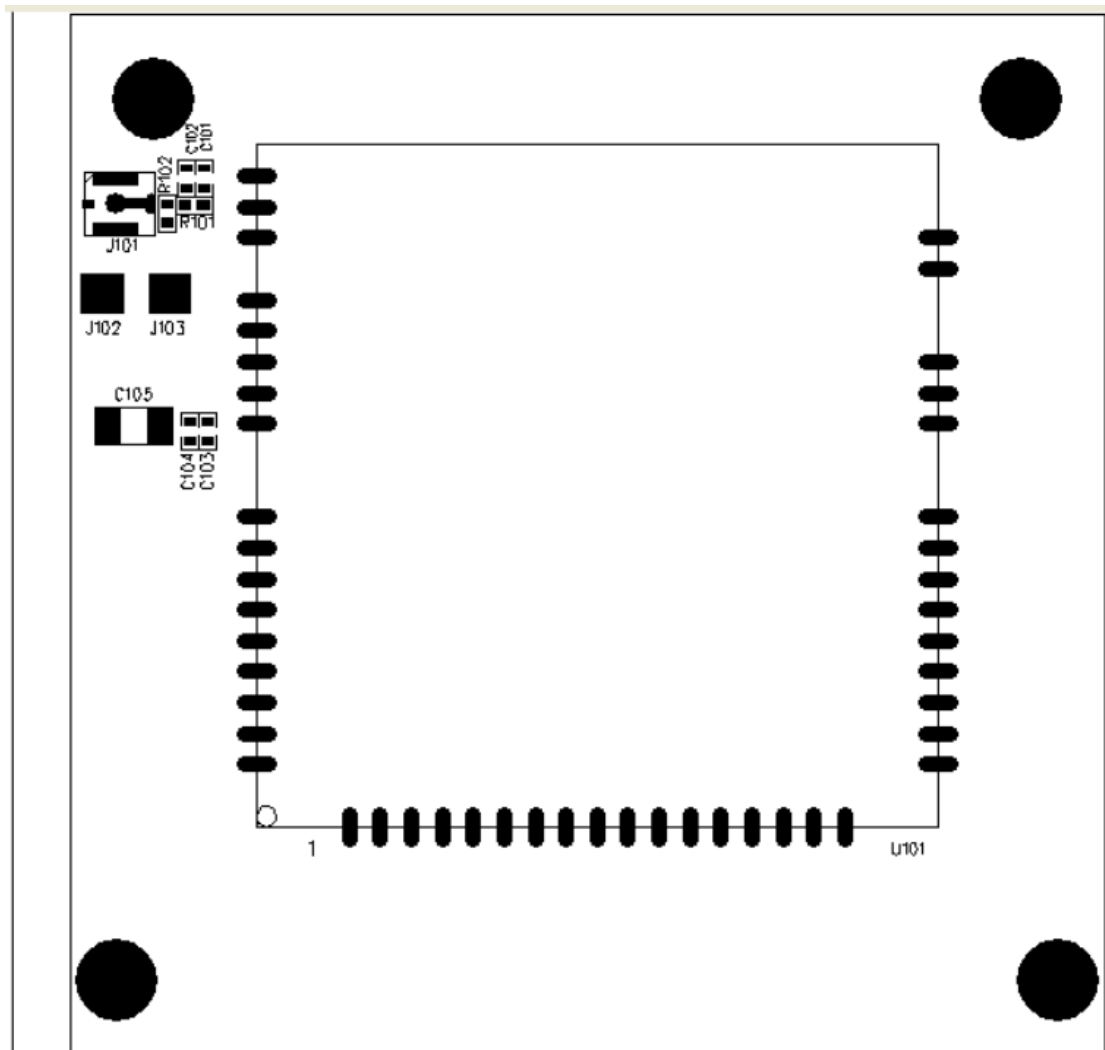
Bottom layer



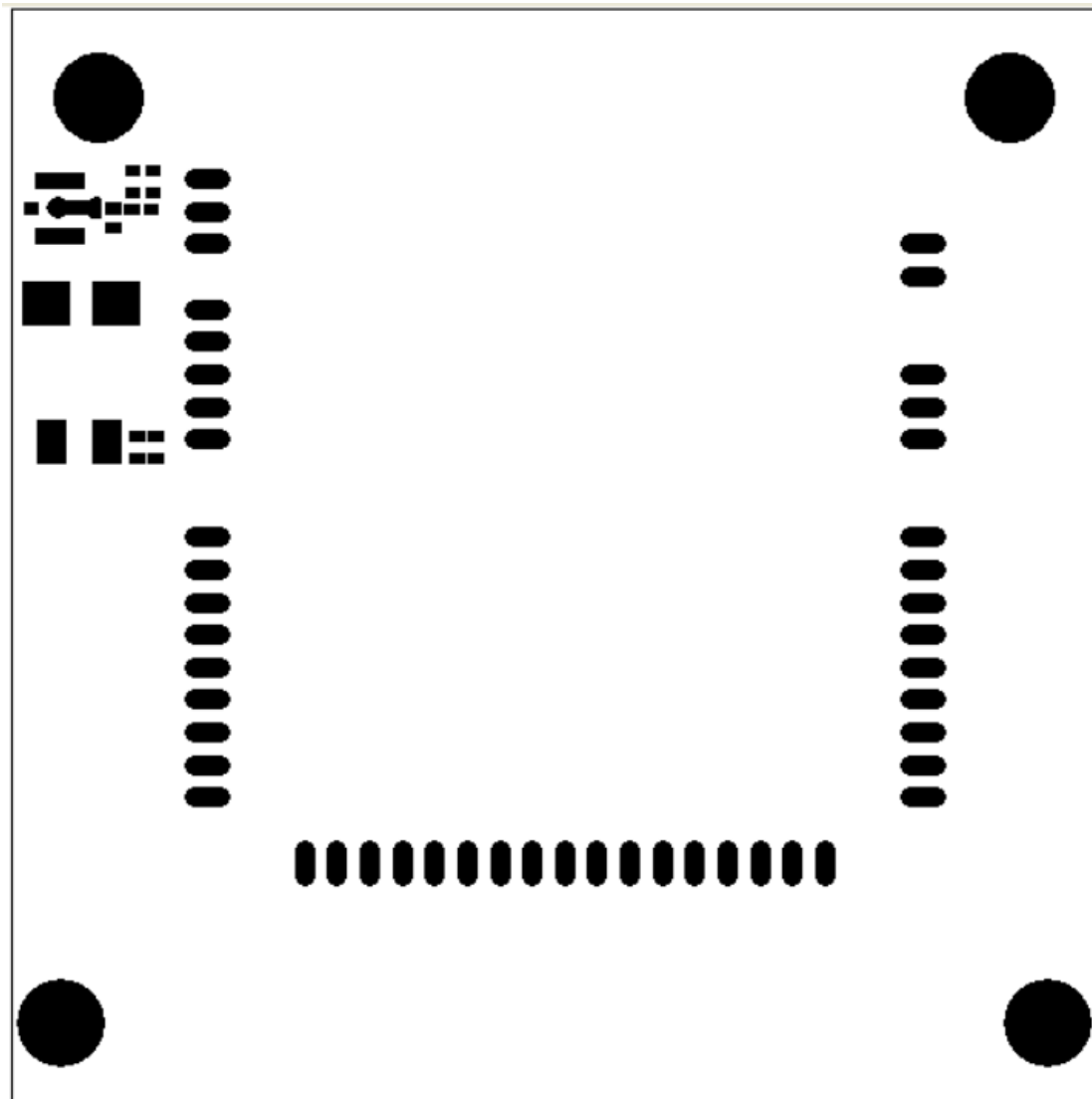
Silkscreen Top



Reference designator Top

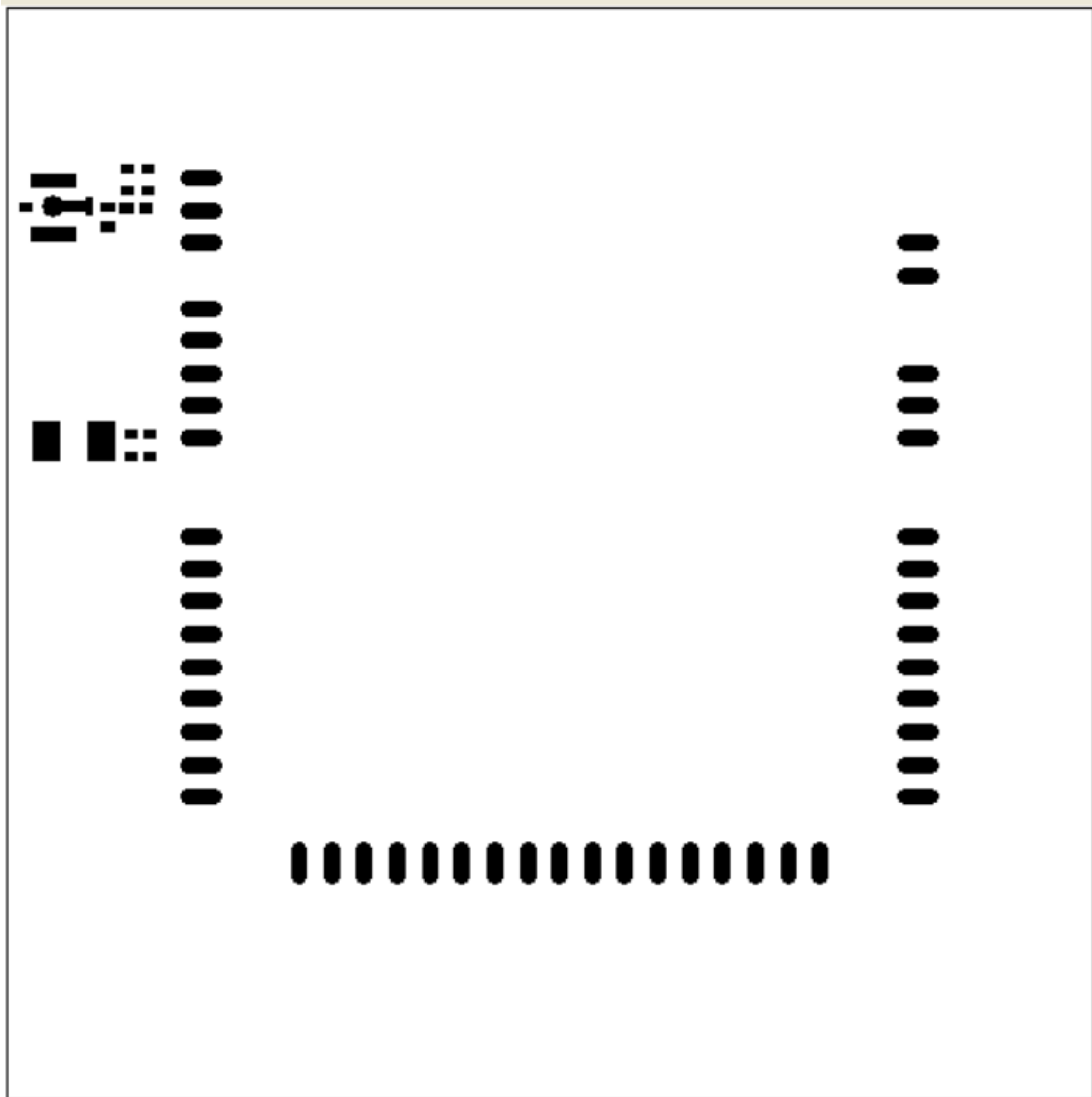


Solder mask Top

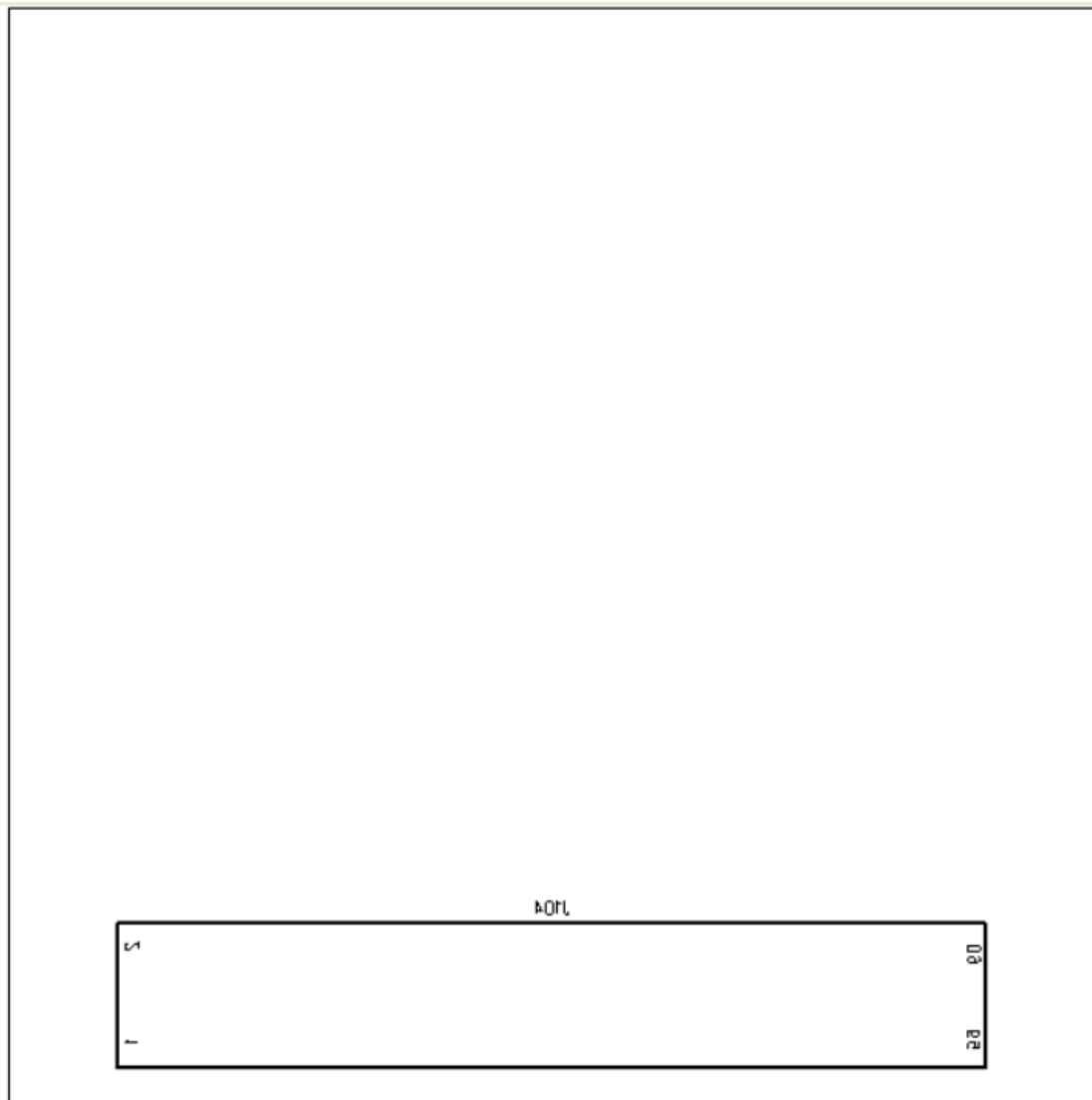




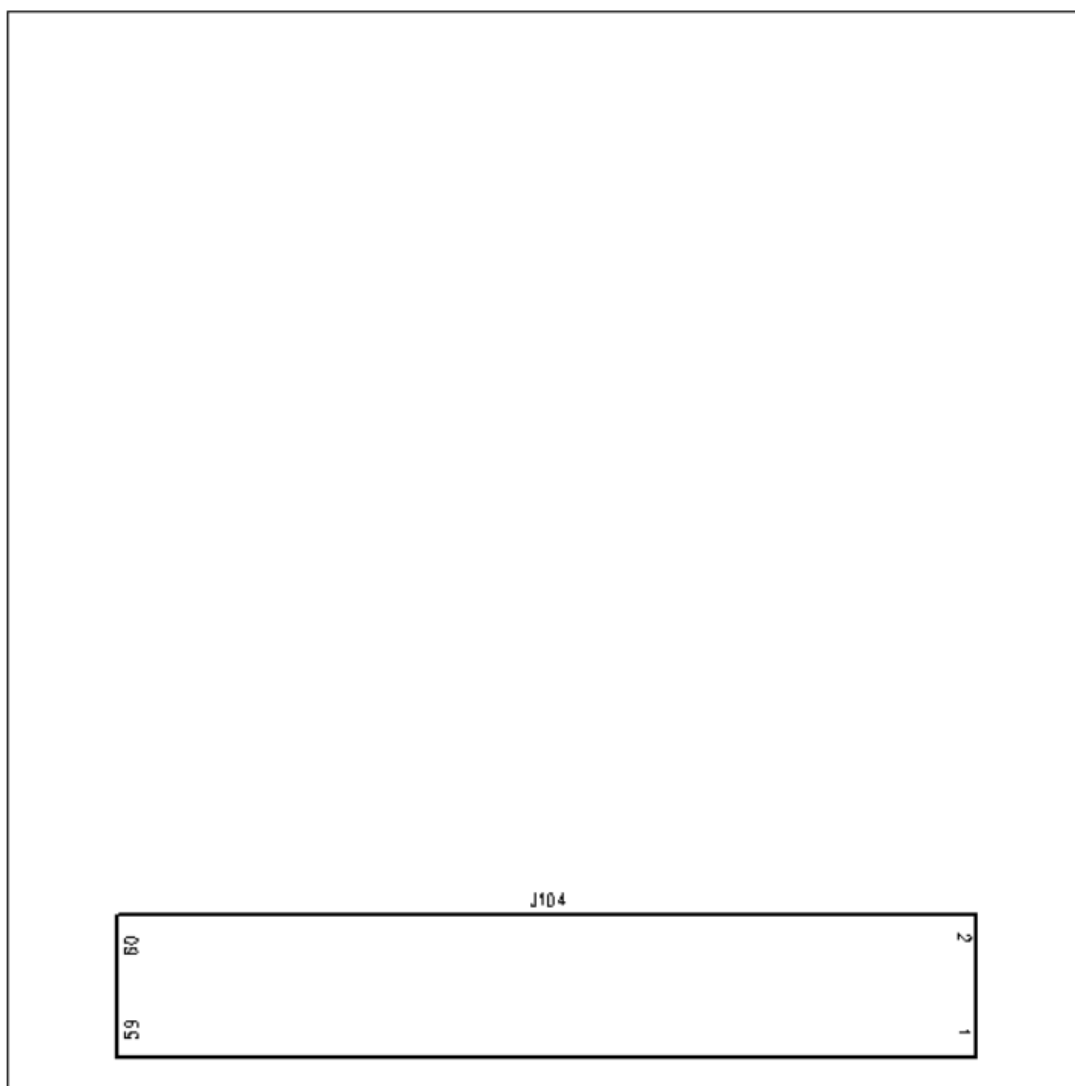
Paste mask Top



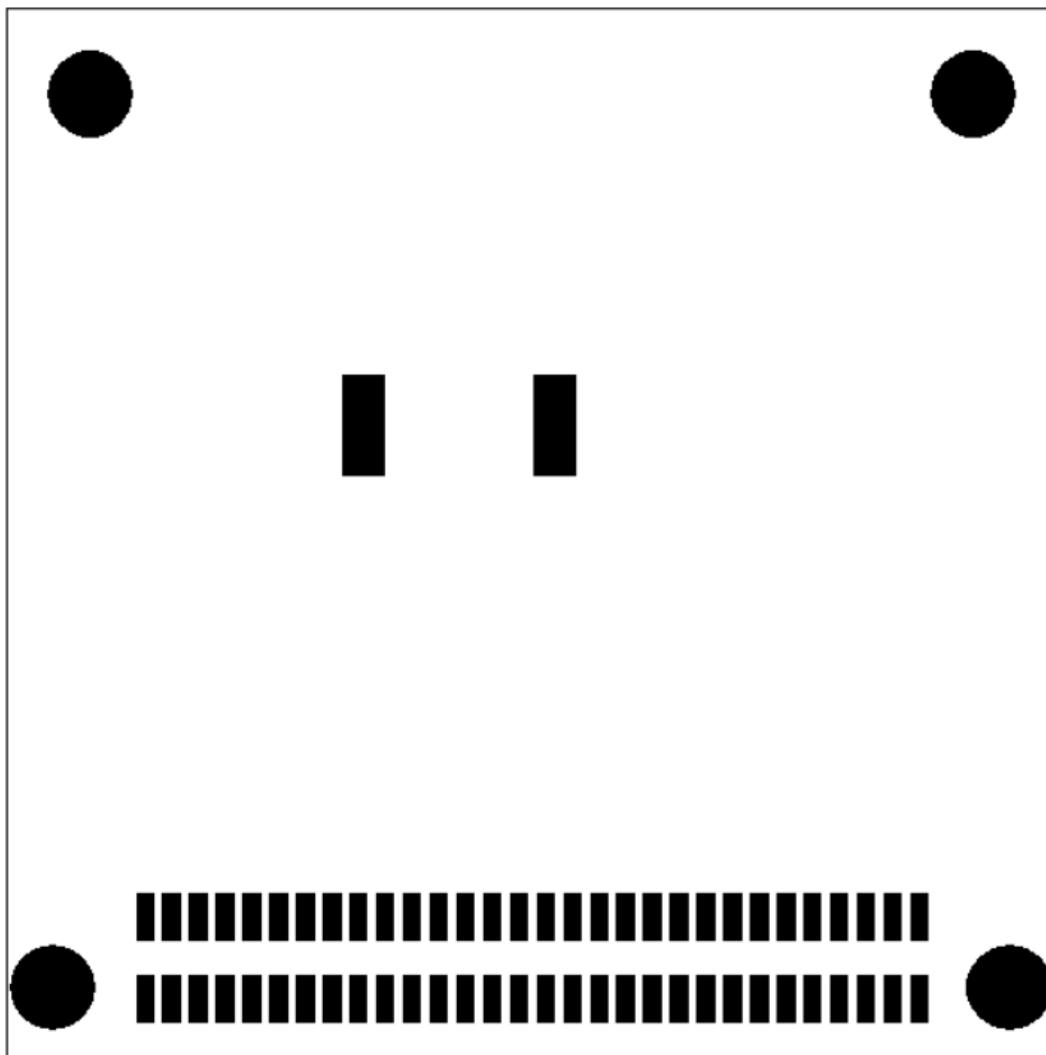
Silkscreen Bottom



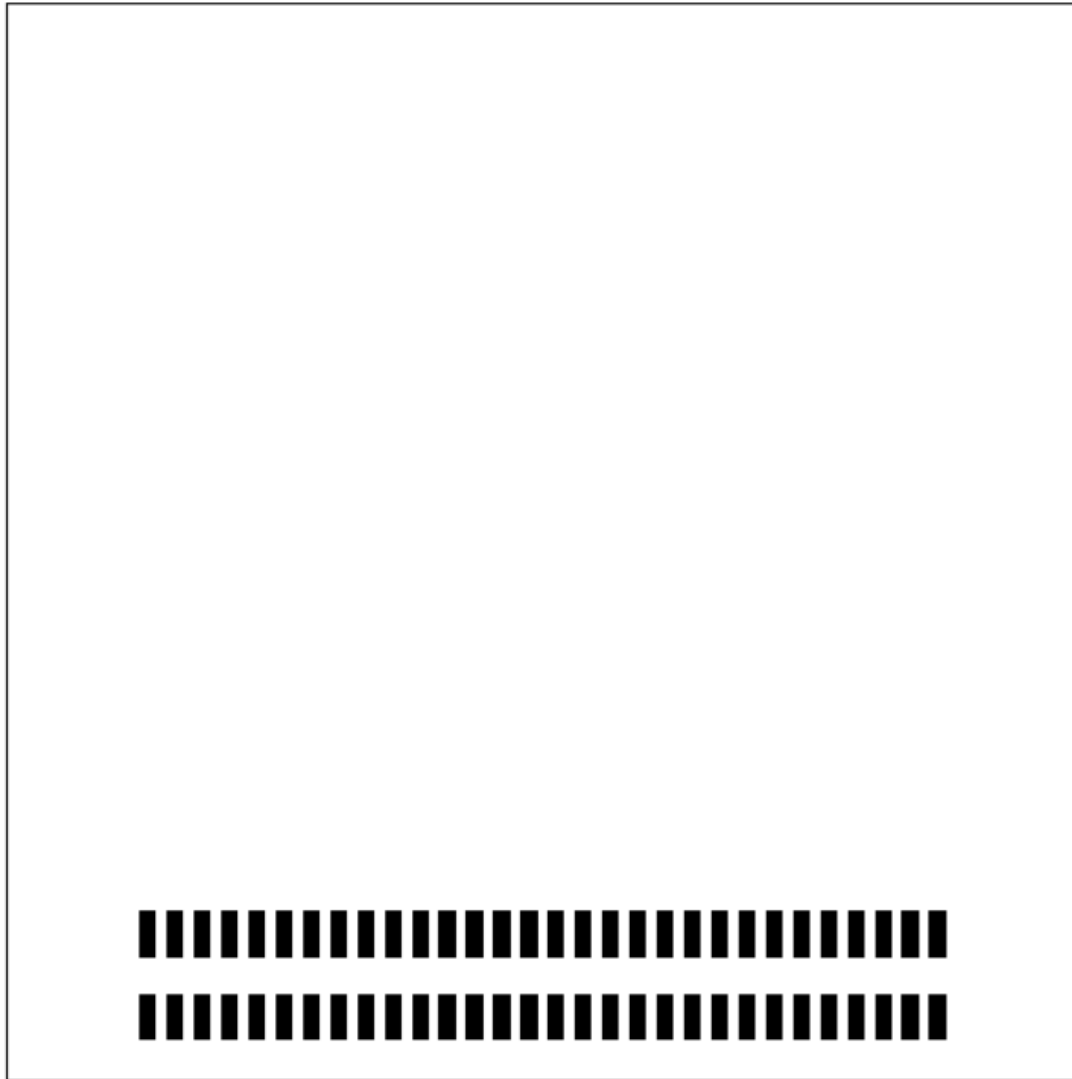
Reference designator Bottom



Solder mask Bottom



Paste mask Bottom



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