

1024MB DDR – unbuffered DDR1 UDIMM

184PIN UDIMM

SDU01G64H3BJ2SA-xxR

1GByte in TSOP Technology

RoHS compliant

Options:

- | | |
|----------------------------------|-------------|
| ▪ Data Rate / Latency | Marking |
| DDR 400 MT/s CL3 | -50 |
| DDR 333 MT/s CL2.5 | -60 |
| | |
| ▪ Module density | |
| 1024MB with 16 dies and 2 ranks | |
| | |
| Standard Grade (T _A) | 0°C to 70°C |

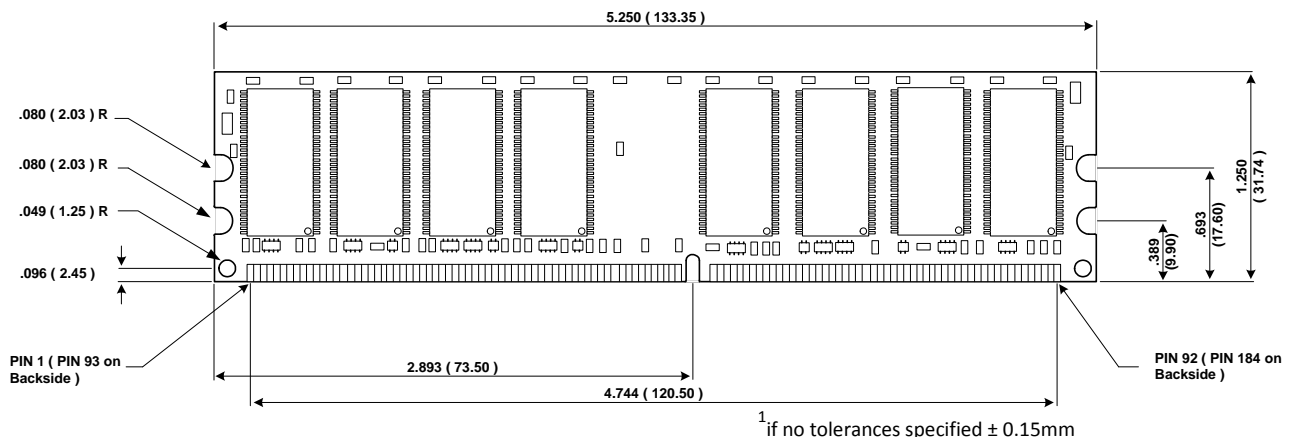
Environmental Requirements:

- Operating temperature (T_A)
Standard Grade 0°C to 70°C
- Operating Humidity
10% to 90% relative humidity, noncondensing
- Operating Pressure
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
-55°C to 100°C
- Storage Humidity
5% to 95% relative humidity, noncondensing
- Storage Pressure
1682 PSI (up to 5000 ft.) at 50°C

Features:

- 184-pin 64-bit unbuffered Dual-In-Line Double Data Rate Synchronous DRAM module
- Module organization: dual rank 128M x 64
- V_{DD} = 2.5V ±0.2V, V_{DDQ} 2.5V ±0.2V
- V_{DD} = 2.6V ±0.1V, V_{DDQ} 2.6V ±0.1V (DDR400)
- 2.5V I/O (SSTL_2 compatible)
- Serial Presence Detect with EEPROM
- Gold-contact pads
- This module is fully pin and functional compatible to the JEDEC PC-3200 spec. and JEDEC-Standard MO-206. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- **DDR-SDRAM component base: Samsung K4H510838J DIE rev. J**
- 64Mx8 DDR1 SDRAM in TSOP66 package
- Internal, pipelined double-data-rate (DDR)
- 2n pre-fetch architecture
- DLL to align DQ and DQS transitions with CK
- Bidirectional data strobe (DQS) transmitted/received with data, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst length: 2,4 or 8
- Adjustable data-output drive strength
- Auto Refresh (CBR) and Self Refresh, 8k Refresh every 64ms

Figure: mechanical dimensions¹



This Swissbit module family is industry standard 184-pin 8-byte Double Data rate synchronous SDRAM Dual-In-line Memory Modules (DIMMs), which are organized as x64 high speed memory arrays designed for use in non-parity applications. DIMMs are assembled in TSOP Technology. The passive devices and the EEPROM are SMD components.

The DIMM use serial presence detects (SPD) implemented via serial EEPROM using the two-pin-I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit DIMMs provide a high performance, flexible 8-byte interface in a 133.35mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

Module Configuration

Organization	DDR SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
128M x 64bit	16 x 64M x 8bit (512Mbit)	13	BA0, BA1	11	8k	S0#, S1#

Module Dimensions in mm
133.35 (long) x 30(high) x 4.00 [max] (thickness)

Product Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SDU01G64H3BJ2SA-50R	1024MB	3.2 GB/s	5.0ns/400MT/s	3.0-3-3
SDU01G64H3BJ2SA-60R	1024MB	2.7 GB/s	6.0ns/333MT/s	2.5-3-3

Pin Name

A0 – A12	Address Inputs
BA0, BA1	Bank Address Inputs
DQ0 – DQ63	Data Input/Output
DM0 – DM7	Input Data Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Read / Write Enable
CKE0 – CKE1	Clock Enable
CK0 – CK1	Clock Inputs, positive line
CK0# – CK1#	Clock Inputs, negative line
DQS0 – DQS7	Data strobes

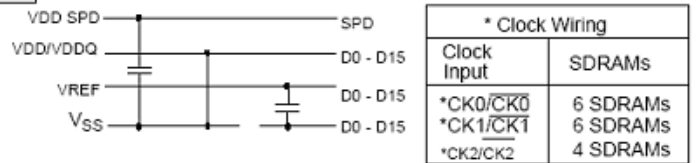
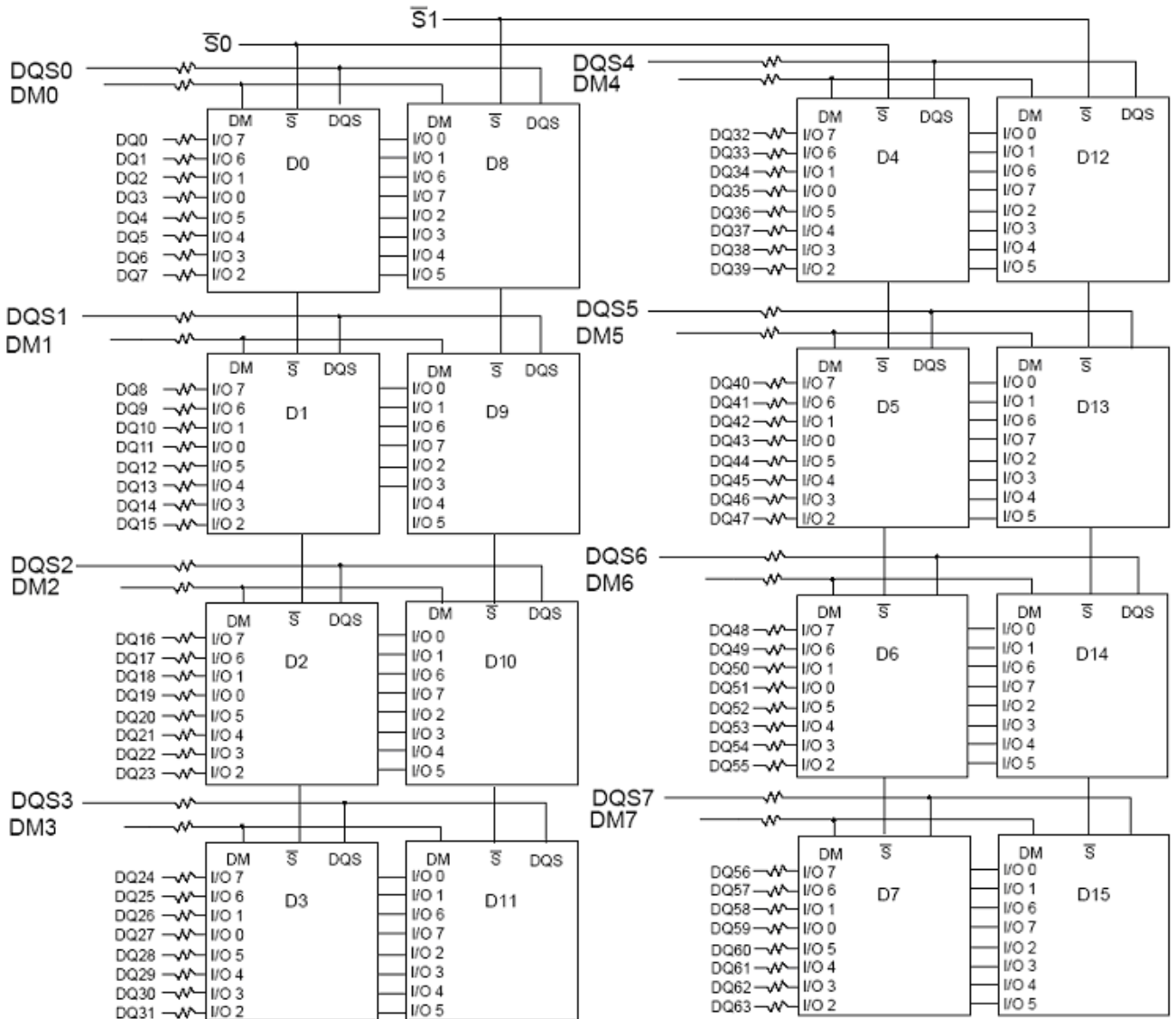
S0# – S1#	Chip Select
V _{DD}	Power (2.5V± 0.2V)
V _{DDQ}	DQ Power (2.5V±0.2V)
V _{DDSPD}	SPD Power
V _{REF}	Input/Output Reference
V _{SS}	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA2	Slave Address Select Bus for Presence Detect
NC	No Connection

Pin Configuration

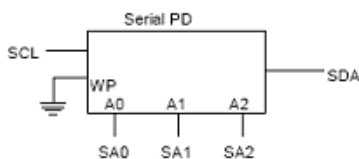
Front Side				Back Side			
PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name
1	V _{REF}	47	DQS8	93	V _{SS}	139	V _{SS}
2	DQ0	48	A0	94	DQ4	140	DM8
3	V _{SS}	49	NC	95	DQ5	141	A10
4	DQ1	50	V _{SS}	96	V _{DDQ}	142	NC
5	DQS0	51	NC	97	DM0	143	V _{DDQ}
6	DQ2	52	BA1	98	DQ6	144	NC
7	V _{DD}	53	DQ32	99	DQ7	145	V _{SS}
8	DQ3	54	V _{DDQ}	100	V _{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	V _{DD}
11	V _{SS}	57	DQ34	103	NC	149	DM4
12	DQ8	58	V _{SS}	104	V _{DDQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V _{SS}
15	V _{DDQ}	61	DQ40	107	DM1	153	DQ44
16	NC	62	V _{DDQ}	108	V _{DD}	154	/RAS
17	NC	63	/WE	109	DQ14	155	DQ45
18	V _{SS}	64	DQ41	110	DQ15	156	V _{DDQ}
19	DQ10	65	/CAS	111	NC	157	/S0
20	DQ11	66	V _{SS}	112	V _{DDQ}	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5
22	V _{DDQ}	68	DQ42	114	DQ20	160	V _{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V _{DD}	116	V _{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC

Front Side				Back Side			
PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name
26	V _{SS}	72	DQ48	118	A11	164	V _{DDQ}
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	V _{SS}	120	V _{DD}	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	V _{DDQ}	76	NC	122	A8	168	V _{DD}
31	DQ19	77	V _{DDQ}	123	DQ23	169	DM6
32	A5	78	DQS6	124	V _{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V _{SS}	80	DQ51	126	DQ28	172	V _{DDQ}
35	DQ25	81	V _{SS}	127	DQ29	173	NC
36	DQS3	82	NC	128	V _{DDQ}	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	V _{DD}	84	DQ57	130	A3	176	V _{SS}
39	DQ26	85	V _{DD}	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	V _{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V _{SS}	88	DQ59	134	NC	180	V _{DDQ}
43	A1	89	V _{SS}	135	NC	181	SA0
44	NC	90	NC	136	V _{DDQ}	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	V _{DD}	92	SCL	138	/CK0	184	V _{DDSPD}

FUNCTIONAL BLOCK DIAGRAM 1024MByte DDR SDRAM DIMM 2RANKS; NON-ECC



- BA0 - BA1 ———— BA0-BA1: SDRAMs D0 - D15
- A0 - A13 ———— A0-A13: SDRAMs D0 - D15
- CKE1 ———— CKE: SDRAMs D9 - D15
- RAS ———— RAS: SDRAMs D0 - D15
- CAS ———— CAS: SDRAMs D0 - D15
- CKE0 ———— CKE: SDRAMs D0 - D7
- WE ———— WE: SDRAMs D0 - D15



DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V _{DD}	2.3	2.7	V
I/O Supply Voltage	V _{DDQ}	2.3	2.7	V
I/O Reference Voltage	V _{REF}	0.49 x V _{DDQ}	0.51x V _{DDQ}	V
I/O Termination Voltage (system)	V _{TT}	V _{REF} - 0.04	V _{REF} + 0.04	V
Input High (Logic 1) Voltage	V _{IH(DC)}	V _{REF} + 0.15	V _{DD} + 0.3	V
Input Low (Logic 0) Voltage	V _{IL(DC)}	-0.3	V _{REF} - 0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ V _{DD} , V _{REF} pin 0V ≤ V _{IN} ≤ 1.35V (All other pins not under test = 0V)	I _I	-10	10	µA
OUTPUT LEAKAGE CURRENT (DQ _S are disabled; 0V ≤ V _{OUT} ≤ V _{DDQ})	I _{OZ}	-10	10	µA
OUTPUT LEVELS: High Current (V _{OUT} = V _{DDQ} -0.373V, minimum V _{REF} , minimum V _{TT})	I _{OH}	-16.8	-	mA
Low Current (V _{OUT} = 0.373V, maximum V _{REF} , maximum V _{TT})	I _{OL}	16.8	-	mA

AC INPUT OPERATING CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	V _{IH(AC)}	V _{REF} + 0.310	-	V
Input Low (Logic 0) Voltage	V _{IL(AC)}	-	V _{REF} - 0.310	V
I/O Reference Voltage	V _{REF(AC)}	0.49 x V _{DDQ}	0.51x V _{DDQ}	V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C ₁₀	4.0	5.0	pF
Input Capacitance: Command and Address	C ₁₁	18.0	27.0	pF
Input Capacitance: /S 0,1	C ₁₁	18.0	27.0	pF
Input Capacitance: CK, /CK	C ₁₂	10.0	14.0	pF
Input Capacitance: CKE	C ₁₃	18.0	27.0	pF

I_{DD} Specifications AND CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

Parameter & Test Condition		max.			
		Symbol	3200-3.0-3-3	2700-2.5-3-3	Unit
OPERATING CURRENT *) : One device bank; Active-Precharge; t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I _{DD0}	1000	880	mA
OPERATING CURRENT :*) One device bank; Active-Read-Precharge; Burst = 2; t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle		I _{DD1}	1440	1120	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; t _{CK} = t _{CK} (Min); CKE = (LOW)		I _{DD2P}	80	80	mA
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; t _{CK} = t _{CK} (Min); CKE = HIGH; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS, and DM		I _{DD2F}	480	480	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; t _{CK} = t _{CK} (Min); CKE = LOW		I _{DD3P}	720	480	mA
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; t _{RC} = t _{RAS} (Max); t _{CK} = t _{CK} (Min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I _{DD3N}	960	720	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (Min); I _{OUT} = 0mA		I _{DD4R}	3000	1160	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (Min); DQ, DM, and DQS inputs changing twice per clock cycle		I _{DD4W}	1440	1240	mA
AUTO REFRESH CURRENT	t _{RC} = t _{RC} (Min)	I _{DD5}	3520	3280	mA
	t _{RC} = 7.8125μs	I _{DD6}	80	80	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V		I _{DD7}	48	48	mA
OPERATING CURRENT*): Four device bank interleaving READs (BL = 4) with auto precharge, t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); Address and control inputs change only during Active READ, or WRITE commands		I _{DD8}	3080	2920	mA

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

AC CHARACTERISTICS		3200-3.0-3-3		2700-2.5-3-3		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
Access window of DQ _s CK/CK#	t _{AC}	-0.50	+0.50	-0.70	+0.70	ns
CK high-level width	t _{CH}	0.45	0.55	0.45	0.55	t _{CK}
CK low-level width	t _{CL}	0.45	0.55	0.45	0.55	t _{CK}
Clock cycle time	CL=2.0	T _{CK(2.0)}	7.5	13.0	7.5	13.0
	CL=2.5	T _{CK(2.5)}	6.0	13.0	6.0	13.0
	CL=3.0	T _{CK(3.0)}	5.0	13.0	-	-
DQ and DM input hold time relative to DQS	t _{DH}	0.40	-	0.45	-	ns
DQ and DM input setup time relative to DQS	t _{DS}	0.40	-	0.45	-	ns
DQ and DM input pulse width (for each input)	t _{DIPW}	1.75	-	1.75	-	ns
Access window of DQS from CK/CK#	t _{DQSCK}	-0.6	+0.6	-0.6	+0.6	ns
DQS input high pulse width	t _{DQSH}	0.35	-	0.35	-	t _{CK}
DQS input low pulse width	t _{DQSL}	0.35	-	0.35	-	t _{CK}
DQS -DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}	-	0.40	-	0.45	ns
Write command to first DQS latching transition	t _{DQSS}	0.72	1.28	0.75	1.25	t _{CK}
DQS falling edge to CK rising- setup time	t _{DSS}	0.2	-	0.2	-	t _{CK}
DQS falling edge from CK rising- hold time	t _{DSH}	0.2	-	0.2	-	t _{CK}
Half clock period	t _{HP}	t _{ch} , t _{cl}	-	t _{ch} , t _{cl}	-	ns
Data-out high-impedance window from CK/CK#	t _{HZ}		+0.7		+0.7	ns
Data-out low-impedance window from CK/CK#	t _{LZ}	-0.7	-	-0.7	-	ns
Address and control input hold time (fast slew rate)	t _{IHF}	0.6	-	0.75	-	ns
Address and control input setup time (fast slew rate)	t _{ISF}	0.6	-	0.75	-	ns
Address and control input hold time (slow slew rate)	t _{IHS}	0.7	-	0.8	-	ns
Address and control input setup time (slow slew rate)	t _{ISS}	0.6	-	0.8	-	ns
LOAD MODE REGISTER command cycle time	t _{MRD}	10	-	12	-	ns
Adress and control input pulse width (for each input)	t _{IPW}	2.2	-	2.2	-	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ns
Data hold skew factor	t _{QHS}	-	0.5	-	0.6	ns

AC CHARACTERISTICS		3200-3.0-3-3		2700-2.5-3-3		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit
ACTIVE to PRECHARGE command	t_{RAS}	40	70.000	42	70.000	ns
ACTIVE to READ with Auto precharge command	t_{RAP}	15	-	15	-	ns
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}	55	-	60	-	ns
AUTO REFRESH command period	t_{RFC}	70	-	72	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	15	-	ns
PRECHARGE command period	t_{RP}	15	-	15	-	ns
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	10	-	12	-	ns
DQS write preamble	t_{WPRE}	0.25	-	0.25	-	t_{CK}
DQS write preamble setup time	t_{WPRES}	0	-	0	-	ns
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Write recovery time	t_{WR}	15	-	15	-	ns
Internal WRITE to READ command delay	t_{WTR}	2	-	1	-	t_{CK}
Data valid output window	N/A	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns
REFRESH to REFRESH command interval	t_{REFC}	-	70.3	-	70.3	μs
Average periodic refresh interval $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$	t_{REFI}	-	7.8	-	7.8	μs
$85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$	$t_{REFI(IT)}$	-	3.9	-	3.9	μs
Terminating voltage delay to V_{DD}	t_{VTD}	0	-	0	-	ns
Exit SELF REFRESH to non-READ command	t_{XSNR}	70	-	75	-	ns
Exit SELF REFRESH to READ command	t_{XSRD}	200	-	200	-	t_{CK}

Note 1: Values for AC timing, IDD, and electrical AC and DC characteristics might have been collected within the standard temperature range and at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified and for the corresponding field of operation according to the actual temperature grade of the module (extended E, I or W; refer to the environmental conditions for more details).

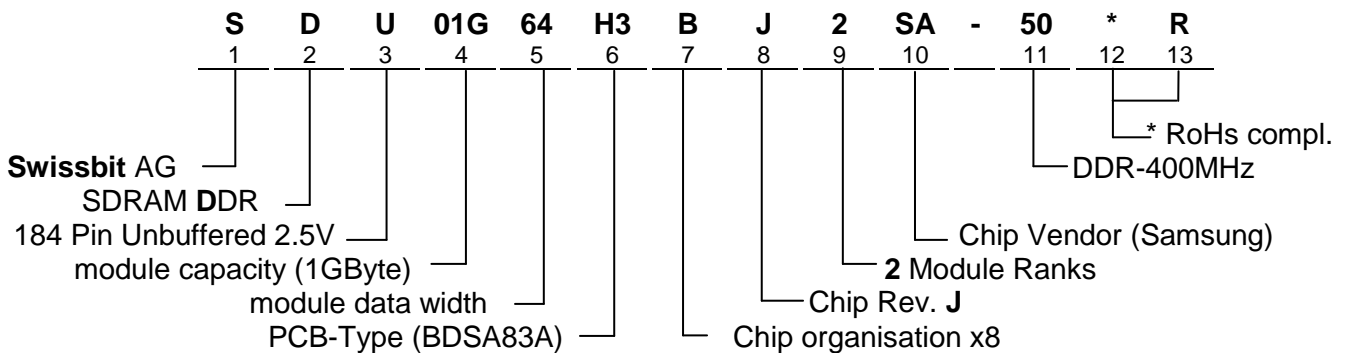
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	3200-3.0-3-3	2700-2.5-3-3
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x07	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0D	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0B	
5	NUMBER OF PHYSICAL BANKS ON DIMM	0x02	
6	MODULE DATA WIDTH	0x40	
7	MODULE DATA WIDTH (continued)	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS (V _{DDQ})	0x04	
9	SDRAM CYCLE TIME, (t _{CK}) (CAS LATENCY =2.5 (2700, 2100) ; CL=3* (3200))	0x50	0x60
10	SDRAM ACCESS FROM CLOCK, (t _{AC}) (CAS LATENCY =2.5 (2700, 2100); CL=3* (3200))	0x65	0x70
11	MODULE CONFIGURATION TYPE	0x00	
12	REFRESH RATE/ TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00	
15	MINIMUM CLOCK DELAY, BACK- TO- BACK RANDOM COLUMN ACCESS	0x01	
16	BURST LENGTHS SUPPORTED	0x0E	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x04	
18	CAS LATENCIES SUPPORTED	0x18	0x0C
19	CS LATENCY	0x01	
20	WE LATENCY	0x02	
21	SDRAM MODULE ATTRIBUTES	0x20	
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0xC0	
23	SDRAM CYCLE TIME, (t _{CK}) (CAS LATENCY=2(2700, 2100) CL=2.5*(3200))	0x60	0x75
24	SDRAM ACCESS FROM CK, (t _{AC}) (CAS LATENCY=2(2700, 2100) CL=2.5*(3200))	0x70	
25	SDRAM CYCLE TIME, (t _{CK}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200))	0x00	
26	SDRAM ACCESS FROM CK, (t _{AC}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200))	0x00	
27	MINIMUM ROW PRECHARGE TIME, (t _{RP})	0x3C	0x48
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t _{RRD})	0x28	0x30
29	MINIMUM RAS# TO CAS# DELAY, (t _{RCD})	0x3C	0x48
30	MINIMUM RAS# PULSE WIDTH, (t _{RAS})	0x28	0x2A
31	MODULE BANK DENSITY	0x80	
32	ADDRESS AND COMMAND SETUP TIME, (t _{IS})	0x60	0x80
33	ADDRESS AND COMMAND HOLD TIME, (t _{IH})	0x60	0x80
34	DATA/DATA MASK INPUT SETUP TIME, (t _{DS})	0x40	0x45
35	DATA/DATA MASK INPUT HOLD TIME, (t _{DH})	0x40	0x45
36-40	RESERVED	0x00	
41	MIN ACTIVE AUTO REFRESH TIME (t _{RC})	0x37	0x3C
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (t _{RFC})	0x46	0x48
43	SDRAM DEVICE MAX CYCLE TIME (t _{CKMAX})	0x28	0x30
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME (t _{DQSQ})	0x28	0x2D
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR (t _{QHS})	0x50	0x55

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	3200-3.0-3-3	2700-2.5-3-3
46-61	RESERVED	0x00	
62	SPD REVISION	0x11	
63	CHECKSUM FOR BYTES 0-62	0xC0	0x69
64	MANUFACTURER`S JEDEC ID CODE	7F	
65	MANUFACTURER`S JEDEC ID CODE	7F	
66	MANUFACTURER`S JEDEC ID CODE	7F	
67	MANUFACTURER`S JEDEC ID CODE (continued)	DA	
72	MANUFACTURING LOCATION	0x01	Switzerland
		0x02	Germany
		0x03	USA
73-90	MODULE PART NUMBER (ASCII)	"SDU01G64H3BJ2SA-xx"	
91	PCB IDENTIFICATION CODE	x	
92	IDENTIFICATION CODE (continued)	x	
93	YEAR OF MANUFACTURE IN BCD	x	
94	WEEK OF MANUFACTURE IN BCD	x	
95-98	MODULE SERIAL NUMBER	x	x

Part Number Code



* optional / additional information

Revision History		
Revision	Changes	Date
1.0	Initial Revision	18.09.2012

Locations

Swissbit AG

Industriestrasse 4

CH – 9552 Bronschhofen

Switzerland

Phone: +41 (0)71 913 03 03

Fax: +41 (0)71 913 03 15

Swissbit Germany GmbH

Wolfener Strasse 36

D – 12681 Berlin

Germany

Phone: +49 (0)30 93 69 54 – 0

Fax: +49 (0)30 93 69 54 – 55

Swissbit NA, Inc.

1202 E. Winding Creek Drive

Eagle, ID 83616

USA

Phone: +1 208 870 4525

Fax: +1 208 870 4525

Swissbit Japan, Inc.

3F Core Koenji,

2-1-24 Koenji-Kita, Suginami-Ku,

Tokyo 166-0002

Japan

Phone: +81 3 5356 3511

Fax: +81 3 5356 3512