

S70GL-P MirrorBit® Flash

S70GL02GP

2 Gigabit, 3.0 Volt-only Page Mode Flash Memory
featuring 90 nm MirrorBit Process Technology

Data Sheet



Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See [Notice On Data Sheet Designations](#) for definitions.

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

“This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice.”

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

“This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications.”

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

“This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur.”

Questions regarding these document designations may be directed to your local sales office.

S70GL-P MirrorBit® Flash

S70GL02GP

2 Gigabit, 3.0 Volt-only Page Mode Flash Memory
featuring 90 nm MirrorBit Process Technology



Data Sheet

General Description

The Spansion S70GL02GP 2-Gigabit Mirrorbit Flash memory device is fabricated on 90 nm process technology. This device offers a fast page access time of 25 ns with a corresponding random access time of 110 ns. It features a Write Buffer that allows a maximum of 32 words/64 bytes to be programmed in one operation, resulting in faster effective programming time than standard single byte/word programming algorithms. This makes the device an ideal product for today's embedded applications that require higher density, better performance and lower power consumption.

Distinctive Characteristics

- **Two 1024 Megabit (S29GL01GP) in a single 64-ball Fortified-BGA package** ([see publication S29GL-P_00 for full specifications](#))
- **Single 3V read/program/erase (3.0V - 3.6V)**
- **90 nm MirrorBit process technology**
- **8-word/16-byte page read buffer**
- **32-word/64-byte write buffer reduces overall programming time for multiple-word writes**
- **Secured Silicon Sector region**
 - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number
 - Can be programmed and locked at the factory or by the customer
- **Uniform 64Kword/128KByte Sector Architecture**
 - S70GL02GP: two thousand forty-eight sectors
- **100,000 erase cycles per sector typical**
- **20-year data retention typical**
- **Offered Packages**
 - 64-ball Fortified BGA
- **Suspend and Resume commands for Program and Erase operations**
- **Write operation status bits indicate program and erase operation completion**
- **Unlock Bypass Program command to reduce programming time**
- **Support for CFI (Common Flash Interface)**
- **Persistent and Password methods of Advanced Sector Protection**
- **WP#/ACC input**
 - Accelerates programming time (when V_{ACC} is applied) for greater throughput during system production
 - Protects first or last sector of each die, regardless of sector protection settings
- **Hardware reset input (RESET#) resets device**
- **Ready/Busy# output (RY/BY#) detects program or erase cycle completion**

Performance Characteristics

Max. Read Access Times (ns) (Note 1)	
Parameter	2 Gb
Random Access Time (t_{ACC})	110
Page Access Time (t_{PACC})	25
CE# Access Time (t_{CE})	110
OE# Access Time (t_{OE})	25

Notes

1. Access times are dependent on V_{CC} and V_{IO} operating ranges. See [Ordering Information on page 6](#) for further details.
2. Contact a sales representative for availability.

Current Consumption (typical values)	
Random Access Read	30 mA
8-Word Page Read	1 mA
Program/Erase	50 mA
Standby	2 μ A

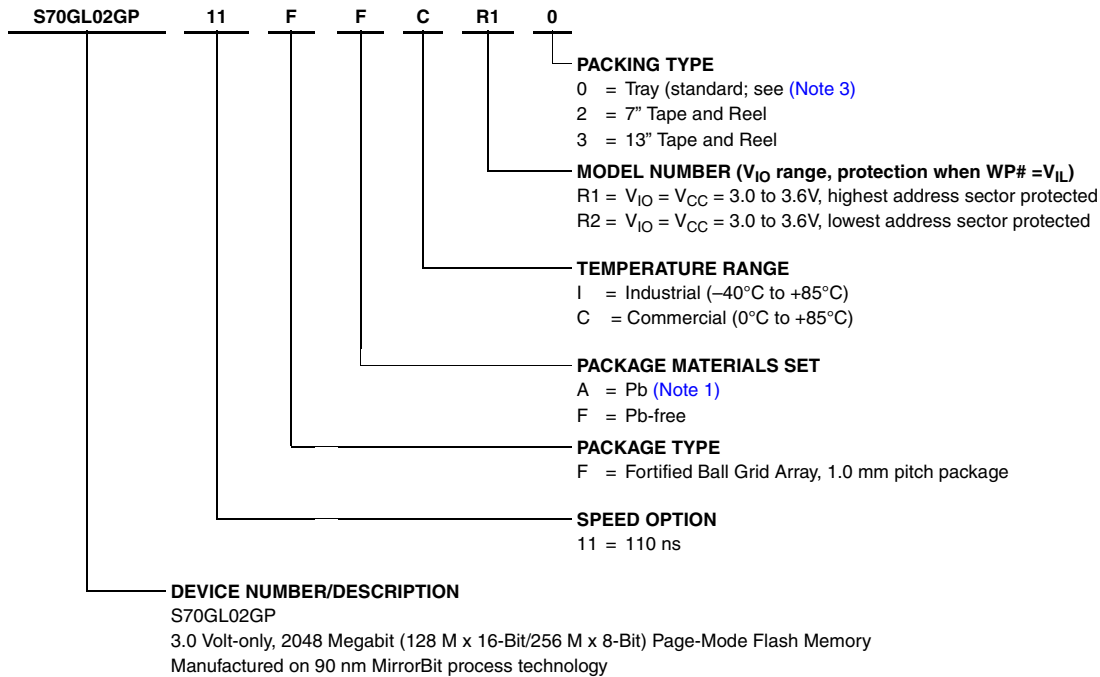
Program & Erase Times (typical values)	
Single Word Programming	60 μ s
Effective Write Buffer Programming (V_{CC}) Per Word	15 μ s
Effective Write Buffer Programming (V_{ACC}) Per Word	15 μ s
Sector Erase Time (64 Kword Sector)	0.5 s

Table of Contents

General Description	3
Distinctive Characteristics	3
Performance Characteristics	4
1. Ordering Information	6
1.1 Recommended Combinations	6
2. Input/Output Descriptions & Logic Symbol	7
2.1 Special Handling Instructions for BGA Package	8
2.2 LSE064—64 ball Fortified Ball Grid Array, 13 x 11 mm	9
3. Memory Map	10
4. Autoselect	10
5. Erase And Programming Performance	10
6. BGA Package Capacitance	11
7. Revision History	12

1. Ordering Information

The ordering part number is formed by a valid combination of the following:



1.1 Recommended Combinations

Recommended Combinations table below list various configurations planned to be available in volume. The table below will be updated as new combinations are released. Check with your local sales representative to confirm availability of specific configuration not listed or to check on newly released combinations.

S29GL-P Recommended Combinations (Note 1)					
Base OPN	Speed (ns)	Package & Temperature	Model Number	Packing Type	Ordering Part Number (x = Packing Type)
S70GL02GP	110	FFC, FAC (Note 2)	R1, R2	0, 2, 3 (Note 3)	S70GL02GP11FFCR1x S70GL02GP11FFCR2x S70GL02GP11FACR1x S70GL02GP11FACR2x

Notes

- Contact a local sales representative for availability.
- BGA package marking omits leading "S29" and packing type designator from ordering part number.
- Packing Type "0" is standard option.

2. Input/Output Descriptions & Logic Symbol

Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions

Symbol	Type	Description
A26–A0	Input	Address lines for GL02GP
DQ14–DQ0	I/O	Data input/output.
DQ15/A-1	I/O	DQ15: Data input/output in word mode. A-1: LSB address input in byte mode.
CE#	Input	Chip Enable.
OE#	Input	Output Enable.
WE#	Input	Write Enable.
V _{CC}	Supply	Device Power Supply.
V _{IO}	Supply	Versatile IO Input.
V _{SS}	Supply	Ground.
RY/BY#	Output	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V _{IL} , the device is actively erasing or programming. At High Z, the device is in ready.
BYTE#	Input	Selects data bus width. At V _{IL} , the device is in byte configuration and data I/O pins DQ0–DQ7 are active. At V _{IH} , the device is in word configuration and data I/O pins DQ0–DQ15 are active.
RESET#	Input	Hardware Reset. Low = device resets and returns to reading array data.
WP#/ACC	Input	Write Protect/Acceleration Input. At V _{IL} , disables program and erase functions in the outermost sectors. At V _{HH} , accelerates programming; automatically places device in unlock bypass mode. Should be at V _{IH} for all other conditions.
NC	No Connect	Not connected internally.

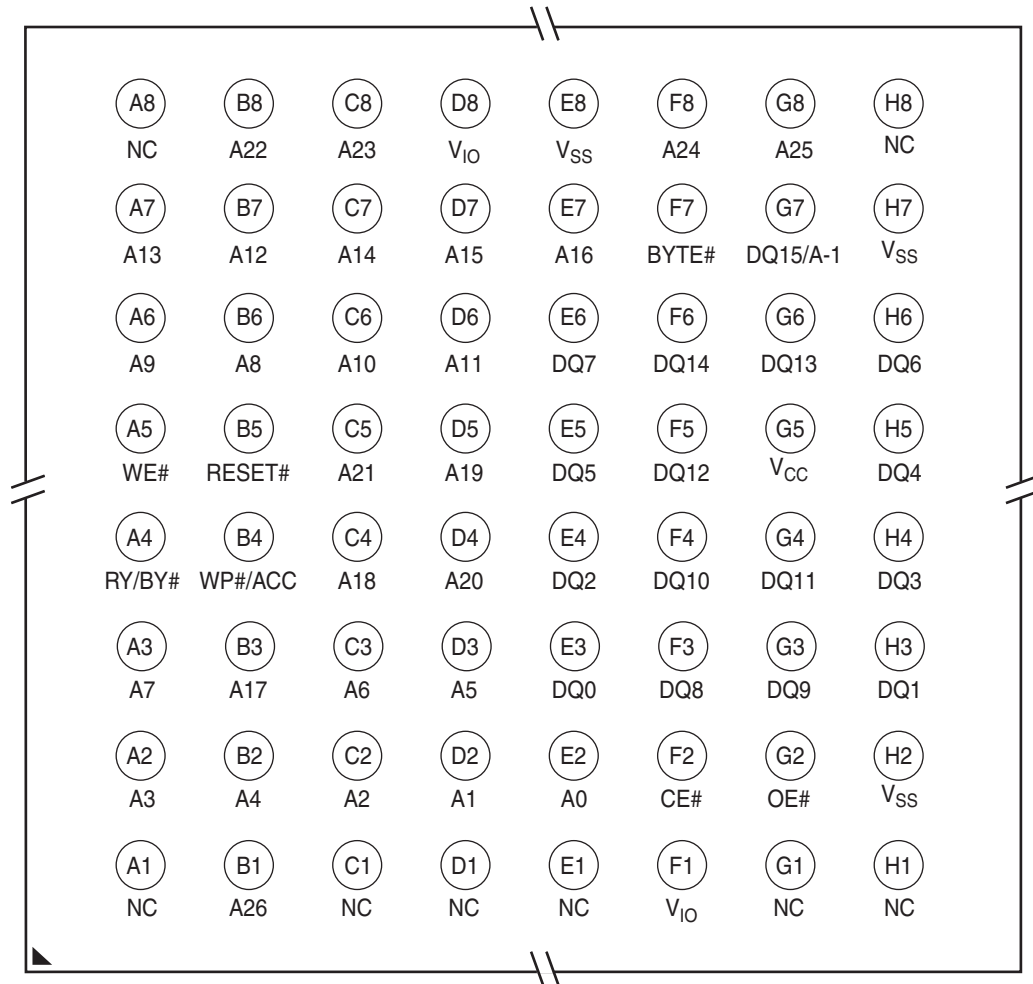
2.1 Special Handling Instructions for BGA Package

Special handling is required for Flash Memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

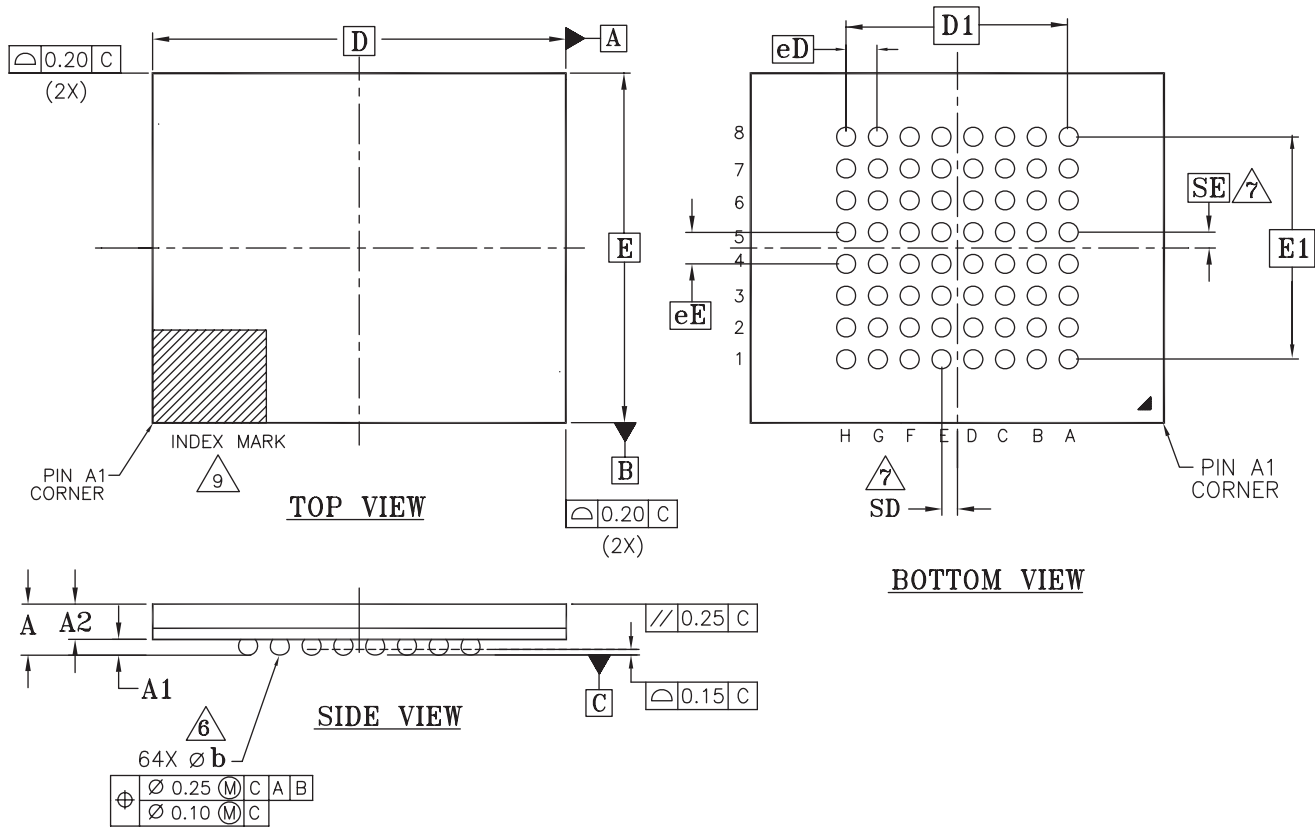
Figure 2.1 64-ball Fortified Ball Grid Array

64-ball Fortified BGA
Top View, Balls Facing Down



2.2 LSE064—64 ball Fortified Ball Grid Array, 13 x 11 mm

Figure 2.2 LSE064—64-ball Fortified Ball Grid Array (FBGA), 13 x 11 mm



PACKAGE	LSE 064			NOTE
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.40	---	---	BALL HEIGHT
A2	0.79	---	0.91	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	64			BALL COUNT
∅b	0.50	0.60	0.70	BALL DIAMETER
eE	1.00 BSC.			BALL PITCH
eD	1.00 BSC.			BALL PITCH
SD / SE	0.50 BSC.			SOLDER BALL PLACEMENT
	---			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]

8 "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3. Memory Map

The S70GL02GP consist of uniform 64 Kword (128 Kb) sectors organized as shown in [Table 3.1](#).

Table 3.1 S70GL02GP Sector & Memory Address Map

Uniform Sector Size	Sector Count	Sector Range	Address Range (16-bit)	Notes
64 Kword/128 Kb	2048	SA00	0000000h–000FFFFh	Sector Starting Address
		:	:	
		SA2047	7FF0000H–7FFFFFFFh	Sector Ending Address

Note

This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001-SA2046) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 Kb sectors have the pattern xxx0000h-xxxFFFFh.

4. Autoselect

[Table 4.1](#) provides the device identification codes for the S70GL02GP. For more information on the autoselect function, refer to the S29GL-P data sheet (publication number S29GL-P_00).

Table 4.1 Autoselect Addresses in System

Description	Address	Read Data (word/byte mode)
Manufacturer ID	(Base) + 00h	xx01h/1h
Device ID, Word 1	(Base) + 01h	227Eh/7Eh
Device ID, Word 2	(Base) + 0Eh	2248h/48h
Device ID, Word 3	(Base) + 0Fh	2201h/01h
Secure Device Verify	(Base) + 03h	For S70GL02GPH: XX19h/19h = Not Factory Locked. XX99h/99h = Factory Locked. For S70GL02GPL: XX09h/09h = Not Factory Locked. XX89h/89h = Factory Locked.
Sector Protect Verify	(SA) + 02h	xx01h/01h = Locked, xx00h/00h = Unlocked

5. Erase And Programming Performance

Table 5.1 Erase And Programming Performance

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 3)
Chip Erase Time	S70GL02GP	1024	4096	
Total Write Buffer Time, for 64 bytes	480		µs	Excludes system level overhead (Note 4)
Total Accelerated Write Buffer Programming Time, for 64 bytes	432		µs	
Chip Program Time	S70GL02GP	1968	sec	

Notes

1. Typical program and erase times assume the following conditions: 25°C, 3.6 V V_{CC}, 10,000 cycles, checkerboard pattern.
2. Under worst case conditions of -40°C, V_{CC} = 3.0 V, 100,000 cycles.
3. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
4. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command.

6. BGA Package Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	20	24	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	16	20	pF
RESET#, WP#/ACC	Separated Control Pin	$V_{IN} = 0$	84	90	pF
CE#	Separated Control Pin	$V_{IN} = 0$	44	50	pF

Notes

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$.

7. Revision History

Section	Description
Revision 01 (December 4, 2006)	
	Initial Release.
Revision 02 (May 19, 2008)	
Global	Changed data sheet designation Added Product Life-cycle notice Removed Table of Figures and Table of Tables
Ordering Information	- Changed sample OPN - Added Commercial temperature range - Changed configuration in "Device Number/description" - Modified "Recommended Combination" table & removed TSOP package option
Erase And Program Performance	Chip Program Time: removed comment
Common Flash Memory Interface	Removed section (see publication S29GL-P_00 for details)
Revision 03 (February 23, 2010)	
Global	Updated available model options. Corrected Chip Program Time.

Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

Trademarks and Notice

The contents of this document are subject to change without notice. This document may contain information on a Spansion product under development by Spansion. Spansion reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Spansion assumes no liability for any damages of any kind arising out of the use of the information in this document.

Copyright © 2006-2010 Spansion Inc. All rights reserved. Spansion®, the Spansion logo, MirrorBit®, MirrorBit® Eclipse™, ORNAND™, EcoRAM™ and combinations thereof, are trademarks and registered trademarks of Spansion LLC in the United States and other countries. Other names used are for informational purposes only and may be trademarks of their respective owners.