

PENTA TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This 5 TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V. This TVS array offers an integrated solution to protect up to 5 data lines where the board space is a premium.

SPECIFICATION FEATURES

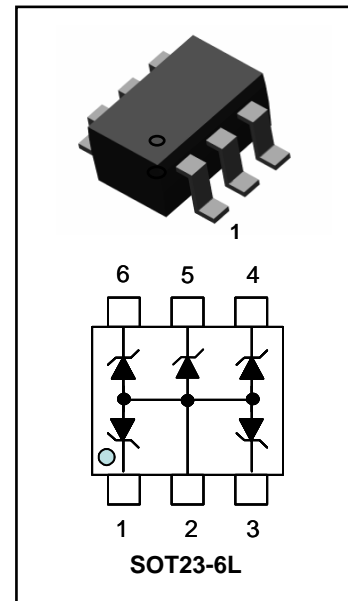
- 350W Power Dissipation (8/20µs Waveform)
- Low Leakage Current, Maximum of 5µA at rated voltage
- Very Low Clamping Voltage
- IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance
- Industry Standard Surface Mount Package SOT23-6L
- 100% Tin Matte Finish (RoHS Compliant)

APPLICATIONS

- Personal Digital Assistant (PDA)
- SIM Card Port Protection (Mobile Phone)
- Portable Instrumentation
- Mobile Phones and Accessories
- Memory Card Port Protection

MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	350	W
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-50 to +125	°C
Storage Temperature Range	T_{stg}	-50 to +150	°C



Device	Marking Code
PJSMS05C	MD5
PJSMS12C	MA2
PJSMS15C	MA5
PJSMS24C	MB4

ELECTRICAL CHARACTERISTICS (Per Device) $T_j = 25^\circ\text{C}$

PJSMS05C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1\text{mA}$	6			V
Reverse Leakage Current	I_R	$V_R = 5\text{V}$			5	µA
Clamping Voltage (8/20µs)	V_C	$I_{pp} = 5\text{A}$			9.5	V
Clamping Voltage (8/20µs)	V_C	$I_{pp} = 24\text{A}$			13	V
Off State Junction Capacitance	C_j	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 2			200	pF
Off State Junction Capacitance	C_j	5 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 2			110	pF



ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMS12C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1mA$	13.3			V
Reverse Leakage Current	I_R	$V_R = 12V$			5	μA
Clamping Voltage (8/20 μs)	V_C	$I_{pp} = 5A$			17	V
Clamping Voltage (8/20 μs)	V_C	$I_{pp} = 15A$			21	V
Off State Junction Capacitance	C_j	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			90	pF

PJSMS15C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1mA$	16.7			V
Reverse Leakage Current	I_R	$V_R = 15V$			5	μA
Clamping Voltage (8/20 μs)	V_C	$I_{pp} = 5A$			22	V
Clamping Voltage (8/20 μs)	V_C	$I_{pp} = 12A$			27	V
Off State Junction Capacitance	C_j	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			70	pF

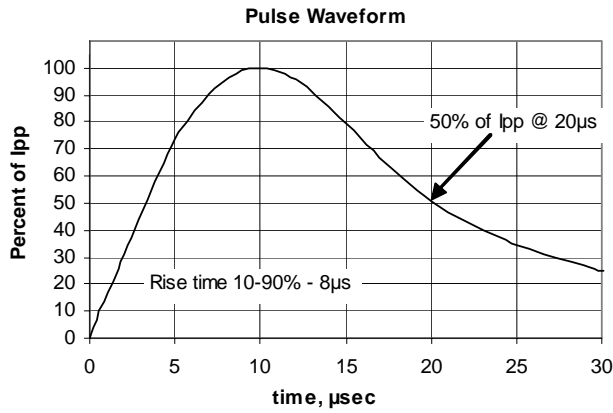
PJSMS24C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1mA$	26.7			V
Reverse Leakage Current	I_R	$V_R = 24V$			5	μA
Clamping Voltage (8/20 μs)	V_C	$I_{pp} = 5A$			35	V
Clamping Voltage (8/20 μs)	V_C	$I_{pp} = 8A$			40	V
Off State Junction Capacitance	C_j	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			50	pF

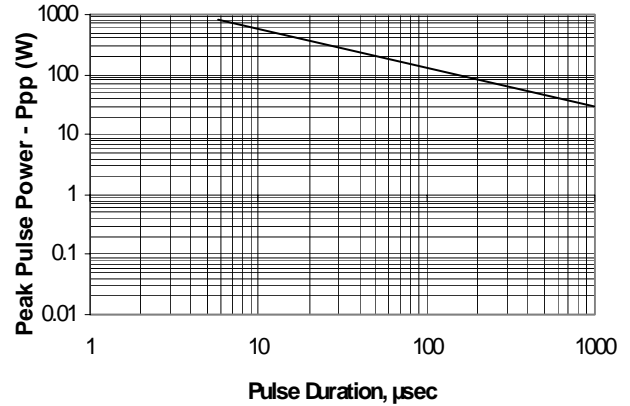


TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

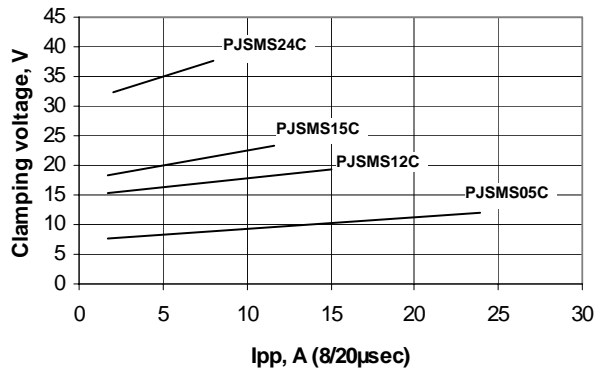
Surge Pulse Waveform Definition



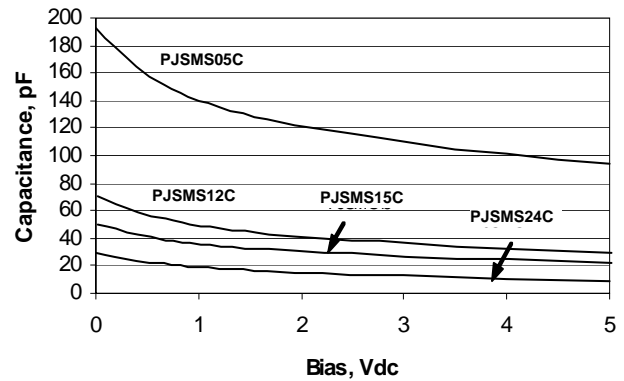
Non-Repetitive Peak Pulse Power vs Pulse Time

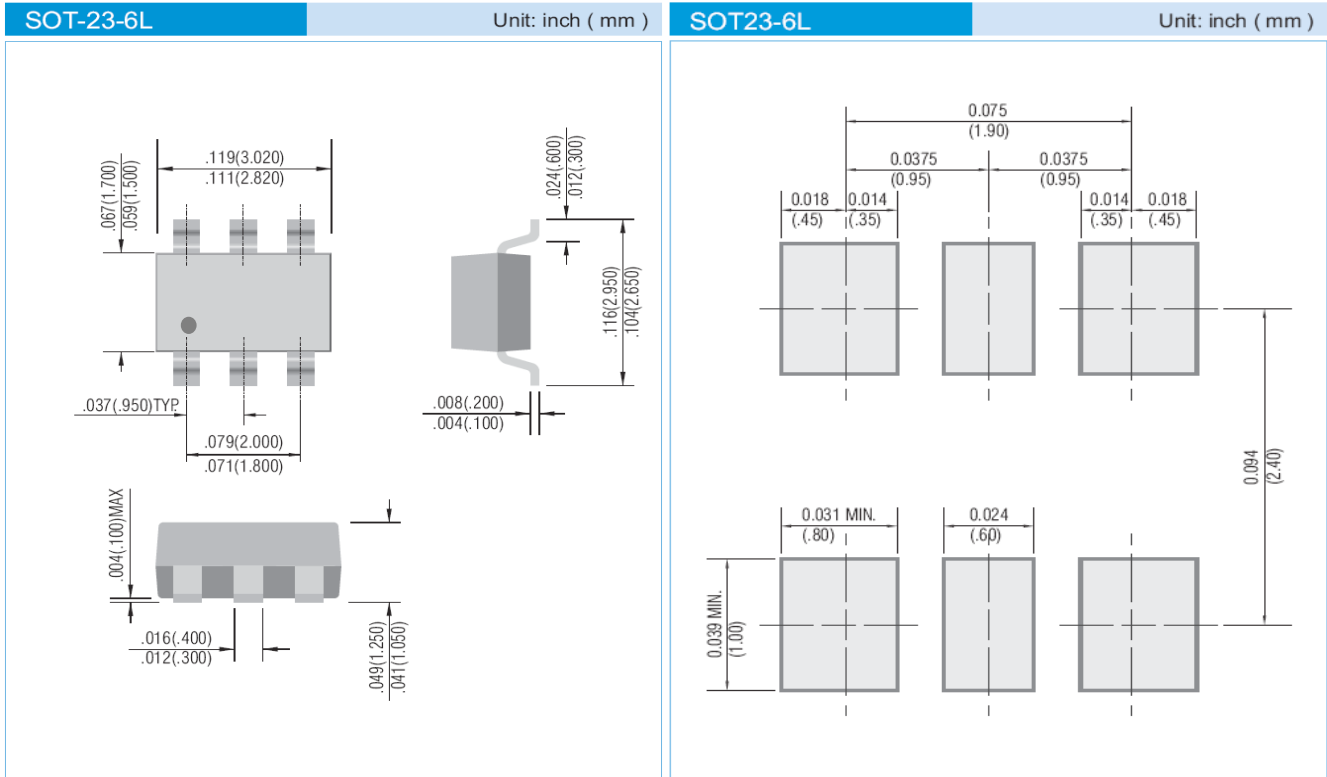


Clamping Voltage vs. Peak current



Off-State Capacitance per Device - 1MHz



PACKAGE AND PAD LAYOUT DIMENSIONS

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