512Mb DDR SDRAM

Features

CAS Latency and Frequency

CAS Latency	Maximum Operating Frequency (MHz)		
	DDR400 (5T)	DDR333 (6K)	DDR266B (75B)
2	-	133	100
2.5	166	166	133
3	200	-	-

- DDR 512M bit, die B, based on 110nm design rules
- Double data rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 / 2.5 (6K & 75B), 2.5 / 3 (6K & 5T)
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- 7.8μs Maximum Average Periodic Refresh Interval
- 2.5V (SSTL_2 compatible) I/O
- $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$ (6K & 75B)
- $V_{DD} = V_{DDQ} = 2.6V \pm 0.1V$ (5T)

Description

NT5DS128M4BF, NT5DS128M4BT, NT5DS128M4BG, NT5DS128M4BS, NT5DS64M8BF, NT5DS64M8BT, NT5DS64M8BG, NT5DS64M8BS, NT5DS32M16BF NT5DS32M16BT, NT5DS32M16BG and NT5DS32M16BS are die B of 512Mb SDRAM devices based using DDR interface. They are all based on Nanya's 110 nm design process.

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a *2n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 512Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going high and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4, or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving Power Down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Ordering Information (Non-Green)

Org.	Part Number	Package	Speed		Comments
			Clock (MHz)	CL-t_{RCD}-t_{RP}	
128M x 4	NT5DS128M4BT-5T	66 pin TSOP-II	200	3-3-3	DDR400
	NT5DS128M4BT-6K		166	2.5-3-3	DDR333
	NT5DS128M4BT-75B		133	2.5-3-3	DDR266
	NT5DS128M4BF-5T	60ball BGA 0.8mmx1.0mm Pitch	200	3-3-3	DDR400
	NT5DS128M4BF-6K		166	2.5-3-3	DDR333
	NT5DS128M4BF-75B		133	2.5-3-3	DDR266
64M x 8	NT5DS64M8BT-5T	66 pin TSOP-II	200	3-3-3	DDR400
	NT5DS64M8BT-6K		166	2.5-3-3	DDR333
	NT5DS64M8BT-75B		133	2.5-3-3	DDR266
	NT5DS64M8BF-5T	60ball BGA 0.8mmx1.0mm Pitch	200	3-3-3	DDR400
	NT5DS64M8BF-6K		166	2.5-3-3	DDR333
	NT5DS64M8BF-75B		133	2.5-3-3	DDR266
32M x 16	NT5DS32M16BT-5T	66 pin TSOP-II	200	3-3-3	DDR400
	NT5DS32M16BT-6K		166	2.5-3-3	DDR333
	NT5DS32M16BT-75B		133	2.5-3-3	DDR266
	NT5DS32M16BF-5T	60ball BGA 0.8mmx1.0mm Pitch	200	3-3-3	DDR400
	NT5DS32M16BF-6K		166	2.5-3-3	DDR333
	NT5DS32M16BF-75B		133	2.5-3-3	DDR266

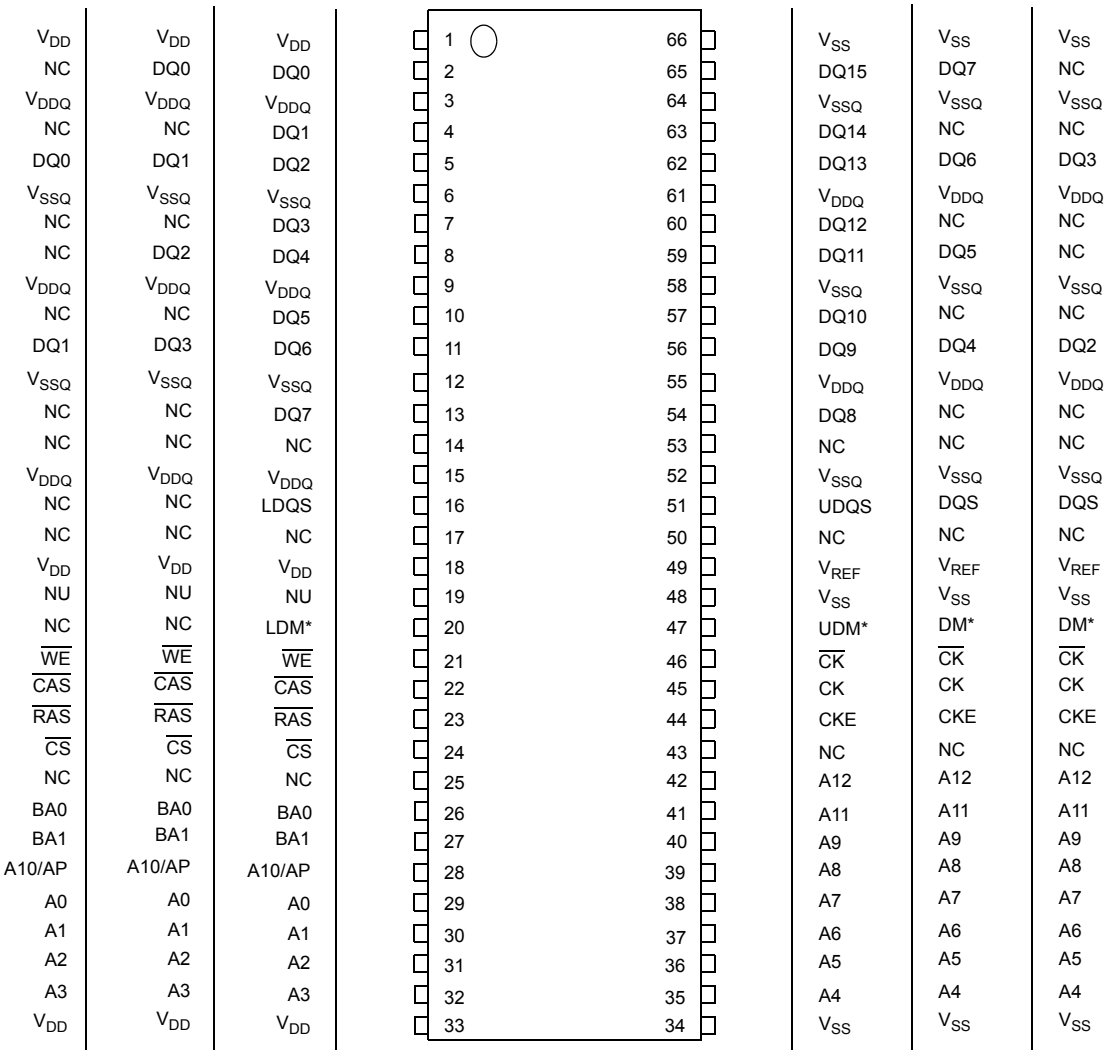
Note:
1. At the present time, there are no plans to support DDR SDRAMs with the $\overline{QFC}$ function. All reference to $\overline{QFC}$ are for information only

Ordering Information (Green)

Org.	Part Number	Package	Speed		Comments
			Clock (MHz)	CL-t_{RCD}-t_{RP}	
128M x 4	NT5DS128M4BS-5T	66 pin TSOP-II	200	3-3-3	DDR400
	NT5DS128M4BS-6K		166	2.5-3-3	DDR333
	NT5DS128M4BS-75B		133	2.5-3-3	DDR266
	NT5DS128M4BG-5T	60ball BGA 0.8mmx1.0mm Pitch	200	3-3-3	DDR400
	NT5DS128M4BG-6K		166	2.5-3-3	DDR333
	NT5DS128M4BG-75B		133	2.5-3-3	DDR266
64M x 8	NT5DS64M8BS-5T	66 pin TSOP-II	200	3-3-3	DDR400
	NT5DS64M8BS-6K		166	2.5-3-3	DDR333
	NT5DS64M8BS-75B		133	2.5-3-3	DDR266
	NT5DS64M8BG-5T	60ball BGA 0.8mmx1.0mm Pitch	200	3-3-3	DDR400
	NT5DS64M8BG-6K		166	2.5-3-3	DDR333
	NT5DS64M8BG-75B		133	2.5-3-3	DDR266
32M x 16	NT5DS32M16BS-5T	66 pin TSOP-II	200	3-3-3	DDR400
	NT5DS32M16BS-6K		166	2.5-3-3	DDR333
	NT5DS32M16BS-75B		133	2.5-3-3	DDR266
	NT5DS32M16BG-5T	60ball BGA 0.8mmx1.0mm Pitch	200	3-3-3	DDR400
	NT5DS32M16BG-6K		166	2.5-3-3	DDR333
	NT5DS32M16BG-75B		133	2.5-3-3	DDR266

Note:
1. At the present time, there are no plans to support DDR SDRAMs with the $\overline{QFC}$ function. All reference to $\overline{QFC}$ are for information only

Pin Configuration - 400mil TSOP II (x4 / x8 / x16)



66-pin Plastic TSOP-II 400mil

32Mb x 16

64Mb x 8

128Mb x 4

Column Address Table

Organization	Column Address
128Mb x 4	A0-A9, A11, A12
64Mb x 8	A0-A9, A11
32Mb x 16	A0-A9

*DM is internally loaded to match DQ and DQS identically.

Pin Configuration - 60 balls 0.8mmx1.0mm Pitch CSP Package

<Top View >

See the balls through the package.

128 X 4

1	2	3		7	8	9
VSSQ	NC	VSS	A	VDD	NC	VDDQ
NC	VDDQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VDDQ	NC
NC	VDDQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DQM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/ AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

64 X 8

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VDD	DQ0	VDDQ
NC	VDDQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VDDQ	NC
NC	VDDQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VDDQ	NC
VREF	VSS	DQM	F	NC	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/ AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

Pin Configuration - 60 balls 0.8mmx1.0mm Pitch CSP Package

<Top View >

See the balls through the package.

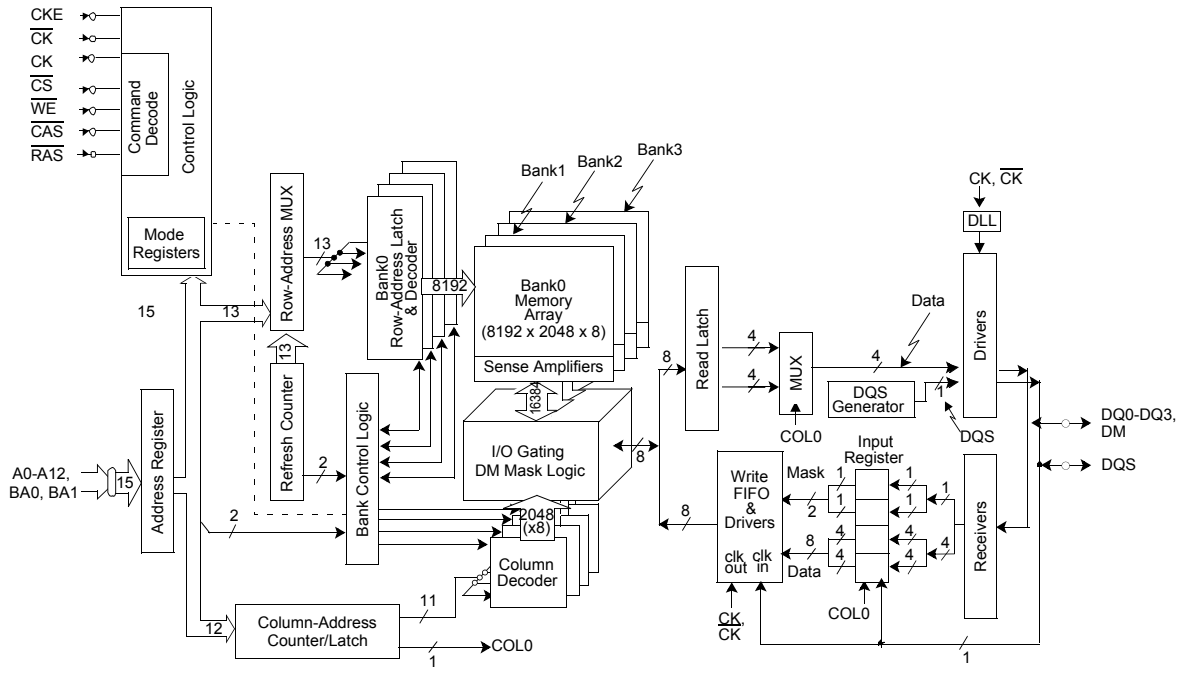
32 X 16

1	2	3		7	8	9
VSSQ	DQ15	VSS	A	VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS	E	LDQS	VDDQ	DQ7
VREF	VSS	UDM	F	LDM	VDD	NC
	CLK	$\overline{CLK}$	G	$\overline{WE}$	$\overline{CAS}$	
	A12	CKE	H	$\overline{RAS}$	$\overline{CS}$	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/ AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VDD	A3	

Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE, CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during self refresh. The standard pinout includes one CKE pin. Optional pinouts might include CKE1 on a different pin, in addition to CKE0, to facilitate independent power down control of stacked devices.
$\overline{CS}$, $\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin. Optional pinouts might include $\overline{CS1}$ on a different pin, in addition to $\overline{CS0}$, to allow upper or lower deck selection on stacked devices.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. During a Read, DM can be driven high, low, or floated.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 low) or all banks (A10 high). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a Mode Register Set command.
DQ	Input/Output	**Data Input/Output:** Data bus.
DQS, LDQS, UDQS	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15
NC		**No Connect:** No internal electrical connection is present.
NU		Electrical connection is present. Should not be connected at second level of assembly.
V_{DDQ}	Supply	**DQ Power Supply:** 2.5V ± 0.2V.
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.2V.
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage:** (V_{DDQ} / 2) ± 1%.

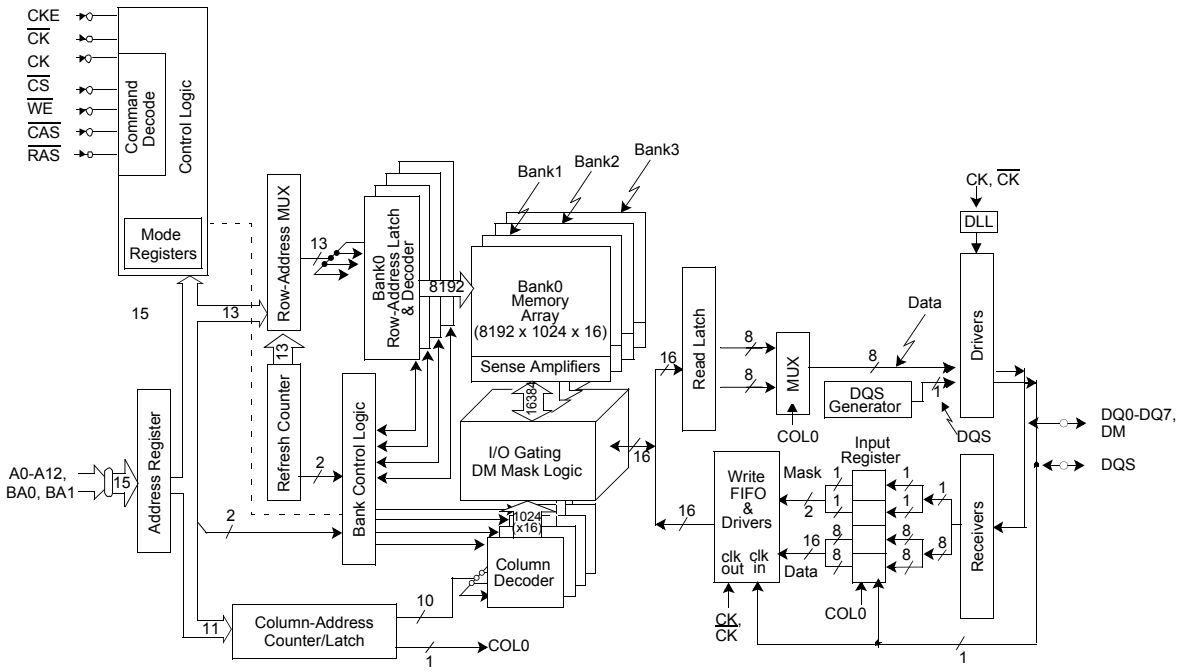
Block Diagram (128Mb x 4)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

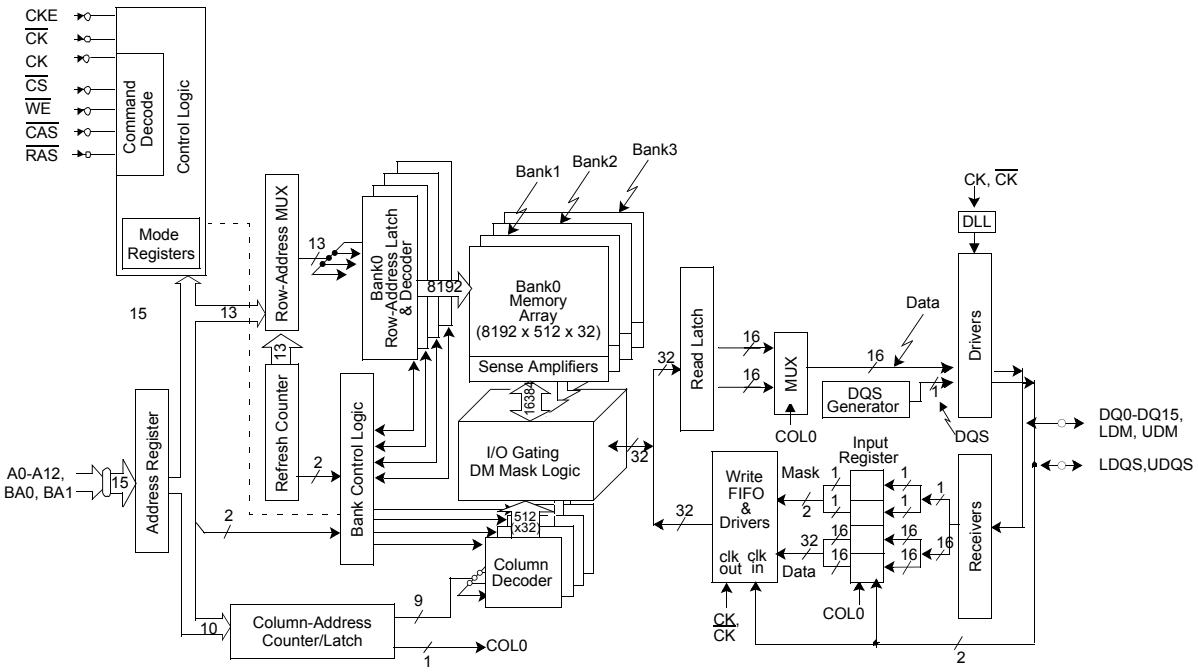
Block Diagram (64Mb x 8)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Block Diagram (32Mb x 16)



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: UDM and LDM are unidirectional signals (input only), but is internally loaded to match the load of the bidirectional DQ, UDQS, and LDQS signals.

Functional Description

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The 512Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 512Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR SDRAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

Only one of the following two conditions must be met.

• No power sequencing is specified during power up or power down given the following criteria:
  V_{DD} and V_{DDQ} are driven from a single power converter output
  V_{TT} meets the specification
  A minimum resistance of 42 ohms limits the input current from the VTT supply into any pin and
  V_{REF} tracks V_{DDQ} /2

or

• The following relationships must be followed:
  V_{DDQ} is driven after or with V_{DD} such that $V_{DDQ} < V_{DD} + 0.3V$
  V_{TT} is driven after or with V_{DDQ} such that $V_{TT} < V_{DDQ} + 0.3V$
  V_{REF} is driven after or with V_{DDQ} such that $V_{REF} < V_{DDQ} + 0.3V$

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200μs delay prior to applying an executable command.

Once the 200μs delay has been satisfied, a Deselect or NOP command should be applied, and CKE must be brought HIGH. Following the NOP command, a Precharge ALL command must be applied. Next a Mode Register Set command must be issued for the Extended Mode Register, to enable the DLL, then a Mode Register Set command must be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A Precharge ALL command should be applied, placing the device in the “all banks idle” state

Once in the idle state, two auto refresh cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

DDR SDRAM’s may be reinitialized at any time during normal operation by asserting a valid MRS command to either the base or extended mode registers without affecting the contents of the memory array. The contents of either the mode register or extended mode register can be modified at any valid time during device operation without affecting the state of the internal address refresh counters used for device refresh.

Register Definition

Mode Register

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode. The Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements results in unspecified operation.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A_2-Ai when the burst length is set to four and by A_3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Mode Register Operation

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0*	0*	Operating Mode						CAS Latency			BT	Burst Length			Mode Register

A12 - A9	A8	A7	A6 - A0	Operating Mode
0	0	0	Valid	Normal operation Do not reset DLL
0	1	0	Valid	Normal operation in DLL Reset
0	0	1	VS**	Vendor-Specific Test Mode
–	–	–		Reserved

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (Option)
1	0	0	Reserved
1	0	1	1.5 (Option)
1	1	0	2.5
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

VS** Vendor Specific

* BA0 and BA1 must be 0, 0 to select the Mode Register (vs. the Extended Mode Register).

Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-A i selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A i selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A i selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in *Burst Definition* on page 14.

Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks for DDR266/333 and 3 clocks for DDR400.

If a Read command is registered at clock edge n, and the latency is *m* clocks, the data is available nominally coincident with clock edge *n* + m.

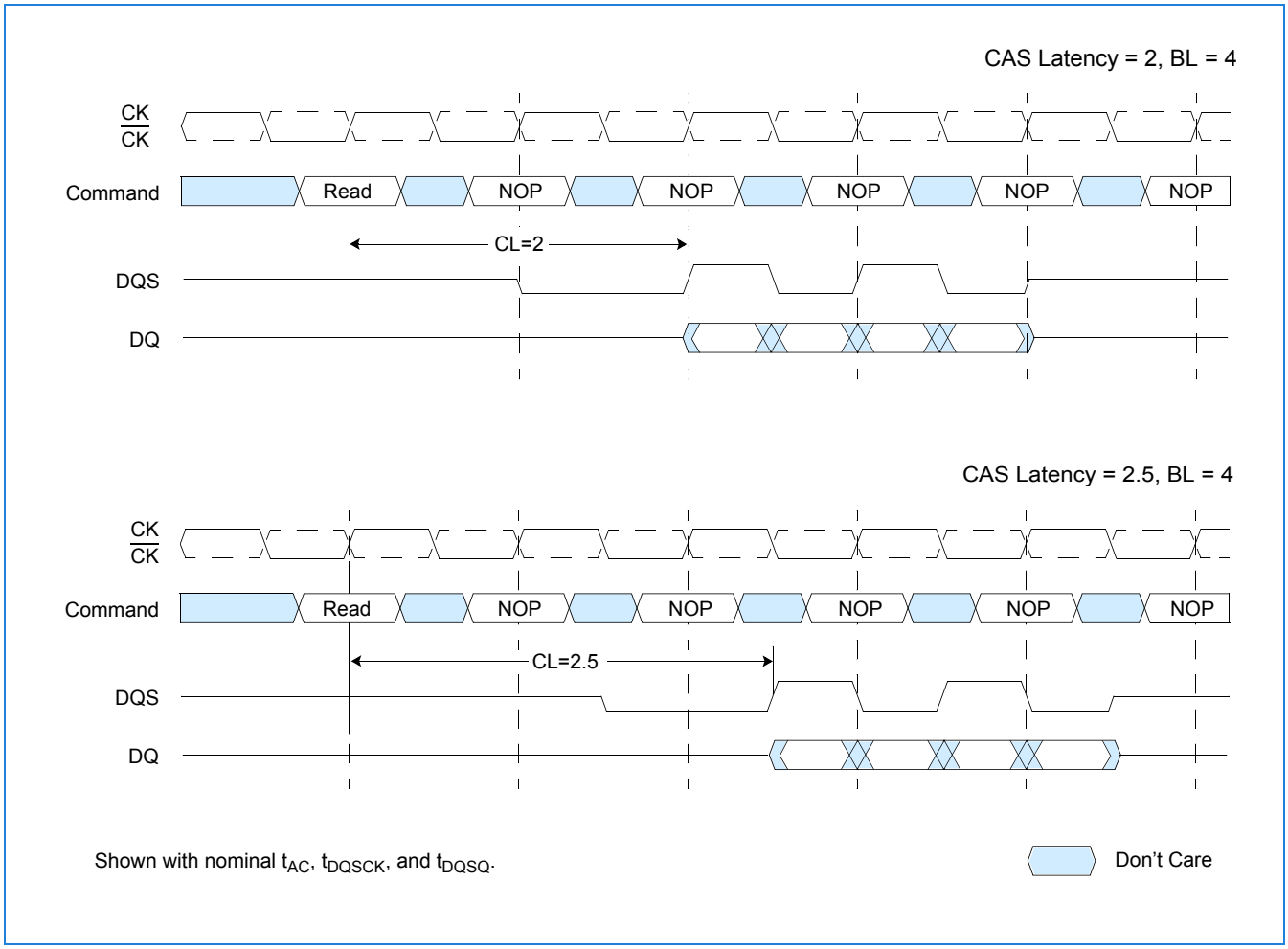
Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latencies



Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, bit A0; output drive strength selection, bit A1; and $\overline{QFC}$ output enable/disable, bit A2 (NTC optional). These functions are controlled via the bit settings shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before a Read command can be issued. This is the reason for introducing timing parameter t_{XSRD} for DDR SDRAM's (Exit Self Refresh to Read Command). Non- Read commands can be issued 2 clocks after the DLL is enabled via the EMRS command (t_{MRD}) or 10 clocks after the DLL is enabled via self refresh exit command (t_{XSNR}, Exit Self Refresh to Non-Read Command).

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II.

$\overline{QFC}$ Enable/Disable

The $\overline{QFC}$ signal is an optional DRAM output control used to isolate module loads (DIMMs) from the system memory bus by means of external FET switches when the given module (DIMM) is not being accessed. The $\overline{QFC}$ function is an optional feature for NANYA and is not included on all DDR SDRAM devices.

Extended Mode Register Definition

BA1	BA0	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address Bus
0*	1*	Operating Mode										$\overline{QFC}$	DS	DLL	Extended Mode Register

A12 - A3	A2 - A0	Operating Mode
0	Valid	Normal Operation
–	–	All other states Reserved

Drive Strength

A_1	Drive Strength
0	Normal
1	Reserved

A_2	$\overline{QFC}$
0	Disable
1	Enable (Optional)

A_0	DLL
0	Enable
1	Disable

* BA0 and BA1 must be 1, 0 to select the Extended Mode Register (vs. the base Mode Register)

Commands

Truth Tables 1a and 1b provide a reference of the commands supported by DDR SDRAM devices. A verbal description of each commands follows.

Truth Table 1a: Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Notes
Deselect (Nop)	H	X	X	X	X	NOP	1, 9
No Operation (Nop)	L	H	H	H	X	NOP	1, 9
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1, 3
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1, 4
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1, 4
Burst Terminate	L	H	H	L	X	BST	1, 8
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1, 5
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR / SR	1, 6, 7
Mode Register Set	L	L	L	L	Op-Code	MRS	1, 2

1. CKE is high for all commands shown except Self Refresh.
2. BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.)
3. BA0-BA1 provide bank address and A0-A12 provide row address.
4. BA0, BA1 provide bank address; A0-A*i* provide column address (where *i* = 9 for x8 and 9, 11 for x4); A10 high enables the Auto Precharge feature (non-persistent), A10 low disables the Auto Precharge feature.
5. A10 LOW: BA0, BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care.”
6. This command is auto refresh if CKE is high; Self Refresh if CKE is low.
7. Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts
9. Deselect and NOP are functionally interchangeable.

Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

1. Used to mask write data; provided coincident with the corresponding data.

Deselect

The Deselect function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The No Operation (NOP) command is used to perform a NOP to a DDR SDRAM. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Mode Register Set

The mode registers are loaded via inputs A0-A12, BA0 and BA1 while issuing the Mode Register Set Command. See mode register descriptions in the Register Definition section. The Mode Register Set command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

Write

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Precharge

The Precharge command is used to deactivate (close) the open row in a particular bank or the open row(s) in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A precharge command is treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

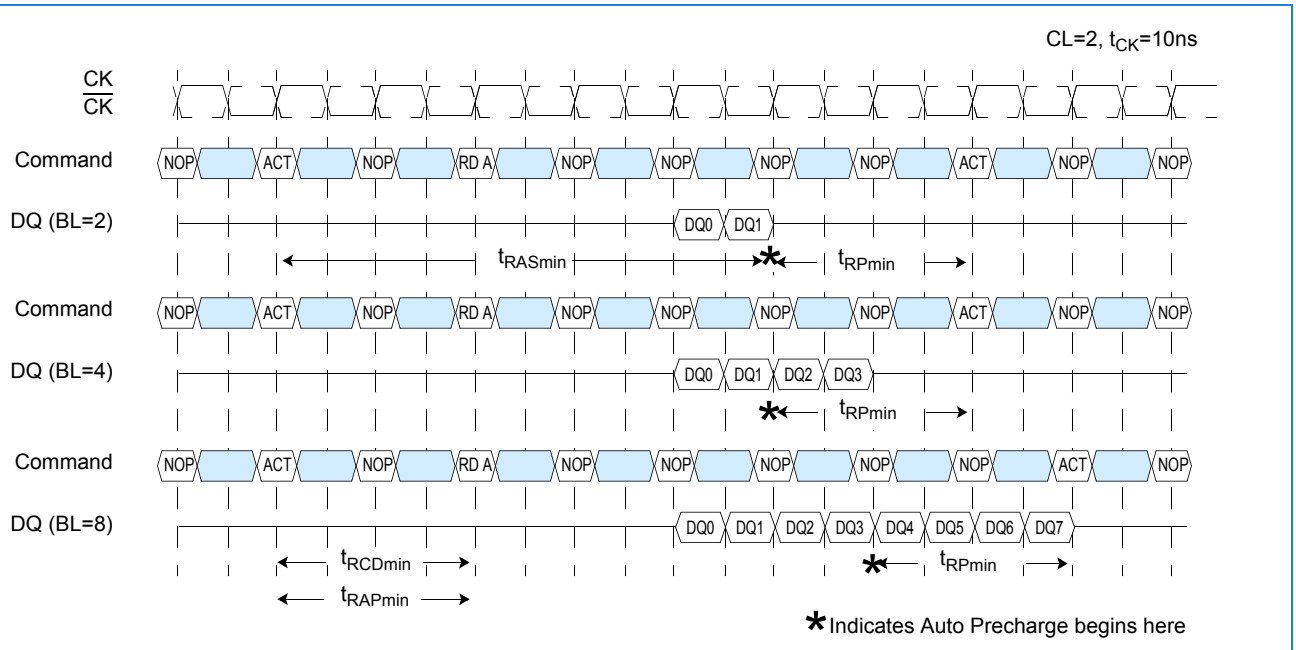
Auto Precharge

Auto Precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst. Auto Precharge is non-persistent in that it is either enabled or disabled for each individual Read or Write command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This is determined as if an explicit Precharge command was issued at the earliest possible time without violating t_{RAS}(min). The user must not issue another command to the same bank until the precharge (t_{RP}) is completed.

The NTC DDR SDRAM devices supports the optional t_{RAS} lockout feature. This feature allows a Read command with Auto Precharge to be issued to a bank that has been activated (opened) but has not yet satisfied the t_{RAS}(min) specification. The t_{RAS} lockout feature essentially delays the onset of the auto precharge operation until two conditions occur. One, the entire burst length of data has been successfully prefetched from the memory array; and two, t_{RAS}(min) has been satisfied.

As a means to specify whether a DDR SDRAM device supports the t_{RAS} lockout feature, a new parameter has been defined, t_{RAP} (RAS Command to Read Command with Auto Precharge or better stated Bank Activate to Read Command with Auto Precharge). For devices that support the t_{RAS} lockout feature, t_{RAP} = t_{RCD}(min). This allows any Read Command (with or without Auto Precharge) to be issued to an open bank once t_{RCD}(min) is satisfied.

t_{RAP} Definition



The above timing diagrams show the effects of t_{RAP} for devices that support t_{RAS} lockout. In these cases, the Read with Auto Precharge command (RDA) is issued with t_{RCD}(min) and dataout is available with the shortest latency from the Bank Activate command (ACT). The internal precharge operation, however, does not begin until after t_{RAS}(min) is satisfied.

Burst Terminate

The Burst Terminate command is used to truncate read bursts (with Auto Precharge disabled). The most re-cently registered Read command prior to the Burst Terminate command is truncated, as shown in the Operation section of this data sheet. Write burst cycles are not to be terminated with the Burst Terminate command.

Auto Refresh

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to $\overline{CAS}$ Before $\overline{RAS}$ (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an Auto Refresh command. The 512Mb DDR SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8μs (maximum).

Self Refresh

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are “Don’t Care” during Self Refresh operation.

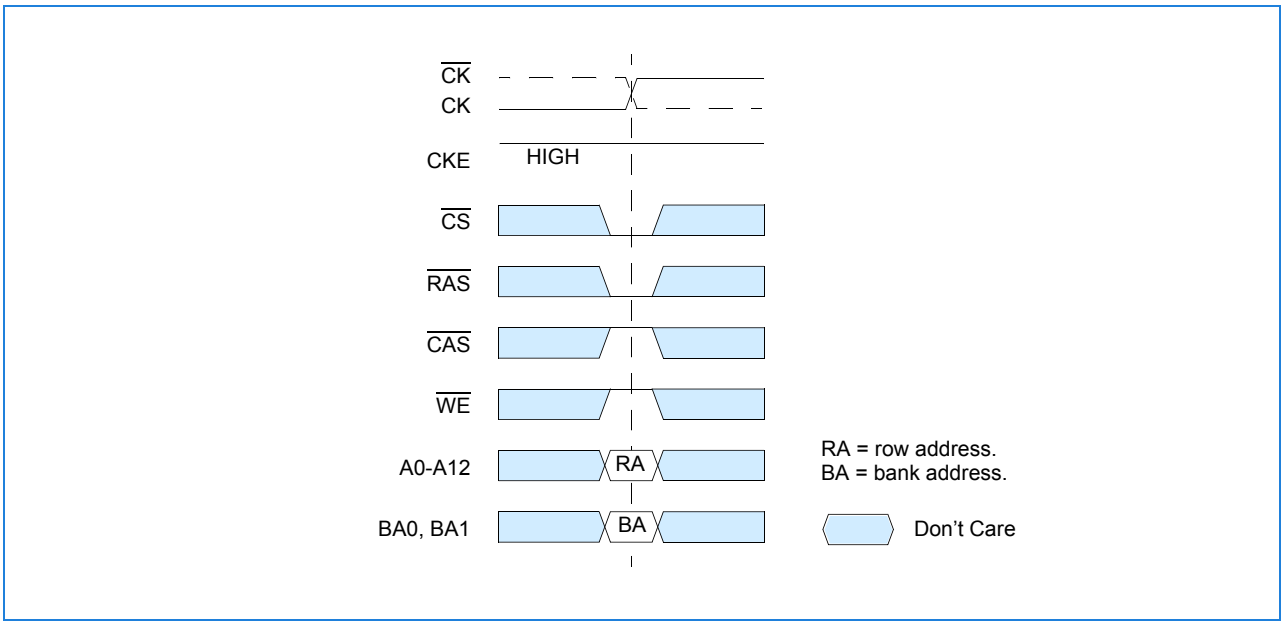
The procedure for exiting self refresh requires a sequence of commands. CK (and $\overline{CK}$) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Operations

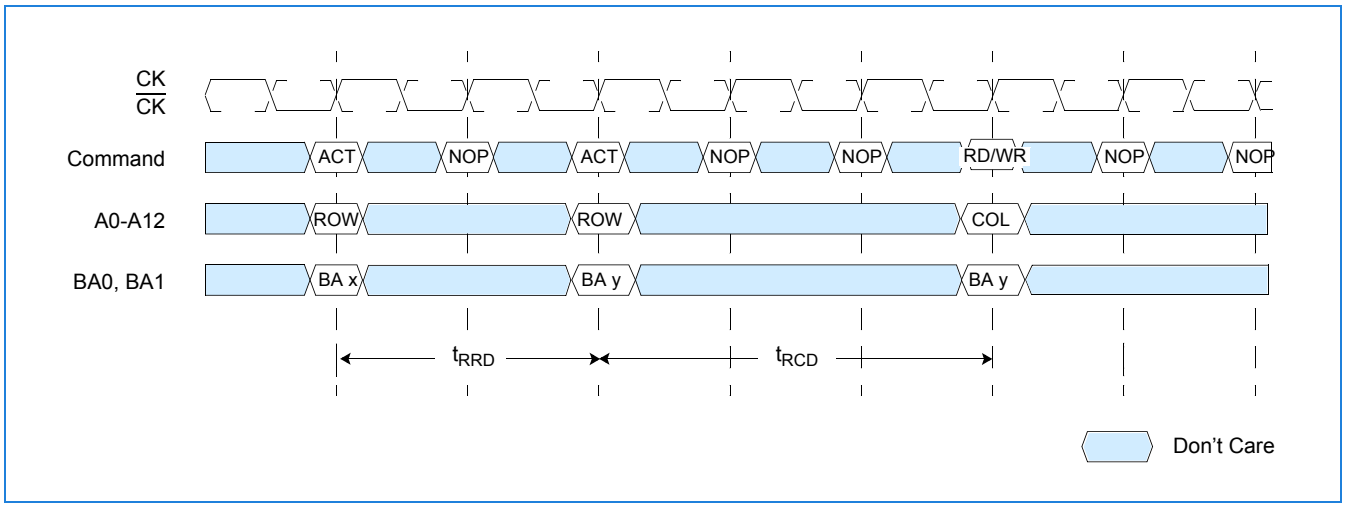
Bank/Row Activation

Before any Read or Write commands can be issued to a bank within the DDR SDRAM, a row in that bank must be “opened” (activated). This is accomplished via the Active command and addresses A0-A12, BA0 and BA1 (see Activating a Specific Row in a Specific Bank), which decode and select both the bank and the row to be activated. After opening a row (issuing an Active command), a Read or Write command may be issued to that row, subject to the t_{RCD} specification. A subsequent Active command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive Active commands to the same bank is defined by t_{RC}. A subsequent Active command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.

Activating a Specific Row in a Specific Bank



t_{RCD} and t_{RRD} Definition



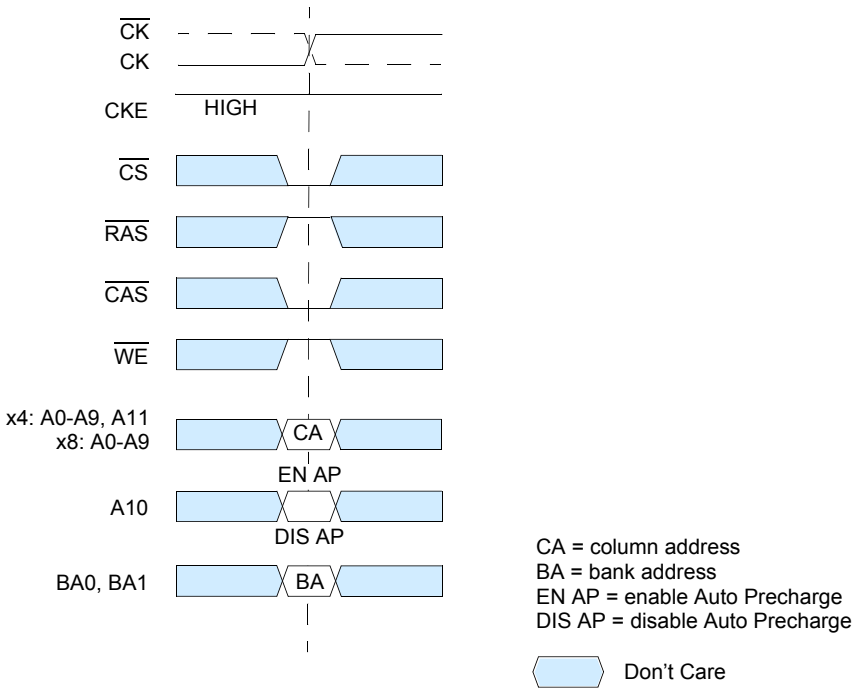
Reads

Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command.

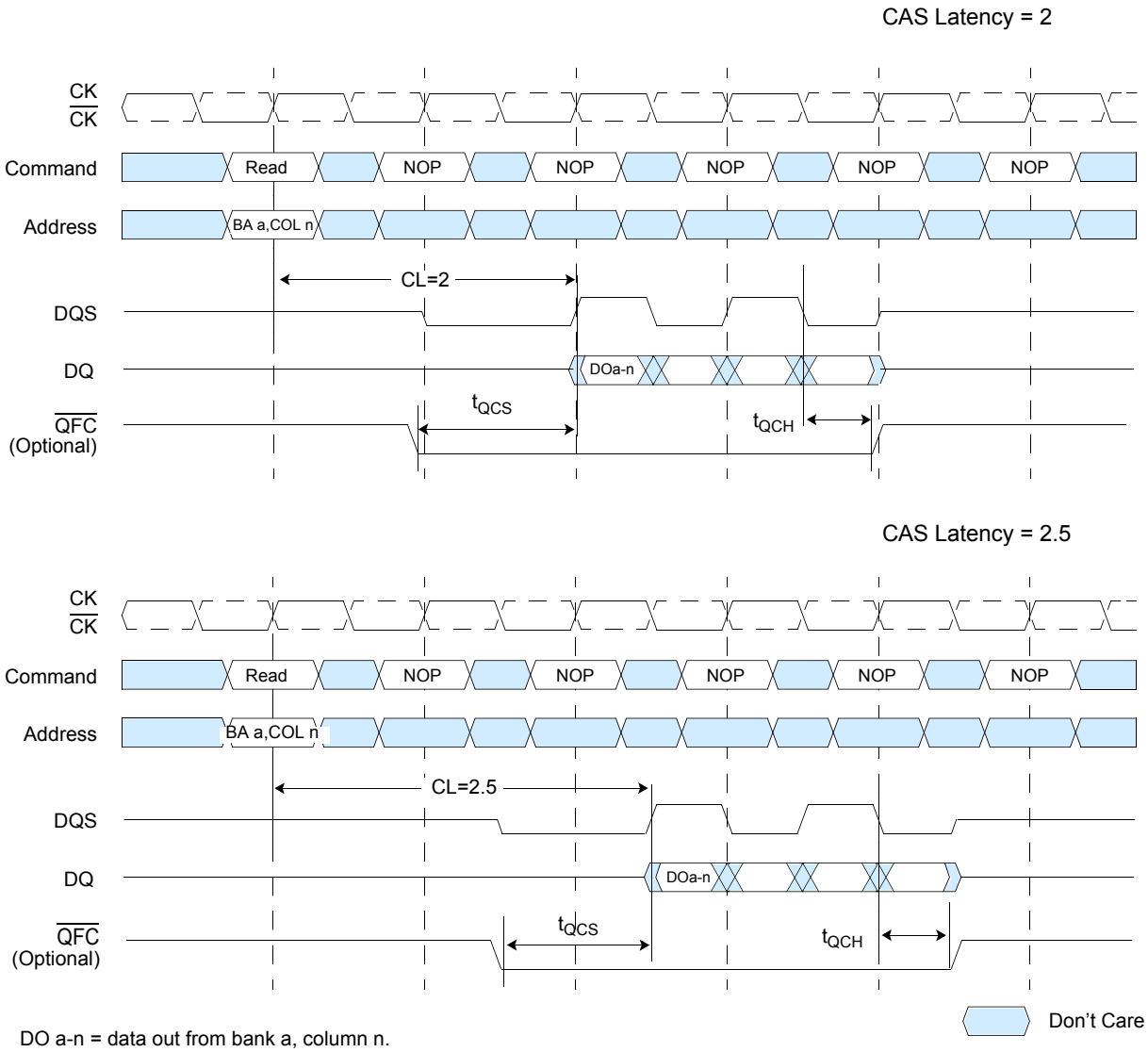
The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and $\overline{CK}$). The following timing figure entitled “Read Burst: CAS Latencies (Burst Length=4)” illustrates the general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS goes High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure entitled “Consecutive Read Bursts: CAS Latencies (Burst Length =4 or 8)”. A Read command can be initiated on any positive clock cycle following a previous Read command. Nonconsecutive Read data is shown in timing figure entitled “Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)”. Full-speed Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8) within a page (or pages) can be performed as shown on page 28.

Read Command

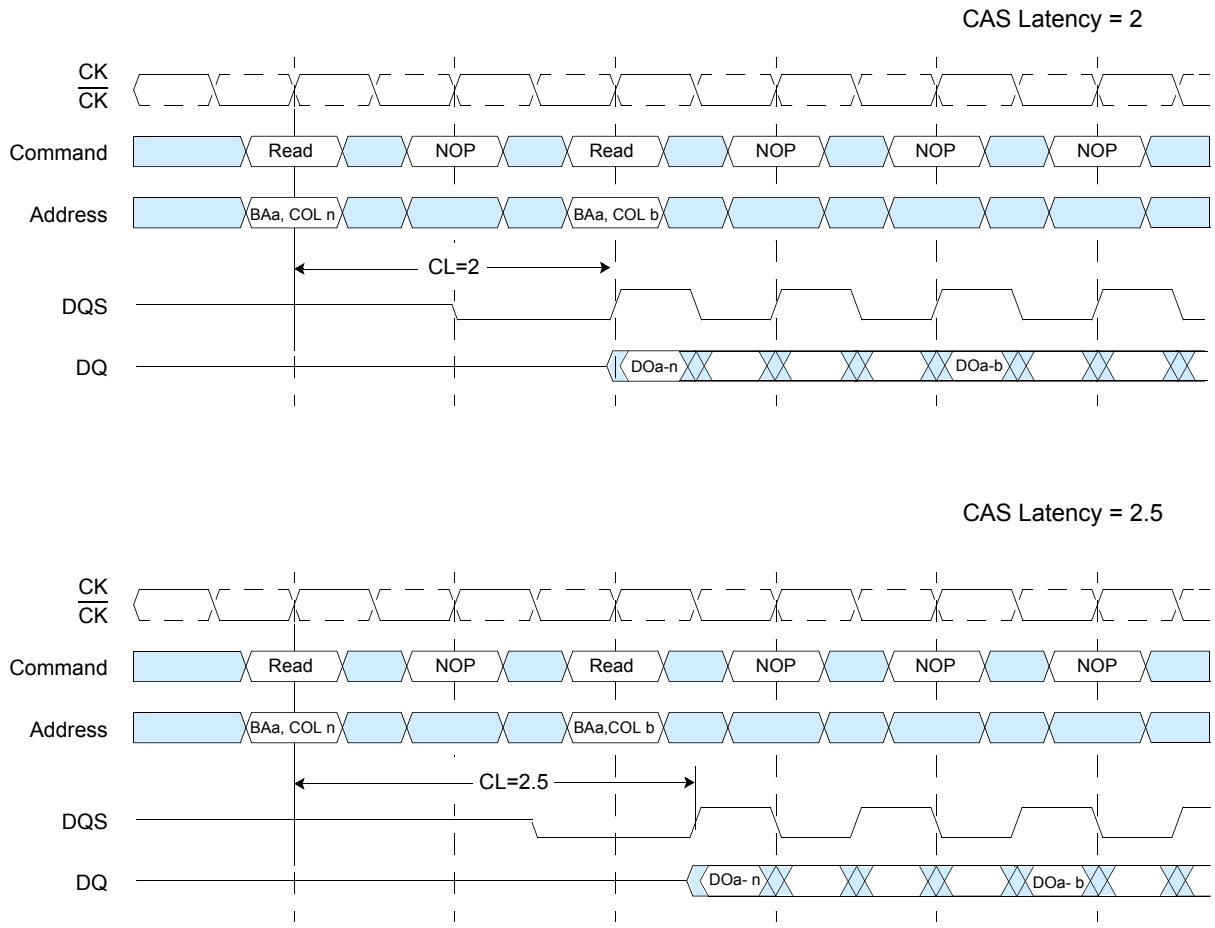


Read Burst: CAS Latencies (Burst Length = 4)



DO a-n = data out from bank a, column n.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.
$\overline{QFC}$ is an open drain driver. The output high level is achieved through an external pull up resistor connected to V_{DDQ}.

Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)

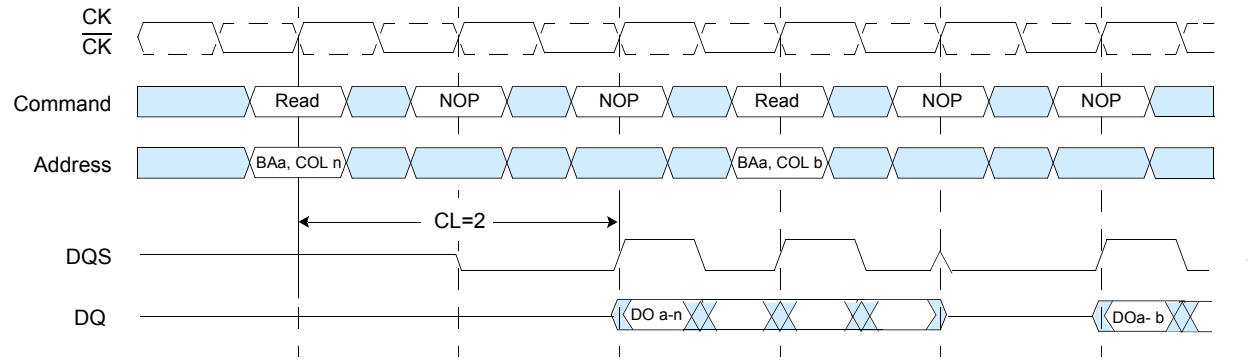


DO a-n (or a-b) = data out from bank a, column n (or bank a, column b).
When burst length = 4, the bursts are concatenated.
When burst length = 8, the second burst interrupts the first.
3 subsequent elements of data out appear in the programmed order following DO a-n.
3 (or 7) subsequent elements of data out appear in the programmed order following DO a-b.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

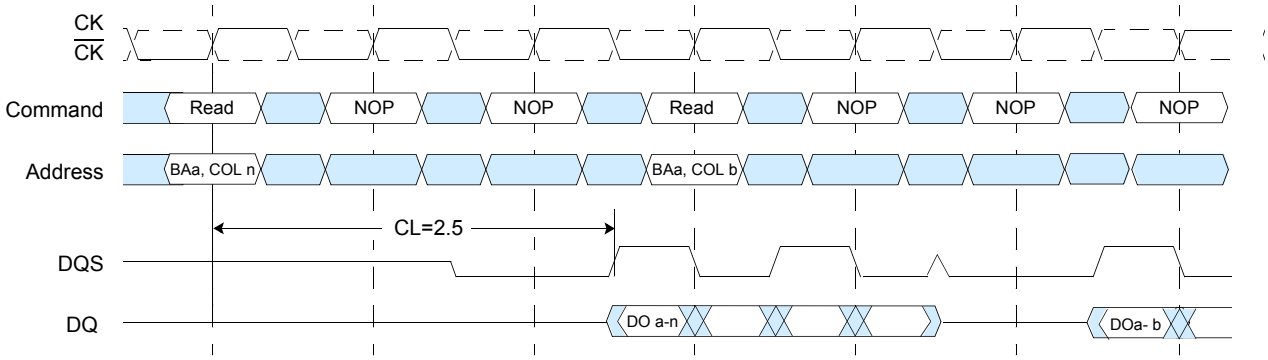
Don't Care

Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)

CAS Latency = 2



CAS Latency = 2.5

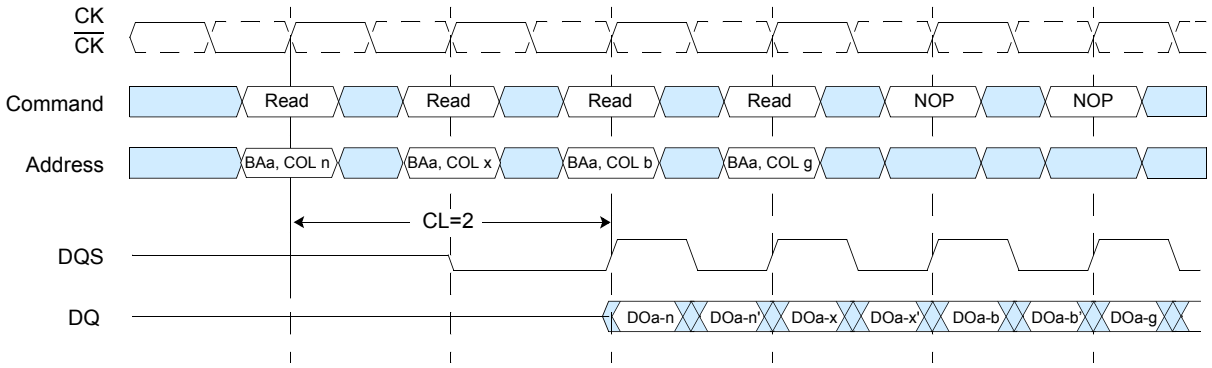


DO a-n (or a-b) = data out from bank a, column n (or bank a, column b).
3 subsequent elements of data out appear in the programmed order following DO a-n (and following DO a-b).
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

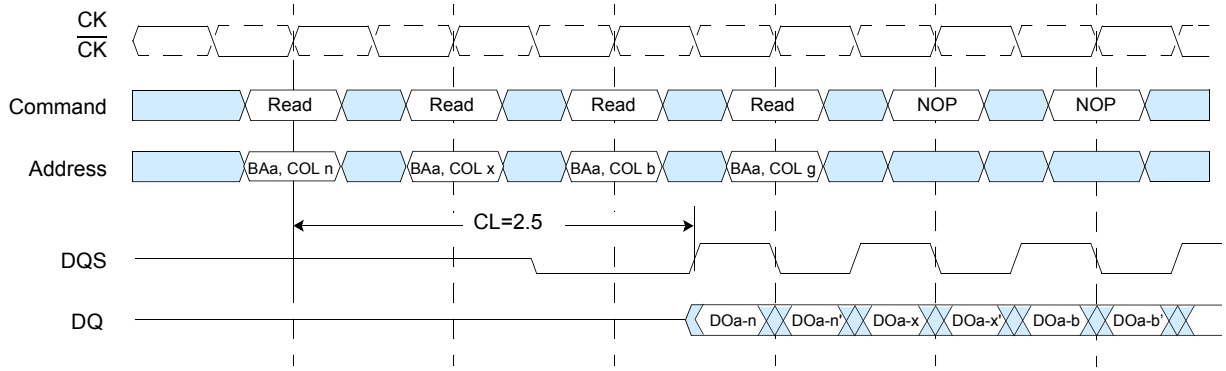
Don't Care

Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)

CAS Latency = 2



CAS Latency = 2.5



DO a-n, etc. = data out from bank a, column n etc.
n' etc. = odd or even complement of n, etc. (i.e., column address LSB inverted).
Reads are to active rows in any banks.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

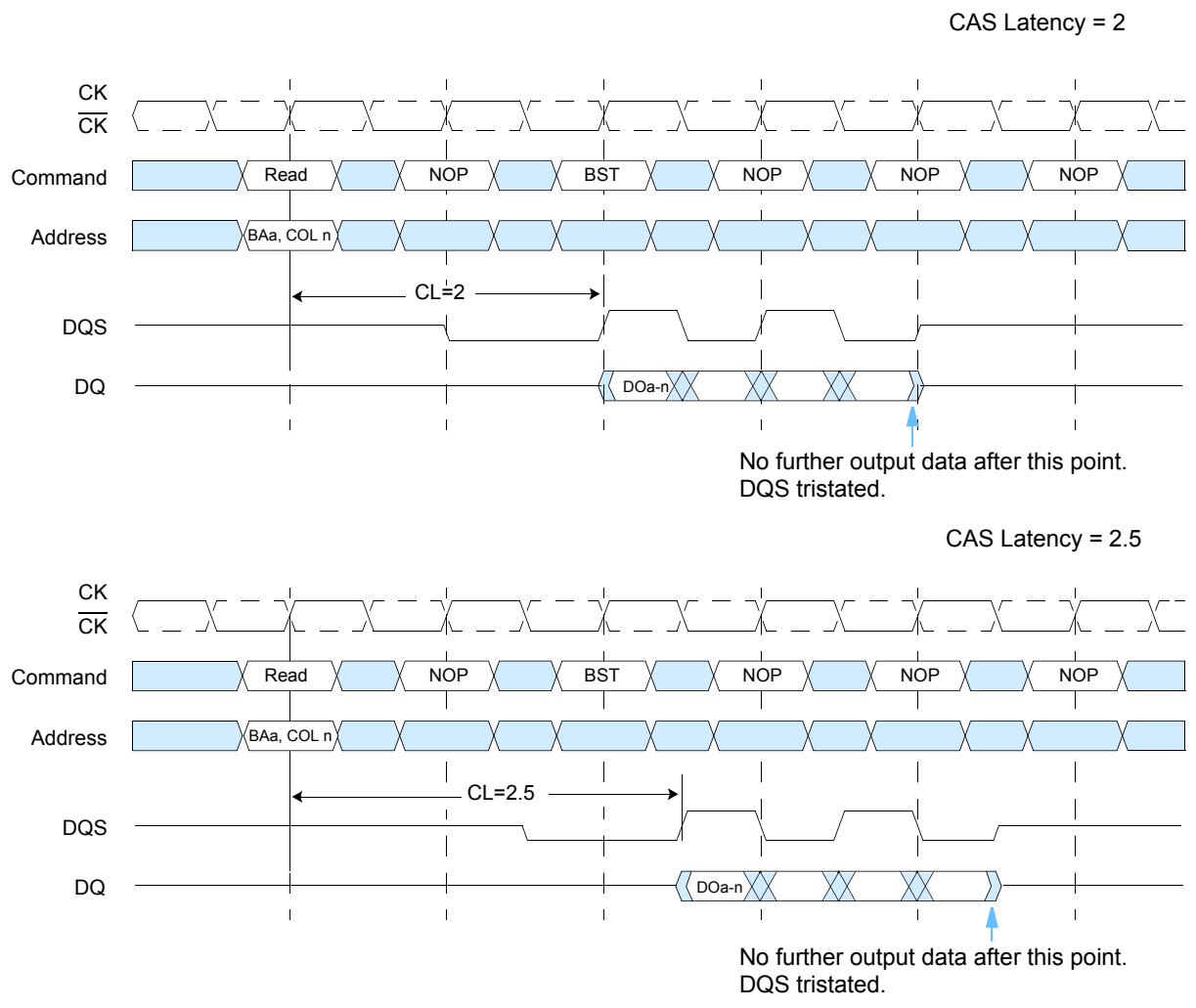
Data from any Read burst may be truncated with a Burst Terminate command, as shown in timing figure entitled *Terminating a Read Burst: CAS Latencies (Burst Length = 8)* on page 30. The Burst Terminate latency is equal to the read (CAS) latency, i.e. the Burst Terminate command should be issued x cycles after the Read command, where x equals the number of desired data element pairs.

Data from any Read burst must be completed or truncated before a subsequent Write command can be issued. If truncation is necessary, the Burst Terminate command must be used, as shown in timing figure entitled *Read to Write: CAS Latencies (Burst Length = 4 or 8)* on page 31. The example is shown for t_{DQSS}(min). The t_{DQSS}(max) case, not shown here, has a longer bus idle time. t_{DQSS}(min) and t_{DQSS}(max) are defined in the section on Writes.

A Read burst may be followed by, or truncated with, a Precharge command to the same bank (provided that Auto Precharge was not activated). The Precharge command should be issued x cycles after the Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown in timing figure *Read to Precharge: CAS Latencies (Burst Length = 4 or 8)* on page 32 for Read latencies of 2 and 2.5. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a Read being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same Read burst with Auto Precharge enabled. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

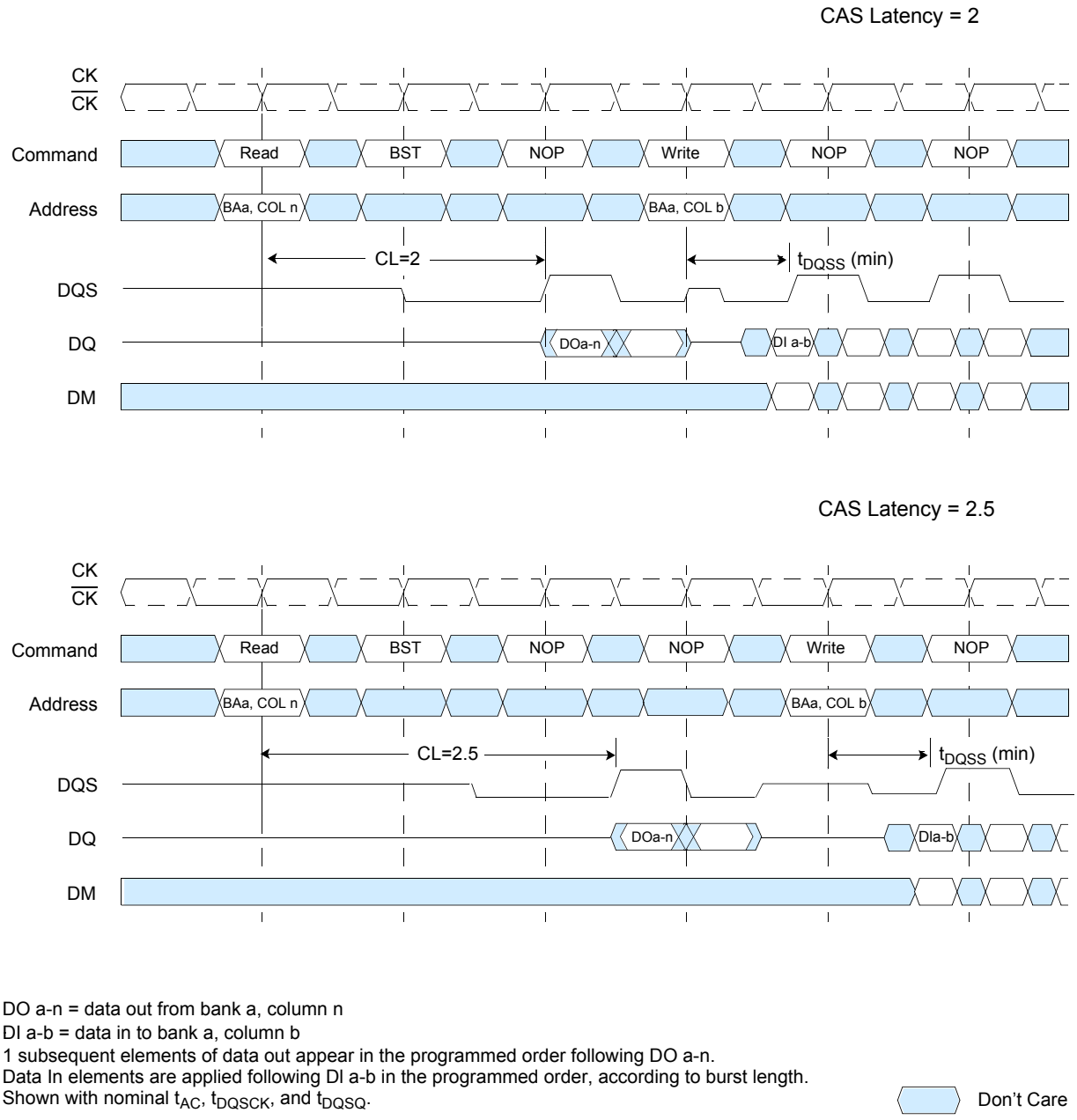
Terminating a Read Burst: CAS Latencies (Burst Length = 8)



DO a-n = data out from bank a, column n.
Cases shown are bursts of 8 terminated after 4 data elements.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

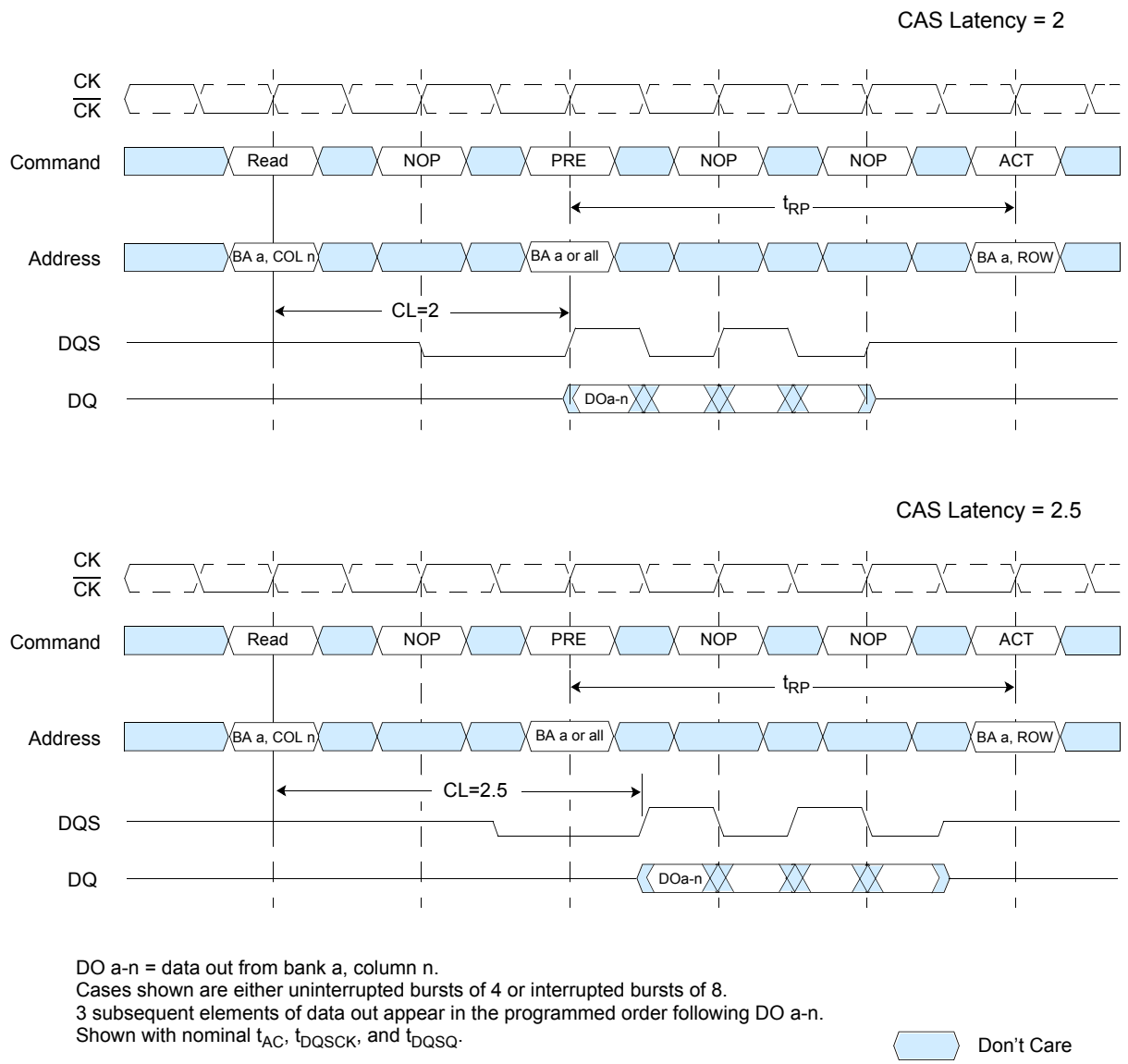
Read to Write: CAS Latencies (Burst Length = 4 or 8)



DO a-n = data out from bank a, column n
DI a-b = data in to bank a, column b
1 subsequent elements of data out appear in the programmed order following DO a-n.
Data In elements are applied following DI a-b in the programmed order, according to burst length.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Read to Precharge: CAS Latencies (Burst Length = 4 or 8)



DO a-n = data out from bank a, column n.
Cases shown are either uninterrupted bursts of 4 or interrupted bursts of 8.
3 subsequent elements of data out appear in the programmed order following DO a-n.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Writes

Write bursts are initiated with a Write command, as shown in timing figure *Write Command* on page 34.

The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble. The time between the Write command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. t_{DQSS}(min) and t_{DQSS}(max)). Timing figure *Write Burst (Burst Length = 4)* on page 35 shows the two extremes of t_{DQSS} for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enters High-Z and any additional input data is ignored.

Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). Timing figure *Write to Write (Burst Length = 4)* on page 36 shows concatenated bursts of 4. An example of non-consecutive Writes is shown in timing figure *Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)* on page 37. Full-speed random write accesses within a page or pages can be performed as shown in timing figure *Random Write Cycles (Burst Length = 2, 4 or 8)* on page 38. Data for any Write burst may be followed by a subsequent Read command. To follow a Write without truncating the write burst, t_{WTR} (Write to Read) should be met as shown in timing figure *Write to Read: Non-Interrupting (CAS Latency = 2; Burst Length = 4)* on page 39.

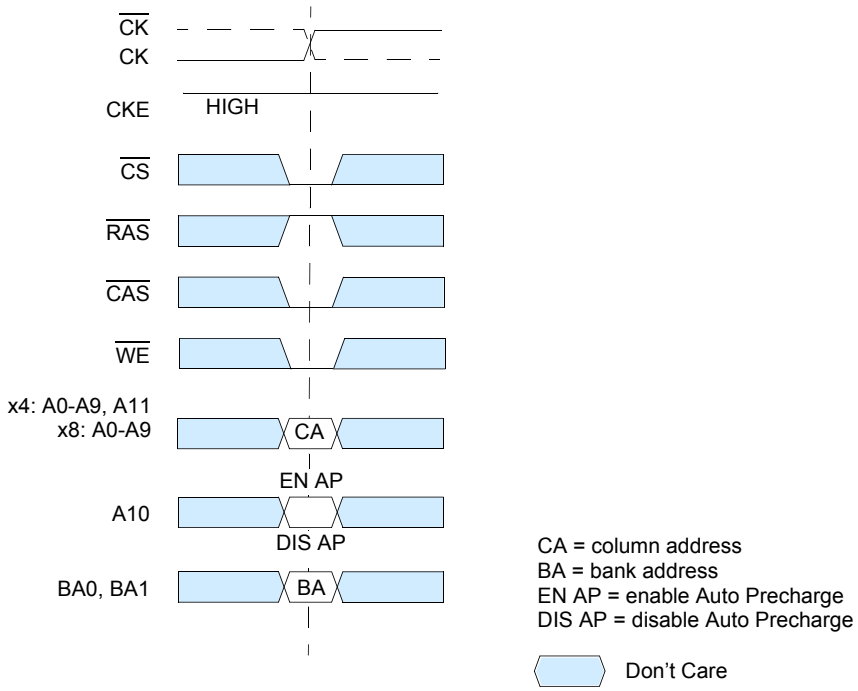
Data for any Write burst may be truncated by a subsequent (interrupting) Read command. This is illustrated in timing figures "Write to Read: Interrupting (CAS Latency =2; Burst Length = 8)", "Write to Read: Minimum D_{QSS}, Odd Number of Data (3 bit Write), Interrupting (CAS Latency = 2; Burst Length = 8)", and "Write to Read: Nominal D_{QSS}, Interrupting (CAS Latency = 2; Burst Length = 8)". Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in the diagrams noted previously.

Data for any Write burst may be followed by a subsequent Precharge command. To follow a Write without truncating the write burst, t_{WR} should be met as shown in timing figure *Write to Precharge: Non-Interrupting (Burst Length = 4)* on page 43.

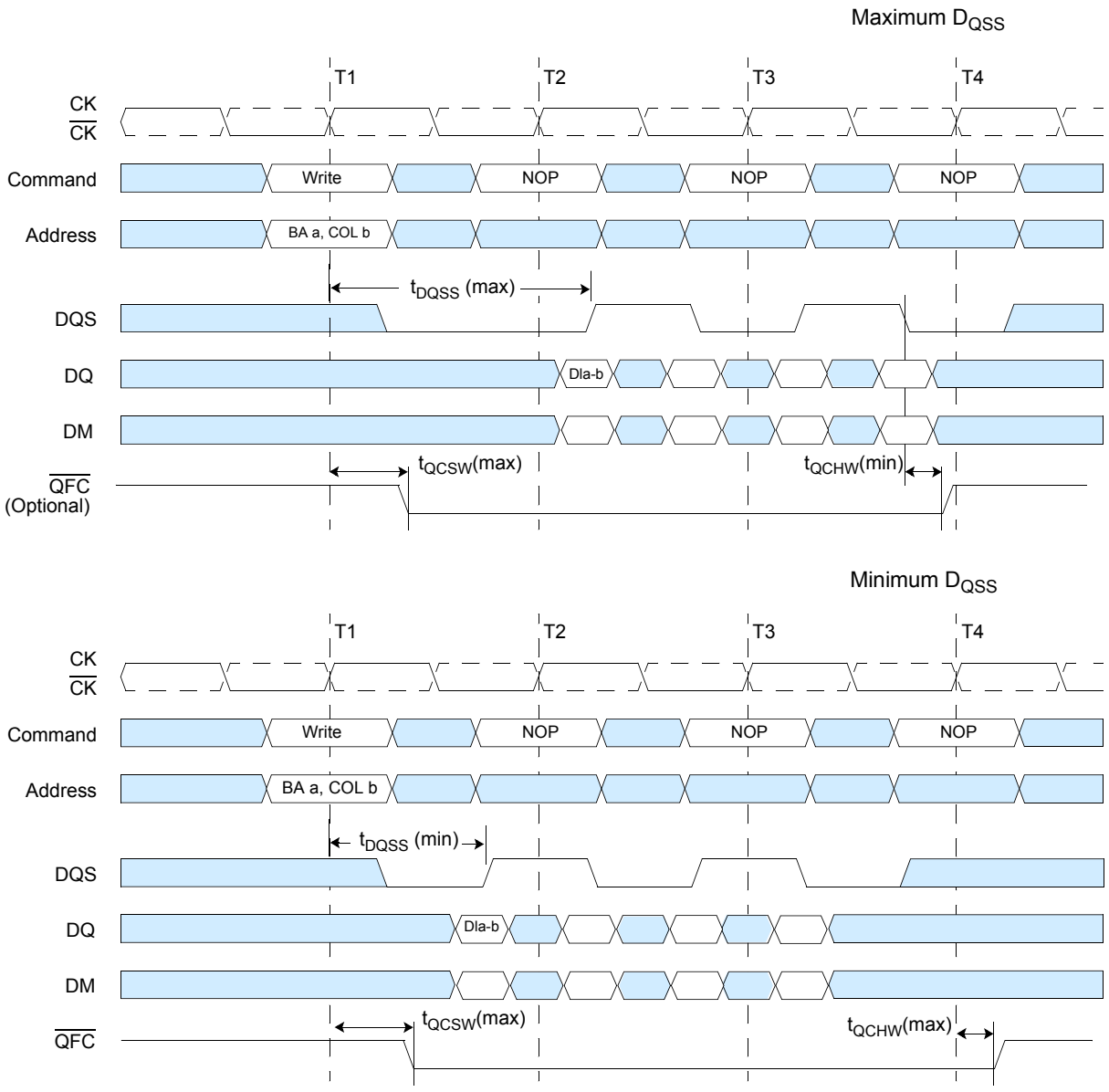
Data for any Write burst may be truncated by a subsequent Precharge command, as shown in timing figures *Write to Precharge: Interrupting (Burst Length = 4 or 8)* on page 44 to *Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)* on page 46. Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data in should be masked with DM. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

In the case of a Write burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same burst with Auto Precharge. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

Write Command



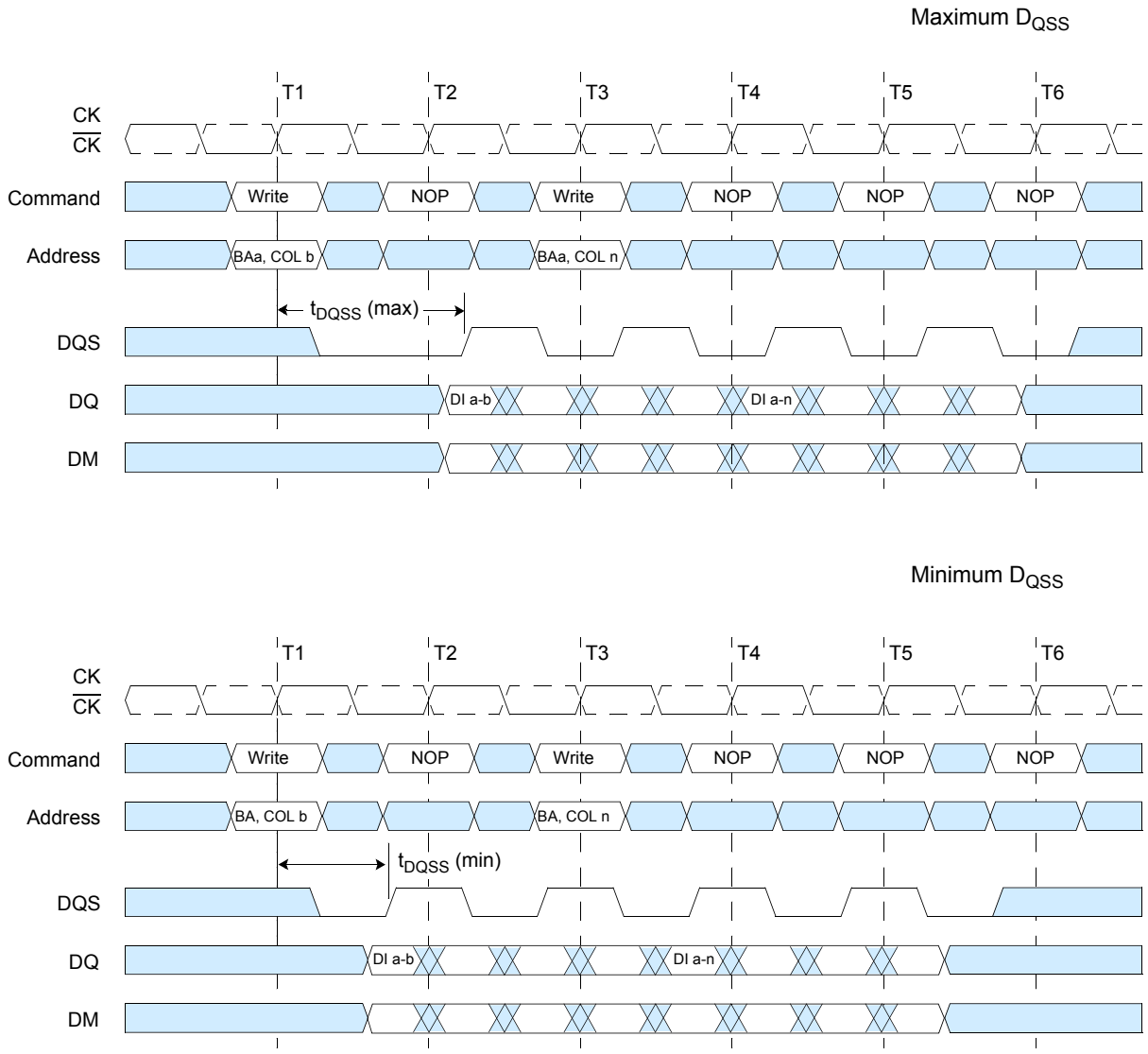
Write Burst (Burst Length = 4)



DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
A10 is Low with the Write command (Auto Precharge is disabled).
$\overline{QFC}$ is an open drain driver. Its output high level is achieved through an externally connected pull up resistor connected to V_{DDQ}.

Don't Care

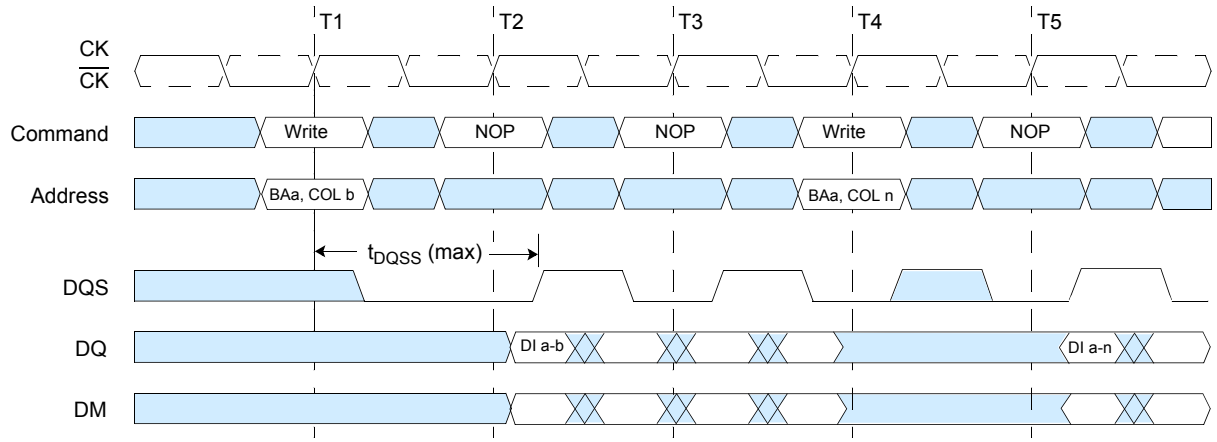
Write to Write (Burst Length = 4)



DI a-b = data in for bank a, column b, etc.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
3 subsequent elements of data in are applied in the programmed order following DI a-n.
A non-interrupted burst is shown.
Each Write command may be to any bank.

Don't Care

Write to Write: Max DQSS, Non-Consecutive (Burst Length = 4)

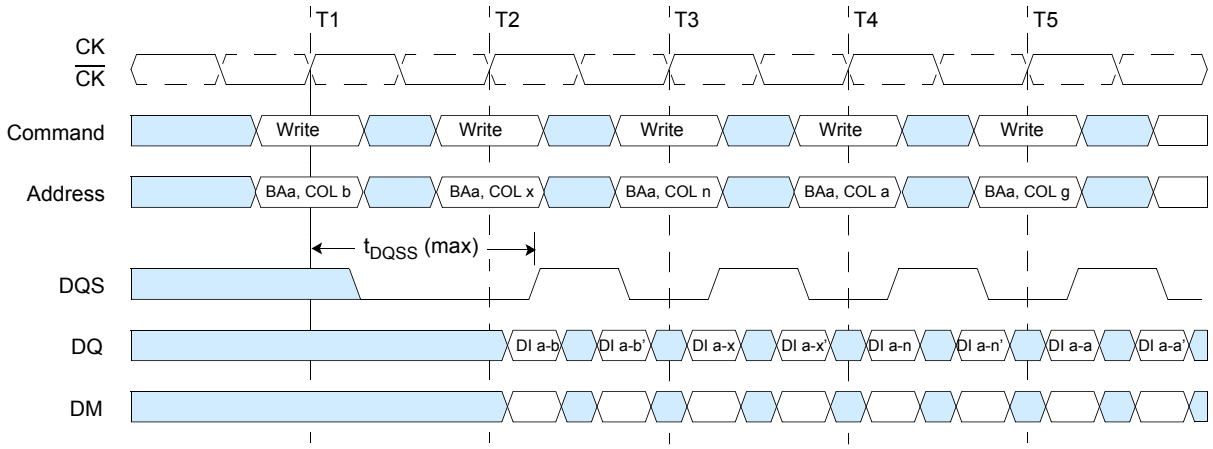


DI a-b, etc. = data in for bank a, column b, etc.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
3 subsequent elements of data in are applied in the programmed order following DI a-n.
A non-interrupted burst is shown.
Each Write command may be to any bank.

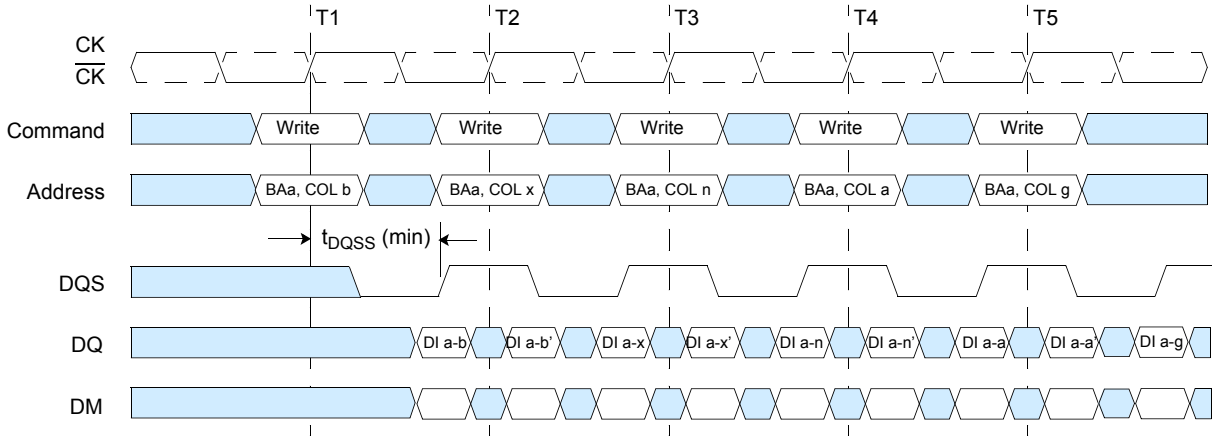
Don't Care

Random Write Cycles (Burst Length = 2, 4 or 8)

Maximum D_{QSS}



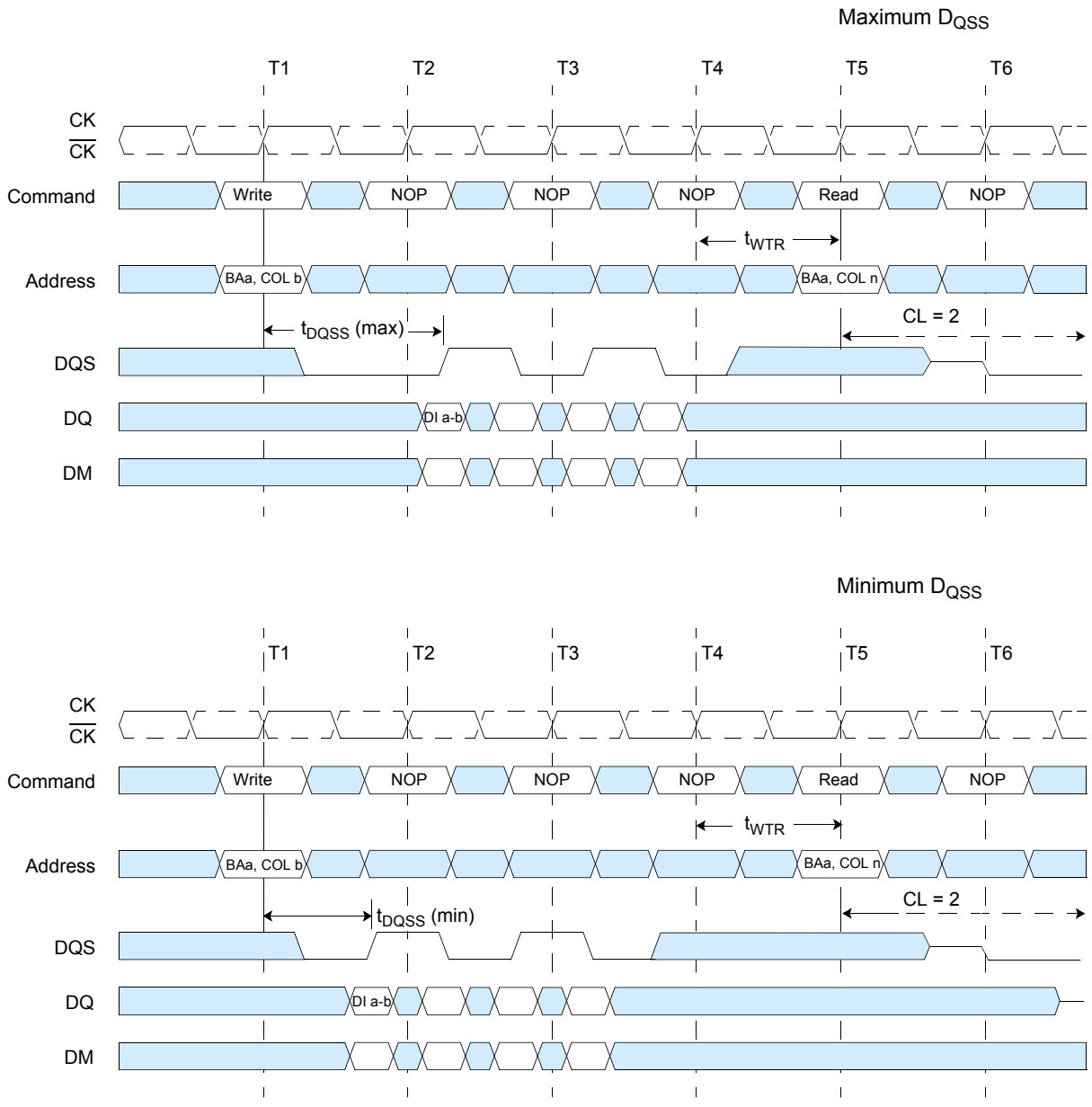
Minimum D_{QSS}



DI a-b, etc. = data in for bank a, column b, etc.
b', etc. = odd or even complement of b, etc. (i.e., column address LSB inverted).
Each Write command may be to any bank.

Don't Care

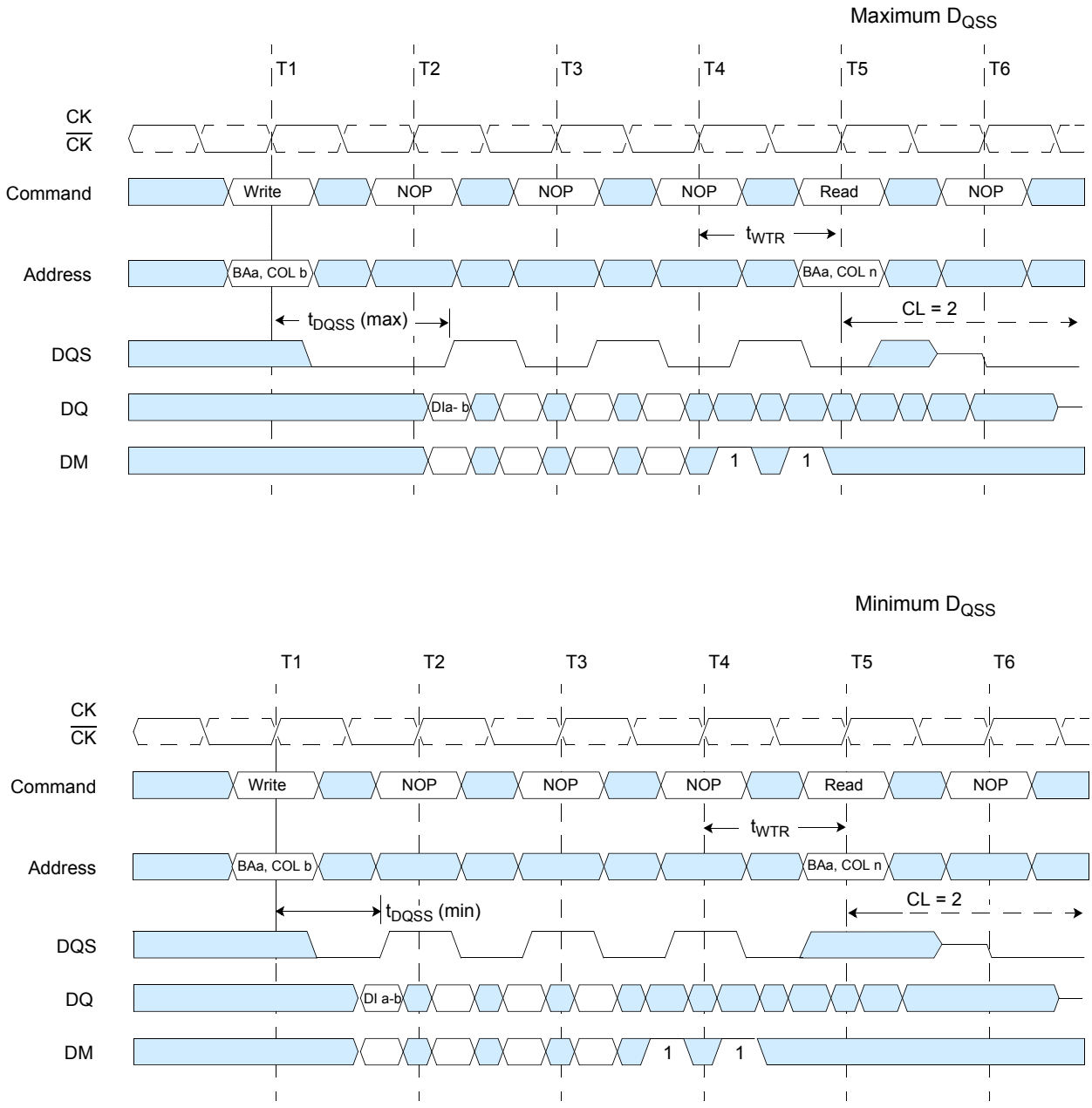
Write to Read: Non-Interrupting (CAS Latency = 2; Burst Length = 4)



DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
t_{WTR} is referenced from the first positive CK edge after the last data in pair.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands may be to any bank.

Don't Care

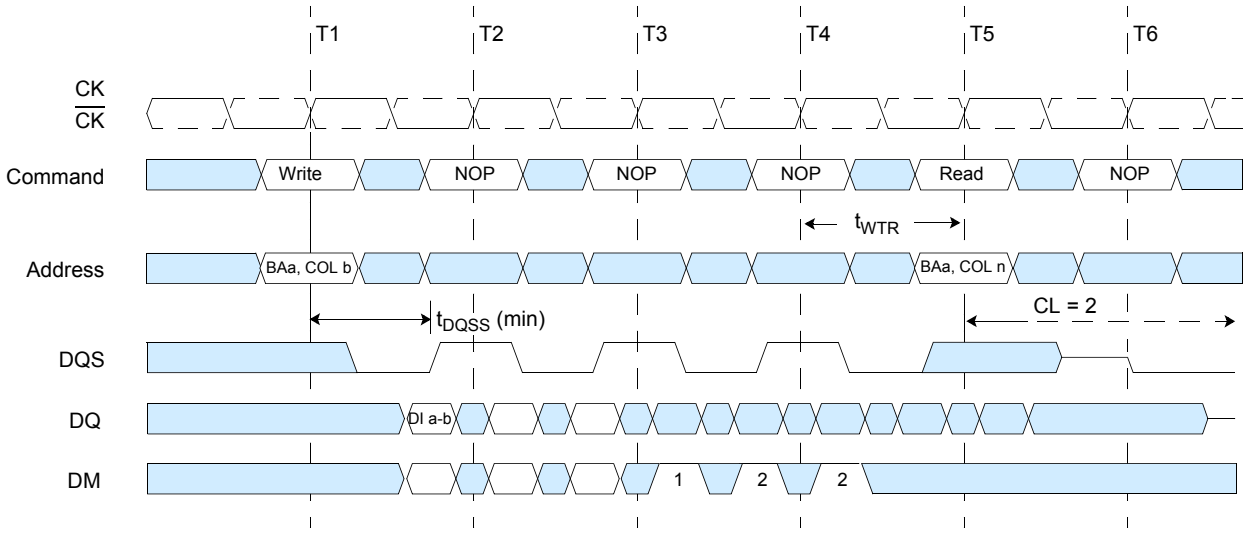
Write to Read: Interrupting (CAS Latency = 2; Burst Length = 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 4 data elements are written.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
t_{WTR} is referenced from the first positive CK edge after the last data in pair.
The Read command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands are not necessarily to the same bank.
1 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

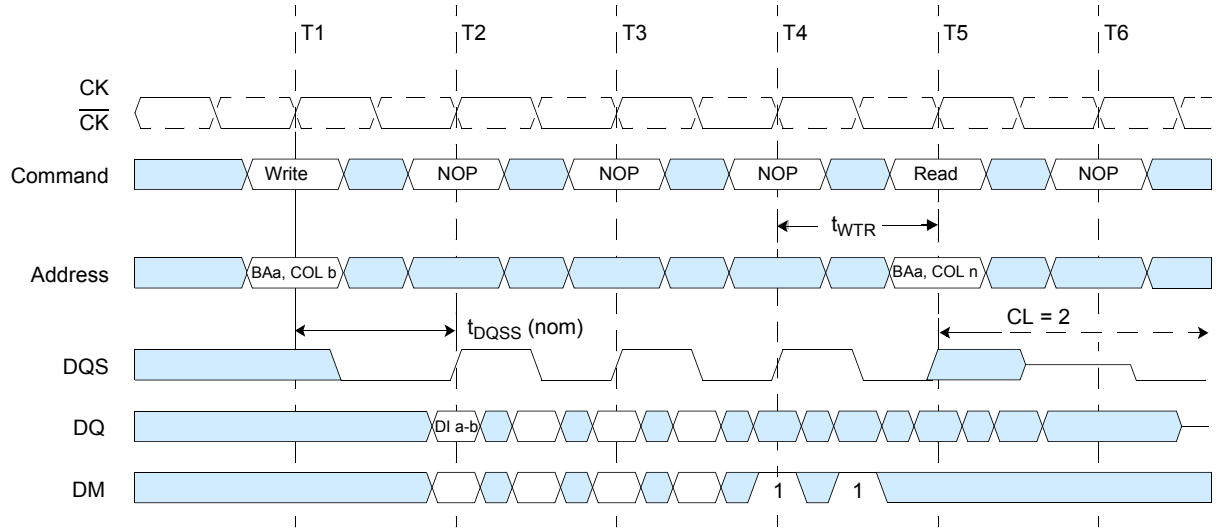
Write to Read: Minimum DQSS, Odd Number of Data (3 bit Write), Interrupting (CAS Latency = 2; Burst Length = 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 3 data elements are written.
2 subsequent elements of data in are applied in the programmed order following DI a-b.
t_{WTR} is referenced from the first positive CK edge after the last desired data in pair (not the last desired data in element)
The Read command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands are not necessarily to the same bank.
1 = This bit is correctly written into the memory array if DM is low.
2 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

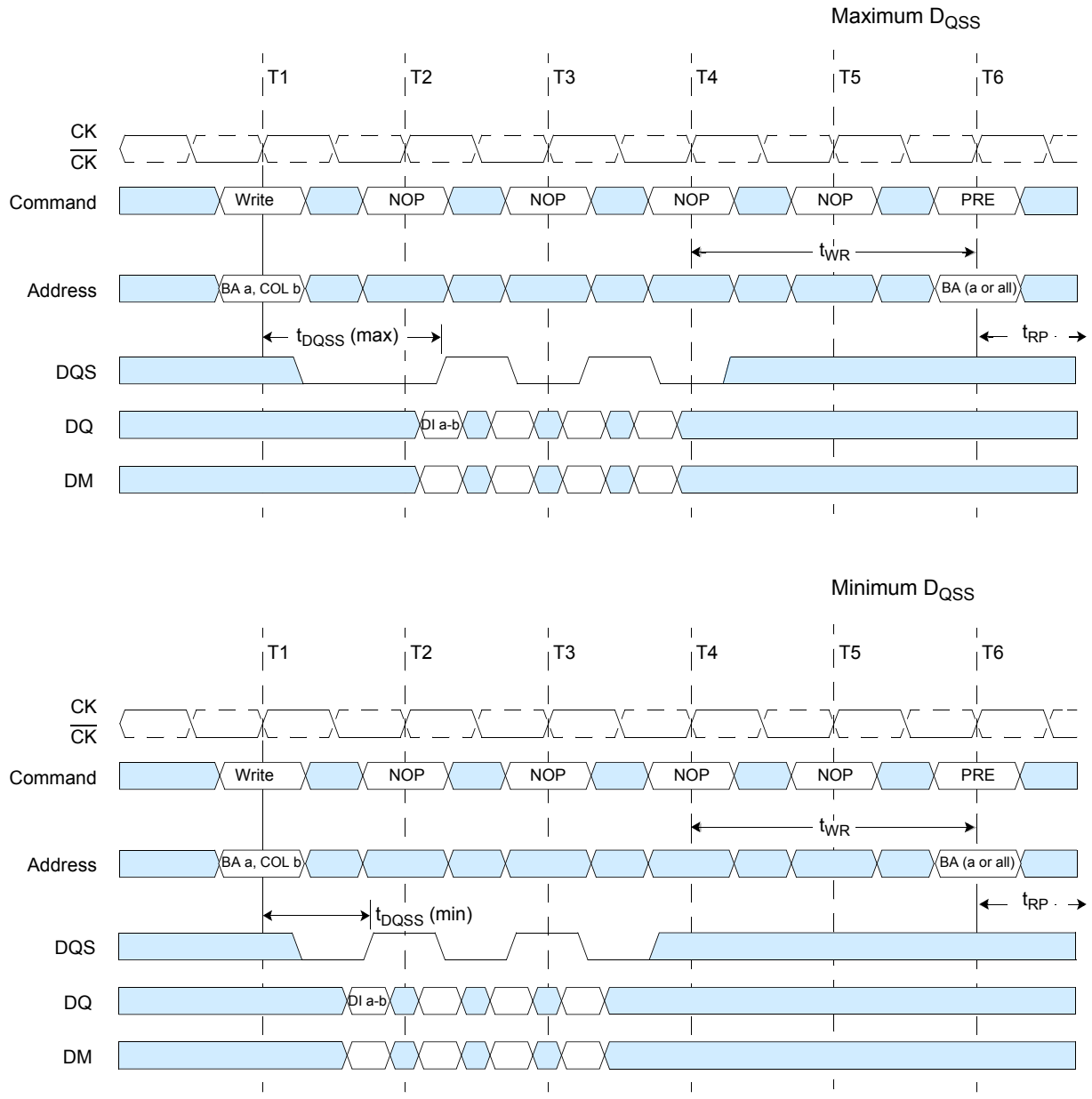
Write to Read: Nominal DQSS, Interrupting (CAS Latency = 2; Burst Length = 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 4 data elements are written.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
t_{WTR} is referenced from the first positive CK edge after the last desired data in pair.
The Read command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
The Read and Write commands are not necessarily to the same bank.
1 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

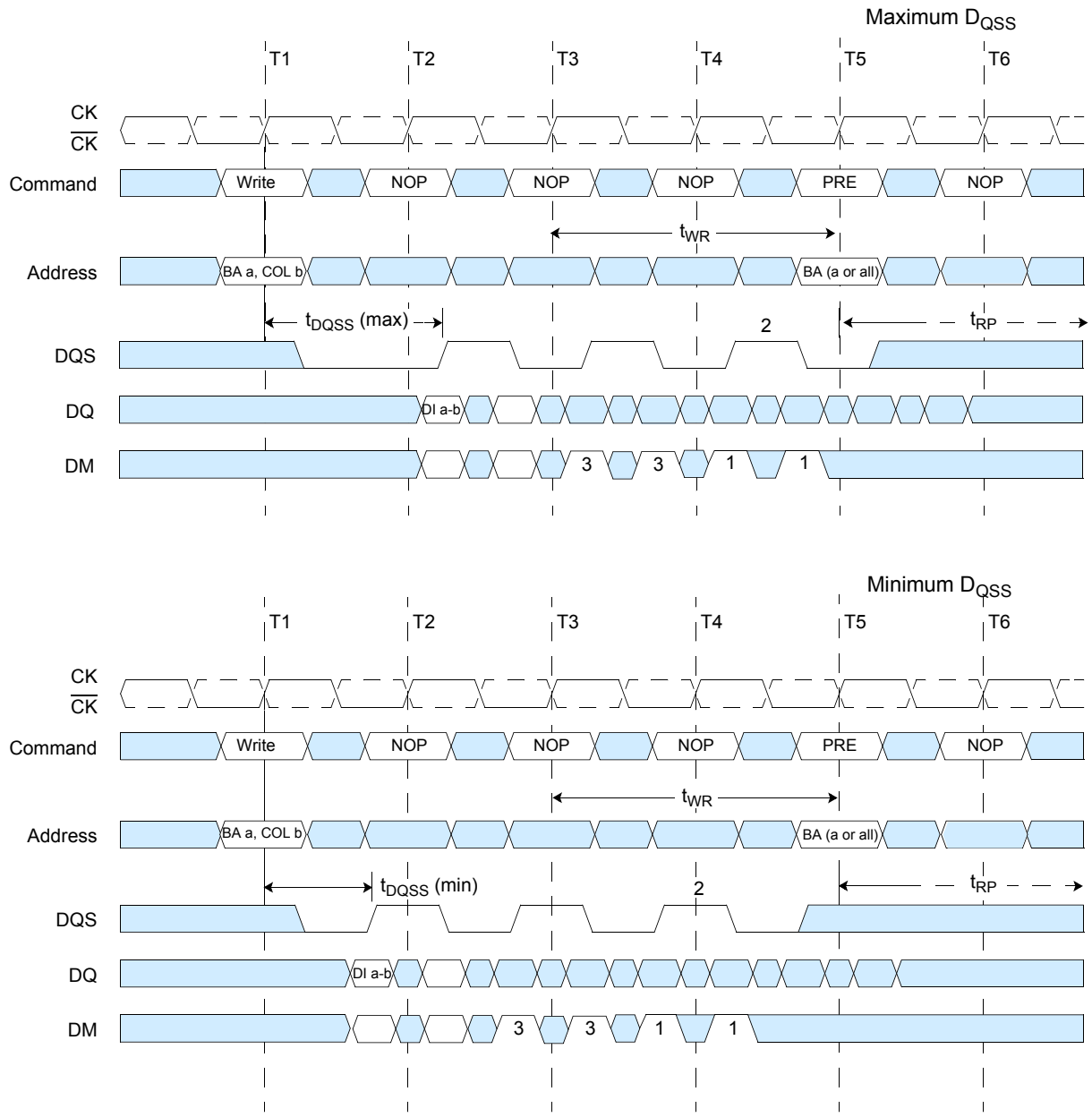
Write to Precharge: Non-Interrupting (Burst Length = 4)



DI a-b = data in for bank a, column b.
3 subsequent elements of data in are applied in the programmed order following DI a-b.
A non-interrupted burst is shown.
t_{WR} is referenced from the first positive CK edge after the last data in pair.
A10 is Low with the Write command (Auto Precharge is disabled).

Don't Care

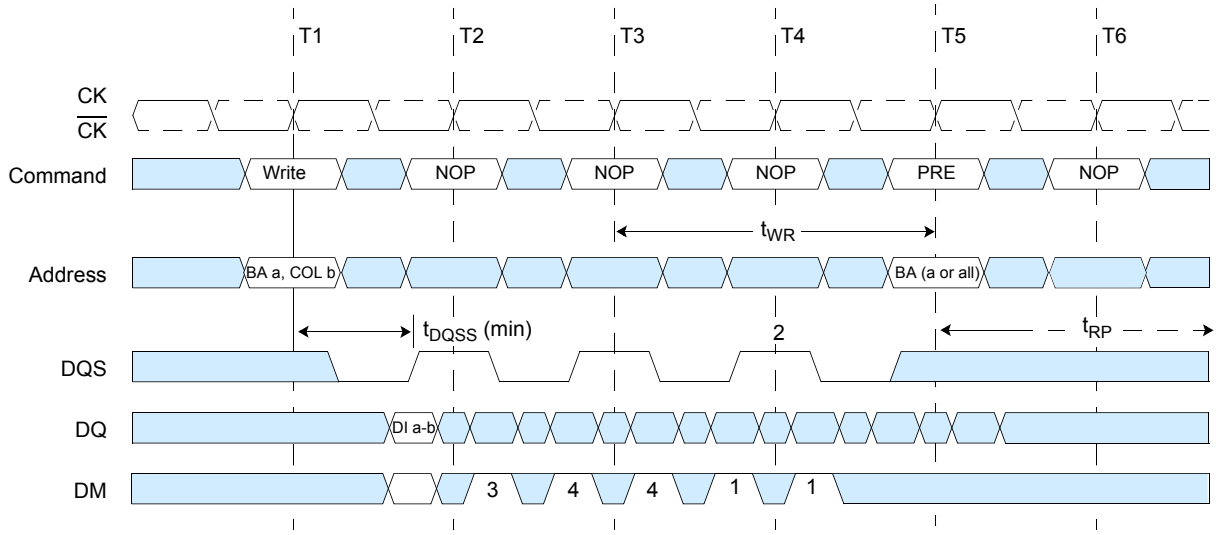
Write to Precharge: Interrupting (Burst Length = 4 or 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst, for burst length = 8.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

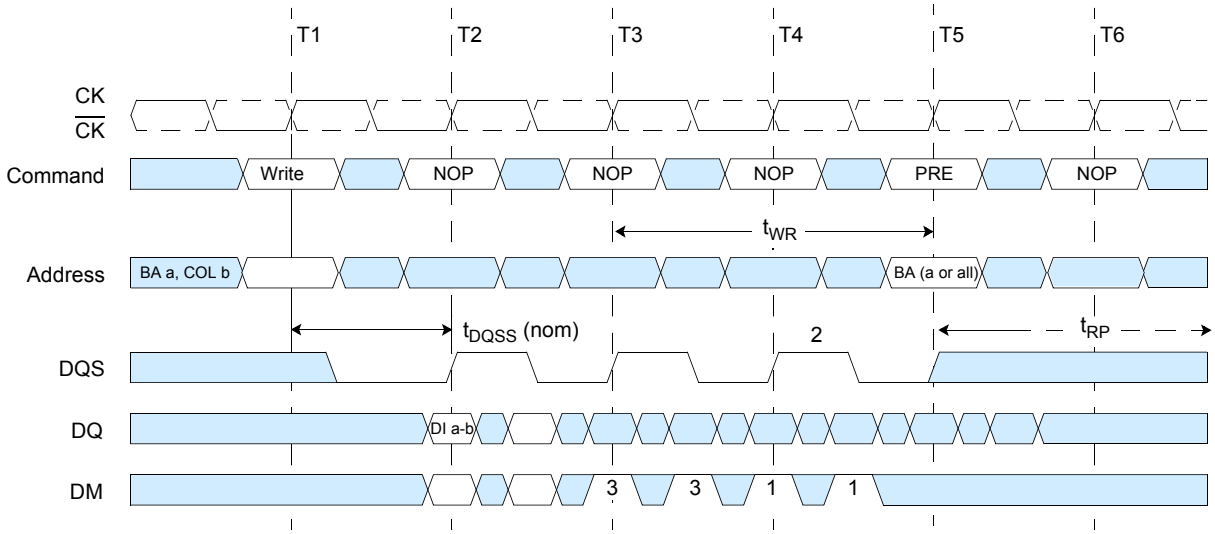
Write to Precharge: Minimum DQSS, Odd Number of Data (1 bit Write), Interrupting (Burst Length = 4 or 8)



DI a-b = data in for bank a, column b.
An interrupted burst is shown, 1 data element is written.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = This bit is correctly written into the memory array if DM is low.
4 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

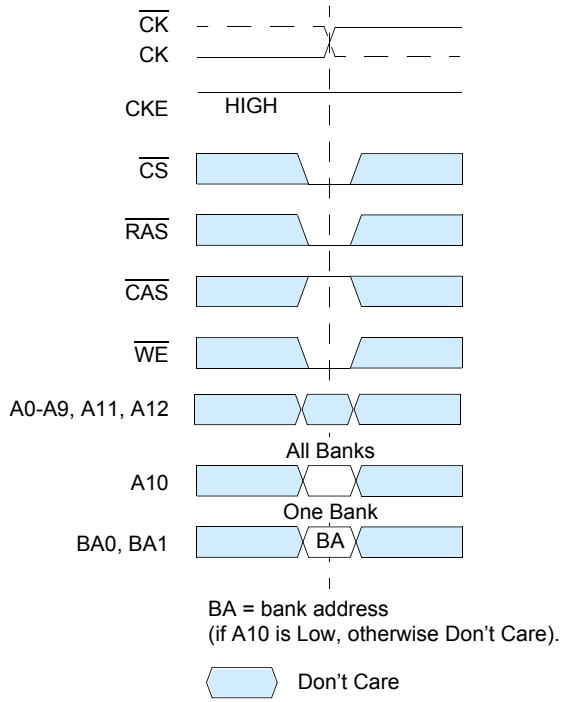
Write to Precharge: Nominal DQSS (2 bit Write), Interrupting (Burst Length = 4 or 8)



DI a-b = Data In for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Precharge Command



Precharge

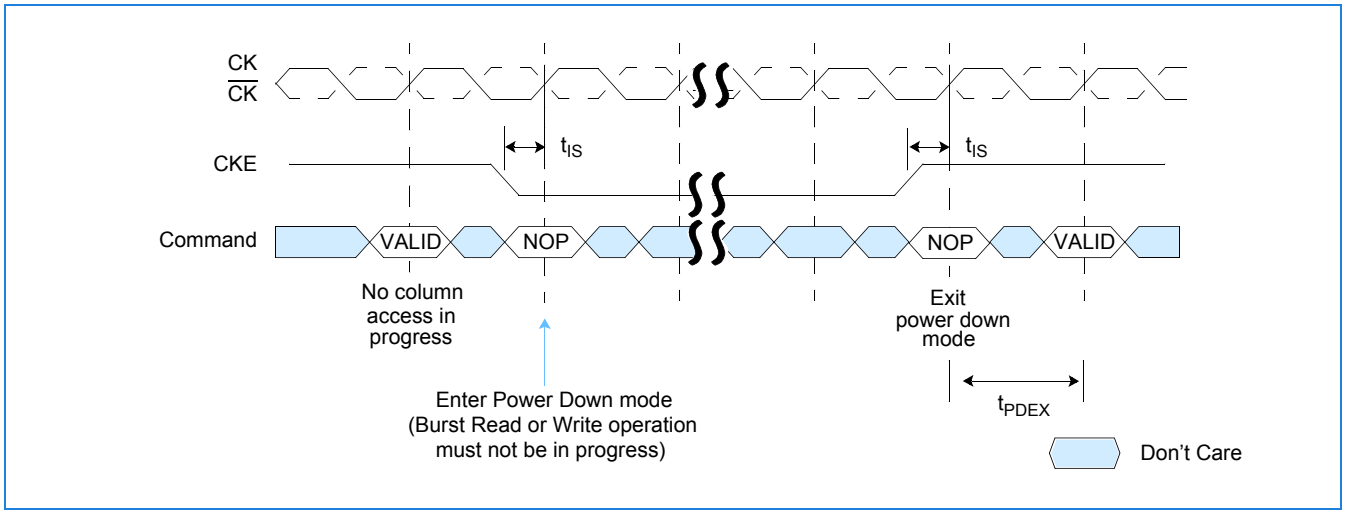
The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) is available for a subsequent row access some specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.

Power Down

Power Down is entered when CKE is registered low (no accesses can be in progress). If Power Down occurs when all banks are idle, this mode is referred to as Precharge Power Down; if Power Down occurs when there is a row active in any bank, this mode is referred to as Active Power Down. Entering Power Down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. The DLL is still running in Power Down mode, so for maximum power savings, the user has the option of disabling the DLL prior to entering Power Down. In that case, the DLL must be enabled after exiting Power Down, and 200 clock cycles must occur before a Read command can be issued. In Power Down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are “Don’t Care”. However, Power Down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled Power Down mode.

The Power Down state is synchronously exited when CKE is registered high (along with a Nop or Deselect command). A valid, executable command may be applied one clock cycle later.

Power Down



Truth Table 2: Clock Enable (CKE)

1. CKE n is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. Command n is the command registered at clock edge n, and action n is a result of command n.
4. All states and sequences not shown are illegal or reserved.

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	1
Power Down	L	L	X	Maintain Power Down	
Power Down	L	H	Deselect or NOP	Exit Power Down	
All Banks Idle	H	L	Deselect or NOP	Precharge Power Down Entry	
All Banks Idle	H	L	Auto Refresh	Self Refresh Entry	
Bank(s) Active	H	L	Deselect or NOP	Active Power Down Entry	
	H	H	See “Truth Table 3: Current State Bank n - Command to Bank n (Same Bank)” on page 50		

1. Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

Truth Table 3: Current State Bank n - Command to Bank n (Same Bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation	1-6
	L	H	H	H	No Operation	NOP. Continue previous operation	1-6
Idle	L	L	H	H	Active	Select and activate row	1-6
	L	L	L	H	Auto Refresh		1-7
	L	L	L	L	Mode Register Set		1-7
Row Active	L	H	L	H	Read	Select column and start Read burst	1-6, 10
	L	H	L	L	Write	Select column and start Write burst	1-6, 10
	L	L	H	L	Precharge	Deactivate row in bank(s)	1-6, 8
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	1-6, 10
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	1-6, 8
	L	H	H	L	Burst Terminate	Burst Terminate	1-6, 9
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	1-6, 10, 11
	L	H	L	L	Write	Select column and start Write burst	1-6, 10
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	1-6, 8, 11

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and t_{RP} has been met.
   - Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank.
   - Precharging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the idle state.
   - Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.
   - Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   - Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to Truth Table 4.
5. The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.
   - Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RFC} is met. Once t_{RFC} is met, the DDR SDRAM is in the “all banks idle” state.
   - Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR SDRAM is in the “all banks idle” state.
   - Precharging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks is in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.
9. Not bank-specific; Burst terminate affects the most recent Read burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
11. Requires appropriate DM masking.

Truth Table 4: Current State Bank n - Command to Bank m (Different bank)

(Part 1 of 2)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP/continue previous operation	1-6
	L	H	H	H	No Operation	NOP/continue previous operation	1-6
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m		1-6
Row Activating, Active, or Precharging	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-7
	L	H	L	L	Write	Select column and start Write burst	1-7
	L	L	H	L	Precharge		1-6
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start new Read burst	1-7
	L	L	H	L	Precharge		1-6
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-8
	L	H	L	L	Write	Select column and start new Write burst	1-7
	L	L	H	L	Precharge		1-6

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Read with Auto Precharge Enabled: See note 10.
   Write with Auto Precharge Enabled: See note 10.
4. Auto Refresh and Mode Register Set commands may only be issued when all banks are idle.
5. A Burst Terminate command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8. Requires appropriate DM masking.
9. A Write command may be applied after the completion of data output.
10. The Read with Auto Precharge enabled or Write with Auto Precharge enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible Precharge command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, Active, Precharge, Read, and Write commands to the other bank may be applied; during the access period, only Active and Precharge commands to the other bank may be applied. In either case, all other related limitations apply (e.g. contention between Read data and Write data must be avoided).

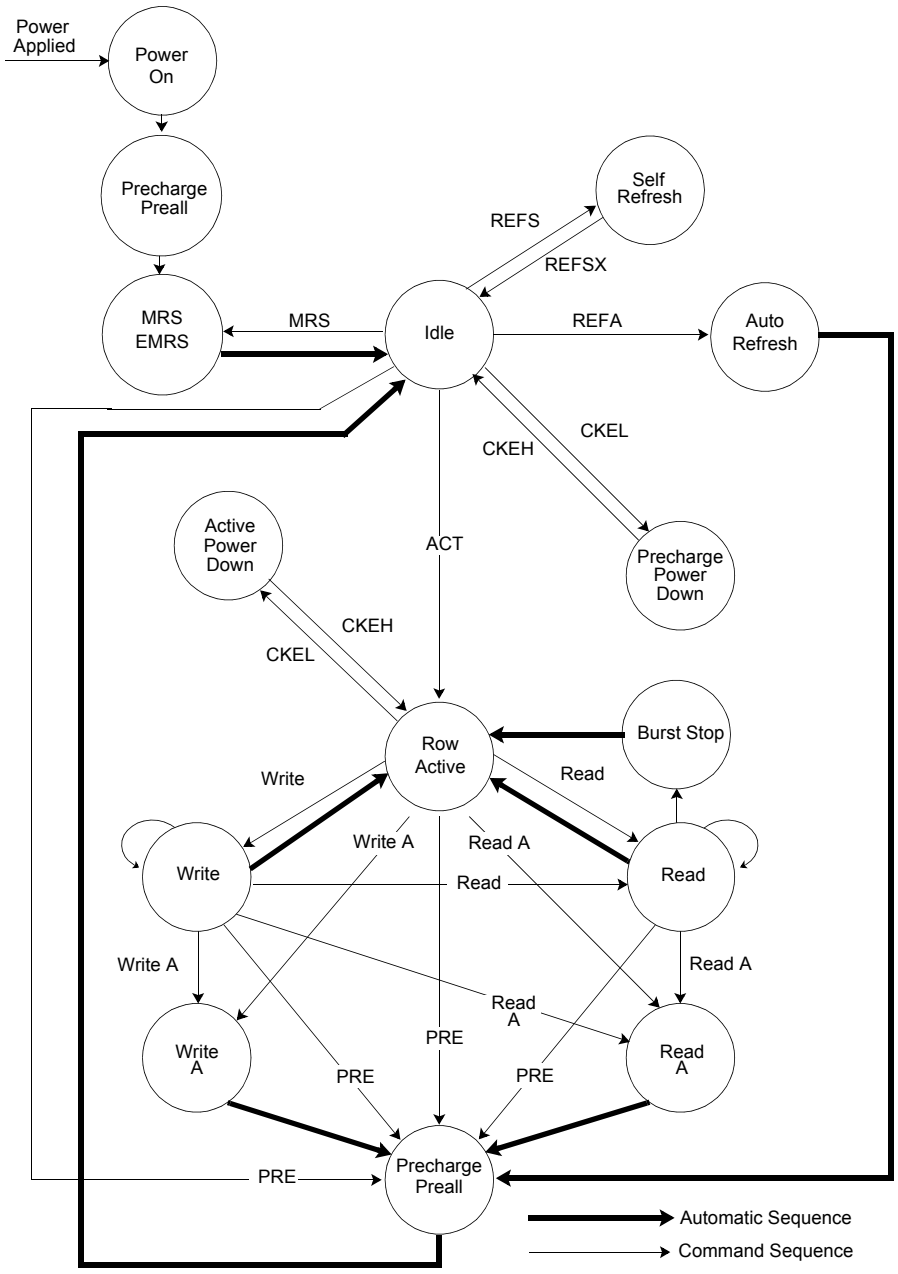
Truth Table 4: Current State Bank n - Command to Bank m (Different bank)

(Part 2 of 2)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start new Read burst	1-7,10
	L	H	L	L	Write	Select column and start Write burst	1-7,9,10
	L	L	H	L	Precharge		1-6
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1-6
	L	H	L	H	Read	Select column and start Read burst	1-7,10
	L	H	L	L	Write	Select column and start new Write burst	1-7,10
	L	L	H	L	Precharge		1-6

1. This table applies when CKE n-1 was high and CKE n is high (see Truth Table 2: Clock Enable (CKE) and after t_{XSNR} / t_{XSRD} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Read with Auto Precharge Enabled: See note 10.
   Write with Auto Precharge Enabled: See note 10.
4. Auto Refresh and Mode Register Set commands may only be issued when all banks are idle.
5. A Burst Terminate command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8. Requires appropriate DM masking.
9. A Write command may be applied after the completion of data output.
10. The Read with Auto Precharge enabled or Write with Auto Precharge enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible Precharge command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, Active, Precharge, Read, and Write commands to the other bank may be applied; during the access period, only Active and Precharge commands to the other bank may be applied. In either case, all other related limitations apply (e.g. contention between Read data and Write data must be avoided).

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	−0.5 to V_{DDQ}+ 0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	−0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	−0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	−0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to +150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Min.	Max.	Units	Notes
Input Capacitance: CK, $\overline{CK}$	CI_1	2.0	3.0	pF	1
Delta Input Capacitance: CK, $\overline{CK}$	delta CI_1		0.25	pF	1
Input Capacitance: All other input-only pins (except DM)	CI_2	2.0	3.0	pF	1
Delta Input Capacitance: All other input-only pins (except DM)	delta CI_2		0.5	pF	1
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	1, 2
Delta Input/Output Capacitance: DQ, DQS, DM	delta C_{IO}		0.5	pF	1

1. $V_{DDQ} = V_{DD} = 2.5V \pm 0.2V$ (minimum range to maximum range), f = 100MHz, $T_A = 25°C$, $VO_{DC} = V_{DDQ/2}$, $VO_{Peak\text{-}Peak} = 0.2V$.
2. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match input propagation times of DQ, DQS and DM in the system.

DC Electrical Characteristics and Operating Conditions

(0°C £ T_A £ 70×C; $V_{DDQ} = V_{DD}$ = + 2.5V ± 0.2V (DDR266/333); $V_{DDQ} = V_{DD}$ = + 2.6V ± 0.1V (DDR400), see AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage DDR266/333	2.3	2.7	V	1
V_{DD}	Supply Voltage DDR400	2.5	2.7	V	1
V_{DDQ}	I/O Supply Voltage DDR266/333	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage DDR400	2.5	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
$V_{IH(DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL(DC)}$	Input Low (Logic0) Voltage	– 0.3	V_{REF} – 0.15	V	1
$V_{IN(DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs	– 0.3	V_{DDQ} + 0.3	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
$V_{IX(DC)}$	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
VI_{Ratio}	V-I Matching Pullup Current to Pulldown Current Ratio	0.71	1.4		5
I_I	Input Leakage Current Any input $0V \le V_{IN} \le V_{DD}$; (All other pins not under test = 0V)	– 2	2	µA	1
I_{OZ}	Output Leakage Current (DQs are disabled; $0V \le V_{out} \le V_{DDQ}$	– 5	5	µA	1

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

DC Electrical Characteristics and Operating Conditions

(0°C £ T_A £ 70×C; V_{DDQ} = V_{DD} = + 2.5V ± 0.2V (DDR266/333); V_{DDQ} = V_{DD} = + 2.6V ± 0.1V (DDR400), see AC Characteristics)

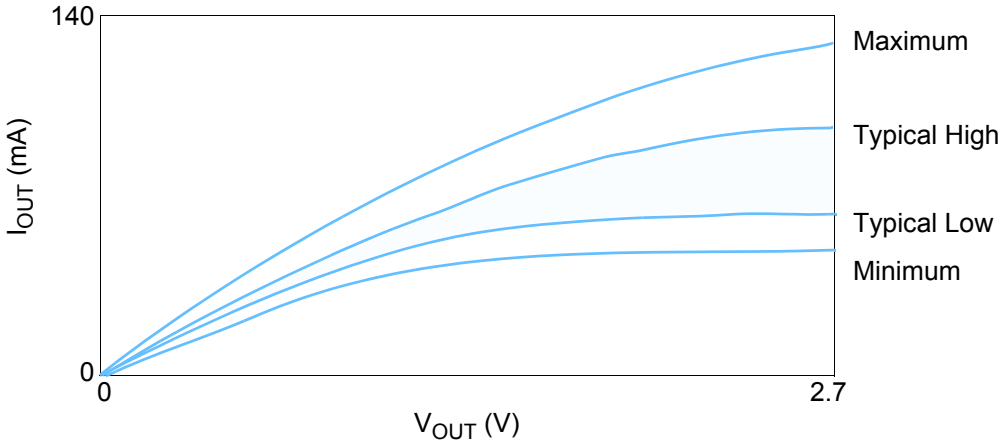
Symbol	Parameter	Min	Max	Units	Notes
I_{OH}	Output Current: Nominal Strength Driver High current (V_{OUT}= V_{DDQ} -0.373V, min V_{REF}, min V_{TT})	– 16.8		mA	1
I_{OL}	Low current (V_{OUT}= 0.373V, max V_{REF}, max V_{TT})	16.8			
I_{OHW}	Output Current: Half- Strength Driver High current (V_{OUT}= V_{DDQ} -0.763V, min V_{REF}, min V_{TT})	– 9.0		mA	1
I_{OLW}	Low current (V_{OUT}= 0.763V, max V_{REF}, max V_{TT})	9.0			

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

Normal Strength Driver Pulldown and Pullup Characteristics

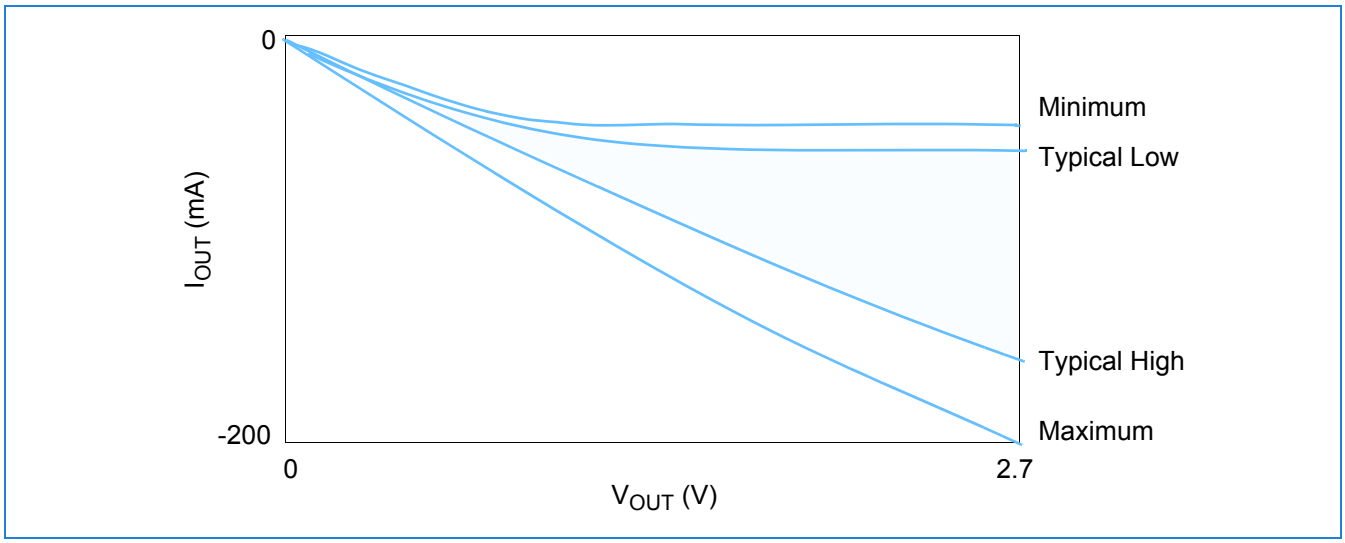
1. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve.
2. It is recommended that the “typical” IBIS pulldown V-I curve lie within the shaded region of the V-I curve.

Normal Strength Driver Pulldown Characteristics



3. The full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve.
4. It is recommended that the “typical” IBIS pullup V-I curve lie within the shaded region of the V-I curve.

Normal Strength Driver Pullup Characteristics



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
6. The full variation in the ratio of the “typical” IBIS pullup to “typical” IBIS pulldown current should be unity ± 10%, for device drain to source voltages from 0.1 to 1.0. This specification is a design objective only. It is not guaranteed.
7. These characteristics are intended to obey the SSTL_2 class II standard.
8. This specification is intended for DDR SDRAM only.

Normal Strength Driver Pulldown and Pullup Currents

	Pulldown Current (mA)				Pullup Current (mA)			
Voltage (V)	Typical Low	Typical High	Min	Max	Typical Low	Typical High	Min	Max
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Normal Strength Driver Evaluation Conditions

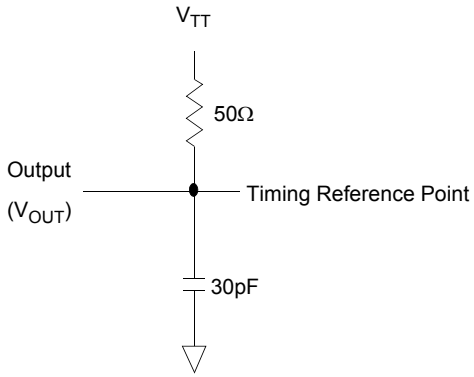
	Typical	Minimum	Maximum
Temperature ($T_{ambient}$)	25 °C	70 °C	0 °C
V_{DDQ}	2.5V	2.3V	2.7V
Process conditions	typical process	slow-slow process	fast-fast process

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.

AC Output Load Circuit Diagrams



AC Input Operating Conditions

(0 °C ≤ T_A ≤ 70 °C; V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR266/333); V_{DD} = V_{DDQ} = 2.6V ± 0.1V (DDR400); See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	V_{REF} + 0.31		V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals		V_{REF} – 0.31	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX(AC)}$	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.5*V_{DDQ} – 0.2	0.5*V_{DDQ} + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

I_{DD} Specifications and Conditions

(0 °C ≤ T_A ≤ 70 °C; V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR266/333); V_{DD} = V_{DDQ} = 2.6V ± 0.1V (DDR400); See AC Characteristics)

Symbol	Parameter/Condition	DDR400 (5T) t_{CK}=5ns	DDR333 (6K) t_{CK}=6ns	DDR266B (75B) t_{CK}=7.5ns	Unit	Notes
I_{DD0}	**Operating Current**: one bank; active / precharge; t_{RC} = t_{RC} (min); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	120	110	100	mA	1
I_{DD1}	**Operating Current**: one bank; active / read / precharge; Burst = 2; t_{RC} = t_{RC} (min); CL = 2.5; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	140	120	105	mA	1
I_{DD2P}	**Precharge Power Down Standby Current**: all banks idle; Power Down mode; CKE ≤ V_{IL} (max)	7	7	7	mA	1
I_{DD2N}	**Idle Standby Current:** $\overline{CS}$ ≥ V_{IH} (min); all banks idle; CKE ≥ V_{IH} (min); address and control inputs changing once per clock cycle	35	35	35	mA	1
I_{DD3P}	**Active Power Down Standby Current**: one bank active; Power Down mode; CKE ≤ V_{IL} (max)	20	15	15	mA	1
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS}$ ≥ V_{IH} (min); CKE ≥ V_{IH} (min); t_{RC} = t_{RAS} (max); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	60	50	50	mA	1
I_{DD4R}	**Operating Current:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; I_{OUT} = 0mA	160	140	120	mA	1
I_{DD4W}	**Operating Current**: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5	210	180	150	mA	1
I_{DD5}	**Auto-Refresh Current**: t_{RC} = t_{RFC} (min)	250	230	210	mA	1
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V	5	5	5	mA	1, 2
I_{DD7}	**Operating current**: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	420	400	380	mA	1

1. I_{DD} specifications are tested after the device is properly initialized.
2. Enables on-chip refresh and address counters.
   Values are averaged from high and low temp values using x16 devices.

Electrical Characteristics & AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C; V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR266/333); V_{DD} = V_{DDQ} = 2.6V ± 0.1V (DDR400); See AC Characteristics)

Symbol	Parameter		DDR400 (5T)		DDR333 (6K)		DDR266B (75B)		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		− 0.65	+ 0.65	− 0.7	+ 0.7	− 0.75	+ 0.75	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		− 0.55	+ 0.55	− 0.6	+ 0.6	− 0.75	+ 0.75	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CK}	Clock cycle time	CL = 3.0	5	8					ns	1-4
		CL = 2.5	6	12	6	12	7.5	12	ns	1-4
		CL = 2.0			7.5	12	10	12	ns	1-4
t_{DH}	DQ and DM input hold time		0.4		0.45		0.5		ns	1-4, 15, 16
t_{DS}	DQ and DM input setup time		0.4		0.45		0.5		ns	1-4, 15, 16
t_{IPW}	Input pulse width		2.2		2.2		2.2		ns	2-4, 12
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		1.75		1.75		ns	1-4
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$		− 0.6	+ 0.6	− 0.7	+ 0.7	− 0.75	+ 0.75	ns	1-4, 5
t_{LZ}	Data-out low-impedance time from CK/$\overline{CK}$		− 0.6	+ 0.6	− 0.7	+ 0.7	− 0.75	+ 0.75	ns	1-4, 5
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	TSOP Package		+ 0.4		+ 0.45		+ 0.5	ns	1-4
		BGA Package		+ 0.4		+ 0.4		+ 0.5	ns	1-4
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		t_{CK}	1-4
t_{QH}	Data output hold time from DQS		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{CK}	1-4
t_{QHS}	Data hold Skew Factor	TSOP Package		0.5		0.55		0.75	ns	1-4
		BGA Package		0.5		0.5		0.75	ns	1-4
t_{DQSS}	Write command to 1st DQS latching transition		0.72	1.28	0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSH}	DQS input high pulse width (write cycle)		0.35		0.35		0.35		t_{CK}	1-4
t_{DQSL}	DQS input low pulse width (write cycle)		0.35		0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		2		2		2		t_{CK}	1-4
t_{WPRES}	Write preamble setup time		0		0		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		0.25		0.25		t_{CK}	1-4
t_{IH}	Address and control input hold time (fast slew rate)		0.6		0.75		0.9		ns	2-4, 9, 11, 12
t_{IS}	Address and control input setup time (fast slew rate)		0.6		0.75		0.9		ns	2-4, 9, 11, 12
t_{IH}	Address and control input hold time (slow slew rate)		0.7		0.8		1.0		ns	2-4, 10-12, 14
t_{IS}	Address and control input setup time (slow slew rate)		0.7		0.8		1.0		ns	2-4, 10, 11, 12, 14
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4

Electrical Characteristics & AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C; V_{DD} = V_{DDQ} = 2.5V ± 0.2V (DDR266/333); V_{DD} = V_{DDQ} = 2.6V ± 0.1V (DDR400); See AC Characteristics)

Symbol	Parameter	DDR400 (5T)		DDR333 (6K)		DDR266B (75B)		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAS}	Active to Precharge command	40	120,000	42	120,000	45	120,000	ns	1-4
t_{RC}	Active to Active/Auto-refresh command period	55		60		65		ns	1-4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	70		72		75		ns	1-4
t_{RCD}	Active to Read or Write delay	15		18		20		ns	1-4
t_{RAP}	Active to Read Command with Autoprecharge	min (t_{RCD}, t_{RAS})		min (t_{RCD}, t_{RAS})		min (t_{RCD}, t_{RAS})		ns	1-4
t_{RP}	Precharge command period	15		18		20		ns	1-4
t_{RRD}	Active bank A to Active bank B command	10		12		15		ns	1-4
t_{WR}	Write recovery time	15		15		15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}	1-4, 13
t_{WTR}	Internal write to read command delay	2		1		1		t_{CK}	1-4
t_{PDEX}	Power down exit time	5		6		7.5		ns	1-4
t_{XSNR}	Exit self-refresh to non-read command	75		75		75		ns	1-4
t_{XSRD}	Exit self-refresh to read command	200		200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval		7.8		7.8		7.8	µs	1-4, 8

Electrical Characteristics & AC Timing - Absolute Specifications Notes

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$ is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For command/address input slew rate $\geq$ 1.0V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
10. For command/address input slew rate $\geq$ 0.5V/ns and < 1.0V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
11. CK/$\overline{CK}$ slew rates are $\geq$ 1.0V/ns.
12. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
13. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time. For example, for DDR266B at CL = 2.5, t_{DAL} = (15ns/7.5ns) + (20ns/7.5ns) = 2 + 3 = 5.

14. An input setup and hold time derating table is used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{IS})	delta (t_{IH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+50	0	ps	1,2
0.3 V/ns	+100	0	ps	1,2

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

15. An input setup and hold time derating table is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+75	+75	ps	1,2
0.3 V/ns	+150	+150	ps	1,2

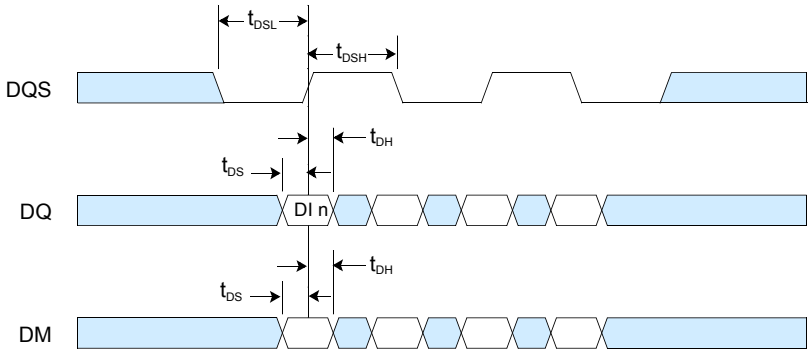
1. I/O slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

16. An I/O Delta Rise, Fall Derating table is used to increase t_{DS} and t_{DH} in the case where DQ, DM, and DQS slew rates differ.

Input Slew Rate	delta (t_{DS})	delta (t_{DH})	Unit	Notes
0.0 V/ns	0	0	ps	1,2,3,4
0.25 V/ns	+50	+50	ps	1,2,3,4
0.5 V/ns	+100	+100	ps	1,2,3,4

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH(AC)}$ to $V_{IL(AC)}$ or $V_{IH(DC)}$ to $V_{IL(DC)}$, similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
   For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns
   Delta rise, fall = (1/0.5) - (1/0.4) [ns/V]
   = -0.5 ns/V
   Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

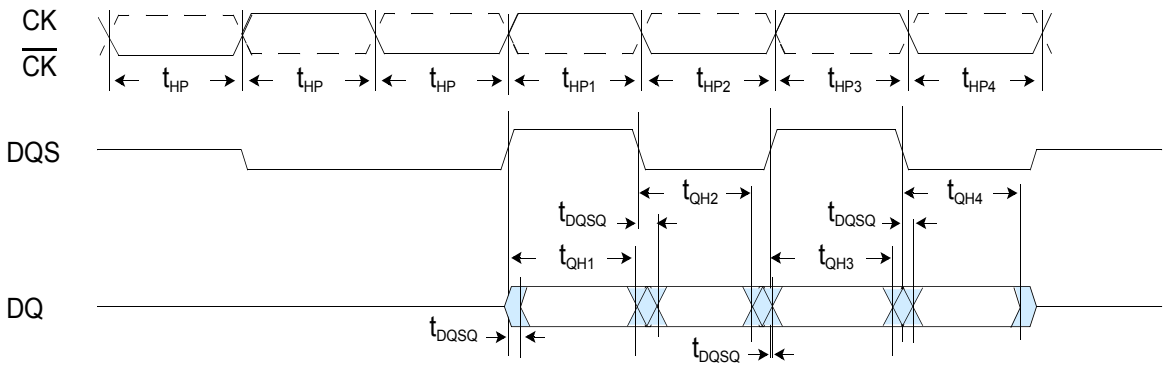
Data Input (Write) (Timing Burst Length = 4)



DI n = Data In for column n.
3 subsequent elements of data in are applied in programmed order following DI n.

Don't Care

Data Output (Read) (Timing Burst Length = 4)

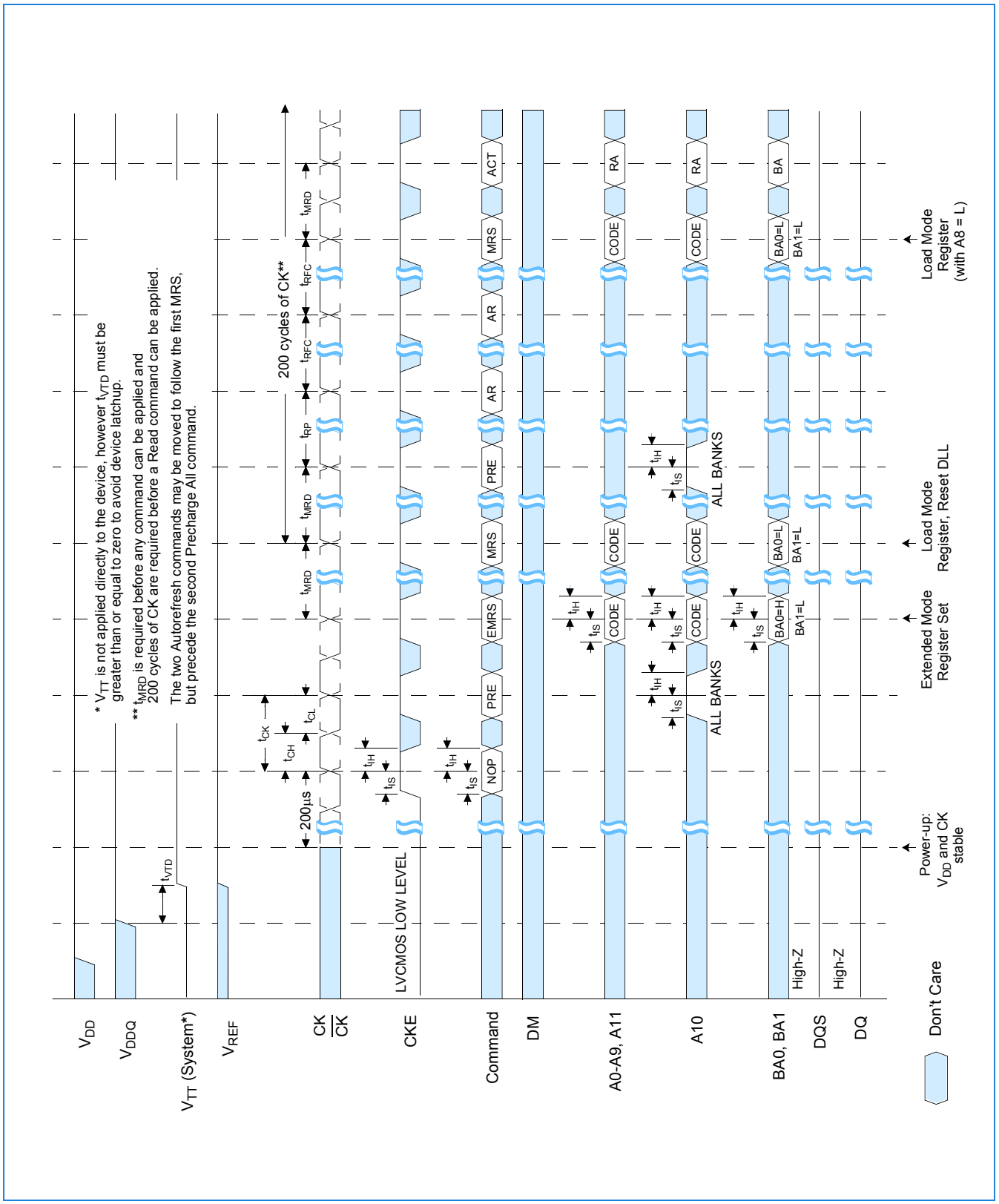


t_{HP} is the half cycle pulse width for each half cycle clock. t_{HP} is referenced to the clock duty cycle only and not to the data strobe (DQS) duty cycle.

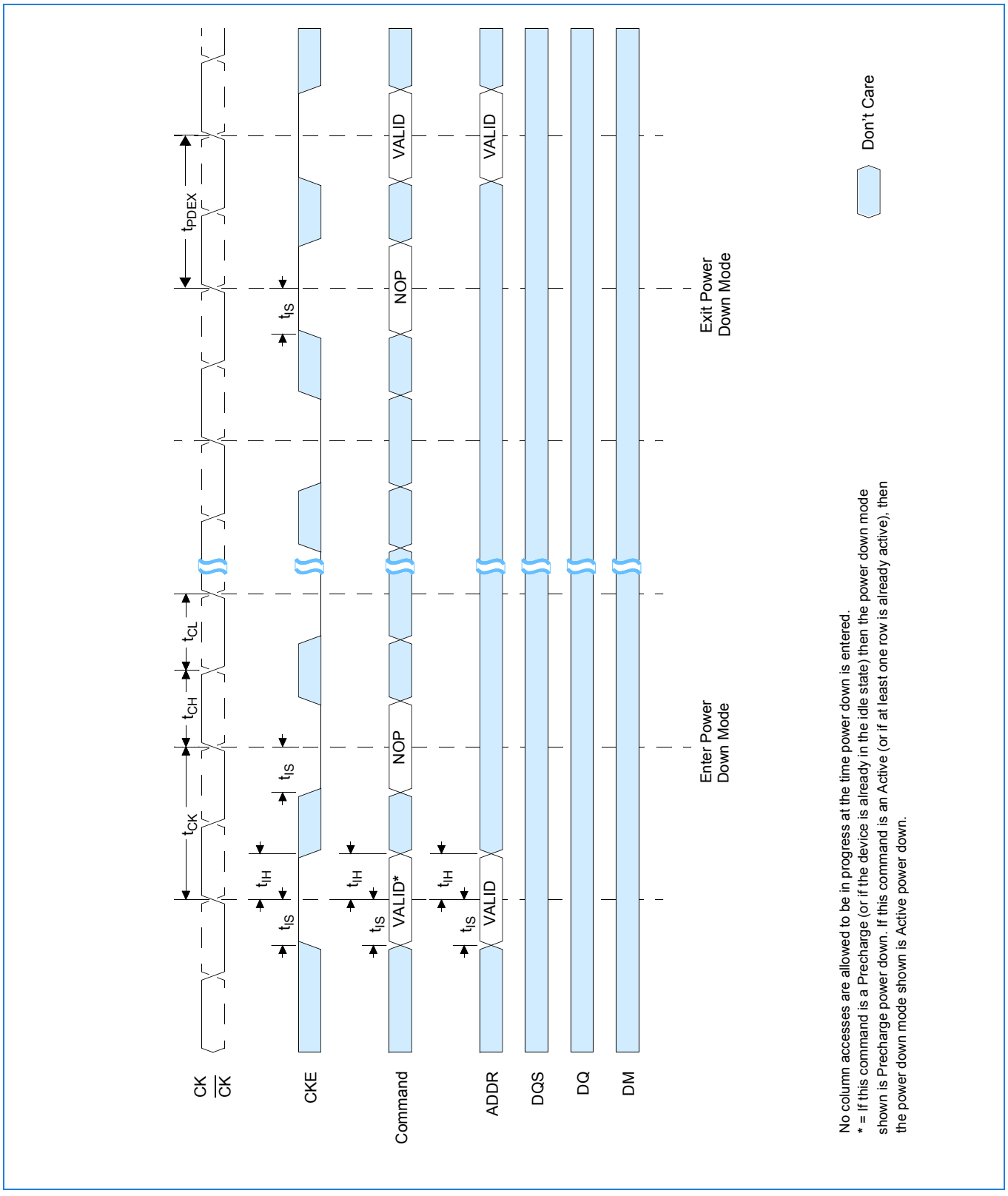
Data Output hold time from Data Strobe is shown as t_{QH}. t_{QH} is a function of the clock high or low time (t_{HP}) for that given clock cycle. Note correlation of t_{HP} to t_{QH} in the diagram above (t_{HP1} to t_{QH1}, etc.).

t_{DQSQ} (max) occurs when DQS is the earliest among DQS and DQ signals to transition.

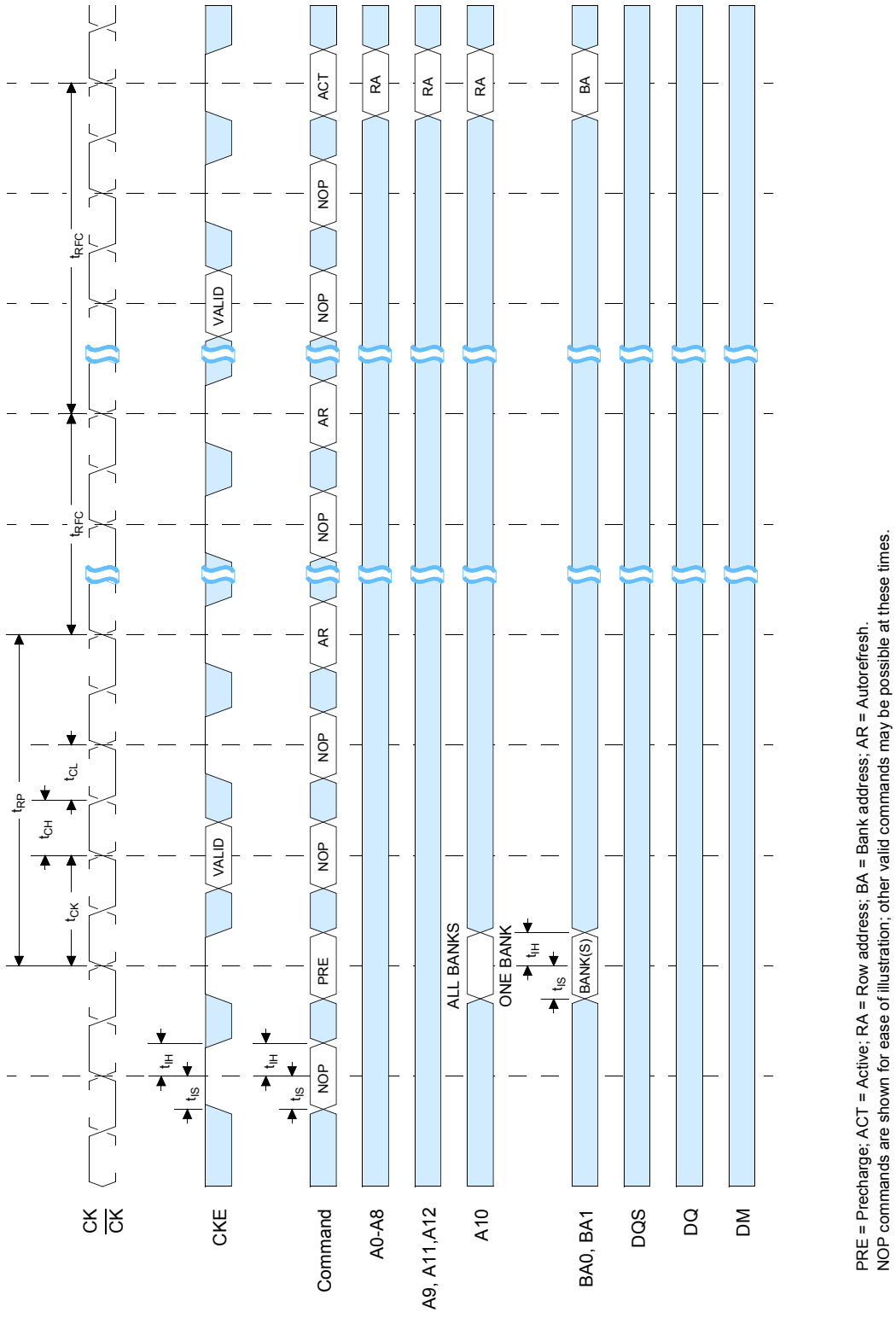
Initialize and Mode Register Sets



Power Down Mode

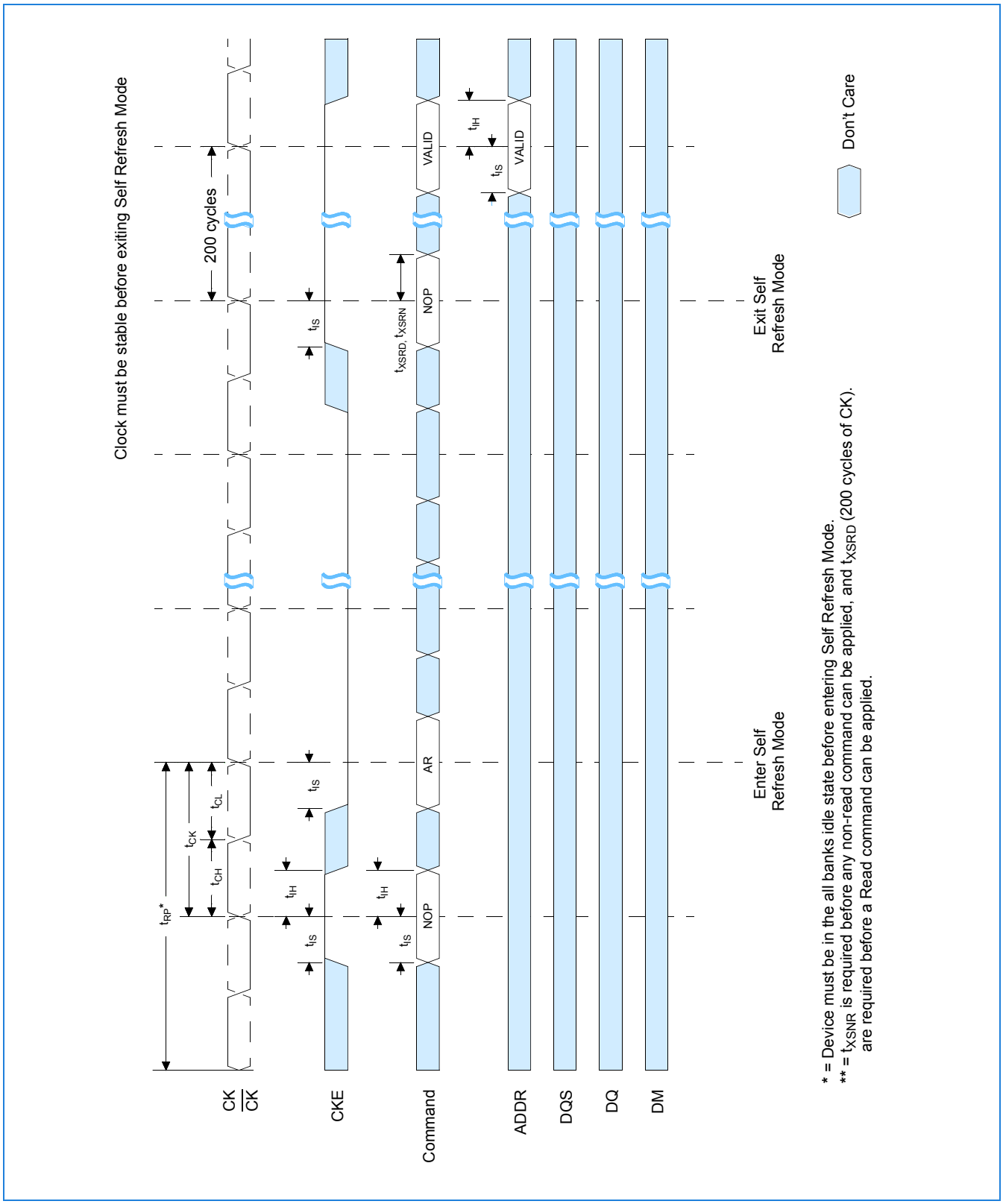


Auto Refresh Mode

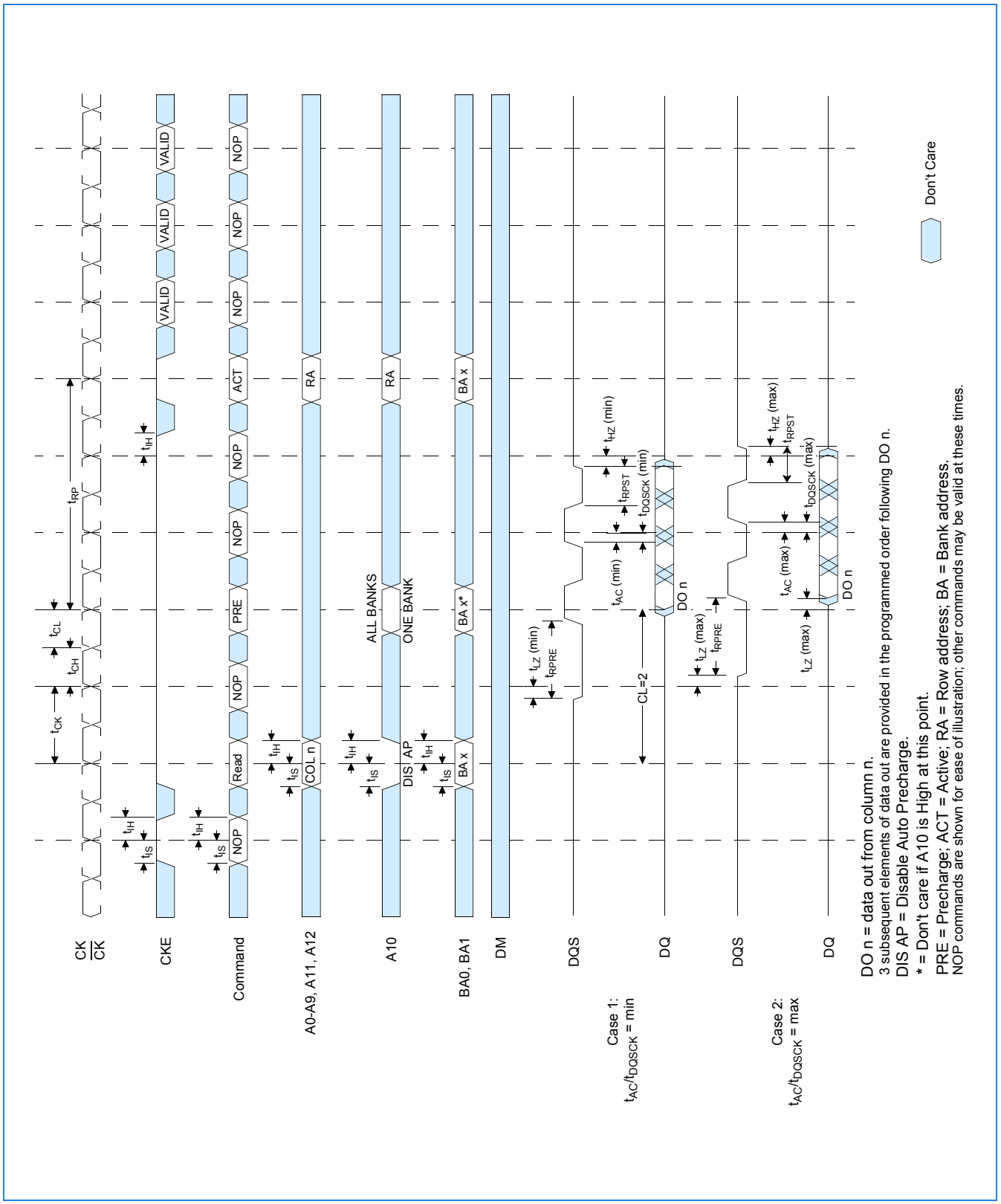


PRE = Precharge; ACT = Active; RA = Row address; BA = Bank address; AR = Autorefresh.
NOP commands are shown for ease of illustration; other valid commands may be possible at these times.
DM, DQ, and DQS signals are all don't care/high-Z for operations shown.

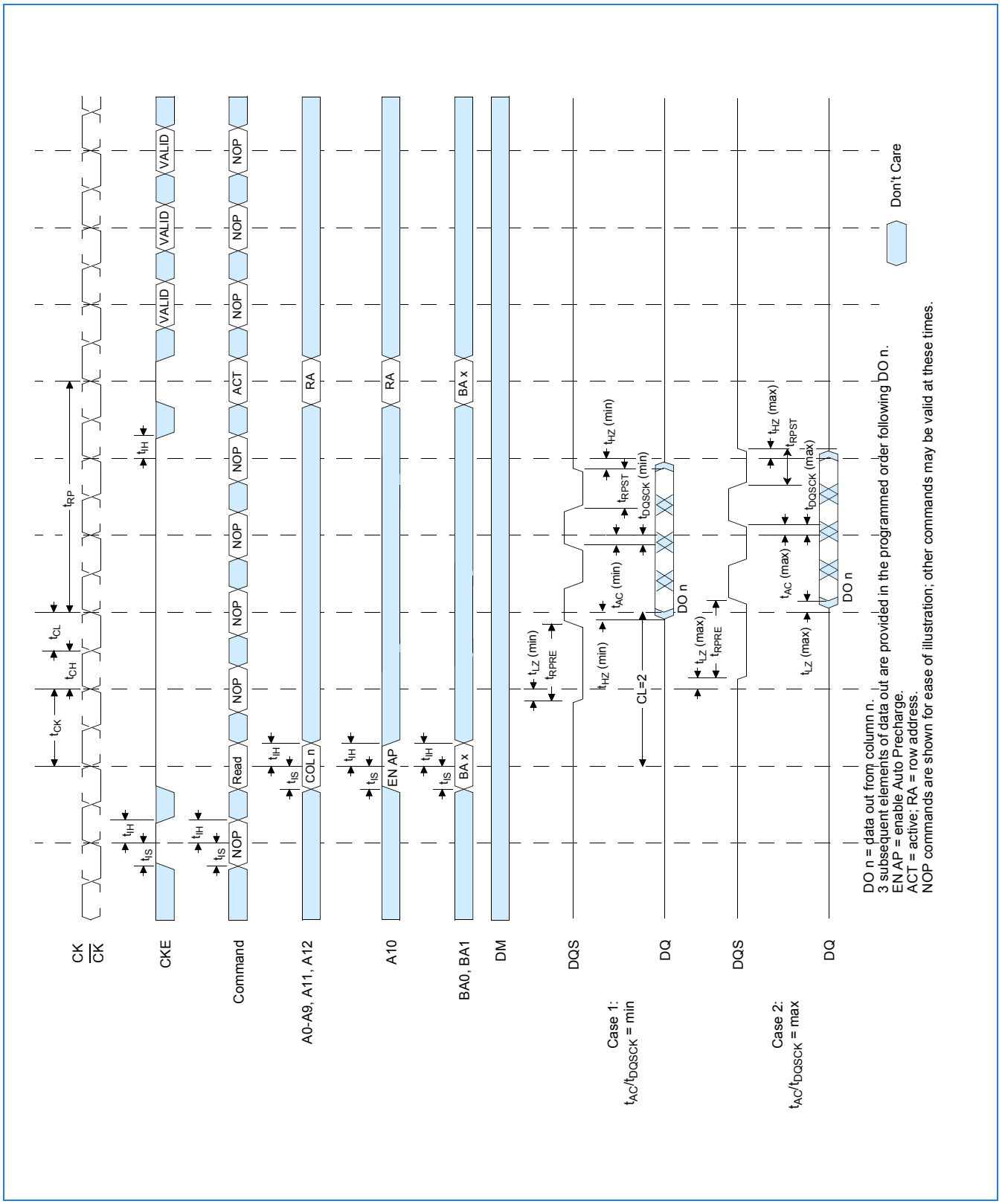
Self Refresh Mode



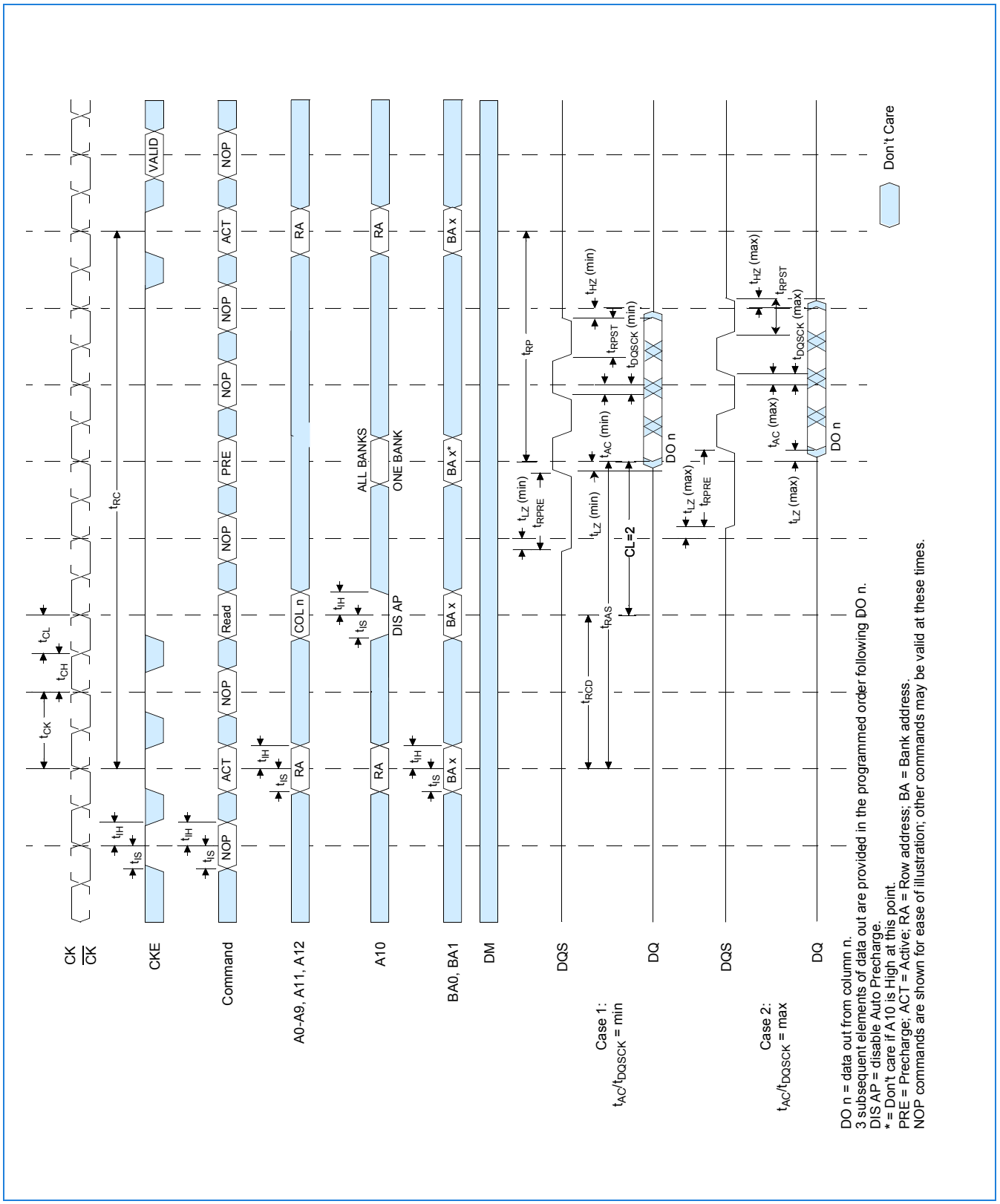
Read without Auto Precharge (Burst Length = 4)



Read with Auto Precharge (Burst Length = 4)

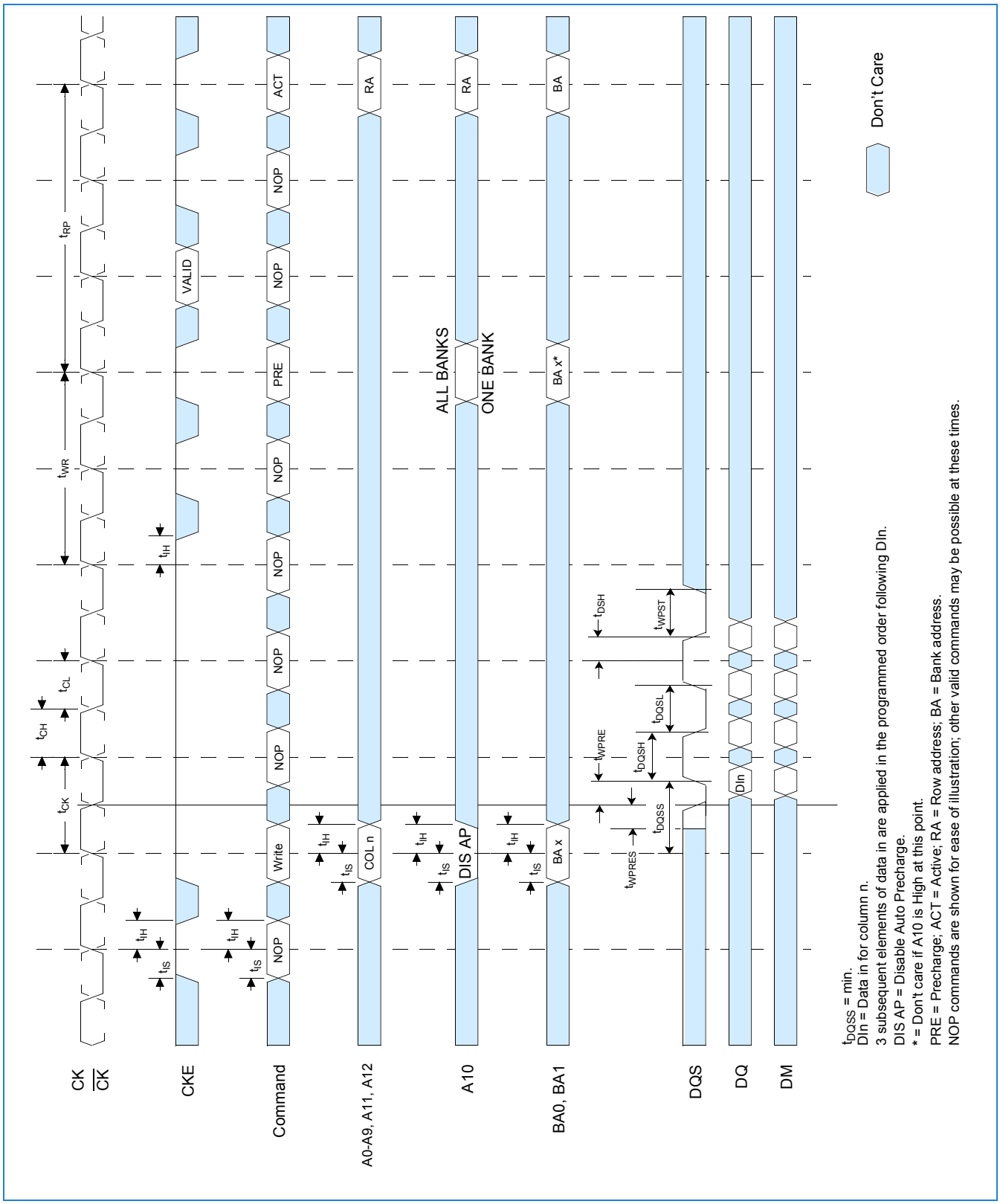


Bank Read Access (Burst Length = 4)

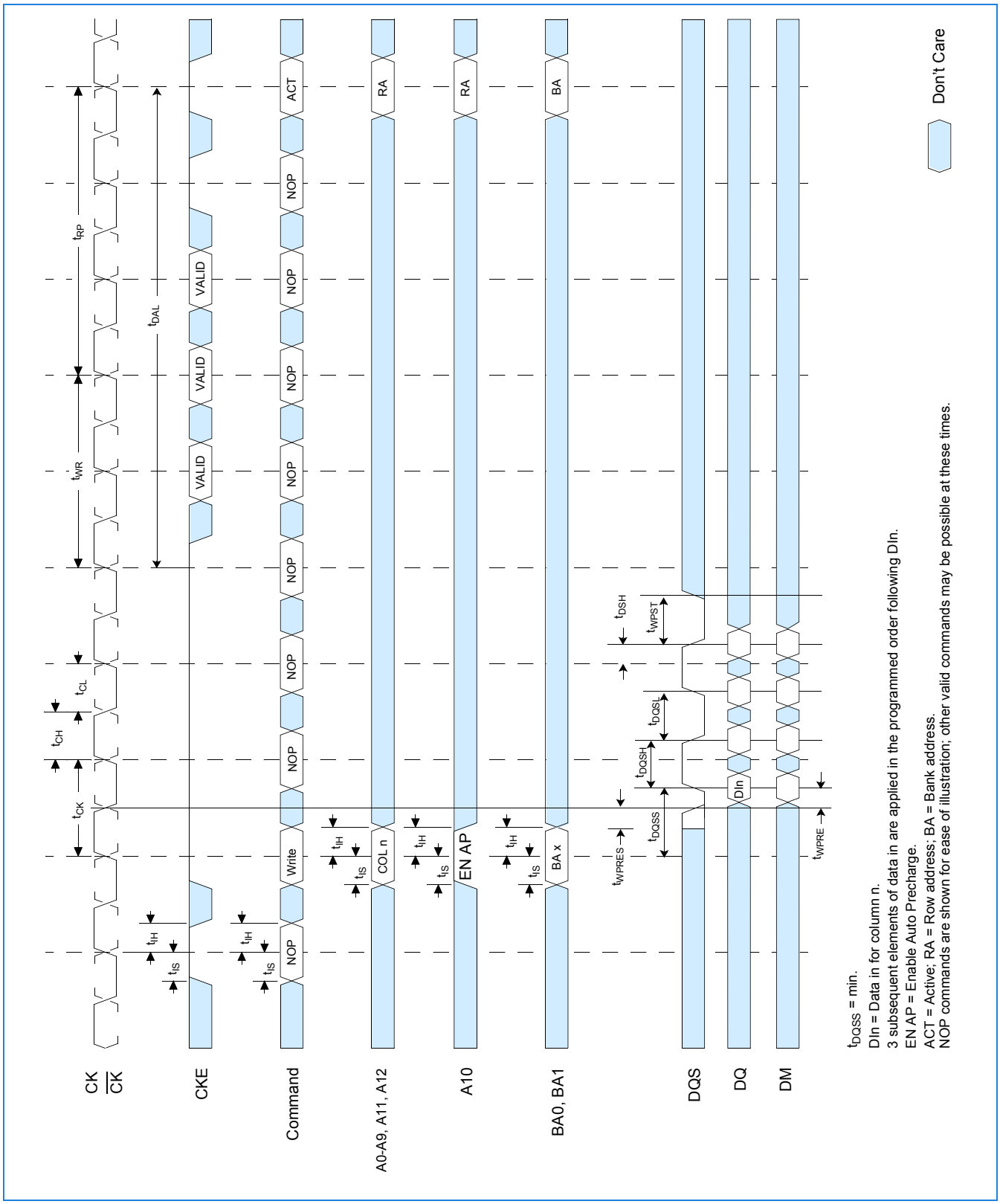


DO n = data out from column n.
3 subsequent elements of data out are provided in the programmed order following DO n.
DIS AP = disable Auto Precharge.
* = Don't care if A10 is High at this point.
PRE = Precharge; ACT = Active; RA = Row address; BA = Bank address.
NOP commands are shown for ease of illustration; other commands may be valid at these times.

Write without Auto Precharge (Burst Length = 4)

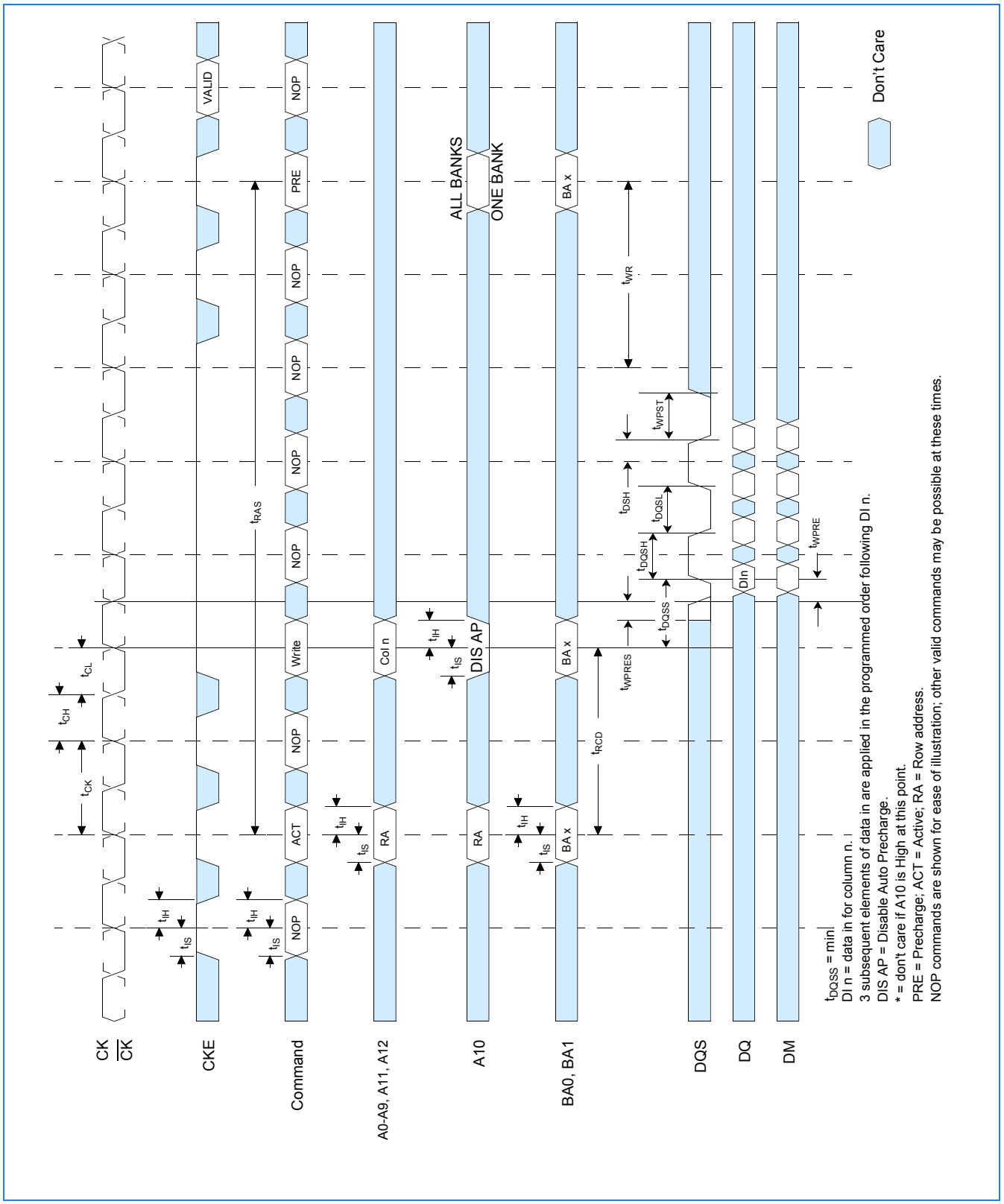


Write with Auto Precharge (Burst Length = 4)

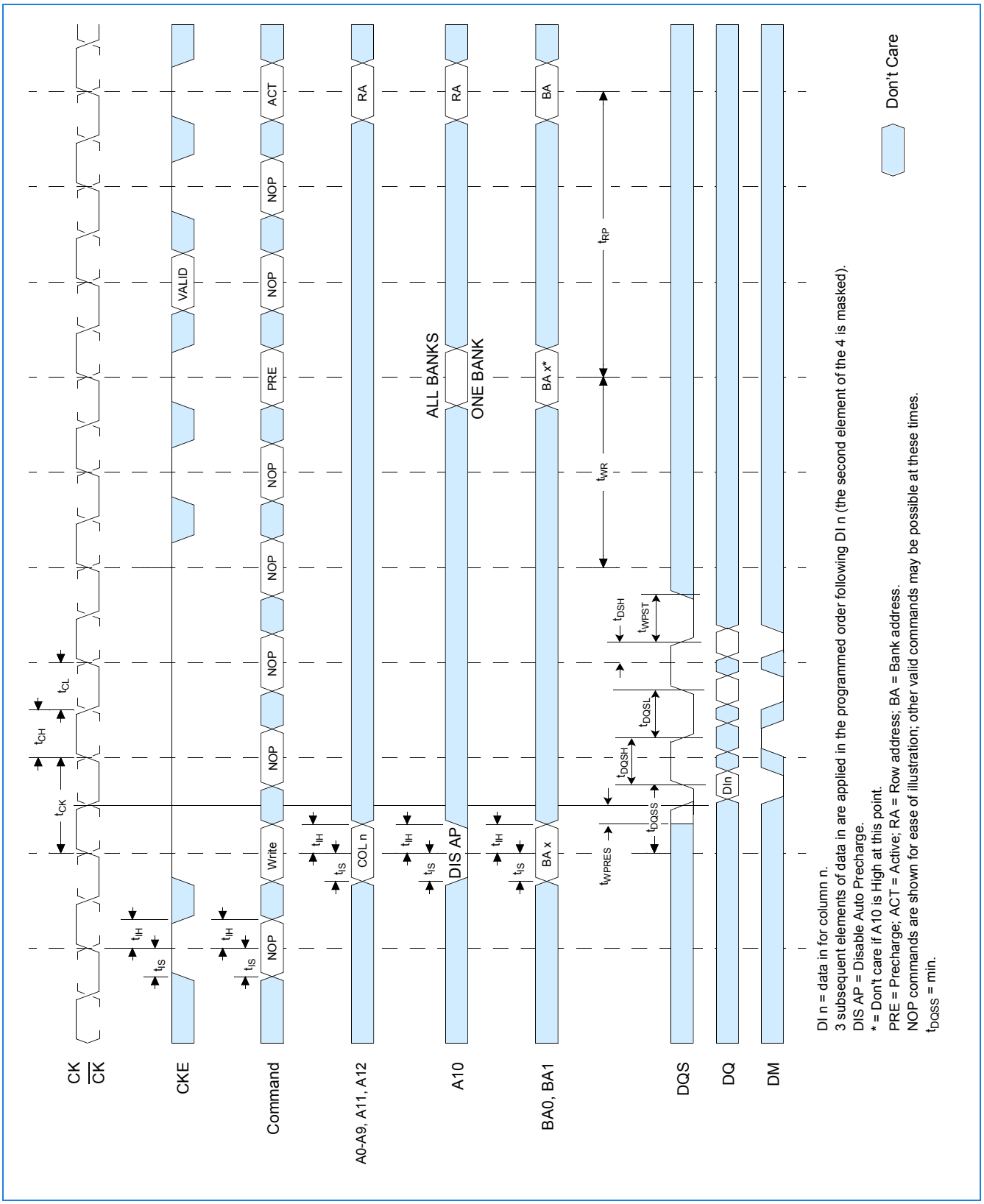


t_{DQSS} = min.
DIn = Data in for column n.
3 subsequent elements of data in are applied in the programmed order following DIn.
EN AP = Enable Auto Precharge.
ACT = Active; RA = Row address; BA = Bank address.
NOP commands are shown for ease of illustration; other valid commands may be possible at these times.

Bank Write Access (Burst Length = 4)

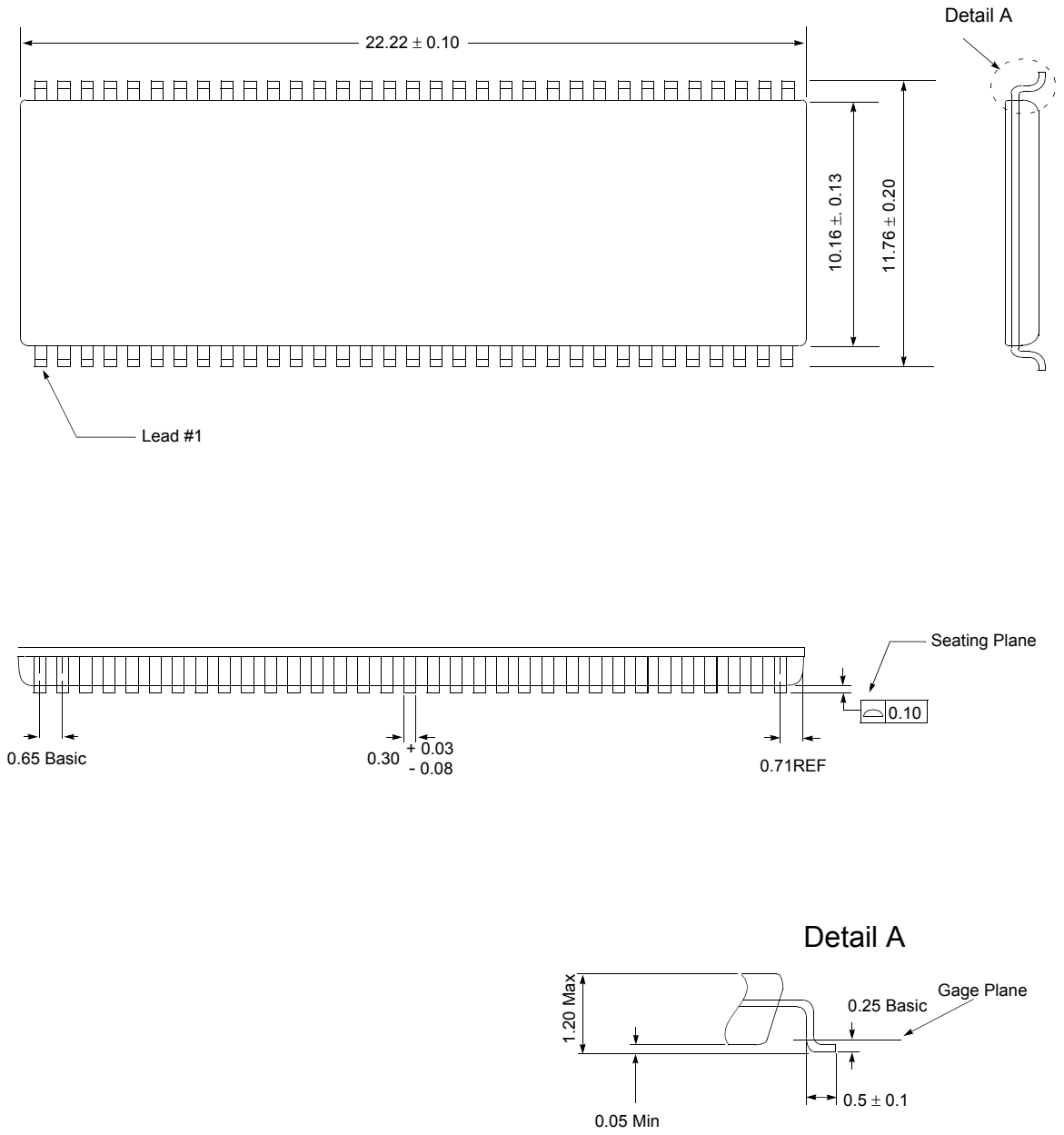


Write DM Operation (Burst Length = 4)

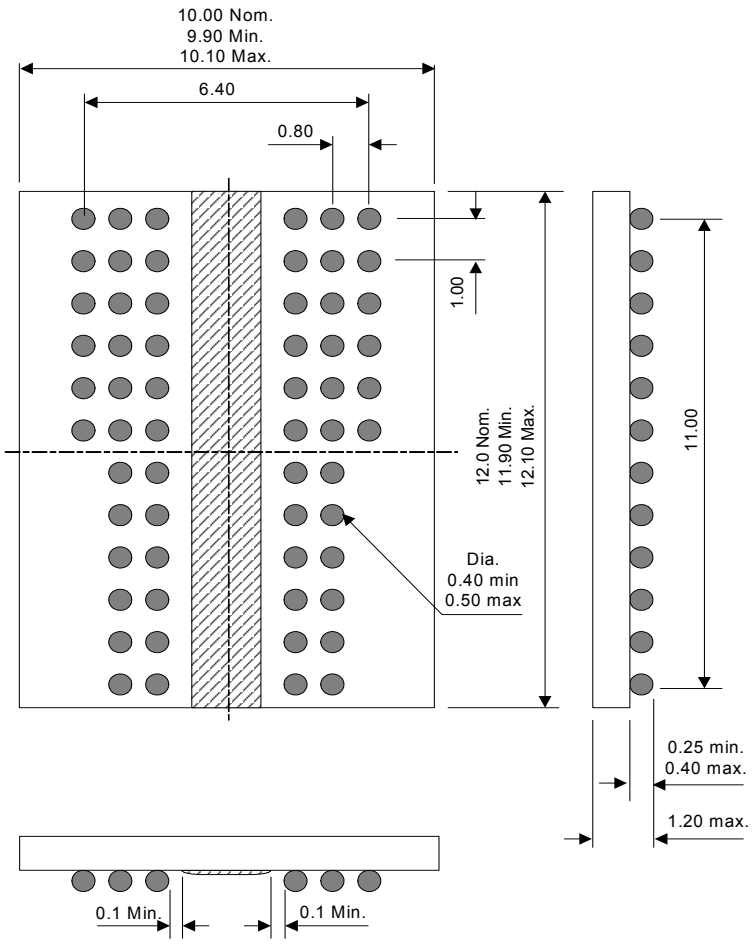


DI n = data in for column n.
3 subsequent elements of data in are applied in the programmed order following DI n (the second element of the 4 is masked).
DIS AP = Disable Auto Precharge.
* = Don't care if A10 is High at this point.
PRE = Precharge; ACT = Active; RA = Row address; BA = Bank address.
NOP commands are shown for ease of illustration; other valid commands may be possible at these times.
t_{DQSS} = min.

Package Dimensions (400mil; 66 lead; Thin Small Outline Package)



Package Dimensions (60 balls; 0.8mmx1.0mm Pitch; wBGA Package)



Note : All dimensions are typical unless otherwise stated.
Unit : Millimeters

Revision Log

Rev	Date	Modification
0.1	22 Mar 2004	Preliminary Release
0.2	14 Apr 2004	Part number updates
0.3	19 Apr 2004	Correction to tck values in AC/DC timing table
1.0	9 Nov 2004	Changed BGA deminsions from 8x13 to 10x12 mm Updated IDD data for 333 & 400 speed grades
1.1	17 Feb 2005	Added green product
1.2	25 Feb 2005	Correction to Idd2P and Idd6 in IDD specificication
1.3	15 Feb 2006	Update Package Dimensions
1.4	16 Aug 2006	Update AC timing.
1.5	13 Jun 2007	Update IDD current.
1.6	27 Nov 2007	Support DDR440

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