DS3579-2.3

MA5101

RADIATION HARD 256 x 4 BIT STATIC RAM

The MA5101 1k Static RAM is configured as 256 x 4 bits and manufactured using CMOS-SOS high performance, radiation hard, 3µm technology.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when CE is in the low state and minimum standby current is drawn.

Operation Mode	$\overline{CS}$	CE	$\overline{OE}$	$\overline{WE}$	I/O	Power
Read	L	H	L	H	D OUT	
Write	L	H	X	L	D IN	ISB1
Output Disable	L	H	H	H	High Z	
Standby	H	X	X	X	High Z	ISB2
	X	L	X	X	X	

Figure 1: Truth Table

FEATURES

- 3µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 90ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{10}$ Rad(Si)/sec
- SEU $<10^{-10}$ Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 10µA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation

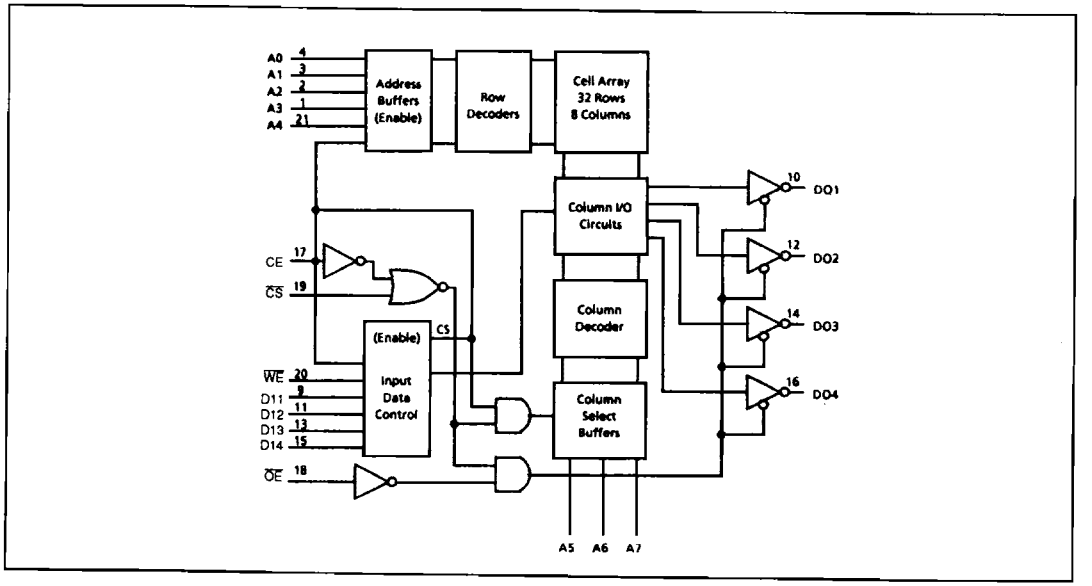


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
1. Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request).
2. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	$V_{DD}/2$	-	V_{DD}	V
V_{IL}	Input Low Voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output High Voltage	I_{OH1} = -1mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA	-	-	0.4	V
I_{LI}	Input Leakage Current (note 2)	V_{IN} = V_{DD} or V_{SS} all inputs	-	-	±10	µA
I_{LO}	Output Leakage Current (note 2)	= $V_{DD}/2$, V_{OUT} = 0 to V_{DD}	-	-	±20	µA
I_{DD}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, f_{RC} = 1MHz, CE, A_{0-7} switching, outputs open, all other inputs V_{DD}	-	10	15	mA
I_{SB}	Standby Supply Current	CE = 0.2V	-	10	1000	µA
I_{SB}	Selected Supply Current	$\overline{CS}$ = V_{SS}, CE = V_{DD} - 0.2V	-	20	30	mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	CE = V_{SS}	2.0	-	-	V
I_{DDR}	Data Retention Current	CE = V_{SS}, V_{DR} = 2.0V	-	5	750	µA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V.
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state.
6. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	Min	Max	Units
T_{AVAVR}	Read Cycle Time	140	-	ns
T_{AVOV}	Address Access Time	-	130	ns
T_{EHOV}	Chip Select Access Time	-	140	ns
T_{SLOV}	Chip Enable Access Time	-	140	ns
T_{EHQX} (5,6)	Chip Selection to Output in Low Z	10	-	ns
T_{SLQX} (5,6)	Chip Enable to Output in Low Z	10	-	ns
T_{ELQZ} (5,6)	Chip Deselection to Output in High Z	0	60	ns
T_{SHQZ} (5,6)	Chip Disable to Output in High Z	0	60	ns
T_{AXQX}	Output Hold from Address Change	10	-	ns
T_{GLQV}	Output Enable Access Time	-	70	ns
T_{GLQX} (5,6)	Output Enable to Output in Low Z	10	-	ns
T_{GHQZ} (5,6)	Output Enable to Output in High Z	0	60	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
T_{AVAVW}	Write Cycle Tlme	140	-	ns
T_{EHWH}	Chip Selection to End of Write	80	-	ns
T_{SLWH}	Chip Enable to End of Write	80	-	ns
T_{AVWH}	Address Valid to End of Write	80	-	ns
T_{AVWL}	Address Set Up Time	20	-	ns
T_{WLWH}	Write Pulse Width	50	-	ns
T_{WHAV}	Write Recovery Time	5	-	ns
T_{WLQZ} (5,6)	Wnte to Output in High Z	0	60	ns
T_{DVWH}	Data to Write Time Overlap	30	-	ns
T_{WHDX}	Data Hold from Write	10	-	ns
T_{WHQX} (5,6)	Output Active from End to Write	5	-	ns
T_{EHWL}	Chip Enable to Write Low	25	-	ns
T_{SLWL}	Chip Selection to Write Low	25	-	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	8	12	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

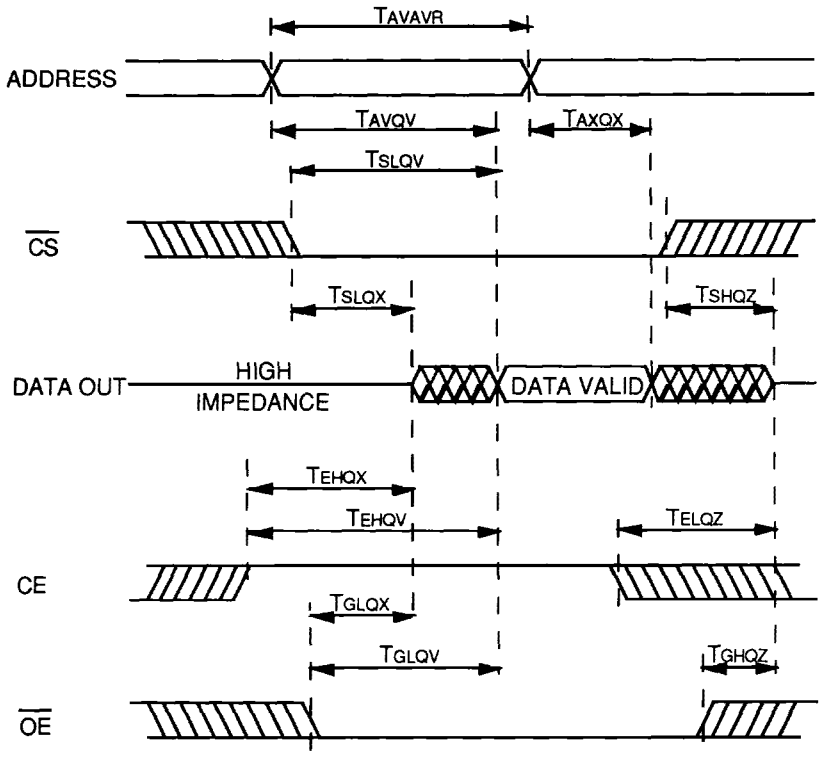
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

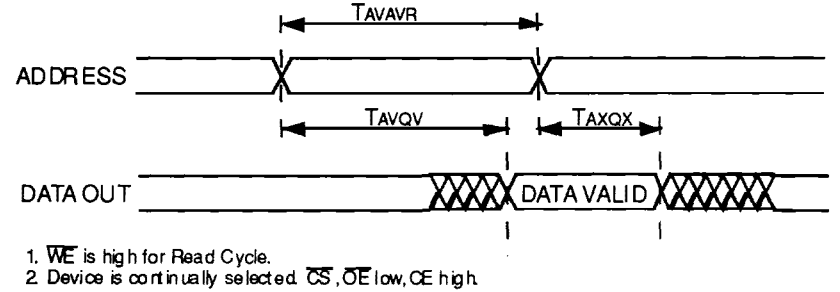
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



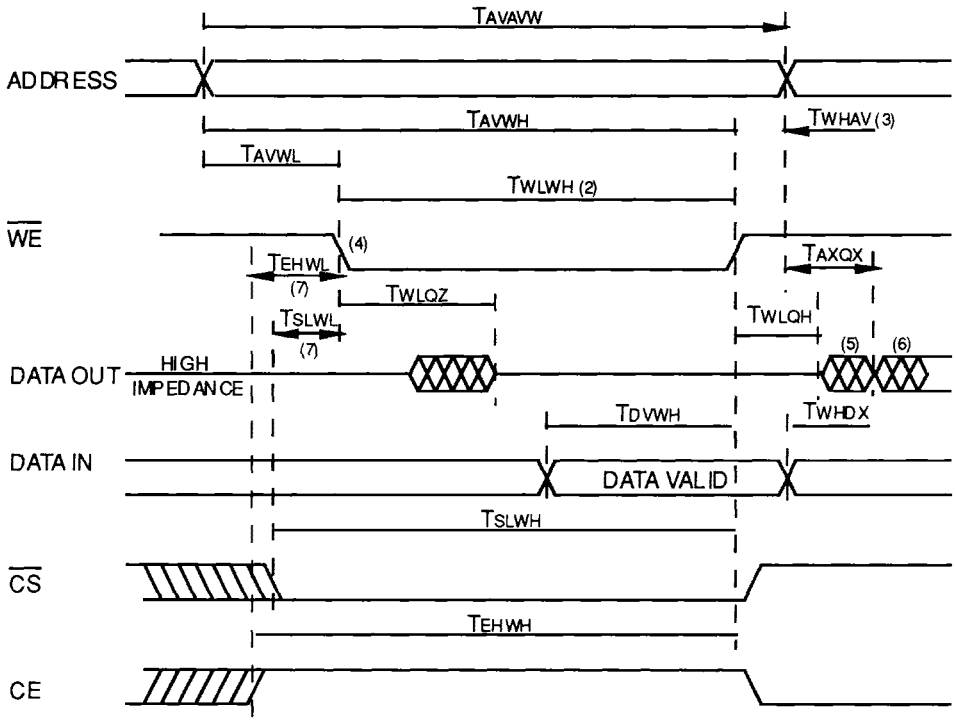
1.$\overline{WE}$ is high for Read Cycle.
2.Address Valid prior to or coincident with $\overline{CS}$ transition low or CE transition high.

Figure 11a: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$, $\overline{OE}$ low, CE high.

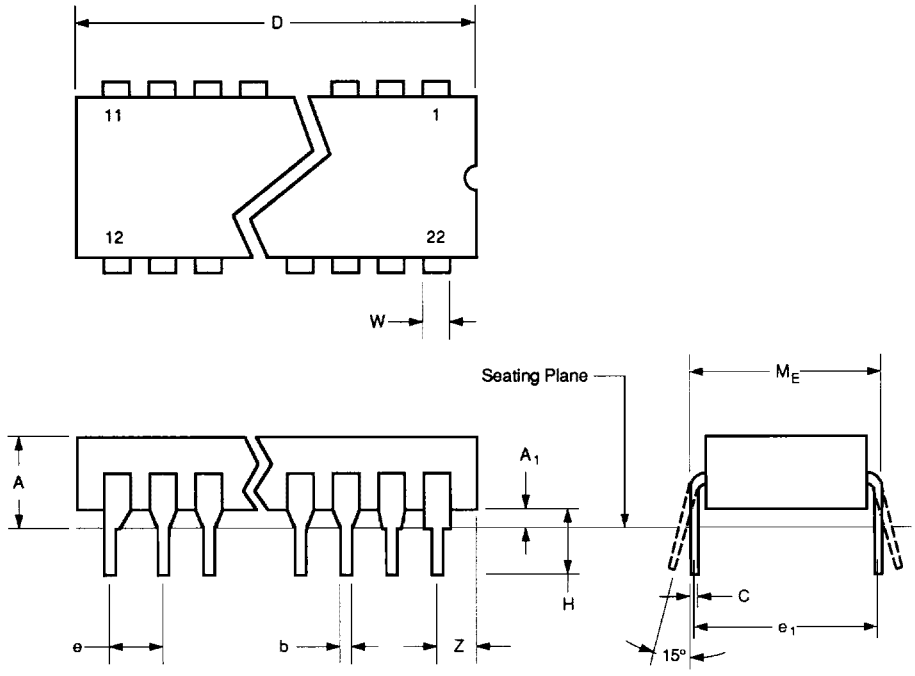
Figure 11b: Read Cycle 2



1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$, a high CE and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high or CE going low, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low or CE high transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is the write data of the current cycle, if selected.
6. DATA OUT is the read data of the next address, if selected.
7. T_{SLWL} and T_{EHWL} must be met to prevent memory corruption.
8. $\overline{OE}$ is low. (If $\overline{OE}$ is high then DATA OUT remains in the high impedance state throughout the cycle).

Figure 12: Write Cycle

OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	27.94	-	-	1.100
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	10.16 Typ.	-	-	0.400 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	17.95	-	-	0.313
Z	-	-	1.35	-	-	0.053
W	-	-	1.53	-	-	0.060

XG462

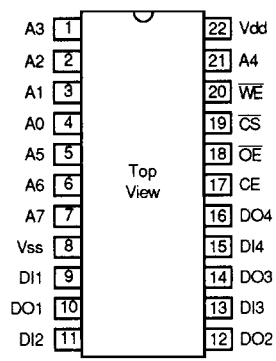


Figure 13: 28-Lead Ceramic DIL (Solder Seal) - Package Style C

Function	Pkg.Opt. C	Via	Burnin			Radiation
			Static 1	Static 2	Dynamic	
A3	1	R	0V	5V	F4	5V
A2	2	R	0V	5V	F3	5V
A1	3	R	0V	5V	F2	5V
A0	4	R	0V	5V	F1	5V
A5	5	R	0V	5V	F6	5V
A6	6	R	0V	5V	F7	5V
A7	7	R	0V	5V	F8	5V
VSS	8	Direct	0V	0V	0V	0V
DI1	9	R	0V	5V	F9	5V
DO1	10	R	0V	5V	LOAD	5V
DI2	11	R	0V	5V	F9	5V
DO2	12	R	0V	5V	LOAD	5V
DI3	13	R	0V	5V	F9	5V
DO3	14	R	0V	5V	LOAD	5V
DI4	15	R	0V	5V	F9	5V
DO4	16	R	0V	5V	LOAD	5V
CE	17	R	0V	5V	F10	5V
OEB	18	R	0V	5V	F11	5V
CSB	19	R	0V	5V	F12	5V
WEB	20	R	0V	5V	F0	5V
A4	21	R	0V	5V	F5	5V
VDD	22	Direct	5V	5V	5V	5V

1. F0 = 150KHz, F1 = F0 /2, F2 = F0 /4, F3 = F0 /8 etc.
2. Burnin R = 4K7
3. Radiation R = 10k

Figure 14: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Basic function)	$1x10^5$ Rad(Si)
Total Dose (Function to specification)	$1x10^6$ Rad(Si)
Transient Upset	$>10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$4.3x10^{-11}$ errors/bitday
Latch-up	Not possible

Figure 15: Typical Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

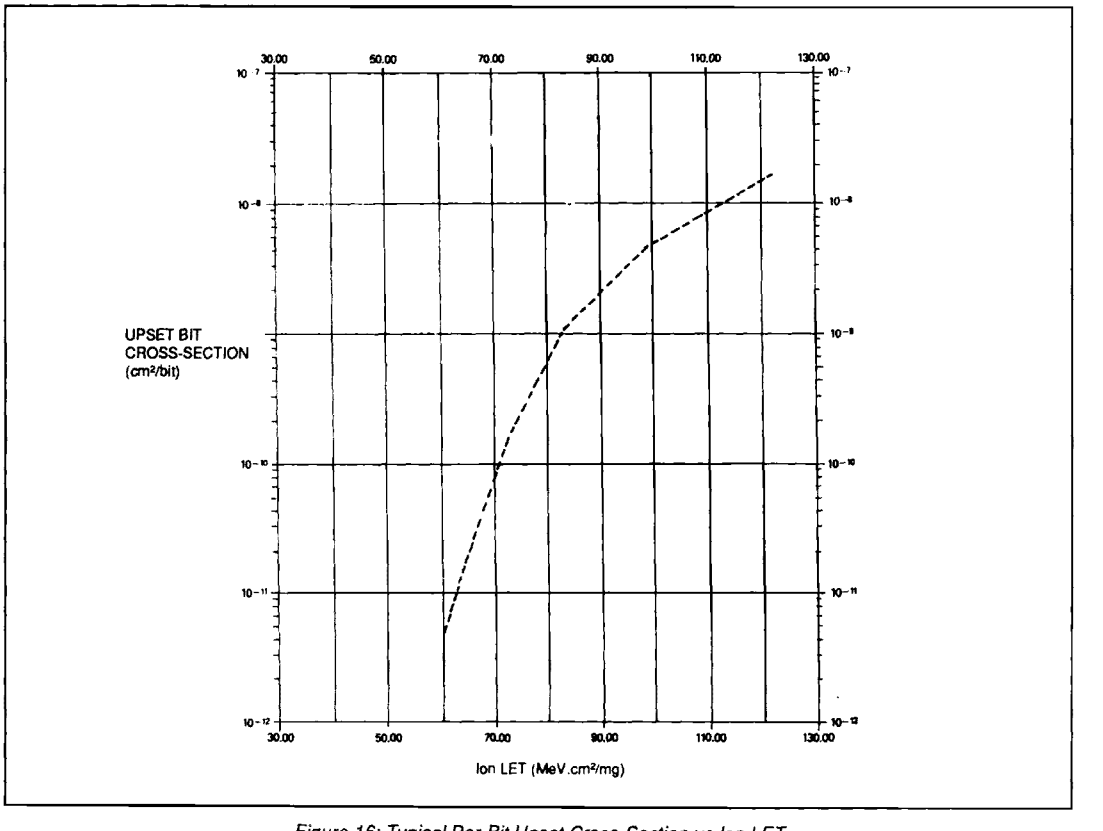
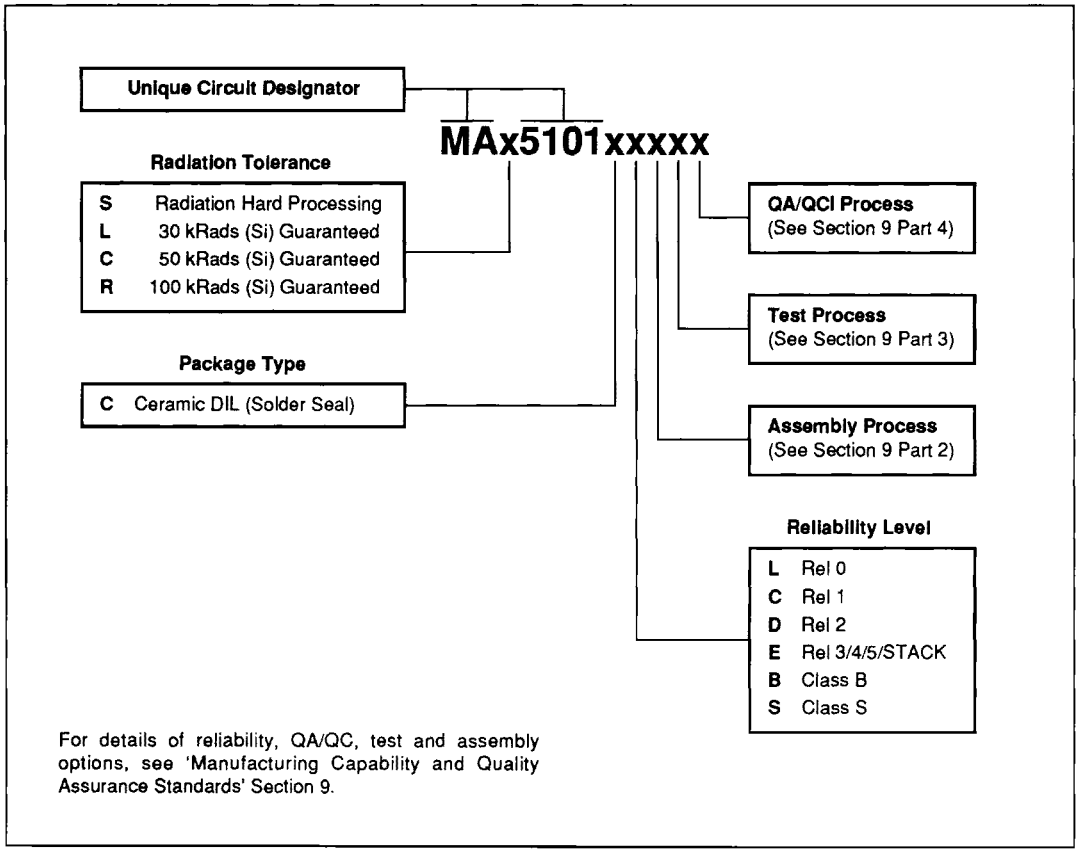


Figure 16: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.