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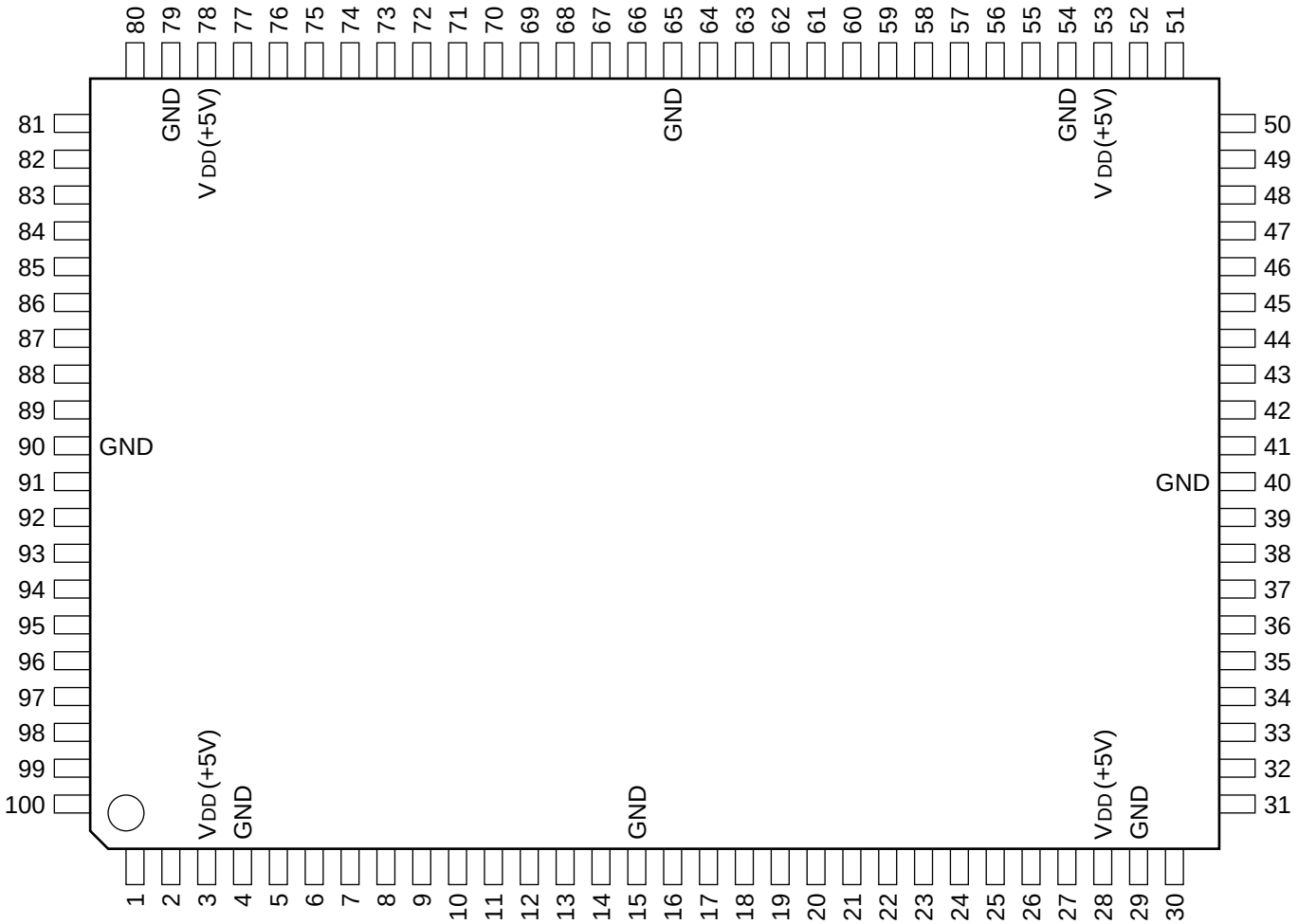
CXD8871Q (1/4)
IL08

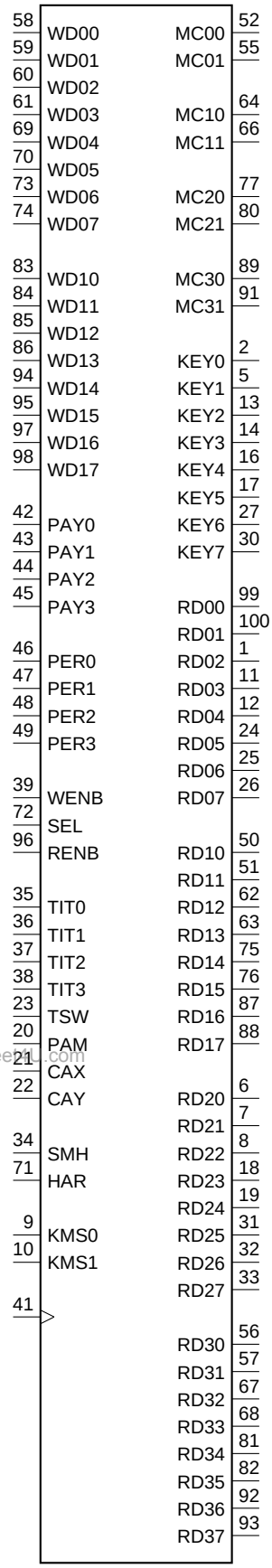
C-MOS MATRIX DATA PROCESSOR

- TOP VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	RD02	26	I/O	RD07	51	I/O	RD11	76	I/O	RD15
2	O	KEY0	27	O	KEY6	52	O	MC00	77	O	MC20
3	–	V_{DD}	28	–	V_{DD}	53	–	V_{DD}	78	–	V_{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	O	KEY1	30	O	KEY7	55	O	MC01	80	O	MC21
6	I/O	RD20	31	I/O	RD25	56	I/O	RD30	81	I/O	RD34
7	I/O	RD21	32	I/O	RD26	57	I/O	RD31	82	I/O	RD35
8	I/O	RD22	33	I/O	RD27	58	I	WD00	83	I	WD10
9	I	KMS0	34	I	SMH	59	I	WD01	84	I	WD11
10	I	KMS1	35	I	TIT0	60	I	WD02	85	I	WD12
11	I/O	RD03	36	I	TIT1	61	I	WD03	86	I	WD13
12	I/O	RD04	37	I	TIT2	62	I/O	RD12	87	I/O	RD16
13	O	KEY2	38	I	TIT3	63	I/O	RD13	88	I/O	RD17
14	O	KEY3	39	I	WENB	64	O	MC10	89	O	MC30
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	O	KEY4	41	I	CK	66	O	MC11	91	O	MC31
17	O	KEY5	42	I	PAY0	67	I/O	RD32	92	I/O	RD36
18	I/O	RD23	43	I	PAY1	68	I/O	RD33	93	I/O	RD37
19	I/O	RD24	44	I	PAY2	69	I	WD04	94	I	WD14
20	I	PAM	45	I	PAY3	70	I	WD05	95	I	WD15
21	I	CAX	46	I	PER0	71	I	HAR	96	I	RENB
22	I	CAY	47	I	PER1	72	I	SEL	97	I	WD16
23	I	TSW	48	I	PER2	73	I	WD06	98	I	WD17
24	I/O	RD05	49	I	PER3	74	I	WD07	99	I/O	RD00
25	I/O	RD06	50	I/O	RD10	75	I/O	RD14	100	I/O	RD01



INPUT

CAX ; X SELECT AT COUNTER ADDRESS MODE

CAY ; Y SELECT AT COUNTER ADDRESS MODE

CL ; SYSTEM CLOCK

HAR ; MATRIX SET (AT SMH=H) EFFECTIVE AREA
L=DATA SET ON H LEVEL, H=DATA SET ON L LEVEL

KMS1, KMS0 ; LINEAR KEY MODE SELECT
0=FFH, 1=00H, 2=LINEAR KEY, 3=TURN OVER KEY

PAM ; ADDRESS MODE SELECT
L=OPERATOR, H=COUNTER

PAY3-PAY0 ; MATRIX DATA SELECT (4 BIT TO 2 BIT)

PER3-PER0 ; MATRIX DATA OPERATION ERROR DATA
H=ERROR, MATRIX DATA SET TO L LEVEL

RENB ; LATCH ENABLE FOR RD0, RD1, RD2 AND RD3

SEL ; READ/WRITE SWITCHING FOR I/O BUFFER
L=RD0 AND RD1 ON READ, RD2 AND RD3 ON WRITE
H=RD2 AND RD3 ON READ, RD0 AND RD1 ON WRITE

SMH ; MATRIX SET
L=NORMALLY OPERATION
H=DATA SET ON H LEVEL

TIT3-TIT0 ; TITLE SIGNALS
H=TITLE (MATRIX DATA CHANGE 11 TO 01)

TSW ; TITLE SWITCH
L=TITLE ON, H=TITLE OFF

WD07-WD00 ; WRITE DATA TO MEMORY (MATCH FOR RD0 AND RD2)

WD17-WD10 ; WRITE DATA TO MEMORY (MATCH FOR RD1 AND RD3)

WENB ; LATCH ENABLE FOR WD0 AND WD1

OUTPUT

KEY7-KEY0 ; LINEAR KEY FOR SOFT EDGE

MC01-MC00 ; BLOCK 0 (LEFT UPPER) MATRIX DATA

MC11-MC10 ; BLOCK 1 (RIGHT UPPER) MATRIX DATA

MC21-MC20 ; BLOCK 2 (LEFT LOWER) MATRIX DATA

MC31-MC30 ; BLOCK 3 (RIGHT LOWER) MATRIX DATA

INPUT/OUTPUT

RD07-RD00, RD17-RD10, RD27-RD20, RD37-RD30
; READ DATA INPUTS, WRITE DATA OUTPUTS

SEL	RD0	RD1	RD2	RD3	MC & KEY
0	IN	IN	WD0 OUT	WD1 OUT	FROM RD0, RD1
1	WD0 OUT	WD1 OUT	IN	IN	FROM RD2, RD3