APL3215/A

ANPEC

Li+ Charger Protection IC with Integrated P-MOSFET

Features

- **Input Over-Voltage Protection**
- **Input Over-Current Protection**
- **Battery Over-Voltage Protection**
- **High Immunity of False Triggering**
- **High Accuracy Protection Threshold**
- **A Built-In P-MOSFET**
- **Thermal Shutdown Protection**
- **Available in a TDFN2x2-8 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Cell Phones**

General Description

The APL3215/A provides complete Li+ charger protection against input over-voltage, input over-current, and battery over-voltage. When any of the monitored parameters are over the threshold, the IC removes the power from the charging system by turning off an internal switch. All protections also have deglitch time against false triggering due to voltage spikes or current transients.
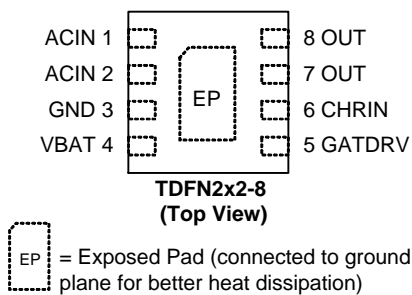
The APL3215/A integrates a P-MOSFET with the body diode reverse protection to replace the external P-MOSFET and Schottky diode for charger function of cell phone's PMIC. When the CHRIN voltage drops below V_{BAT}+20mV, the internal power select circuit will reverse the body diode's terminal to prevent a reverse current flowing from the battery back to CHRIN pin.

The APL3215/A provides complete Li+ charger protections and saves the external MOSFET and Schottky diode for the charger of cell phone's PMIC. The above features and small package make the APL3215/A an ideal part for cell phones applications.
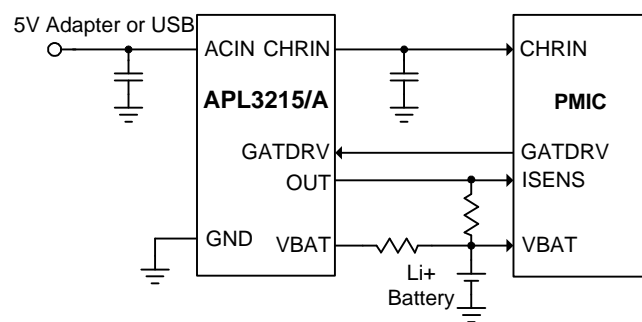
Pin Configuration

ACIN 1
ACIN 2
GND 3
VBAT 4

EP

8 OUT
7 OUT
6 CHRIN
5 GATDRV

TDFN2x2-8 (Top View)

EP = Exposed Pad (connected to ground plane for better heat dissipation)
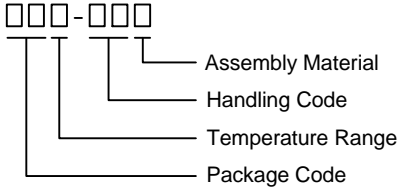
Simplified Application Circuit

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL3215
APL3215A
	□□□-□□□			Package Code
				  QB : TDFN2x2-8
				Operating Ambient Temperature Range
				  I : -40 to 85 °C
				Handling Code
				  TR : Tape & Reel
				Assembly Material
				  G : Halogen and Lead Free Device

		Assembly Material
		    Handling Code
		    Temperature Range
		    Package Code		

APL3215 QB:	L15 X		X - Date Code	
APL3215A QB:	L15A X		X - Date Code	

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{ACIN}	ACIN Input Voltage (ACIN to GND)	-0.3 ~ 20	V
V_{CHRIN}	CHRIN to GND Voltage	-0.3 ~ 7	V
V_{GATDRV}	GATDRV to GND Voltage	-0.3 ~ V_{CHRIN}	V
V_{BAT}	VBAT to GND Voltage	-0.3 ~ 7	V
V_{OUT}	OUT to GND Voltage	-0.3 ~ 7	V
I_{OUT}	OUT Output Current	1.5	A
T_J	Maximum Junction Temperature	150	^{o}C
T_{STG}	Storage Temperature	-65 ~ 150	^{o}C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	^{o}C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristic

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air [Note 2]			$^{o}C/W$
		TDFN2x2-8	75	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN2x2-8 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{ACIN}	ACIN Input Voltage	4.5 ~ 5.5	V
I_{OUT}	Output Current	0 ~ 700	mA
T_A	Ambient Temperature	-40 ~ 85	^oC
T_J	Junction Temperature	-40 ~ 125	^oC

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{ACIN}=5V, V_{BAT}=3.8V and T_A= -40 ~ 85 ^{o}C. Typical values are at T_A=25°C.

| Symbol	Parameter	Test Conditions		APL3215/A			Unit
				Min.	Typ.	Max.	
ACIN INPUT CURRENT AND POWER-ON-RESET (POR)							
I_{ACIN}	ACIN Supply Current	I_{OUT}=0A, I_{CHRIN}=0A, T_A=25°C		-	250	350	μA
V_{ACIN}	ACIN POR Threshold			2.4	-	2.8	V
	ACIN POR Hysteresis			200	275	350	mV
$T_{B(ACIN)}$	ACIN Power-On Blanking Time			-	8	-	ms
INTERNAL SWITCH ON RESISTANCE							
	ACIN to OUT On Resistance	I_{OUT}=0.7A		-	0.5	-	Ω
	CHRIN Discharge On Resistance			-	500	-	Ω
INPUT OVER-VOLTAGE PROTECTION (OVP)							
V_{OVP}	Input OVP Threshold	V_{ACIN} rising	APL3215	6	6.17	6.35	V
			APL3215A	6.6	6.8	7	
	Input OVP Hysteresis			200	300	400	mV
	Input OVP Propagation Delay			-	-	1	μs
$T_{ON(OVP)}$	Input OVP Recovery Time			-	8	-	ms
OVER-CURRENT PROTECTION (OCP)							
I_{OCP}	OCP Threshold	T_A=25°C		1	1.5	-	A
$T_{B(OCP)}$	OCP Blanking Time			-	176	-	μs
$T_{ON(OCP)}$	OCP Recovery Time			-	64	-	ms
BATTERY OVER-VOLTAGE PROTECTION							
V_{BOVP}	Battery OVP Threshold	V_{BAT} rising		4.32	4.35	4.38	V
	Battery OVP Hysteresis			220	270	320	mV
I_{VBAT}	VBAT Pin Leakage Current	V_{BAT} = 4.4V		-	-	20	nA
$T_{B(BOVP)}$	Battery OVP Blanking Time			-	176	-	μs
CHRIN, OUT AND GATDRV							
	V_{CHRIN}-V_{BAT} Lockout Threshold	V_{CHRIN} from low to high, P-MOSFET is controlled by GATDRV		-	150	-	mV
		V_{CHRIN} from high to low, P-MOSFET is off		-	20	-	
	OUT Input Current	V_{CHRIN}=0V, V_{OUT}=4.2V, V_{GATDRV}=0V		-	-	1	μA
	GATDRV Leakage Current	V_{ACIN}=V_{CHRIN}= V_{OUT}=5V, V_{GATDRV}=0V		-	-	1	μA
	OUT Leakage Current	V_{ACIN}=V_{CHRIN}= V_{GATDRV} =5V, V_{OUT}=0V		-	-	1	μA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{ACIN}=5V, V_{BAT}=3.8V and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3215/A			Unit
			Min.	Typ.	Max.	
CHRIN, OUT AND GATDRV (CONT.)						
	P-MOSFET Input Capacitance		-	200	-	pF
	GATDRV Gate Resistance		-	15	-	Ω
	P-MOSFET Gate Threshold Voltage	I_{OUT}=0.7A	-	1.8	-	V
THERMAL SHUTDOWN PROTECTION						
T_{OTP}	Thermal Shutdown Threshold		-	160	-	°C
	Thermal Shutdown Hysteresis		-	40	-	°C

Typical Operating Characteristics

Input OVP Threshold vs. Junction Temperature
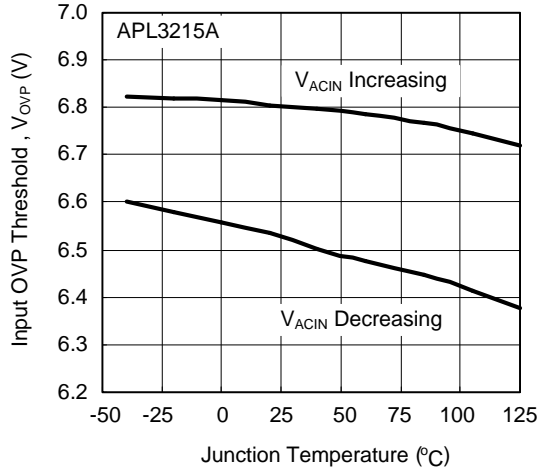
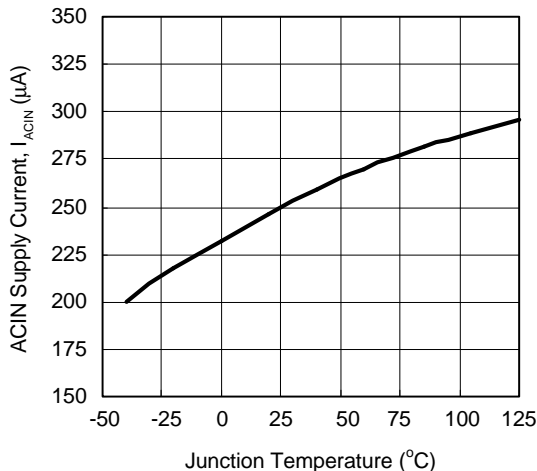
OCP Threshold vs. Junction Temperature
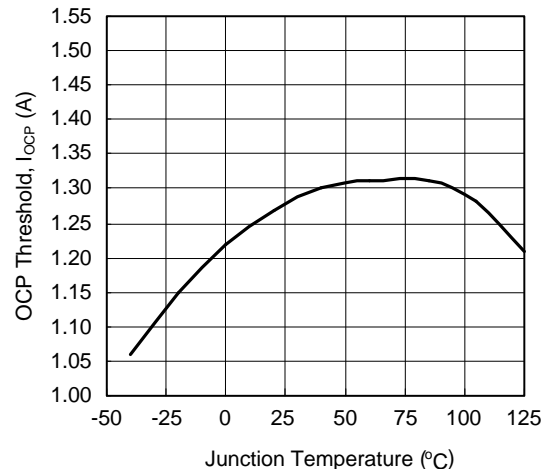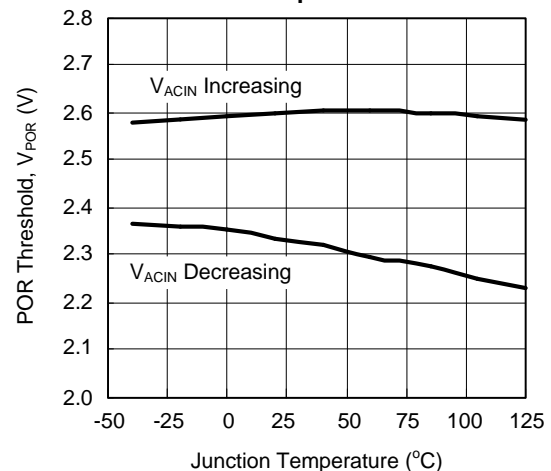

Battery OVP Threshold vs. Junction Temperature
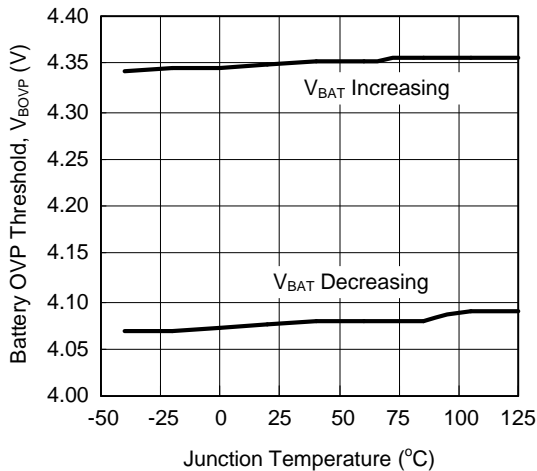
Power Switch On Resistance vs. Junction Temperature
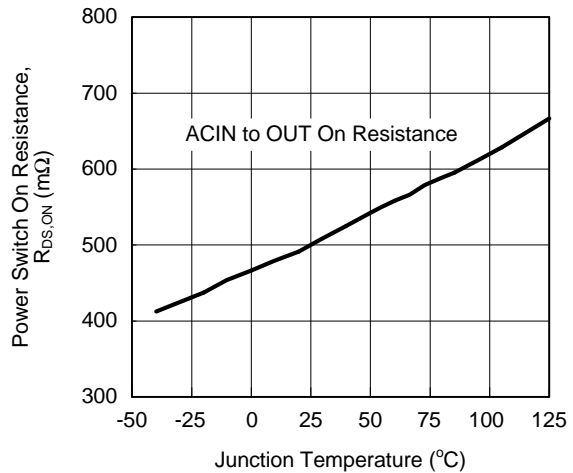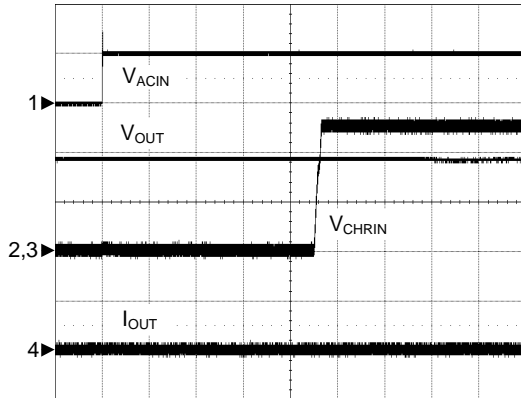

ACIN Supply Current vs. Junction Temperature

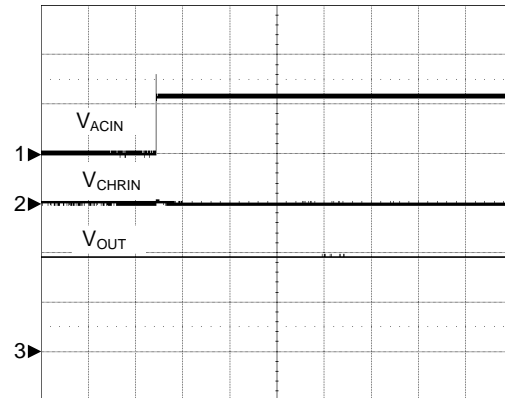**POR Threshold vs. Junction Temperature**

Operating Waveforms

The test condition is V_{ACIN}=5V, V_{BAT}=3.8V, C_{ACIN}=1μF, C_{CHRIN}=1μF, T_A= 25°C unless otherwise specified.
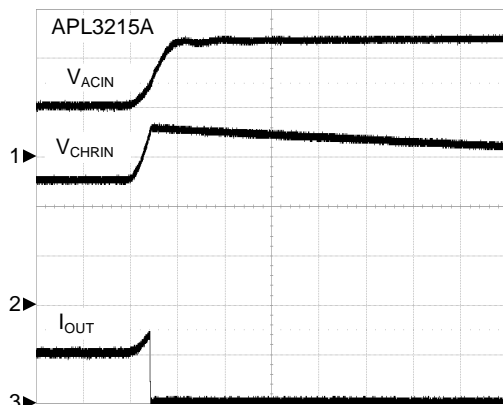
Normal Power On

$V_{GATDRV} = V_{CHRIN}$
CH1: V_{ACIN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{CHRIN}, 2V/Div, DC
CH4: I_{OUT}, 0.2A/Div, DC
TIME: 2ms/Div

OVP at Power On

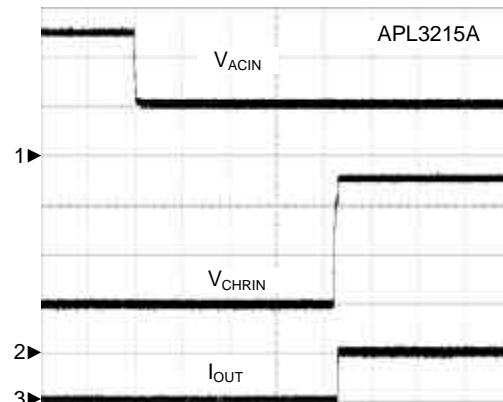V_{ACIN} = 0 to 12V, $V_{GATDRV} = V_{CHRIN}$
CH1: V_{ACIN}, 10V/Div, DC
CH2: V_{CHRIN}, 2V/Div, DC
CH3: V_{OUT}, 2V/Div, DC
TIME: 2ms/Div

Input Over-Voltage Pretection

V_{ACIN} = 5V to 12V, R_{OUT} = 50Ω
CH1: V_{ACIN}, 5V/Div, DC
CH2: V_{CHRIN}, 2V/Div, DC
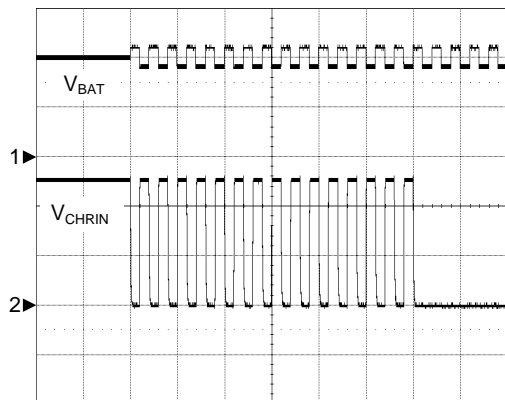CH3: I_{OUT}, 100mA/Div, DC
TIME:5μs/Div

Recovery from Input OVP

V_{ACIN} = 12V to 5V, R_{OUT} = 50Ω
CH1: V_{ACIN}, 5V/Div, DC
CH2: V_{CHRIN}, 2V/Div, DC
CH3: I_{OUT}, 100mA/Div, DC
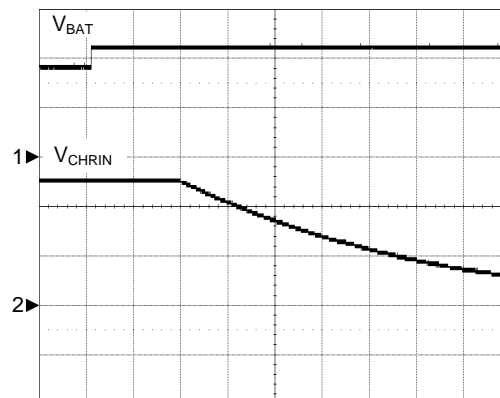TIME: 2ms/Div

Operating Waveforms (Cont.)

The test condition is V_{ACIN}=5V, V_{BAT}=3.8V, C_{ACIN}=1µF, C_{CHRIN}=1µF, T_A= 25°C unless otherwise specified.

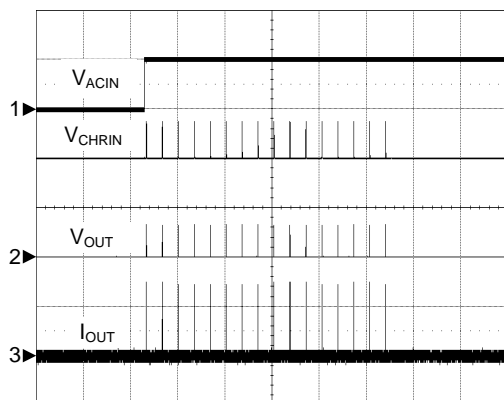**Battery Over-Voltage Protection**

V_{BAT} = 3.6V to 4.4V to 3.6V
CH1: V_{BAT}, 2V/Div, AC
CH2: V_{CHRIN}, 2V/Div, DC
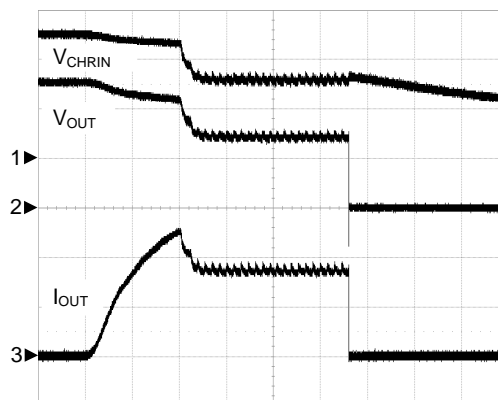TIME: 50ms/Div

Battery Over-Voltage Protection

V_{BAT} = 3.6V to 4.4V
CH1: V_{BAT}, 2V/Div, DC
CH2: V_{CHRIN}, 2V/Div, DC
TIME: 200µs/Div

Over-Current Protection

R_{OUT}=2.5Ω, V_{BAT} = 0V, V_{GATDRV}=0V
CH1: V_{ACIN}, 5V/Div, DC
CH2: V_{CHRIN}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: I_{OUT}, 1A/Div, DC
TIME: 200ms/Div
Note: OUT pin connected with a resistor to ground.

Over-Current Pretection

I_{OUT} = 0A to 1.3A, V_{BAT} = 0V, V_{GATDRV}=0V
CH1: V_{CHRIN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 0.5A/Div, DC
TIME: 50µs/Div
Note: OUT pin connected with a resistor to ground.

Pin Description

PIN		FUNCTION
NO.	NAME	
1,2	ACIN	Power Supply Input. Connect this pin to external DC supply. Bypass to GND with a 1μF (minimum) ceramic capacitor.
3	GND	Ground Terminal.
4	VBAT	Battery Voltage Sense Input. Connect this pin to pack positive terminal through a resistor.
5	GATDRV	Internal P-MOSFET Gate Input.
6	CHRIN	Output Pin. This pin provides supply voltage to the PMIC input. Bypass to GND with a 1μF (minimum) ceramic capacitor.
7,8	OUT	Output Pins. These pins provide supply source current in series with a resistor to battery.
-	EP	Exposed Thermal Pad. Must be electrically connected to the GND pin.

Block Diagram
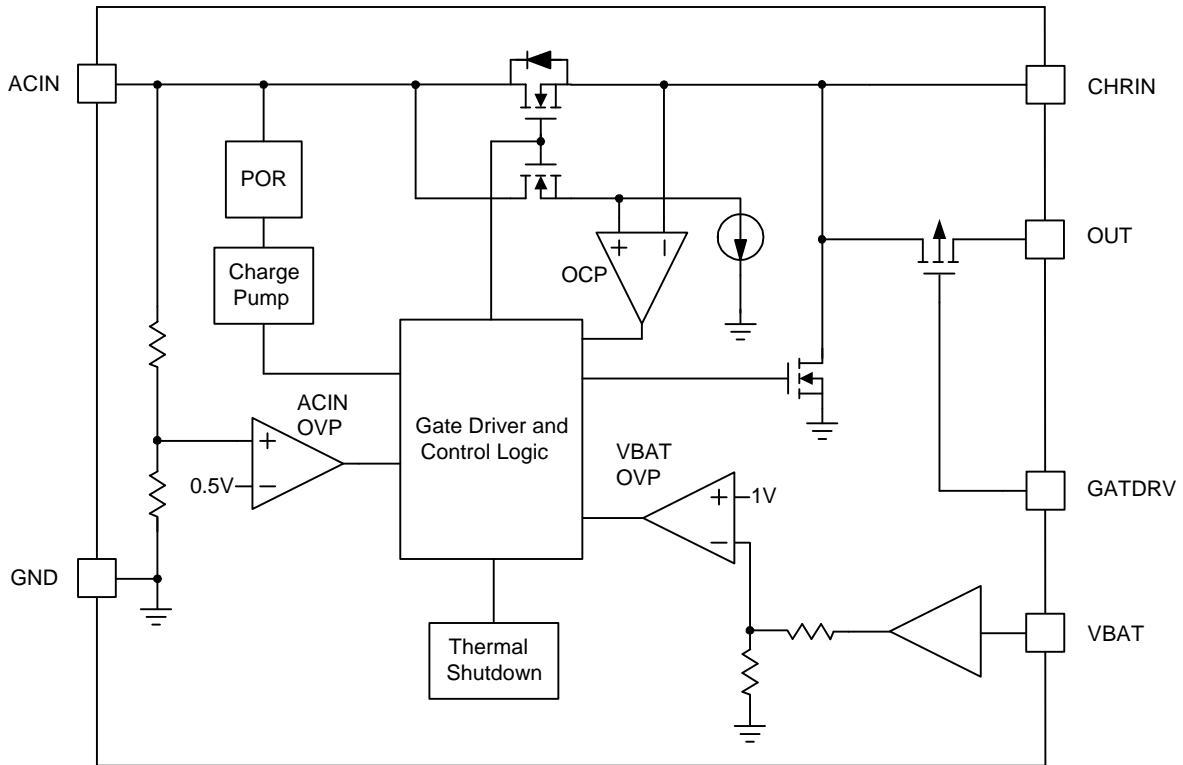
Typical Application Circuit
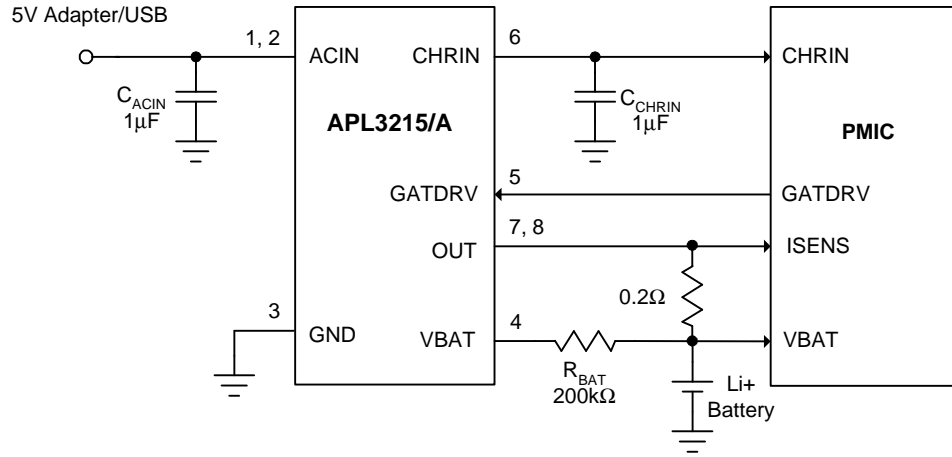
Designation	Description
C_{ACIN}	1µF, 25V, X5R, 0603 Murata GRM188R61E105K
C_{CHRIN}	1µF, 10V, X5R, 0603 Murata GRM188R61A105K

Murata website: www.murata.com

Function Description

ACIN Power-On-Reset (POR)

The APL3215/A has a built-in power-on-reset circuit to keep the output shutting off until internal circuitry is operating properly. The POR circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When the input voltage exceeds the POR threshold and after 8ms blanking time, the output voltage starts a soft-start to reduce the inrush current.

ACIN Over-Voltage Protection (OVP)

The input voltage is monitored by the internal OVP circuit. When the input voltage rises above the input OVP threshold, the internal FET will be turned off within 1µs to protect connected system on OUT pin. When the input voltage returns below the input OVP threshold minus the hysteresis, the FET is turned on again after 8ms recovery time. The input OVP circuit has a 300mV hysteresis and a recovery time of $T_{ON(OVP)}$ to provide noise immunity against transient conditions.

Over-Current Protection (OCP)

The output current is monitored by the internal OCP circuit. When the output current reaches the OCP threshold, the device limits the output current at OCP threshold level. If the OCP condition continues for a blanking time of $T_{B(OCP)}$, the internal power FET is turned off. After the recovery time of $T_{ON(OCP)}$, the FET will be turned on again. The APL3215/A has a built-in counter. When the total count of OCP fault reaches 16, the FET is turned off permanently, requiring a V_{ACIN} POR again to restart.

Battery Over-Voltage Protection

The APL3215/A monitors the VBAT pin voltage for battery over-voltage protection. The battery OVP threshold is internally set to 4.35V. When the VBAT pin voltage exceeds the battery OVP threshold for a blanking time of $T_{B(BOVP)}$, the internal power FET is turned off. When the VBAT voltage returns below the battery OVP threshold minus the hysteresis, the FET is turned on again. The APL3215/A has a built-in counter. When the total count of battery OVP fault reaches 16, the FET is turned off permanently, requiring a V_{ACIN} POR again to restart.

Over-Temperature Protection

When the junction temperature exceeds 160°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 40°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over-temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Internal P-MOSFET

The APL3215/A integrates a P-channel MOSFET with the body diode reverse protection to replace the external P-MOSFET and Schottky diode for cell phone's PMIC. The body diode reverse protection prevents a reverse current flowing from the battery back to CHRIN pin. During power-on, when CHRIN voltage rises above the VBAT voltage by more than 150mV, the body diode of the P-channel MOSFET is forward biased from OUT to CHRIN, and P-MOSFET is controlled by the external GATDRV voltage. When the CHRIN voltage drops below V_{BAT}+20mV, the body diode of the P-channel MOSFET is forward biased from CHRIN to OUT and P-channel MOSFET is turned off. When any of input OVP, OCP, battery OVP, is detected, the internal P-channel MOSFET is also turned off.

ESD Tests

The APL3215/A VIN input pin fully supports the IEC61000-4-2. That means the VIN pin has immunity of ±15kV ESD discharge in Air condition, and immunity of ±8kV ESD discharge in Contact condition.
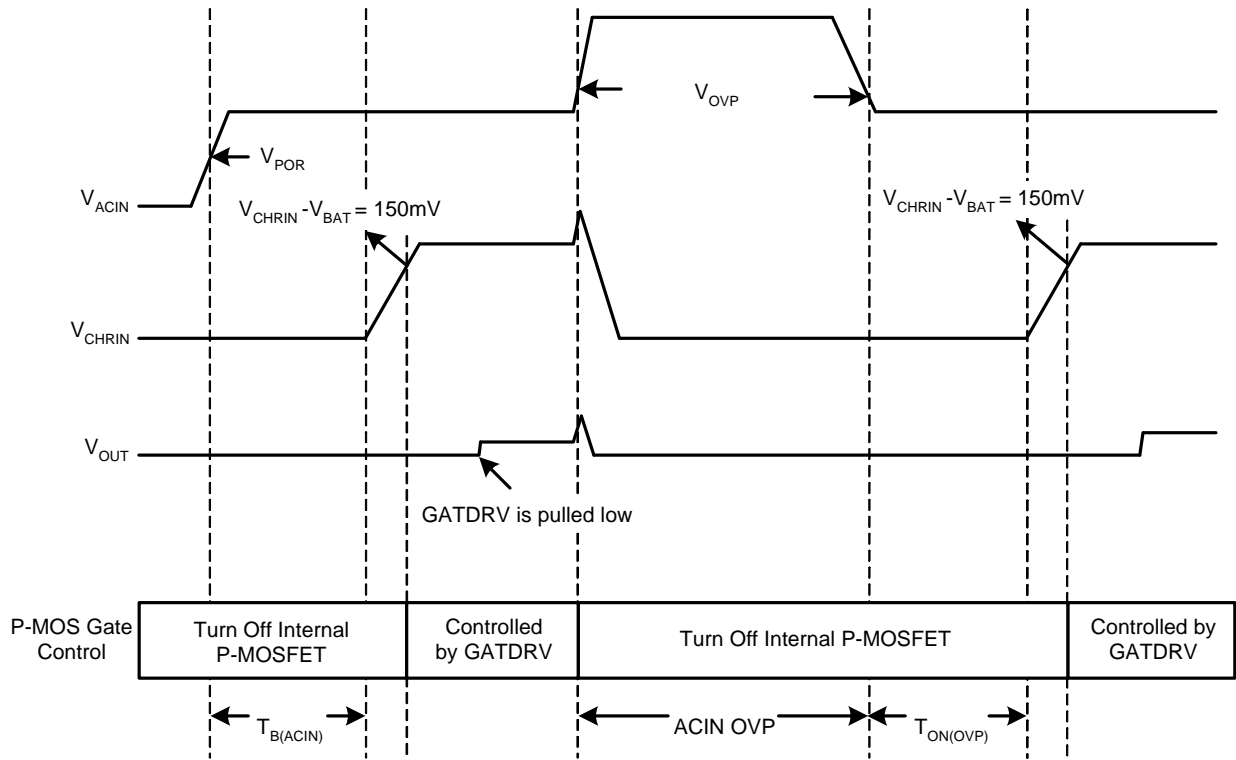
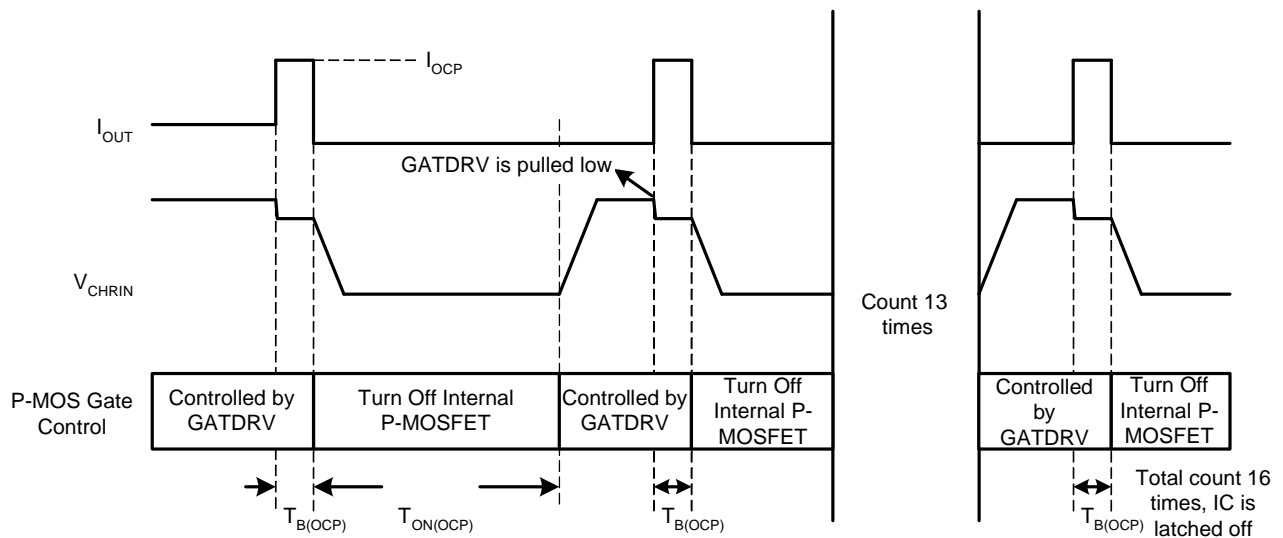## Function Description (Cont.)

Figure 1. OVP Timing Diagram

Figure 2. OCP Timing Diagram

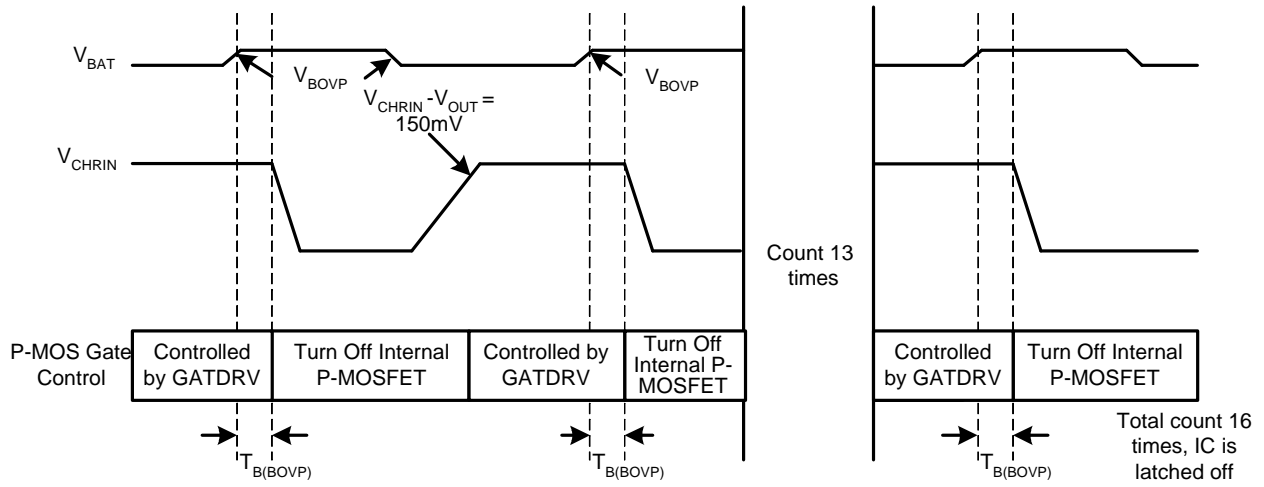## Function Description (Cont.)

Figure 3. Battery OVP Timing Diagram

Application Information

R$_{BAT}$ Selection

Connect the VBAT pin to the positive terminal of battery through a resistor R$_{BAT}$ for battery OVP function. The R$_{BAT}$ limits the current flowing from VBAT to battery in case of VBAT pin is shortened to ACIN pin under a failure mode. The recommended value of R$_{BAT}$ is 200kΩ. In the worse case of an IC failure, the current flowing from the VBAT pin to the battery is:

(20V-3V) / 200kΩ =85μA

where the 20V is the maximum ACIN voltage and the 3V is the minimum battery voltage. The current is so small and can be absorbed by the charger system.

Capacitor Selection

The input capacitor is for decoupling and prevents the input voltage from overshooting to dangerous levels. In the AC adapter hot plug-in applications or load current step-down transient, the input voltage has a transient spike due to the parasitic inductance of the input cable. A 25V, X5R, dielectric ceramic capacitor with a value between 1μF and 4.7μF placed close to the ACIN pin is recommended.

The output capacitor of CHRIN is for CHRIN voltage decoupling. Also, it can be as the input capacitor of the charging circuit. At least, a 1μF, 10V, X5R capacitor is recommended.

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where T$_{J(MAX)}$ is the maximum operation junction temperature, T$_A$ is the ambient temperature and the θ$_{JA}$ is the junction to ambient thermal resistance. For recommended operating conditions specification of APL3215/A, where T$_{J(MAX)}$ is 125°C and T$_A$ is the operated ambient temperature. The junction to ambient thermal resistance θ$_{JA}$ for TDFN2x2-8 package is 75°C/W on a high effective thermal conductivity test board in free air. The maximum power dissipation at T$_A$ = 25°C can be

calculated by the following formula :

$$P_{D(MAX)} = (125°C-25°C) / (75°C/W) = 1.33W$$

for TDFN2x2-8 packages

The maximum power dissipation depends on operating ambient temperature for fixed T$_{J(MAX)}$ and thermal resistance θ$_{JA}$. For APL3215/A packages, the Figure 4 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.
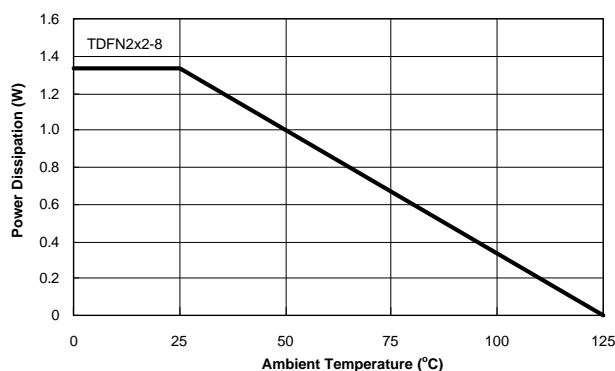

Figure 4. Derating Curves for APL3215/A Packages

Layout Consideration

In some failure modes, a high voltage may be applied to the device. Make sure the clearance constraint of the PCB layout must satisfy the design rule for high voltage. The exposed pad of the TDFN2x2-8 performs the function of channeling heat away. It is recommended that connect the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias to improve heat dissipation. The input and output capacitors should be placed close to the IC. The high current traces like input trace and output trace must be wide and short.

Package Information

TDFN2x2-8
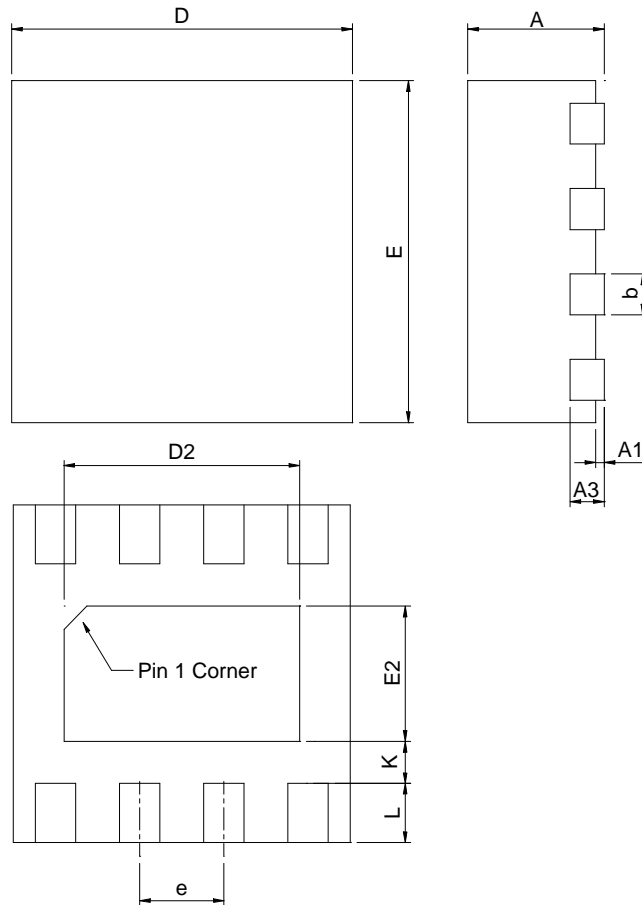
SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions
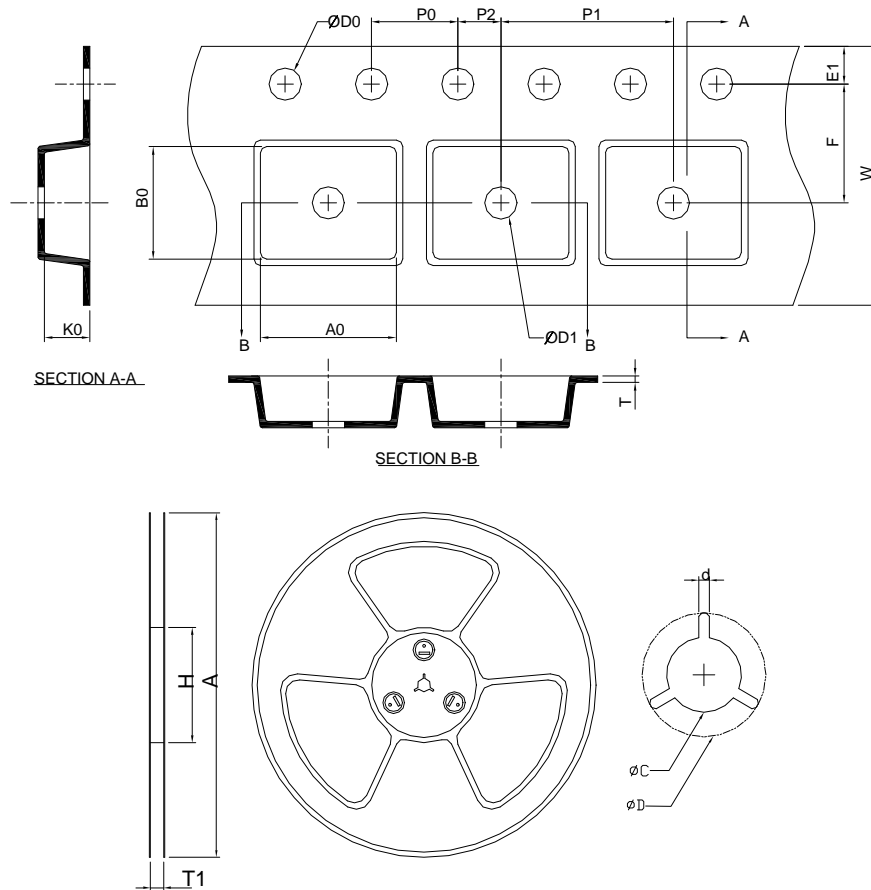
Application	A	H	T1	C	d	D	W	E1	F
	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
TDFN2x2-8	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	3.35 MIN	3.35 MIN	1.30±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8

USER DIRECTION OF FEED
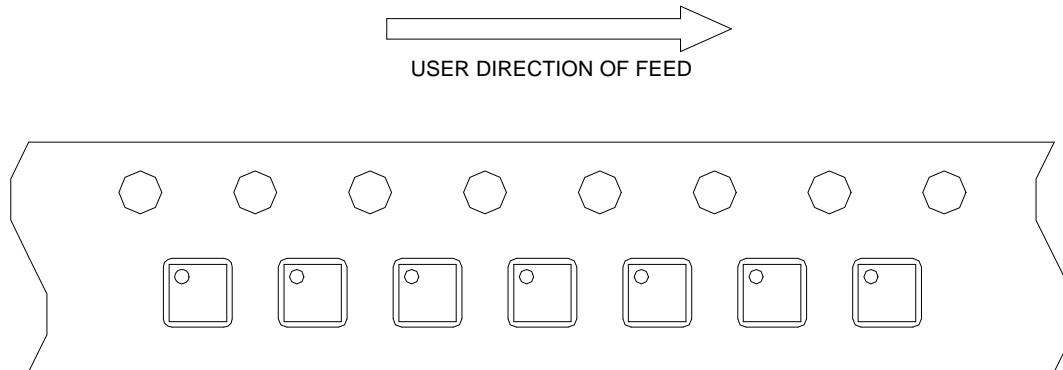
Classification Profile
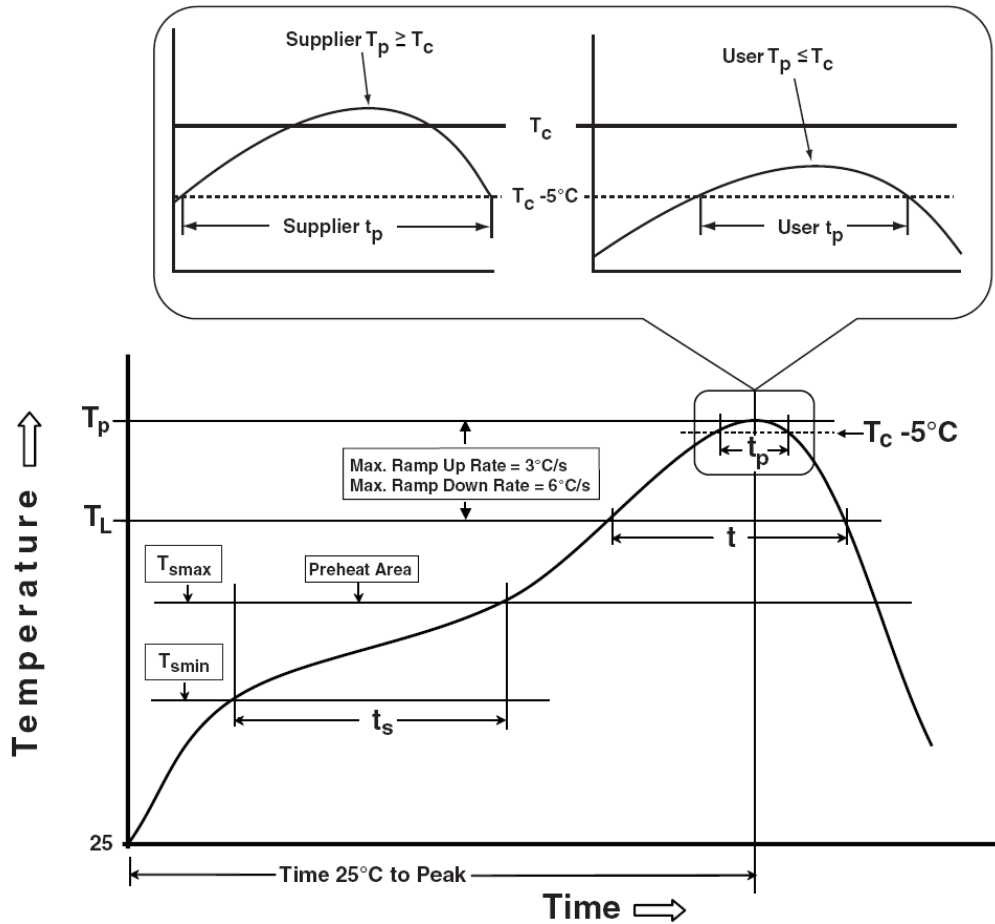
Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1_{tr} 100mA

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