



High speed, low power, operational amplifier

AD847

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD847

2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
AD847-703Q	High speed, low power, operational amplifier
AD847-713Q	Radiation Tested, High speed, low power, operational amplifier

2.1 Case Outline.

<u>Letter</u>	<u>Descriptive designator</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
Q	GDIP1-T8	8-Lead ceramic dual-in-line package (CERDIP)

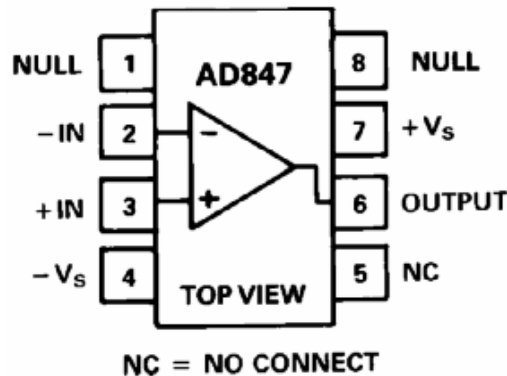


Figure 1 - Terminal connections.

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3.0 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Supply voltage	$\pm 18\text{ V}$
Differential input voltage	$\pm 6\text{ V}$
Input common mode voltage	$\pm V_S$
Operating temperature range.....	-55°C to $+125^\circ\text{C}$
Storage temperature range	-65°C to $+150^\circ\text{C}$
Power dissipation (P_D)	1.1W
Lead temperature (soldering, 10 seconds)	$+300^\circ\text{C}$
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	110°C/W
Junction temperature (T_J)	$+175^\circ\text{C}$

4.0 Electrical Table: See notes at end of table

Table I						
Parameter	Symbol	Conditions <u>1/</u>	Sub-group	<u>2/</u> Min	<u>2/</u> Max	Units
Input offset voltage	V_{IO}		1		± 1.0	mV
			2, 3		± 4.0	
Input bias current	I_B	$V_S = \pm 5\text{V}, \pm 15\text{V}$	1		5.0	μA
			2, 3		7.5	
Input offset current	I_{IO}		1		± 300	nA
			2, 3		± 400	
Common mode input voltage range <u>3/</u>	IVR	$V_S = \pm 15\text{V}$	1, 2, 3		± 2.5	V
			1, 2, 3		± 12	
Open loop gain	AVO	$V_{OUT} = \pm 2.5\text{V}, R_L = 500\Omega$	1	2.0		V/mV
			2, 3	1.0		
		$V_{OUT} = \pm 10\text{V}, R_L = 1\text{k}\Omega, V_S = \pm 15\text{V}$	1	3.0		
			2, 3	1.5		
Common mode rejection ratio	CMRR	$V_{CM} = \pm 2.5\text{V}$	1	80		dB
			1	80	$V_{CM} = \pm 12\text{V}, V_S = \pm 15\text{V}$	
Output current <u>4/</u>	I_{OUT}	$V_{OUT} = \pm 2.5\text{V}$	4	13		mA
			4	20		
Output voltage swing	$+V_{OUT}$	$R_L = 500\Omega$	1	3.0		V
			2, 3	2.5		
		$R_L = 150\Omega$	1	2.5		
			1, 2, 3	12		
			1	10		
	$-V_{OUT}$	$R_L = 500\Omega$	1	-3.0		
			2, 3	-2.5		
		$R_L = 150\Omega$	1	-2.5		
			1, 2, 3	-12		
			1	-10		
Quiescent power supply current	I_{CC}		1		5.7	mA
			2, 3		7.8	
			1		6.3	
			2, 3		8.4	
Power supply rejection ratio	PSRR	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	1	75		dB
			2, 3	72		
Differential input resistance <u>4/</u>	R_{IN}	$V_S = \pm 5\text{V}, \pm 15\text{V}$	4	80		k Ω

Table I						
Parameter	Symbol	Conditions <u>1/</u>	Sub-group	<u>2/</u> Min	<u>2/</u> Max	Units
Slew rate <u>6/ 4/</u>	+SR	$V_{OUT} = -2.5V$ to $+2.5V$, $R_L = 500\Omega$, $A_V = 1V/V$, Measured from 10% to 90%	4	120		V/ μ S
			5, 6	90		
	-SR	$V_{OUT} = +2.5V$ to $-2.5V$, $R_L = 500\Omega$, $A_V = 1V/V$, Measured from 10% to 90%	4	90		
			5, 6	65		
	+SR	$V_{OUT} = -5V$ to $+5V$, $R_L = 1K\Omega$, $V_S = \pm 15V$ Measured from 10% to 90%	4	200		
			5, 6	130		
-SR	$V_{OUT} = +5V$ to $-5V$, $R_L = 1K\Omega$, $V_S = \pm 15V$ Measured from 10% to 90%	4	145			
		5, 6	120			
Gain bandwidth product <u>4/</u>	GBWP	$V_{OUT} = \pm 100mV$, $R_L = 500\Omega$	4	25		MHz
		$V_{OUT} = \pm 100mV$, $R_L = 1K\Omega$, $V_S = \pm 15V$		40		
Full power bandwidth <u>4/</u>	FPBW	$V_{PK} = 2.5V$, $R_L = 500\Omega$	4	5.7		
		$V_{PK} = 10V$, $R_L = 1K\Omega$, $V_S = \pm 15V$		2.8		
Closed loop stable gain <u>4/</u>	CLSG	$R_L = 1K\Omega$, $V_S = \pm 5V$, $\pm 15V$	4, 5, 6	1.0		V/V
Rise time <u>4/ 8/</u>	t_r	$V_{OUT} = 0V$ to $+200mV$, $A_V = +1$, $R_L = -1K\Omega$, $V_S = \pm 15V$	4, 5, 6		10	nS
	t_f	$V_{OUT} = 0V$ to $-200mV$, $A_V = +1$, $R_L = -1K\Omega$, $V_S = \pm 15V$	4, 5, 6		10	
Settling time <u>4/</u>	t_s	$A_V = -1V/V$, 10V step at 0.1% of the fixed value, $R_L = 1K\Omega$			150	
		$A_V = -1V/V$, 10V step at 0.01% of the fixed value, $R_L = 1K\Omega$			200	
Overshoot <u>4/</u>	+OS	$V_{OUT} = 0V$ to $+200mV$, $A_V = +1$, $R_L = 1K\Omega$, $V_S = \pm 15V$	4		30	%
	-OS	$V_{OUT} = 0V$ to $-200mV$, $A_V = +1$, $R_L = 1K\Omega$, $V_S = \pm 15V$	4		30	

TABLE I NOTES:

- 1/ Unless otherwise specified for dc tests, $V_S = \pm 5V$, $R_S < 100\Omega$, $R_L > 100k\Omega$, $V_{OUT} = 0V$, and $C_L \leq 10pF$.
Unless otherwise specified for ac tests, $A_V = \pm 1 V/V$, $R_L = 1k\Omega$, and $C_L = 10pF$.
- 2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only.
Negative current shall be defined as conventional current flow out of a device terminal.
- 3/ This parameter is guaranteed by CMRR test.
- 4/ If not tested, shall be guaranteed to the limits specified in table I herein.
- 5/ Quiescent power consumption is based on quiescent supply current test maximum (no load at the output).
- 6/ Slew rate test limits are guarantee after 5 minutes of warm-up.
- 7/ Full power bandwidth = $SR/(2\pi V_{PK})$.
- 8/ Rise and fall times measured between 10% and 90% point.

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4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.

2/ See Table III for delta parameters. See table I for conditions.

4.2 Table III. Burn-in test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
V _{OS}	±1	±1.5	±0.5	mV
±I _B	5	7.5	2.5	µA
I _{IO}	±300	±500	±200	nA

5.0 Life Test/Burn-In Circuit:

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	July 20, 2000
B	Update web address	Feb. 7, 2002
C	Update web address. Delete Burn-In circuit.	June 20, 2003
D	Update header/footer & add to 1.0 scope description.	Feb. 25, 2008

