μPD424263A/L, 42S4263A/L
262,144 x 16-Bit
Dynamic CMOS RAM

Description

The μPD424263A/L and μPD42S4263A/L are fast-page dynamic RAMs with the write-per-bit option, organized as 262,144 words by 16 bits, and designed to operate from a single power supply.

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424263A	+5 V
424263L	+3.3 V
42S4263A	+5 V; self-refresh mode
42S4263L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{UCAS}$ and $\overline{LCAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining $\overline{UCAS}$ or $\overline{LCAS}$ low. Data outputs return to high impedance when either $\overline{UCAS}$ or $\overline{LCAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{UCAS}$ or $\overline{LCAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle ($\overline{CBR}$) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

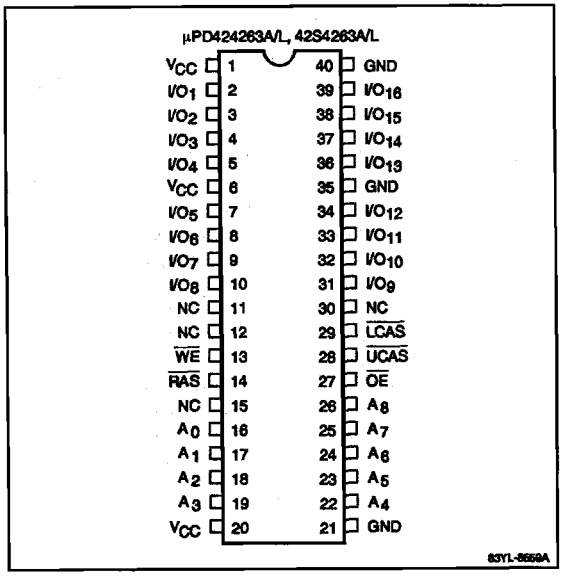
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a $\overline{CBR}$ cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 262,144 by 16-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Byte read/write control with $\overline{UCAS}$ and $\overline{LCAS}$
- Write-per-bit option; independent write control on 16 I/O's
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 512 refresh cycles every 8 ms
- 40-pin SOJ, 40-pin ZIP, and 44/40-pin TSOP plastic packaging

Pin Configurations

40-Pin Plastic SOJ



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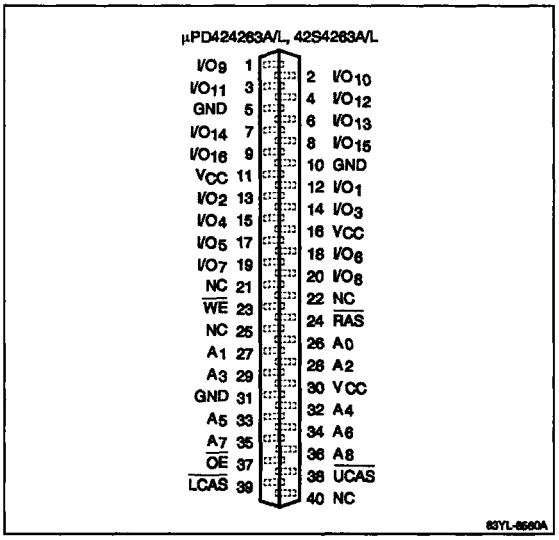
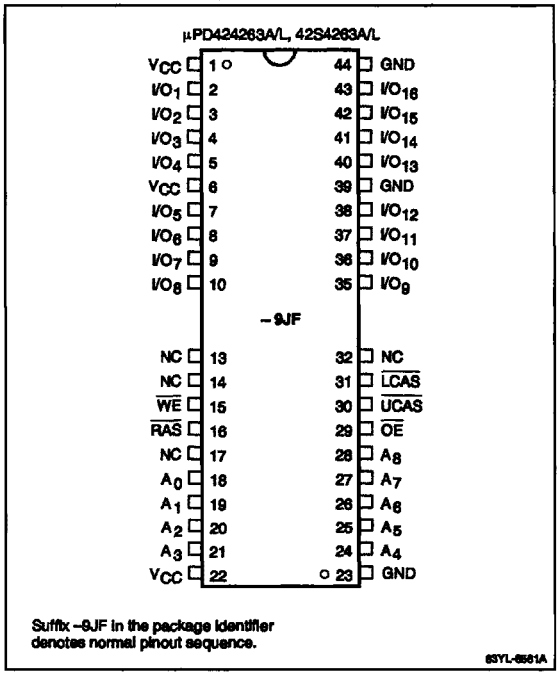
Pin Configurations (cont)

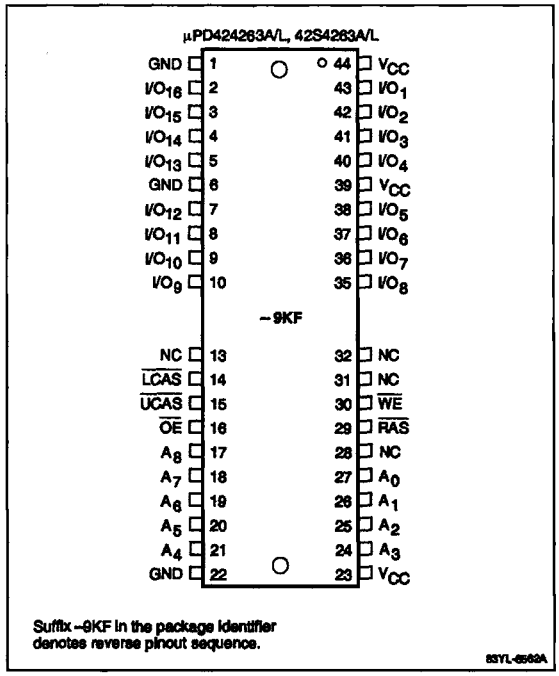
40-Pin Plastic ZIP



44/40-Pin Plastic TSOP (Normal Pinouts)



44/40-Pin Plastic TSOP (Reverse Pinouts)



Pin Identification

A_0 - A_8	Address inputs
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{LCAS}$, $\overline{UCAS}$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

Ordering Information, μPD424263A (+ 5-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424263ALE-60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-70	70 ns	45 ns		
LE-80	80 ns	50 ns		
μPD424263AV-60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-70	70 ns	45 ns		
V-80	80 ns	50 ns		
μPD424263AG5-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns		
G5-80	80 ns	50 ns		
μPD424263AG5M-60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns		
G5M-80	80 ns	50 ns		

Ordering Information, μPD424263L (+ 3.3-volt power)

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	$\overline{CAS}$ Access Time (max)	Package
μPD424263LLE-A60	60 ns	40 ns	20 ns	40-pin plastic SOJ
LE-A70	70 ns	45 ns		
LE-A80	80 ns	50 ns		
μPD424263LV-A60	60 ns	40 ns	20 ns	40-pin plastic ZIP
V-A70	70 ns	45 ns		
V-A80	80 ns	50 ns		
μPD424263LG5-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns		
G5-A80	80 ns	50 ns		
μPD424263LG5M-A60	60 ns	40 ns	20 ns	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns		
G5M-A80	80 ns	50 ns		

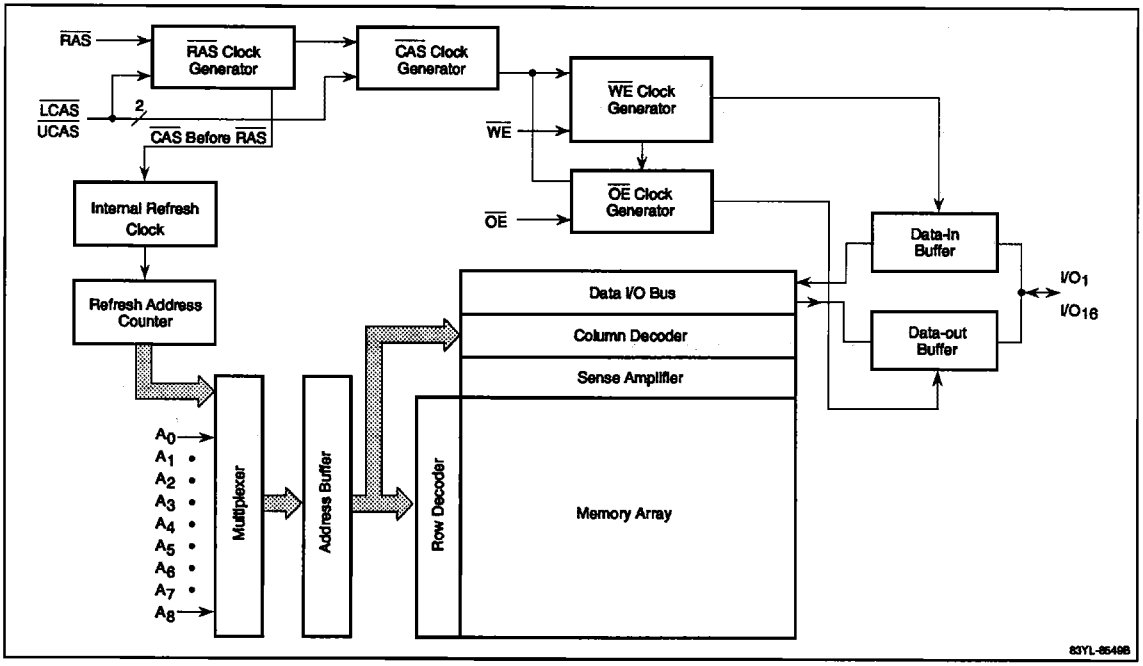
Ordering Information, μPD42S4263A (+ 5-volt power; self-refresh mode)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4263ALE-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4263AV-60	60 ns	40 ns	20 ns	300 μA	40-pin plastic ZIP
V-70	70 ns	45 ns			
V-80	80 ns	50 ns			
μPD42S4263AG5-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (normal pinouts)
G5-70	70 ns	45 ns			
G5-80	80 ns	50 ns			
μPD42S4263AG5M-60	60 ns	40 ns	20 ns	300 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	45 ns			
G5M-80	80 ns	50 ns			

Ordering Information, μPD42S4263L (+ 3.3-volt power; self-refresh mode)

Part Number	RAS Access Time (max)	Fast-Page Cycle Time (max)	CAS Access Time (max)	Self-Refresh Current (max)	Package
μPD42S4263LLE-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic SOJ
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			
μPD42S4263LV-A60	60 ns	40 ns	20 ns	100 μA	40-pin plastic ZIP
V-A70	70 ns	45 ns			
V-A80	80 ns	50 ns			
μPD42S4263LG5-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (normal pinouts)
G5-A70	70 ns	45 ns			
G5-A80	80 ns	50 ns			
μPD42S4263LG5M-A60	60 ns	40 ns	20 ns	100 μA	44/40-pin plastic TSOP (reverse pinouts)
G5M-A70	70 ns	45 ns			
G5M-A80	80 ns	50 ns			

Block Diagram



Truth Table

Function	RAS	LCAS	UCAS	WE	OE	I/O_1 - I/O_8	I/O_9 - I/O_{16}
Standby	H	X	X	X	X	High-Z	High-Z
Refresh cycle	L	H	H	X	X	High-Z	High-Z
Byte read cycle	L	L	H	H	L	Data output	High-Z
	L	H	L	H	L	High-Z	Data output
Word read cycle	L	L	L	H	L	Data output	Data output
Byte write cycle	L	L	H	L	H	Data input	—
	L	H	L	L	H	—	Data input
Word write cycle	L	L	L	L	H	Data input	Data input
——	L	L	L	H	H	High-Z	High-Z

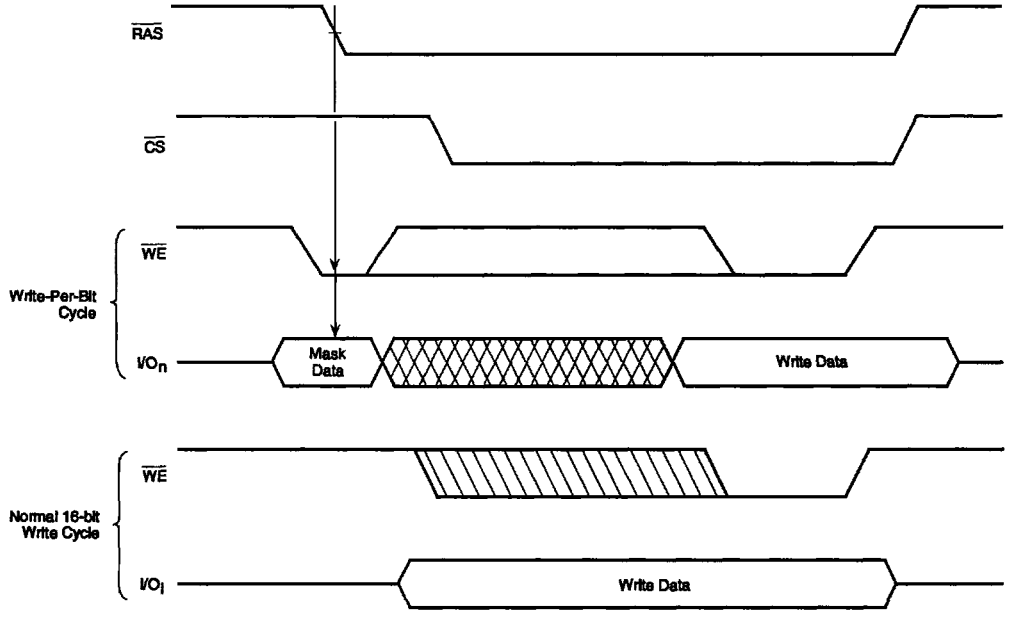
X = don't care.

7d

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 16-bit word. The mask is loaded from the I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE}$ = V_{IL}. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If the I/O line is low, the bit does not change. A mask loaded during fast-page operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed only at the falling edge of $\overline{RAS}$.

Comparison of Write-Per-Bit Cycle Versus Standard 16-Bit Write Cycle



I/O	Mask Data		Write Operation
I/O_1 ~ I/O_{16}	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

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Absolute Maximum Ratings

Voltage on any pin relative to GND	
5-volt devices	−1.0 to +7.0 V
3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
5-volt devices	50 mA
3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{16}

Recommended Operating Conditions

		5-Volt Devices			3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4263A) or +3.3 V ±0.3 V (42S4263L)

Symbol	42S4263A	42S4263L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

DC Characteristics; 5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

DC Characteristics; 3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

μPD424263A, 42S4263A: V_{CC} = +5.0 V ±10%

μPD424263L, 42S4263L: V_{CC} = +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		140		130		120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (+3.3)		130		120		110		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		140		130		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (+3.3)		130		120		110		
Operating current, fast-page cycle, average	I_{CC4} (+5)		90		80		70	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (+3.3)		90		80		70		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		140		130		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (+3.3)		130		120		110		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 3, 4, 7, 8, 16)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	(Note 15)
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	−35		−40		−50		ns	For 42S4263A/L only
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Notes 4, 7)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	(Note 14)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 13)
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 9)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 8)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	For 42S4263A/L
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	For 42S4263A/L
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	(Note 11)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	(Note 4)
Write-per-bit hold time	t_{WBH}	10		10		15		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write command hold time	t_{WCH}	15		15		15		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)
Write mask data hold time	t_{WH}	10		10		15		ns	
Write command pulse width	t_{WP}	15		15		15		ns	(Note 12)
Write mask data setup time	t_{WS}	0		0		0		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 volts and V_{OL} = 0.8 volt (ac reference levels)

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max); if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of one of the $\overline{CAS}$ signals for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD} and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

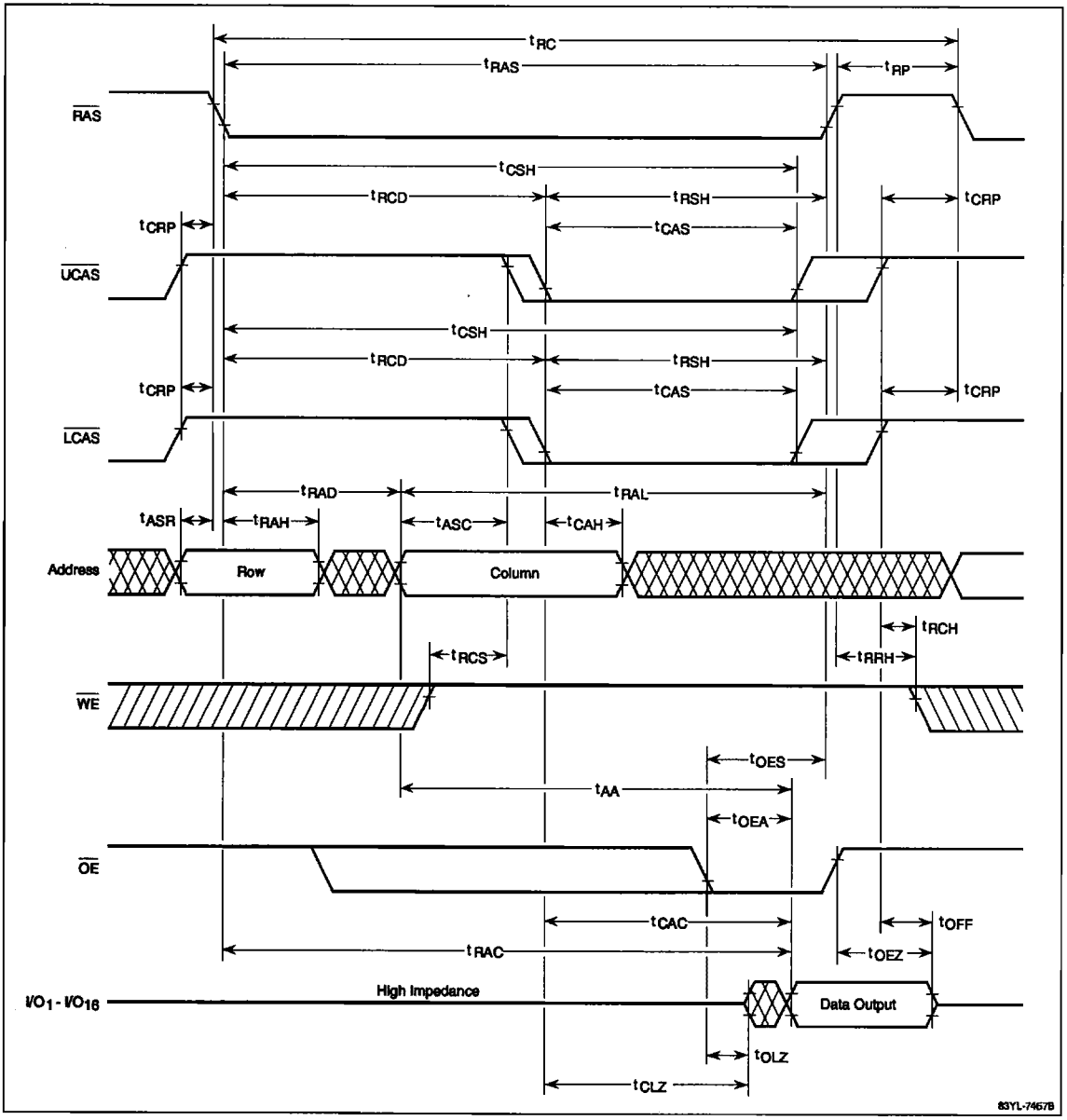
(15) Holding $\overline{LCAS}$ or $\overline{UCAS}$ low prior to $\overline{RAS}$ going negative will initiate a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (t_{CSR} and t_{CHR} must be satisfied).

(16) The first $\overline{CAS}$ falling edge is used as a reference for the start of t_{ACP} ($\overline{CAS}$ precharge access time).

7d

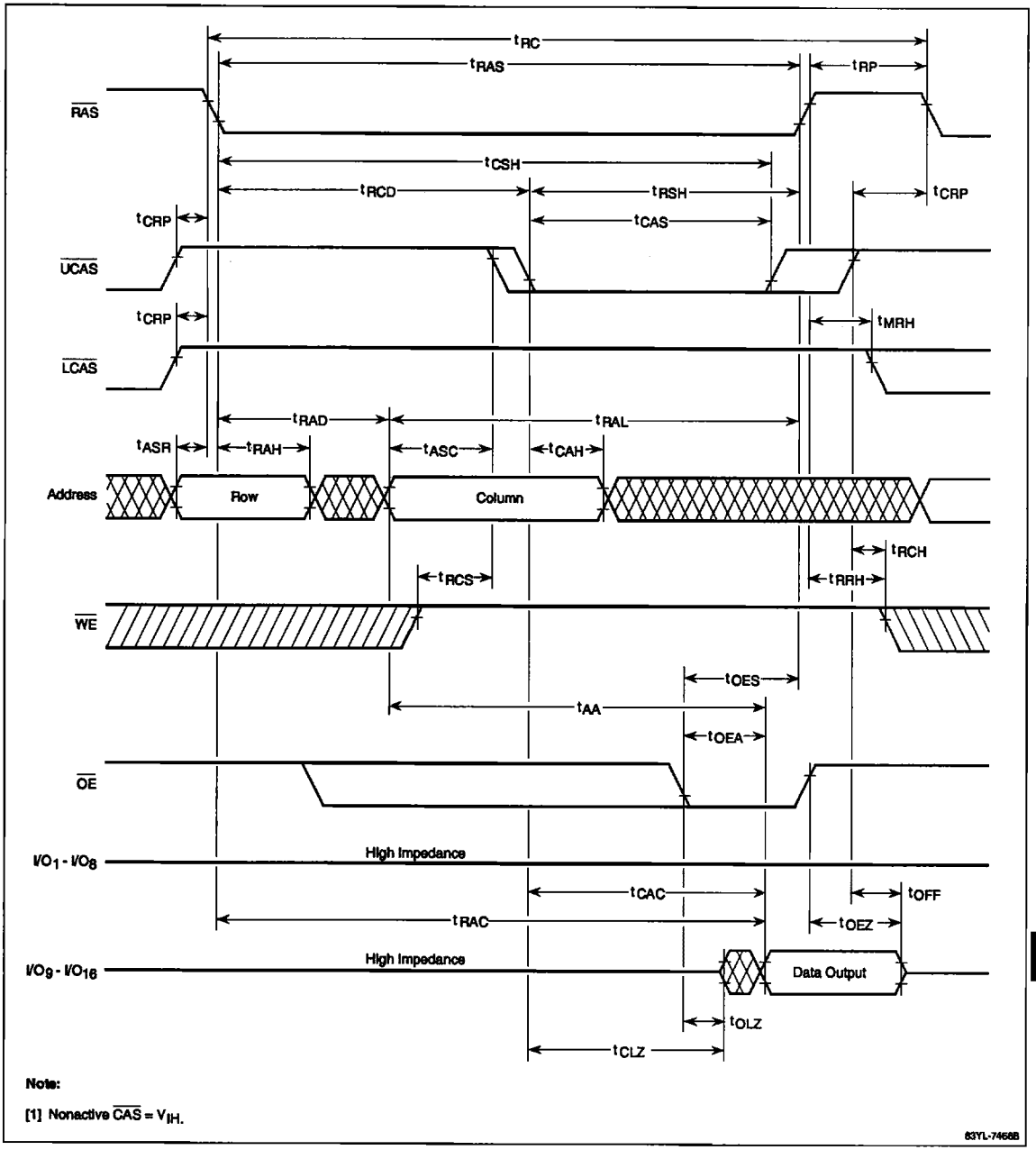
Timing Waveforms

Word Read Cycle



Timing Waveforms (cont)

Byte Read Cycle



Note:

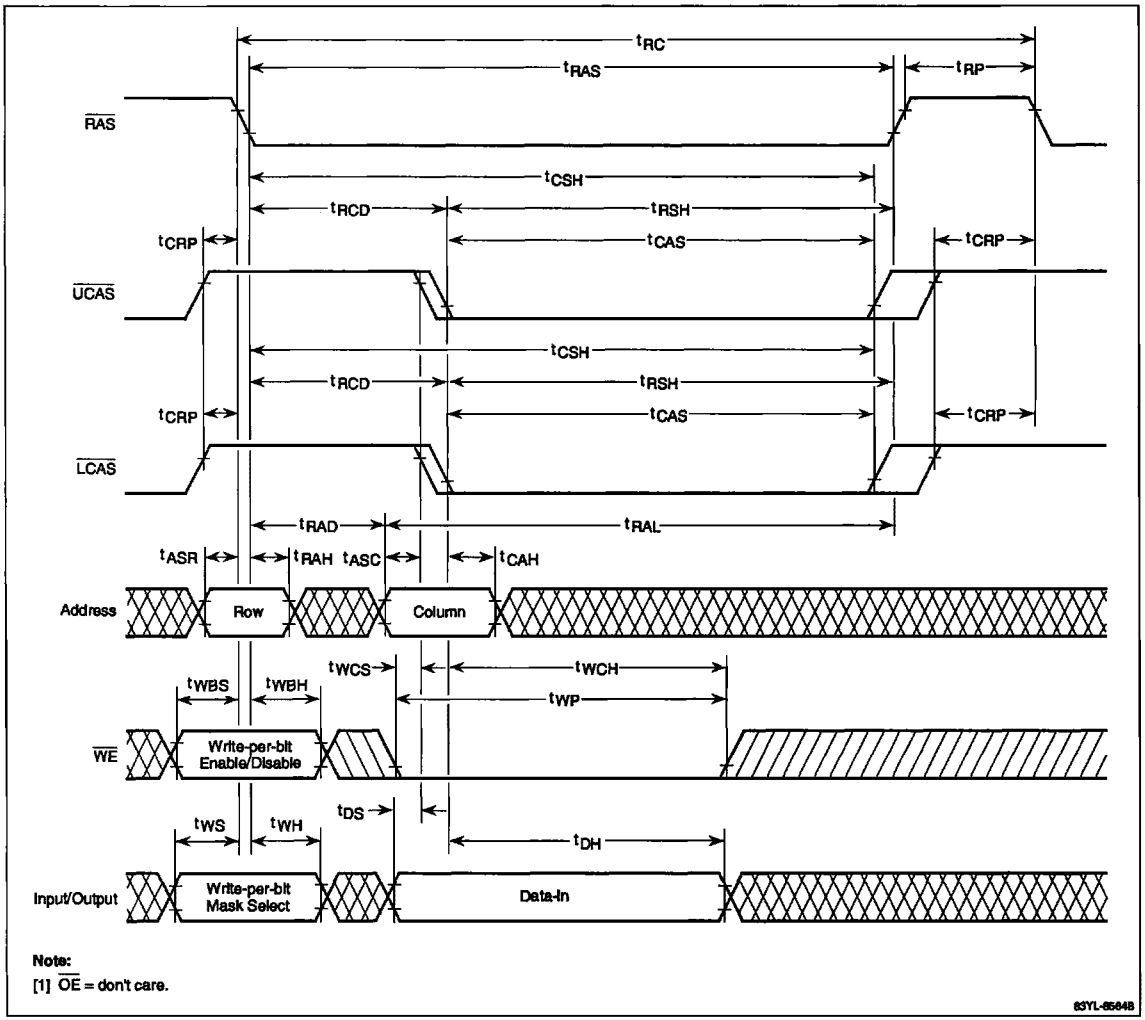
[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7466B

7d

Timing Waveforms (cont)

Word Early-Write Cycle

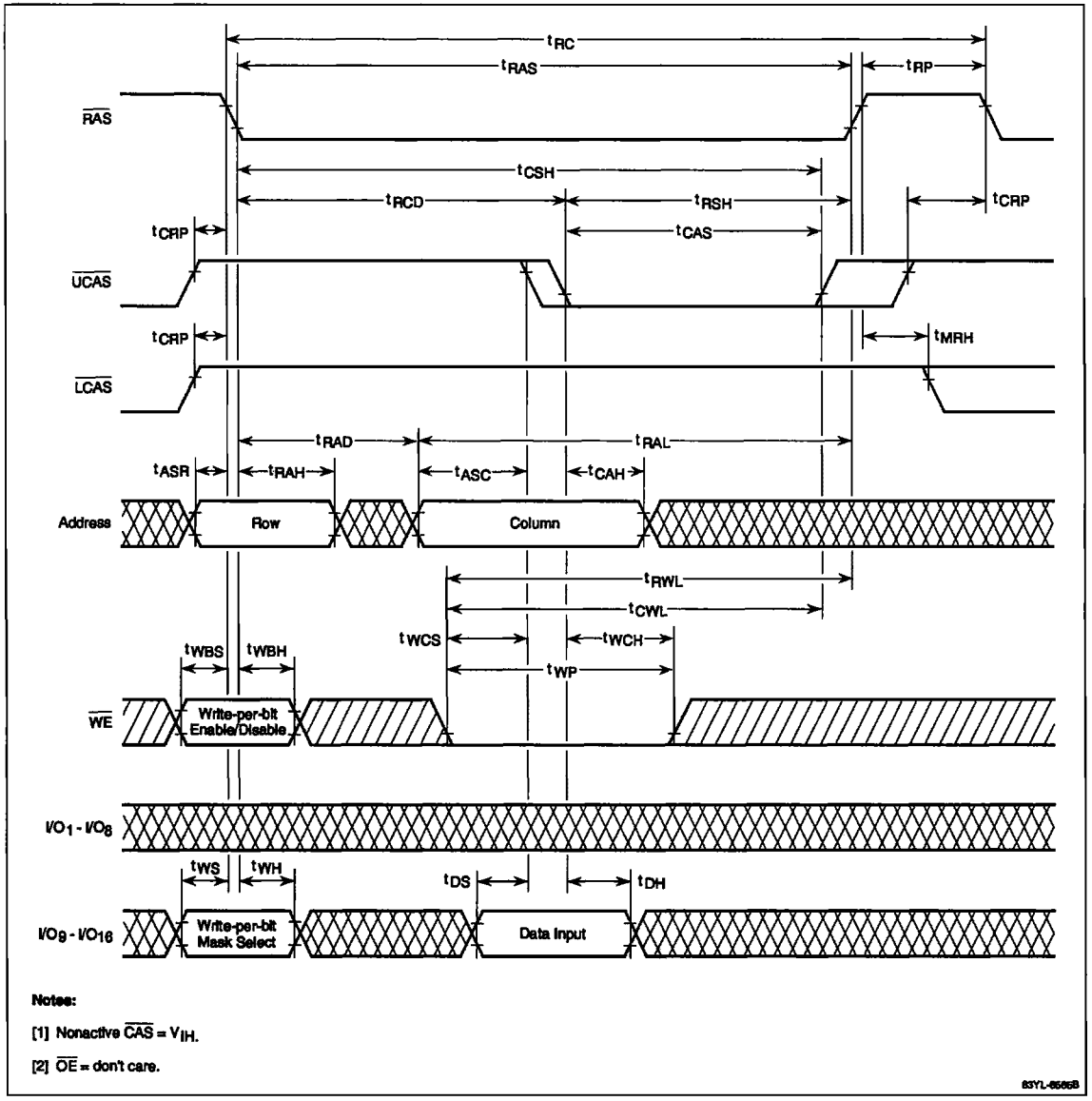


Note:
[1] $\overline{OE}$ = don't care.

83YL-6564B

Timing Waveforms (cont)

Byte Early-Write Cycle



Notes:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

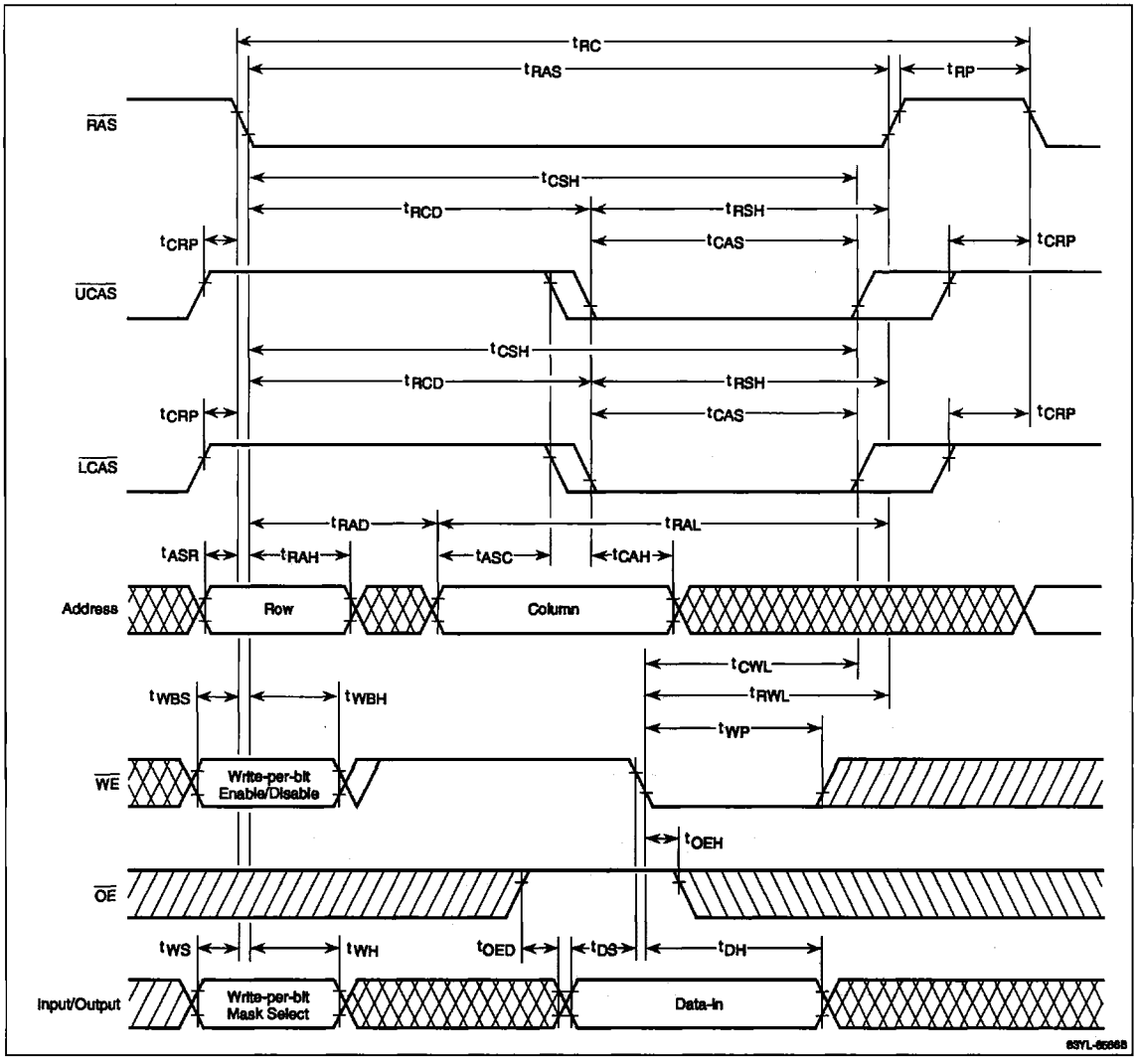
[2] $\overline{OE}$ = don't care.

83YL-8566B

7d

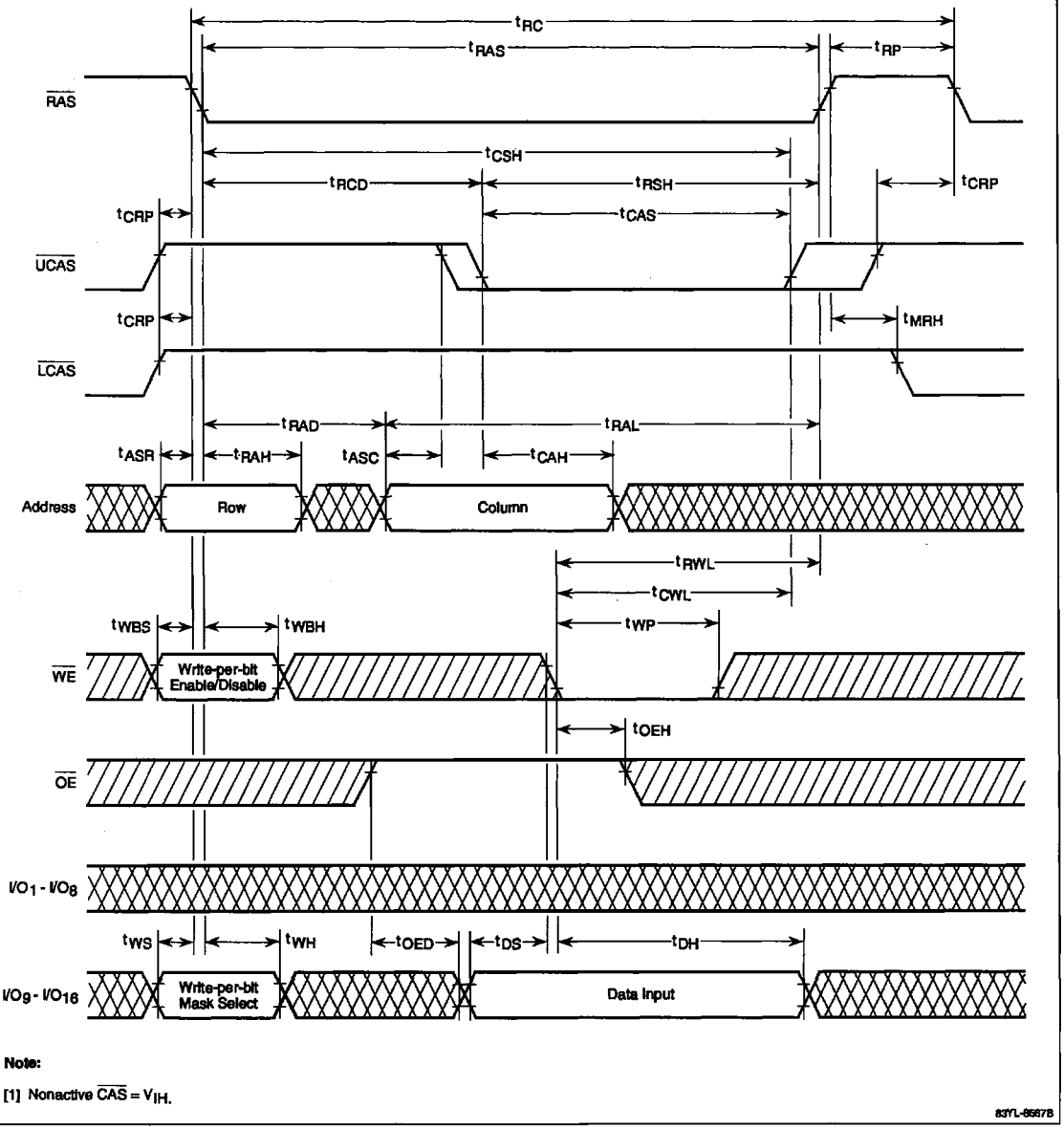
Timing Waveforms (cont)

Word Late-Write Cycle



Timing Waveforms (cont)

Byte Late-Write Cycle



Note:

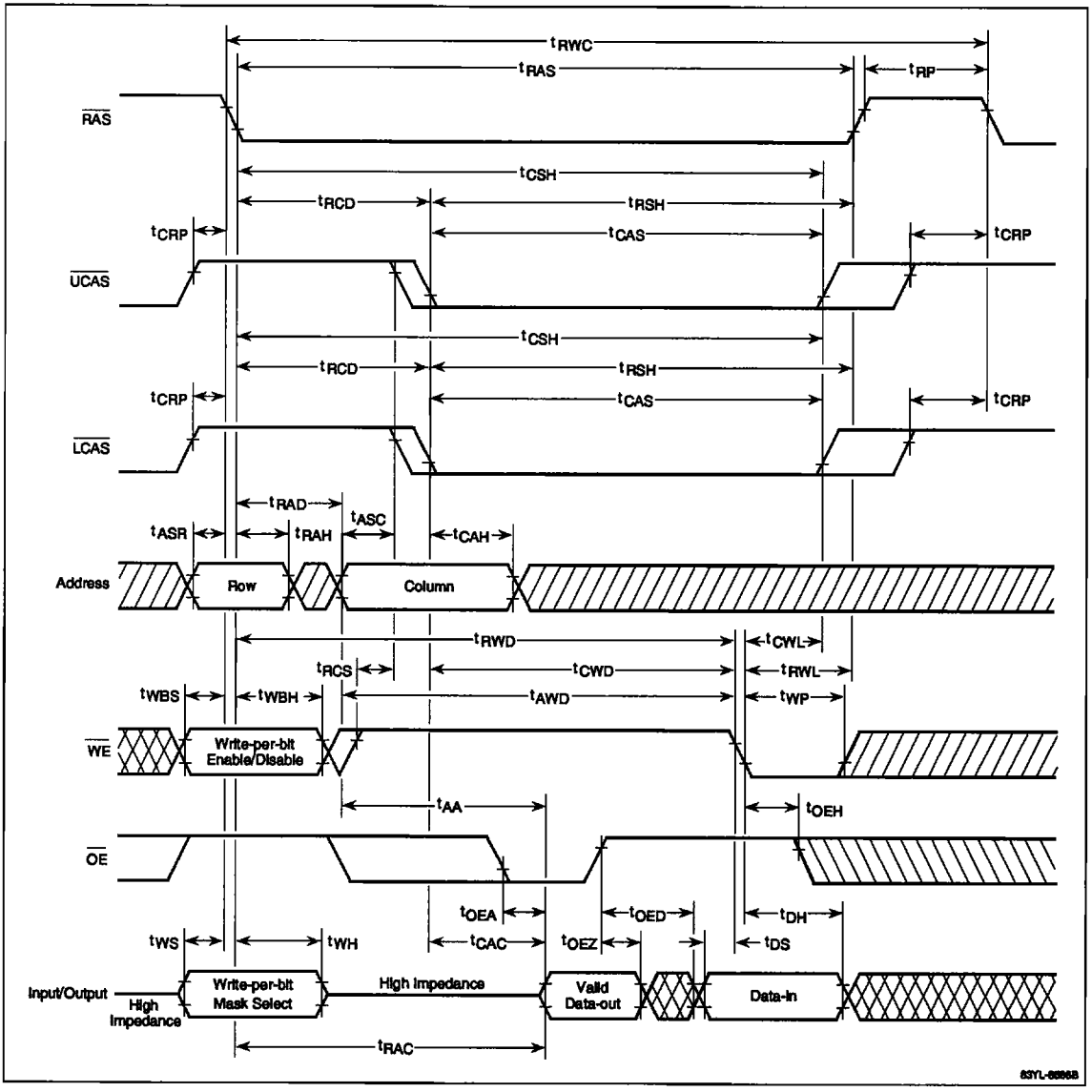
[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-8667B

7d

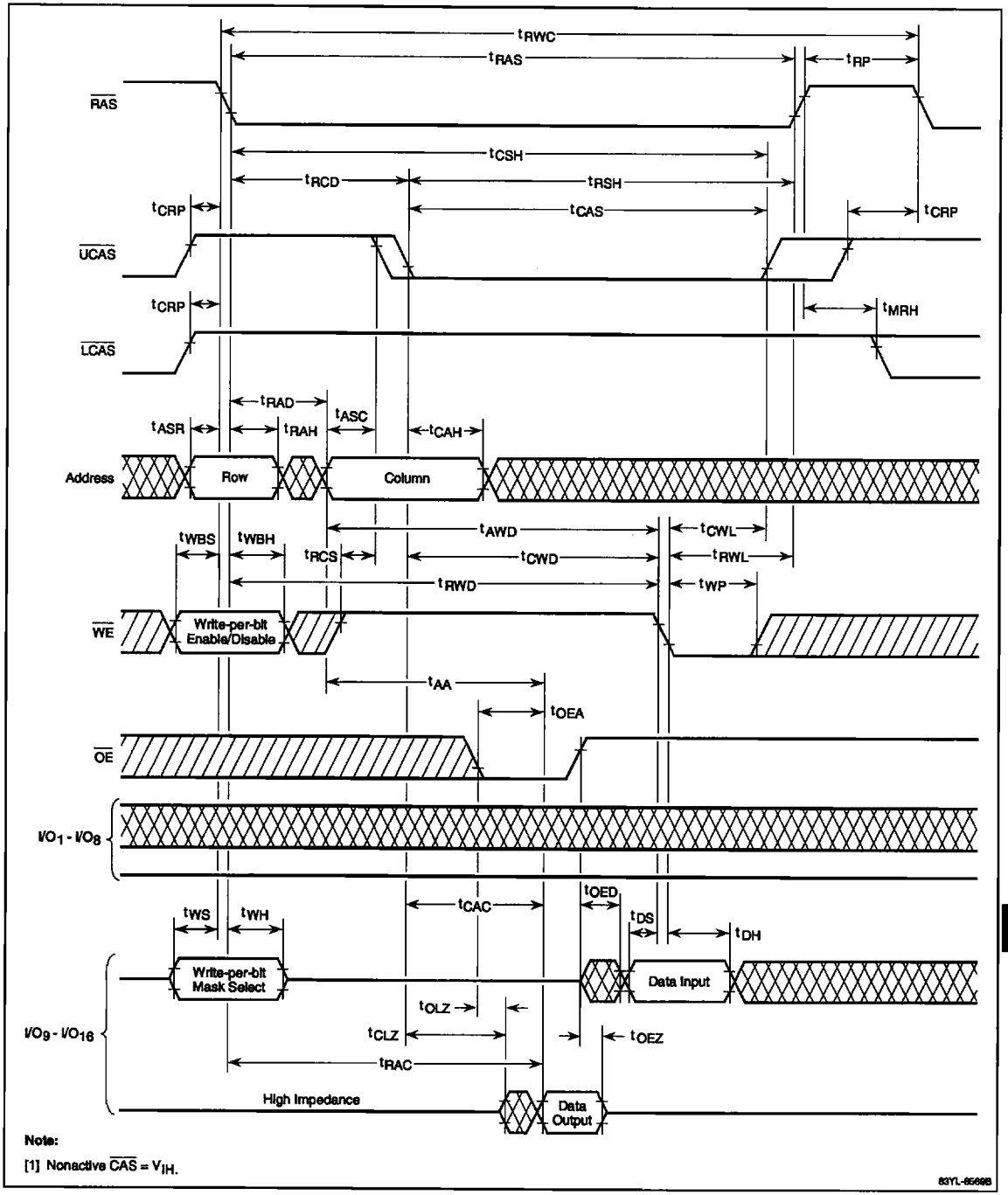
Timing Waveforms (cont)

Word Read-Modify-Write Cycle



Timing Waveforms (cont)

Byte Read-Modify-Write Cycle



Note:

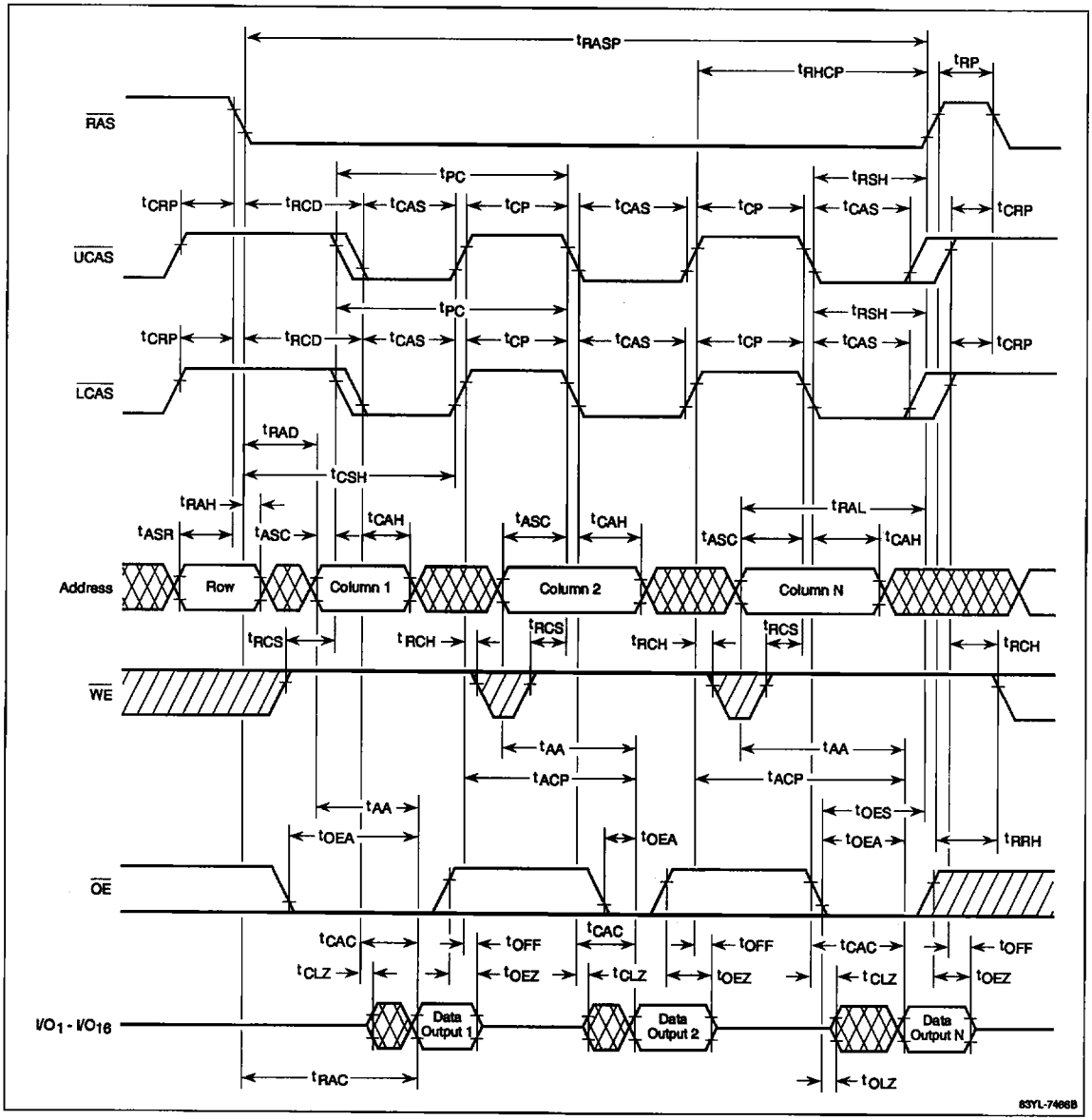
[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-85698

7d

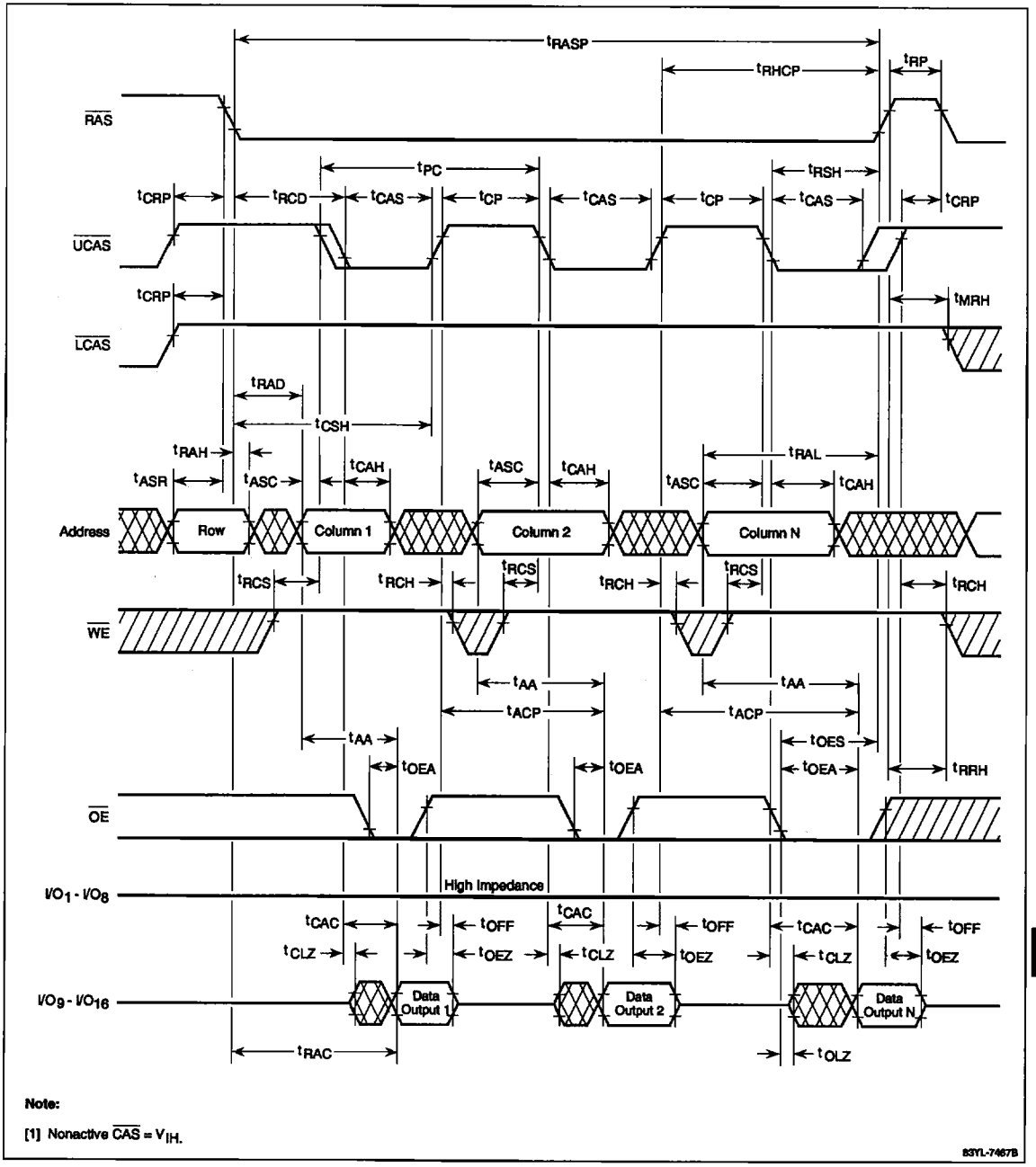
Timing Waveforms (cont)

Word Fast-Page Read Cycle



Timing Waveforms (cont)

Byte Fast-Page Read Cycle



Note:

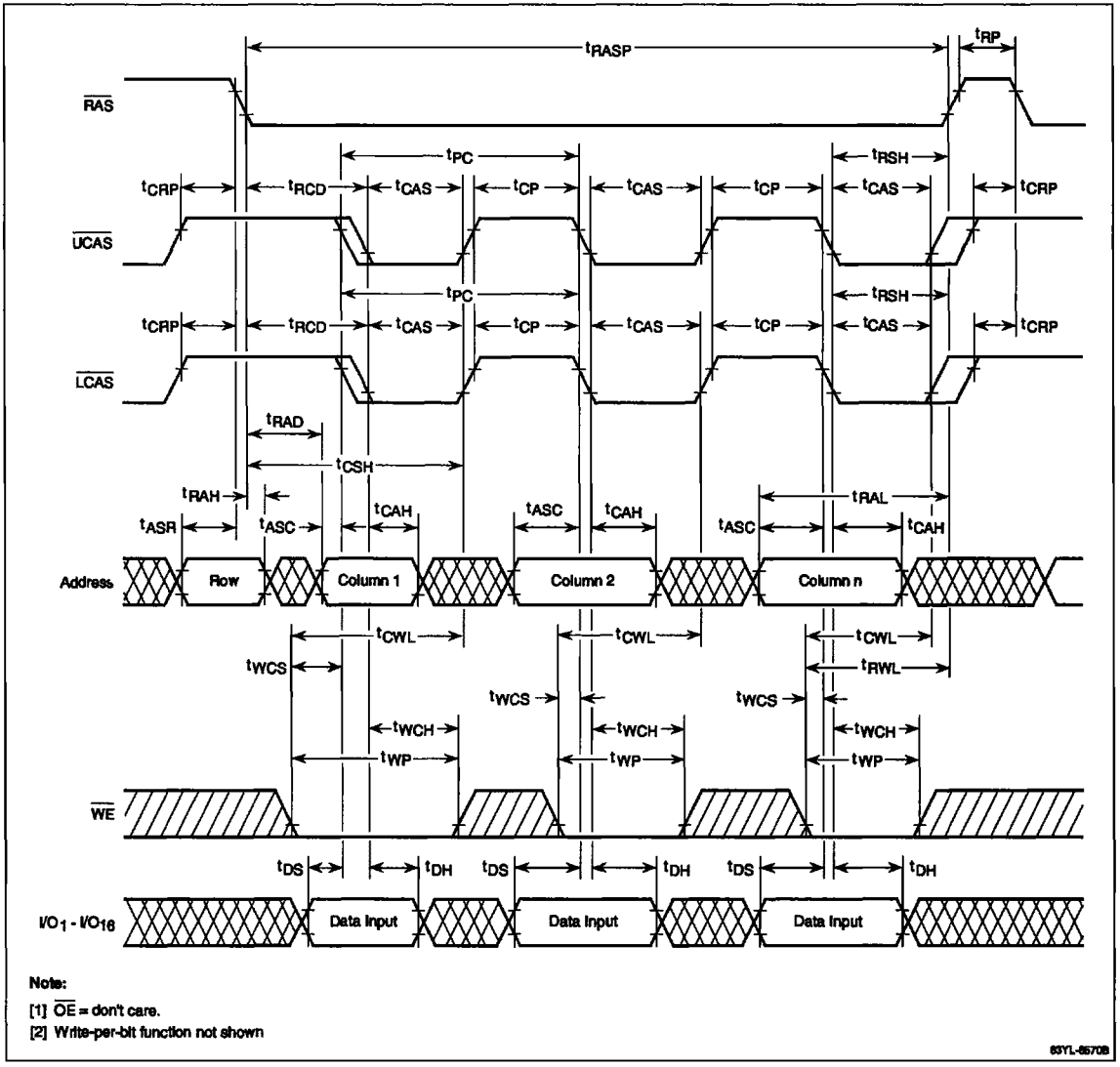
[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7467B

7d

Timing Waveforms (cont)

Word Fast-Page Early-Write Cycle



Note:

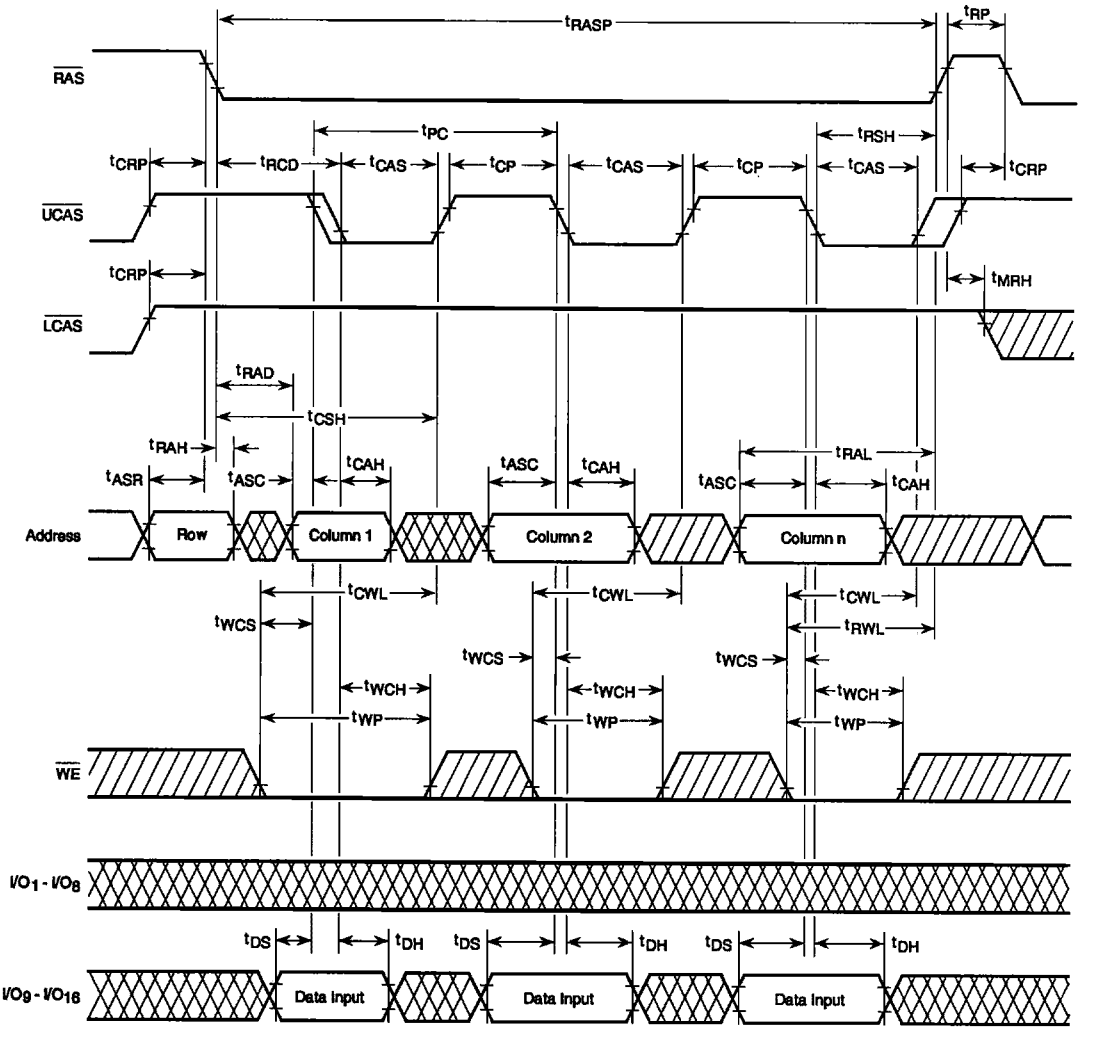
[1] $\overline{OE}$ = don't care.

[2] Write-per-bit function not shown

63YL-8570B

Timing Waveforms (cont)

Byte Fast-Page Early-Write Cycle



Notes:

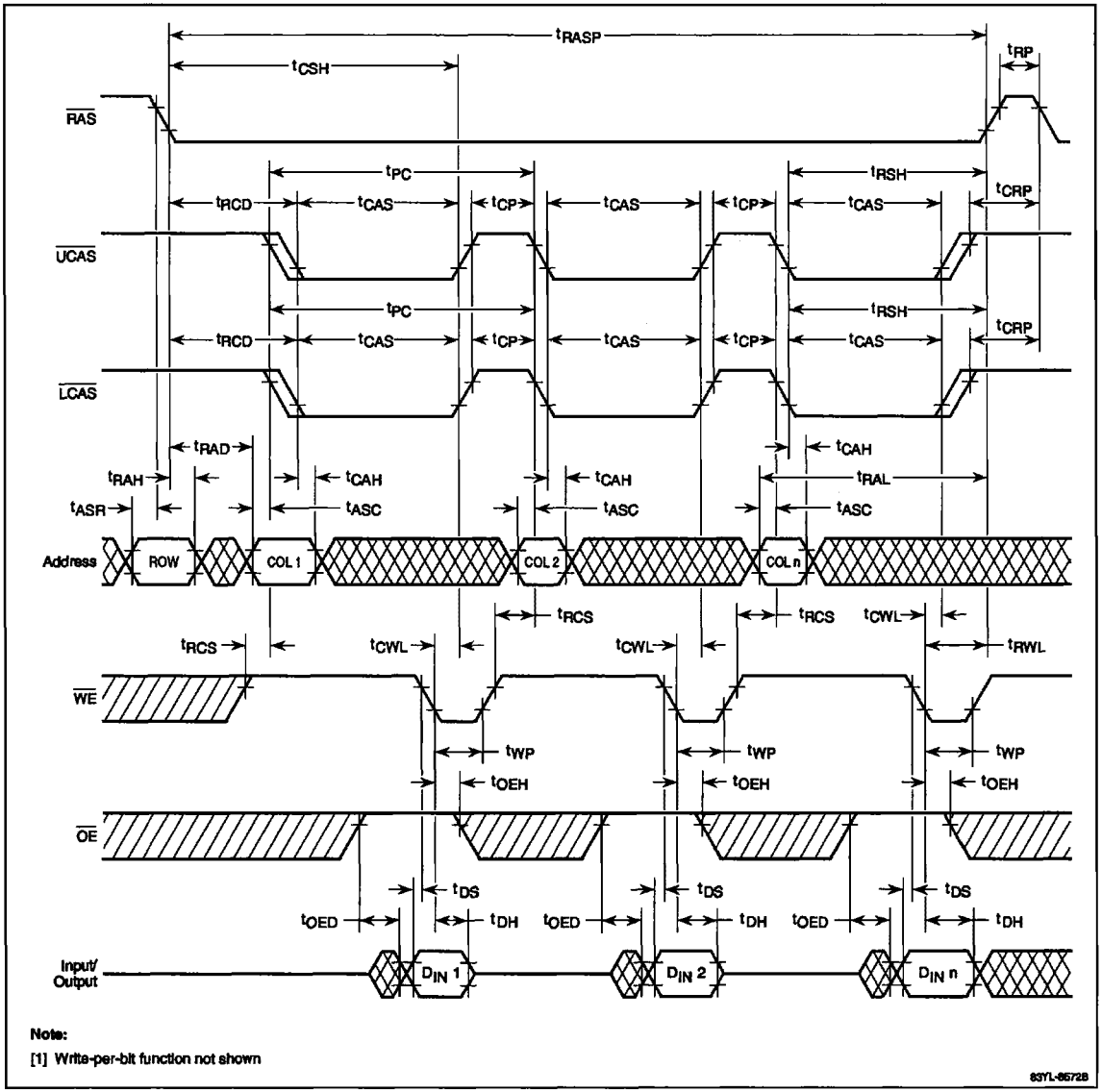
[1] Nonactive $\overline{CAS}$ = V_{IH}.
[2] $\overline{OE}$ = don't care.
[3] Write-per-bit function not shown

83YL-8571B

7d

Timing Waveforms (cont)

Word Fast-Page Late-Write Cycle



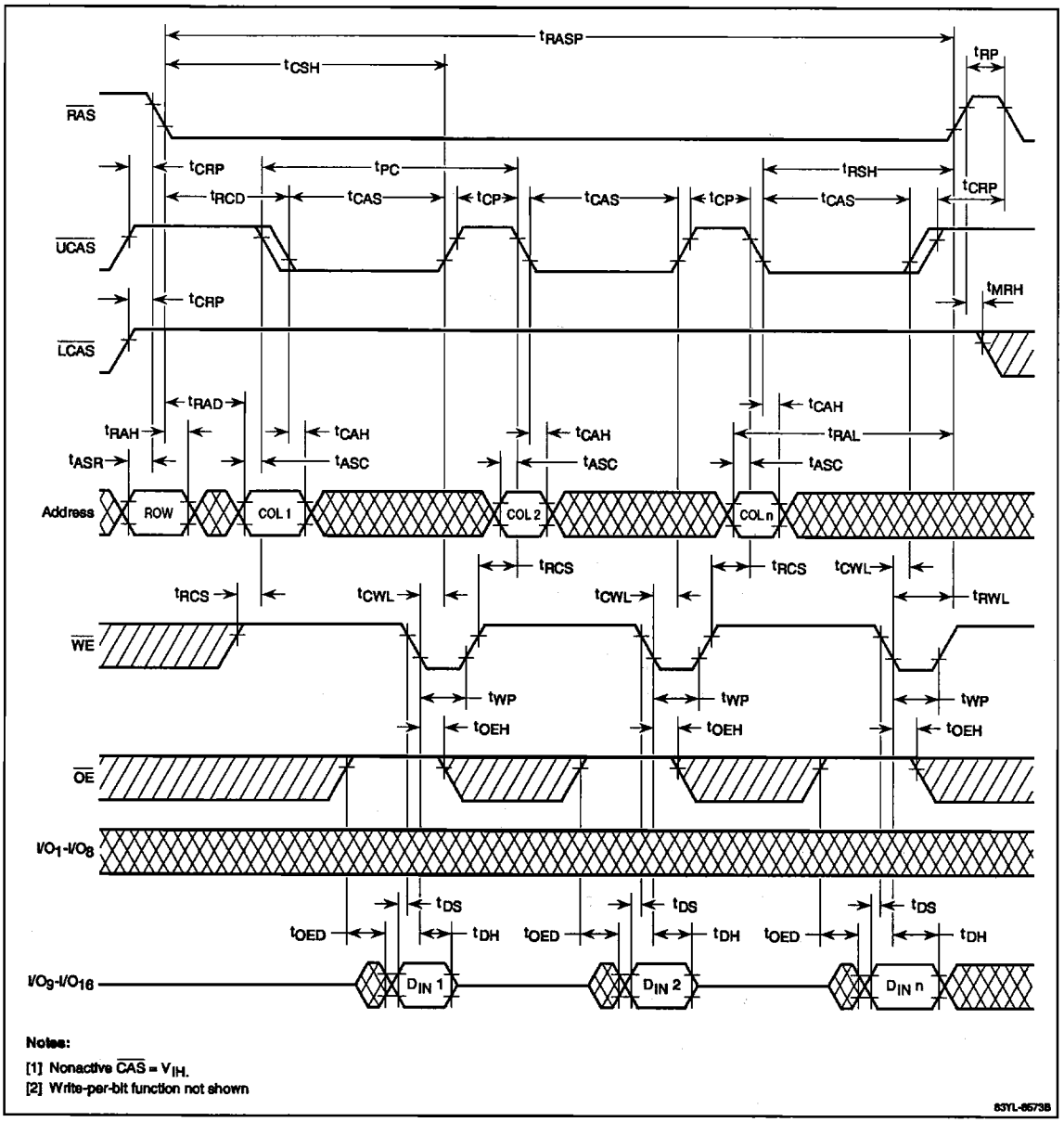
Note:

[1] Write-per-bit function not shown

83YL-85728

Timing Waveforms (cont)

Byte Fast-Page Late-Write Cycle



Notes:

[1] Nonactive $\overline{CAS}$ = V_{IH}.

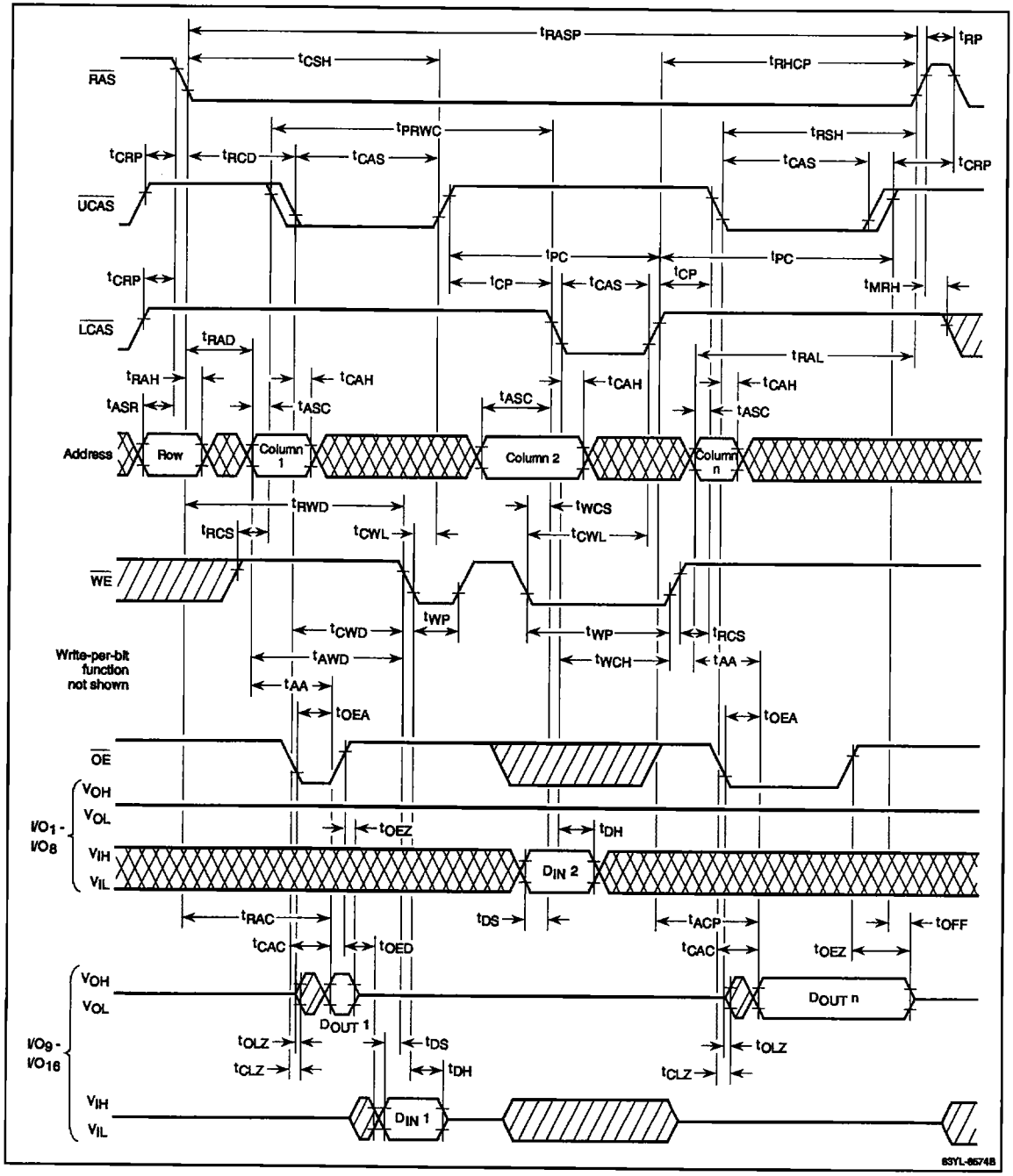
[2] Write-per-bit function not shown

83YL-8573B

7d

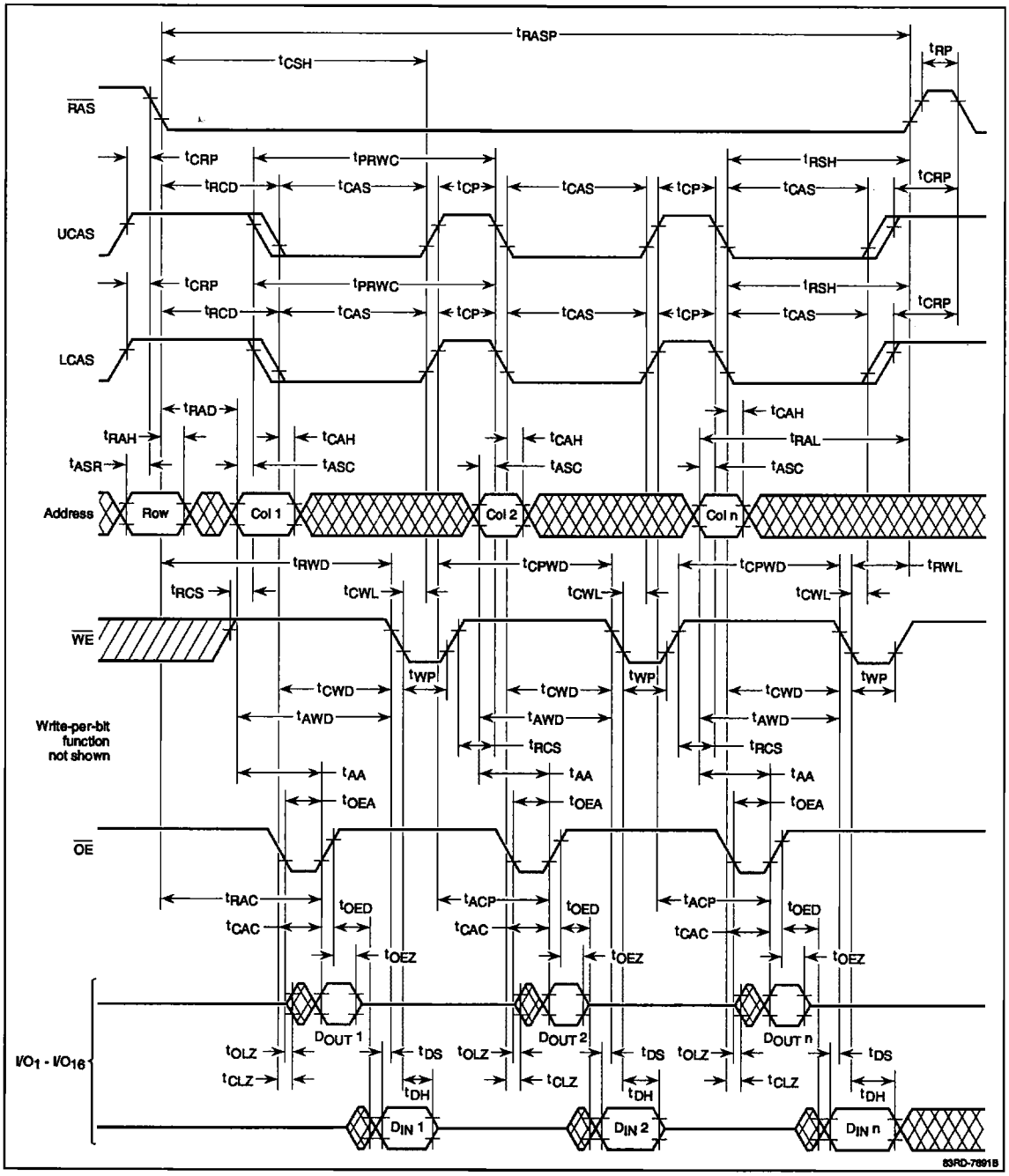
Timing Waveforms (cont)

Byte Fast-Page Read/Write Cycle



Timing Waveforms (cont)

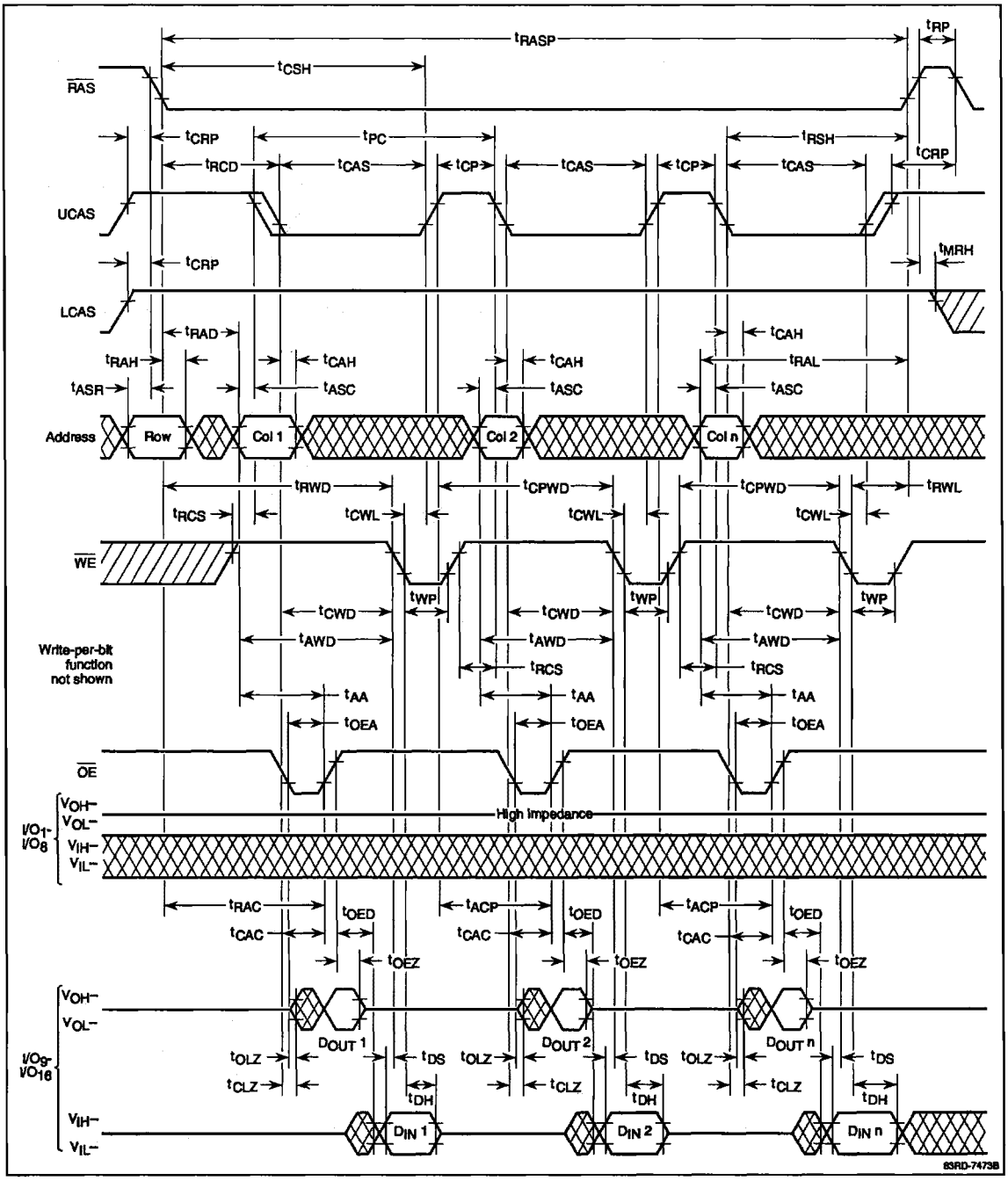
Word Fast-Page Read-Modify-Write Cycle



7d

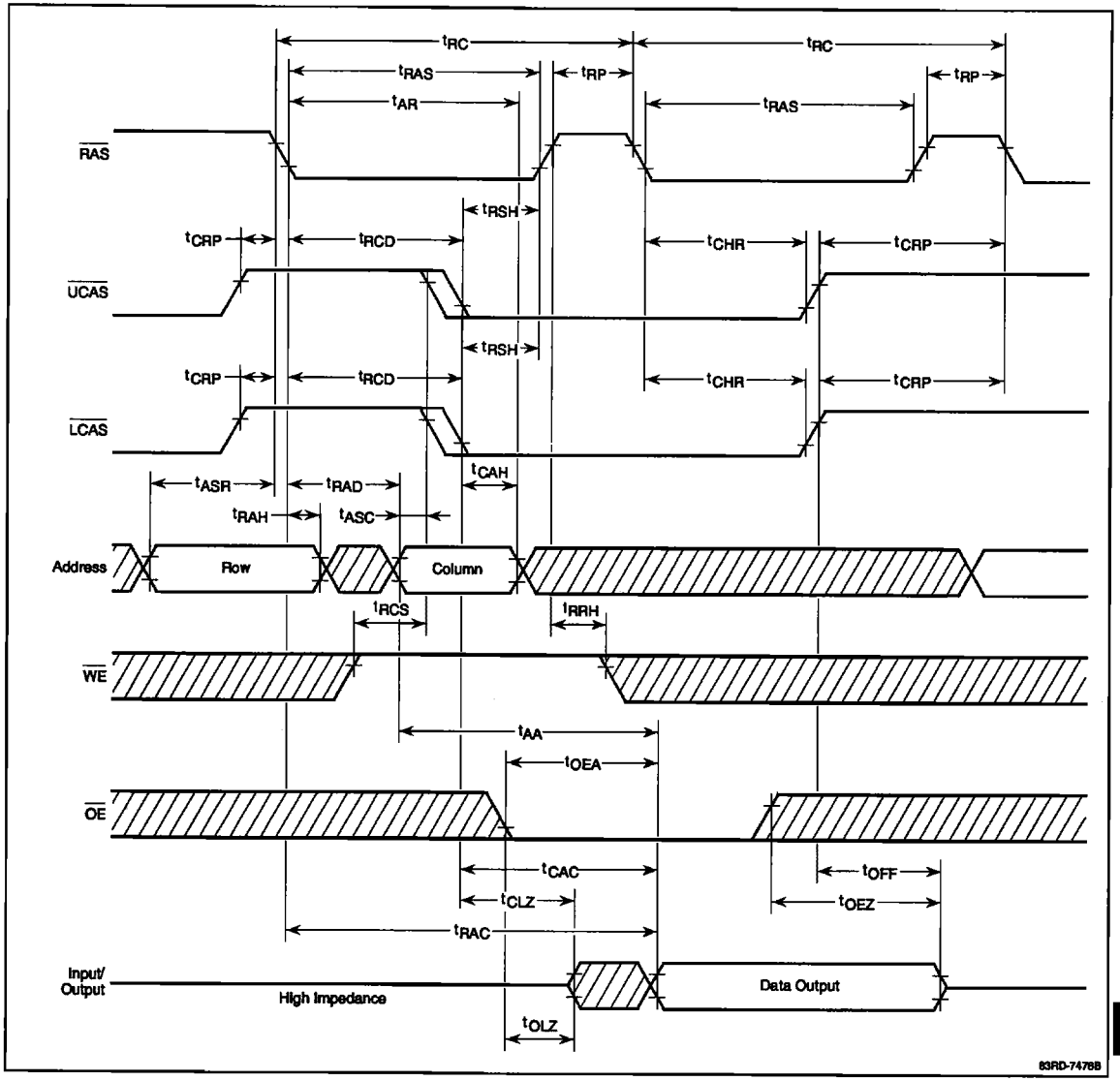
Timing Waveforms (cont)

Byte Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

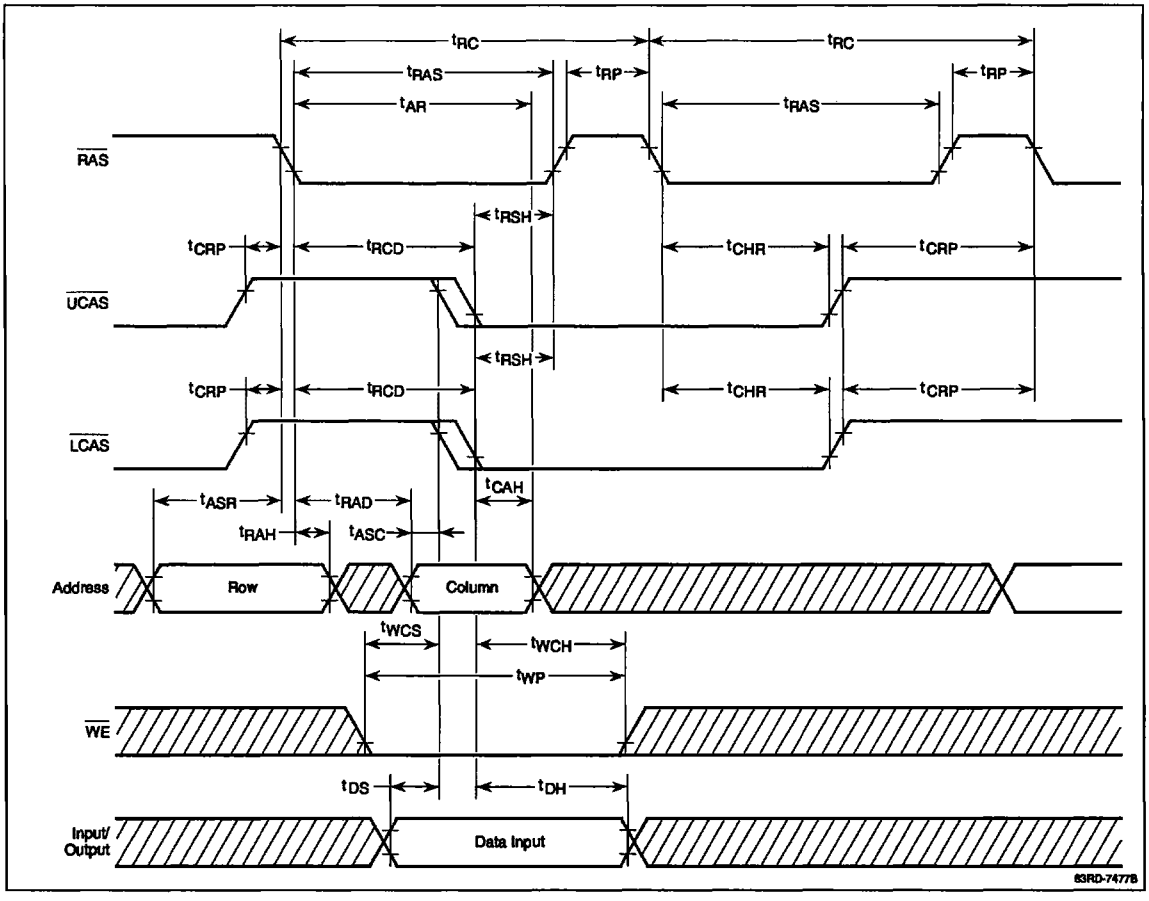
Hidden Refresh Cycle (Word Read Cycle)



7d

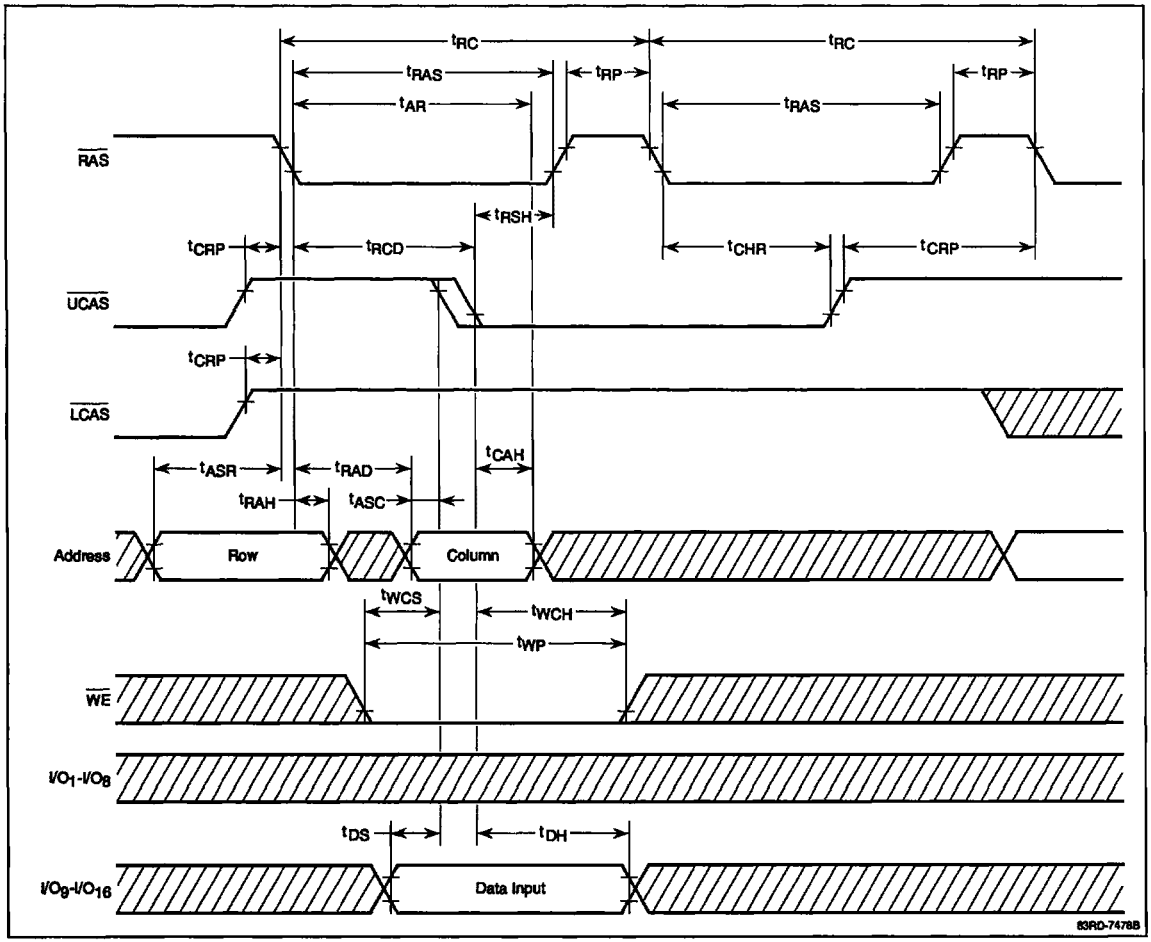
Timing Waveforms (cont)

Hidden Refresh Cycle (Word Write Cycle)



Timing Waveforms (cont)

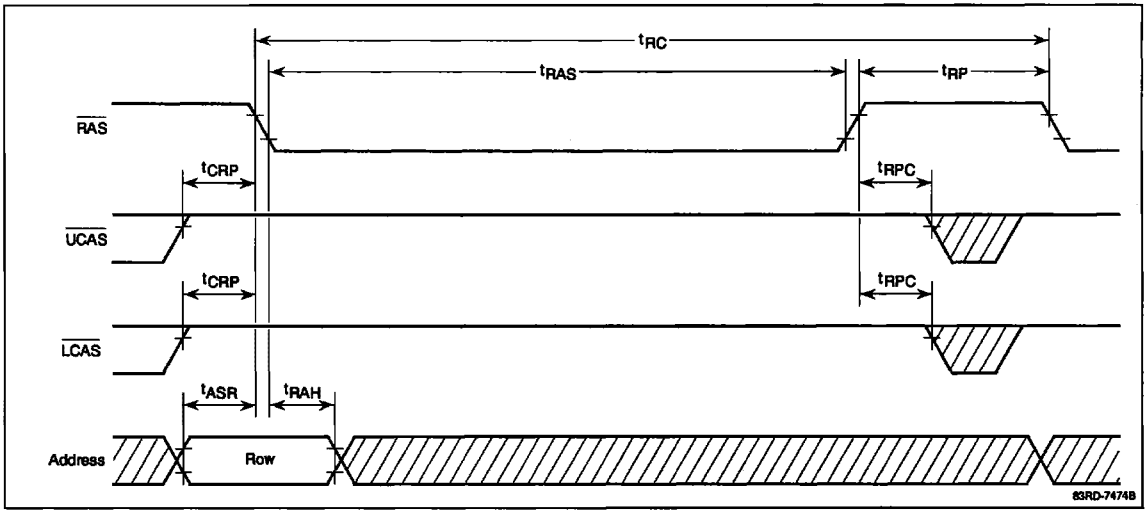
Hidden Refresh Cycle (Byte Write Cycle)



7d

Timing Waveforms (cont)

$\overline{\text{RAS}}$-Only Refresh Cycle



$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle