

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Ultra-High-Speed U-MOSⅢ)

# TK40A10J1

## Switching Regulator Applications

- Small gate charge:  $Q_g = 76\text{nC}$  (typ.)
- Low drain-source ON-resistance:  $R_{DS(ON)} = 11.5\text{ m}\Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 90\text{S}$
- Low leakage current:  $I_{DSS} = 10\text{ }\mu\text{A}$  (max) ( $V_{DS} = 100\text{ V}$ )
- Enhancement mode:  $V_{th} = 1.1\text{ to }2.3\text{ V}$  ( $V_{DS} = 10\text{ V}$ ,  $I_D = 1\text{ mA}$ )

## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	100	V
Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )		$V_{DGR}$	100	V
Gate-source voltage		$V_{GSS}$	$\pm 20$	V
Drain current	DC (Note 1)	$I_D$	40	A
	Pulse (Note 1)	$I_{DP}$	160	
Drain power dissipation ( $T_c = 25^\circ\text{C}$ )		$P_D$	40	W
Single pulse avalanche energy (Note 2)		$E_{AS}$	202	mJ
Avalanche current		$I_{AR}$	40	A
Repetitive avalanche energy (Note 3)		$E_{AR}$	2.4	mJ
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range		$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

## Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	3.125	$^\circ\text{C/W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	62.5	$^\circ\text{C/W}$

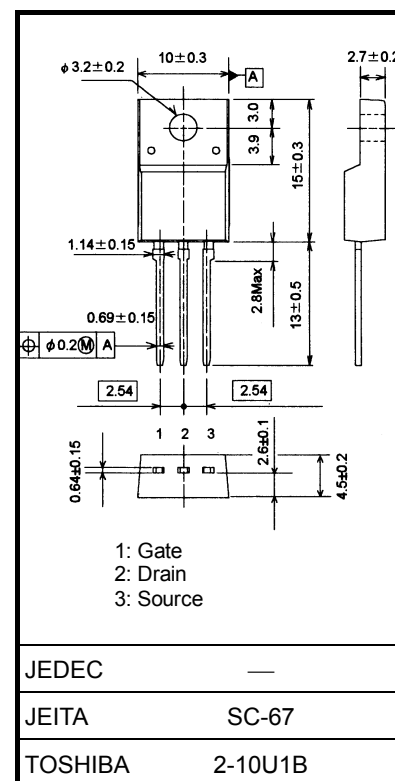
Note 1: Ensure that the channel and lead temperatures do not exceed  $150^\circ\text{C}$ .

Note 2:  $V_{DD} = 25\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$ ,  $L = 200\text{ }\mu\text{H}$ ,  $I_{AR} = 40\text{ A}$ ,  $R_G = 1\text{ }\Omega$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

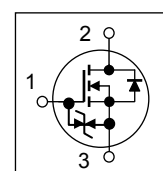
This transistor is an electrostatic- sensitive device. Handle with care.

Unit: mm

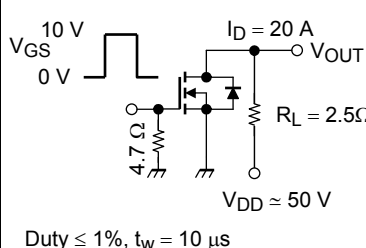


Weight: 1.7 g (typ.)

Internal Connection



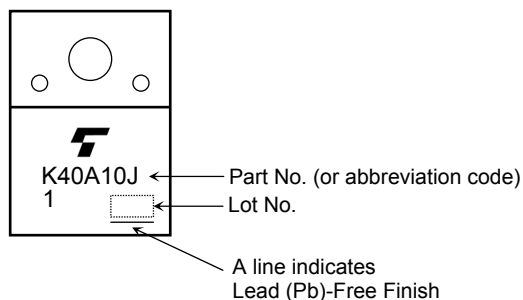
## Electrical Characteristics (Ta = 25°C)

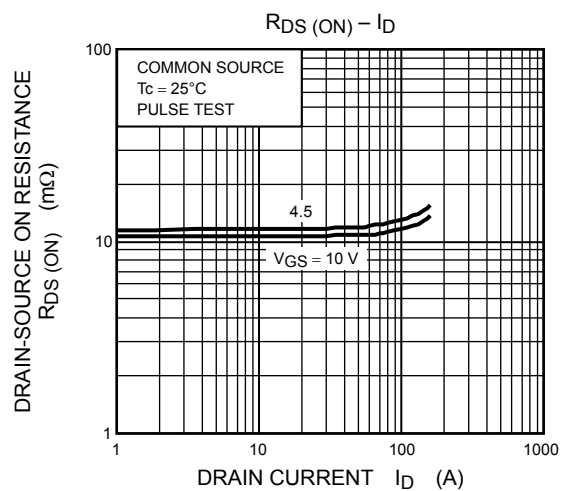
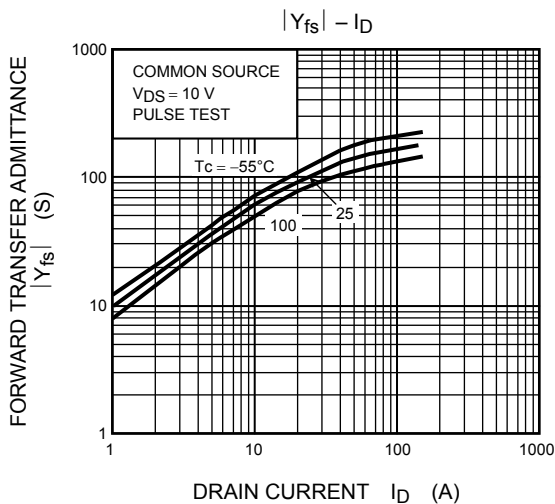
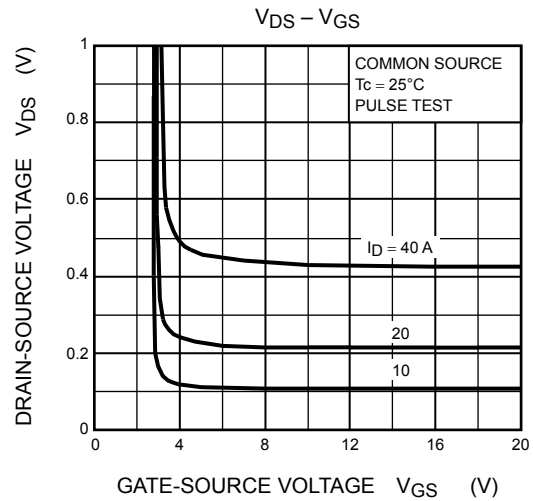
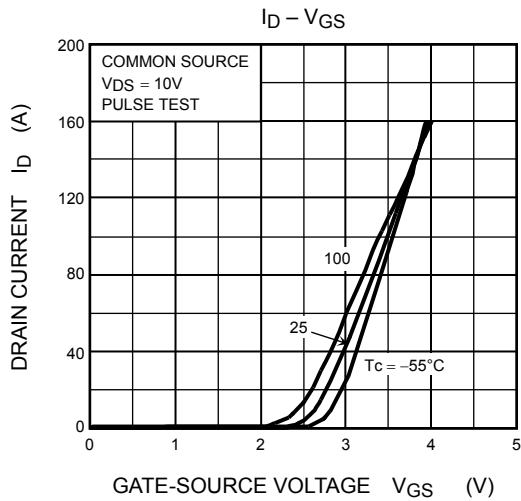
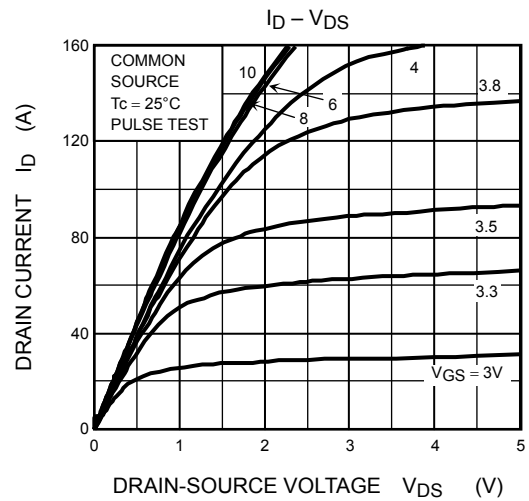
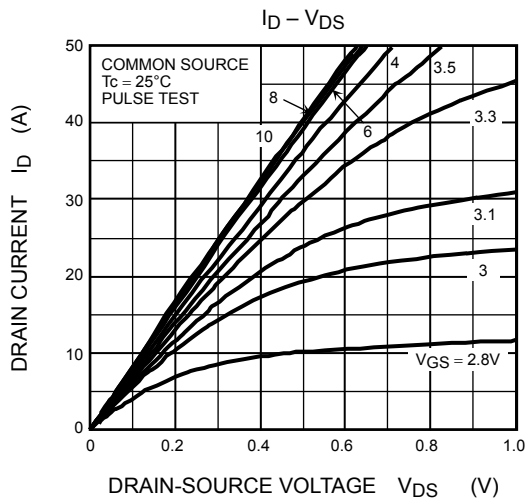
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V	—	—	±10	μA
Drain cut-OFF current		I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	—	—	10	μA
Drain-source breakdown voltage		V (BR) DSS	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	100	—	—	V
		V (BR) DSX	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = -20 V	60	—	—	
Gate threshold voltage		V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.1	—	2.3	V
Drain-source ON resistance		R <sub>DS (ON)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20A	—	13	17	mΩ
			V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20A	—	11.5	15	
Forward transfer admittance		Y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A	45	90	—	S
Input capacitance		C <sub>iss</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	4300	—	pF
Reverse transfer capacitance		C <sub>rss</sub>		—	230	—	
Output capacitance		C <sub>oss</sub>		—	790	—	
Switching time	Rise time	t <sub>r</sub>		—	14	—	ns
	Turn-ON time	t <sub>on</sub>		—	22	—	
	Fall time	t <sub>f</sub>		—	24	—	
	Turn-OFF time	t <sub>off</sub>		—	115	—	
Total gate charge (gate-source plus gate-drain)		Q <sub>g</sub>	V <sub>DD</sub> ≈ 80 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 40A	—	44	—	nC
			V <sub>DD</sub> ≈ 80 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40A	—	76	—	
Gate-source charge 1		Q <sub>gs1</sub>	V <sub>DD</sub> ≈ 80 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40A	—	11	—	
Gate-drain (“miller”) charge		Q <sub>gd</sub>		—	21	—	
Gate switch charge		Q <sub>sw</sub>		—	24	—	

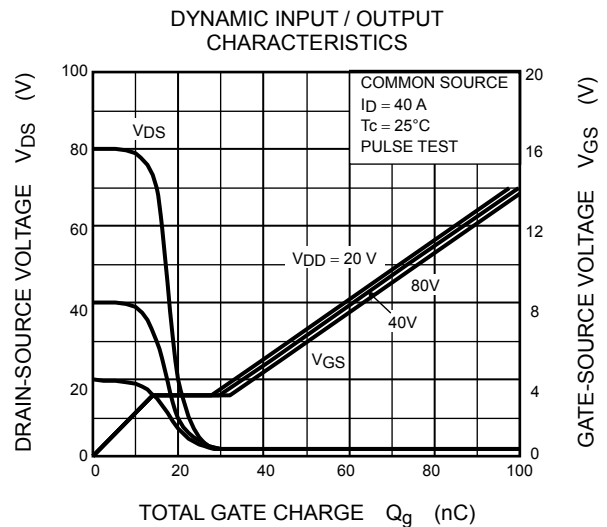
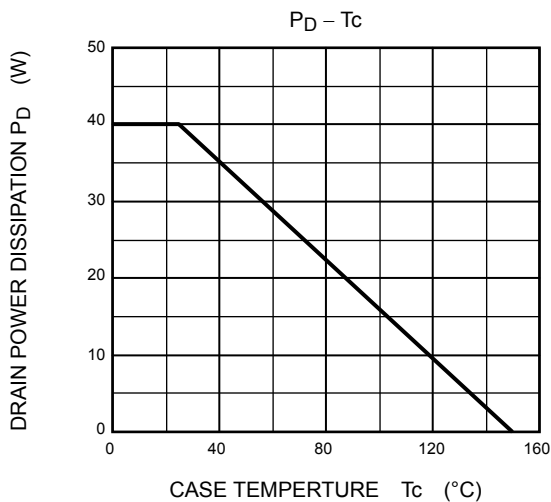
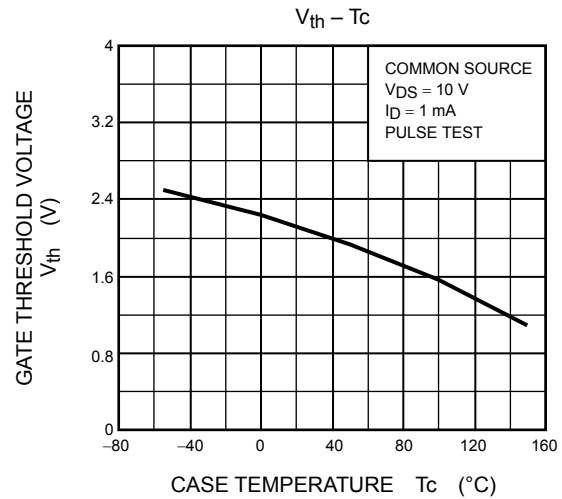
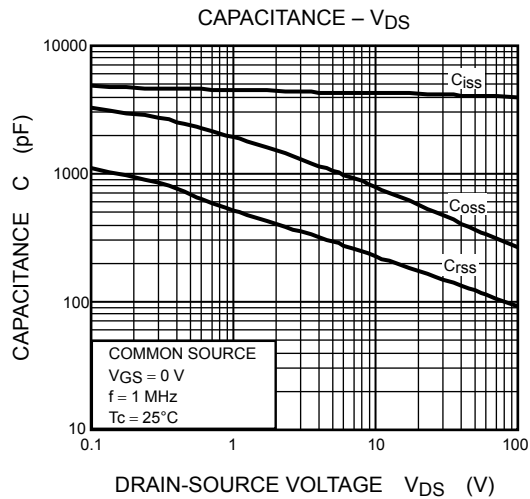
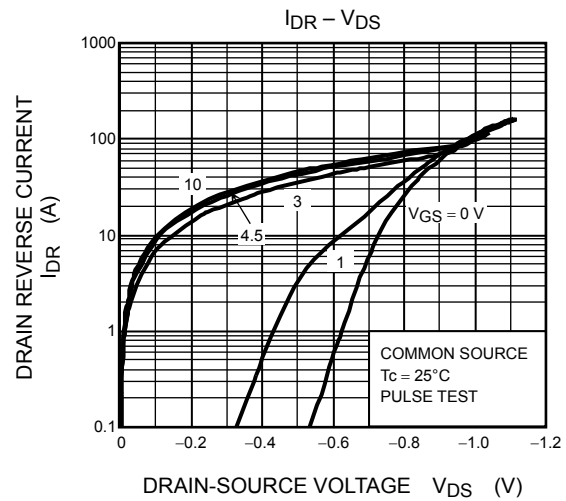
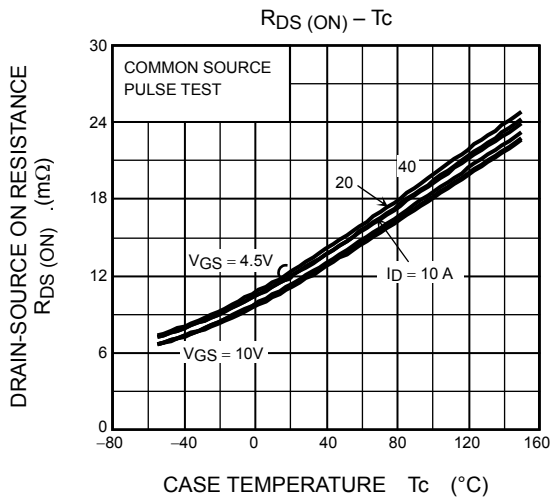
## Source-Drain Ratings and Characteristics (Ta = 25°C)

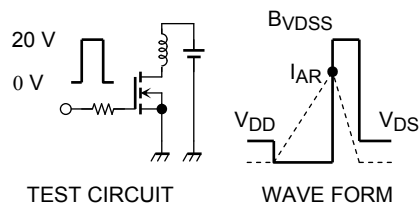
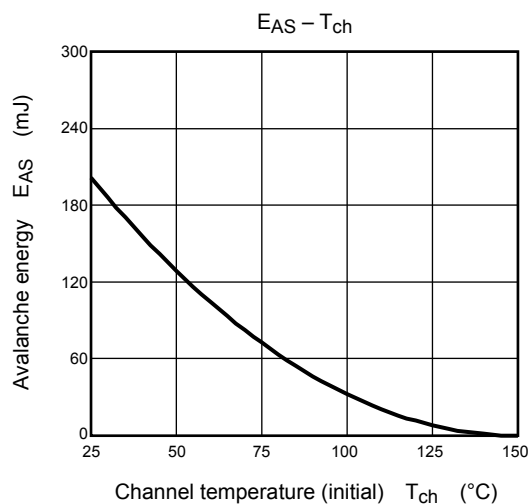
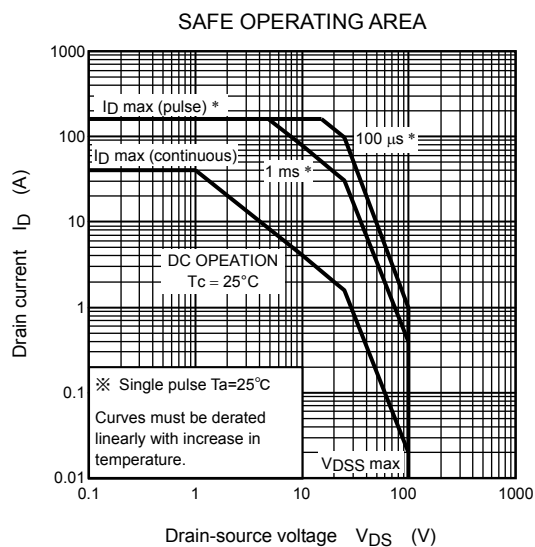
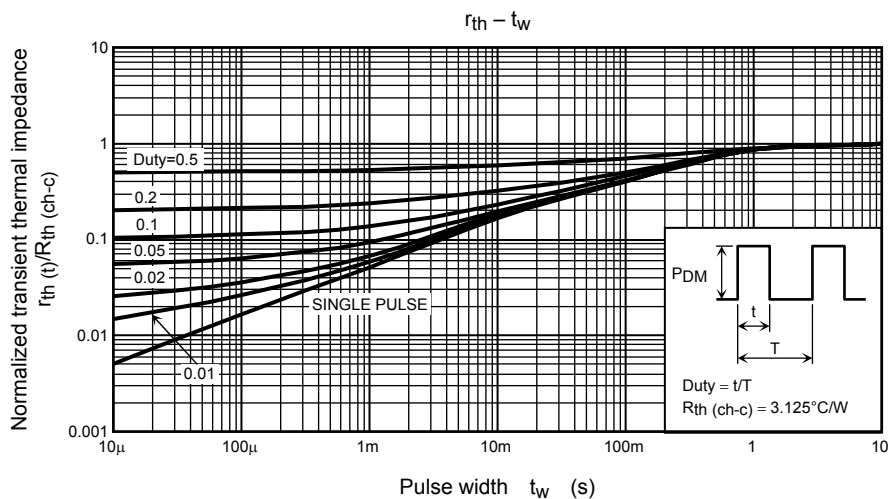
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	$I_{DR}$	—	—	—	40	A
Pulse drain reverse current (Note 1)	$I_{DRP}$	—	—	—	160	A
Forward voltage (diode)	$V_{DSF}$	$I_{DR} = 40 \text{ A}, V_{GS} = 0 \text{ V}$	—	-0.9	-1.2	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 40 \text{ A}, V_{GS} = 0 \text{ V},$	—	55	—	ns
Reverse recovery charge	$Q_{rr}$	$dI_{DR}/dt = 50 \text{ A}/\mu\text{s}$	—	63	—	nC

## Marking









$$R_G = 1 \Omega$$

$$V_{DD} = 25 V, L = 200 \mu H$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{B_{VDS}}{B_{VDS} - V_{DD}} \right)$$

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