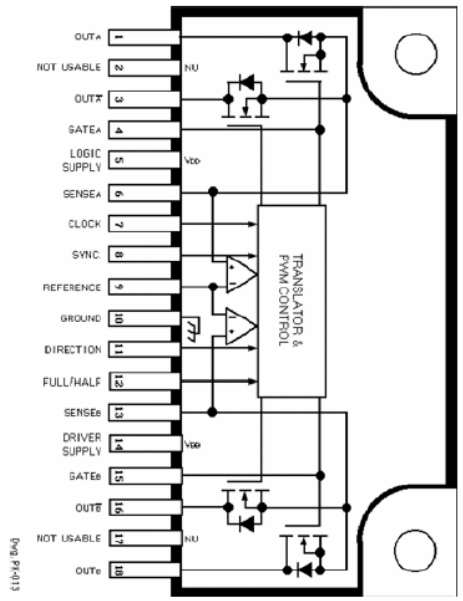
SLA7051M

October 2005

UNIPOLAR STEPPER-MOTOR TRANSLATOR/PWM DRIVER



ABSOLUTE MAXIMUM RATINGS

Driver Supply Voltage, V_{BB} ..... **46 V**
Load Supply Voltage, V_M ..... **46 V**
Output Current, I_O ..... **2.0 A***
Logic Supply Voltage, V_{DD} ..... **7.0 V**
Logic Input Voltage Range, V_I ..... **-0.3 V to V_{DD}+ 0.3 V**
Sense Voltage, V_S ..... **±2.0 V†**
Reference Input Voltage Range, V_{REF} ..... **-0.3 V to V_{DD}+ 0.3 V**
Package Power Dissipation, P_D ..... **See Graph**
Junction Temperature, T_J ..... **+150°C**
Operating Temperature Range, T_A ..... **-20°C to +85°C**
Storage Temperature Range, T_S ..... **-30°C to +150°C**

* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or junction temperature.
† Internal filtering provides protection against transients during the first 1 µs of the current-sense pulse.

Combining low-power CMOS logic with high-current, high-voltage power FET outputs, the SLA7051M translator/driver provides complete control and drive for a two-phase unipolar stepper motor with internal fixed off time, pulse-width modulation (PWM) control of the output current in a power multi-chip module (PMCM™).

The CMOS logic section provides the sequencing logic, direction, full/half-step control, synchronous/asynchronous PWM operation, and a "sleep" function. The minimum CLOCK input is an ideal fit for applications where a complex µP is unavailable or overburdened. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure a proper input-logic high. For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. The NMOS outputs are capable of sinking up to 2 A and withstanding 46 V in the off state. Ground-clamp and flyback diodes provide protection against inductive transients. Special power-up sequencing is not required.

Full-step (2 phase) and half-step operation are externally selectable. Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This sequence mode offers an improved torque-speed product, greater detent torque, and is less susceptable to motor resonance. Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD D-DA), providing an eight-step sequence.

The SLA7051M is supplied in an 18-pin single in-line power-tab package with leads formed for vertical mounting (suffix LF871) or horizontal mounting (suffix LF872). The tab is at ground potential and needs no insulation. For high-current or high-frequency applications, external heat sinking may be required. This device is rated for continuous operation between -20°C and +85°C.

FEATURES

- 2 A Output Rating
- Internal Sequencer for Full or Half-Step Operation
- PWM Constant-Current Motor Drive
- Cost-Effective, Multi-Chip Solution
- 100 V, Avalanche-Rated NMOS
- Low $r_{DS(on)}$ NMOS Outputs (300 mΩ typical)
- Advanced, Improved Body Diodes
- Half-Step and Full-Step Unipolar Drive
- Inputs Compatible with 3.3 V or 5 V Control Signals
- Sleep Mode
- Internal Clamp Diodes

Always order by complete part number, e.g., **SLA7051MLF871**.

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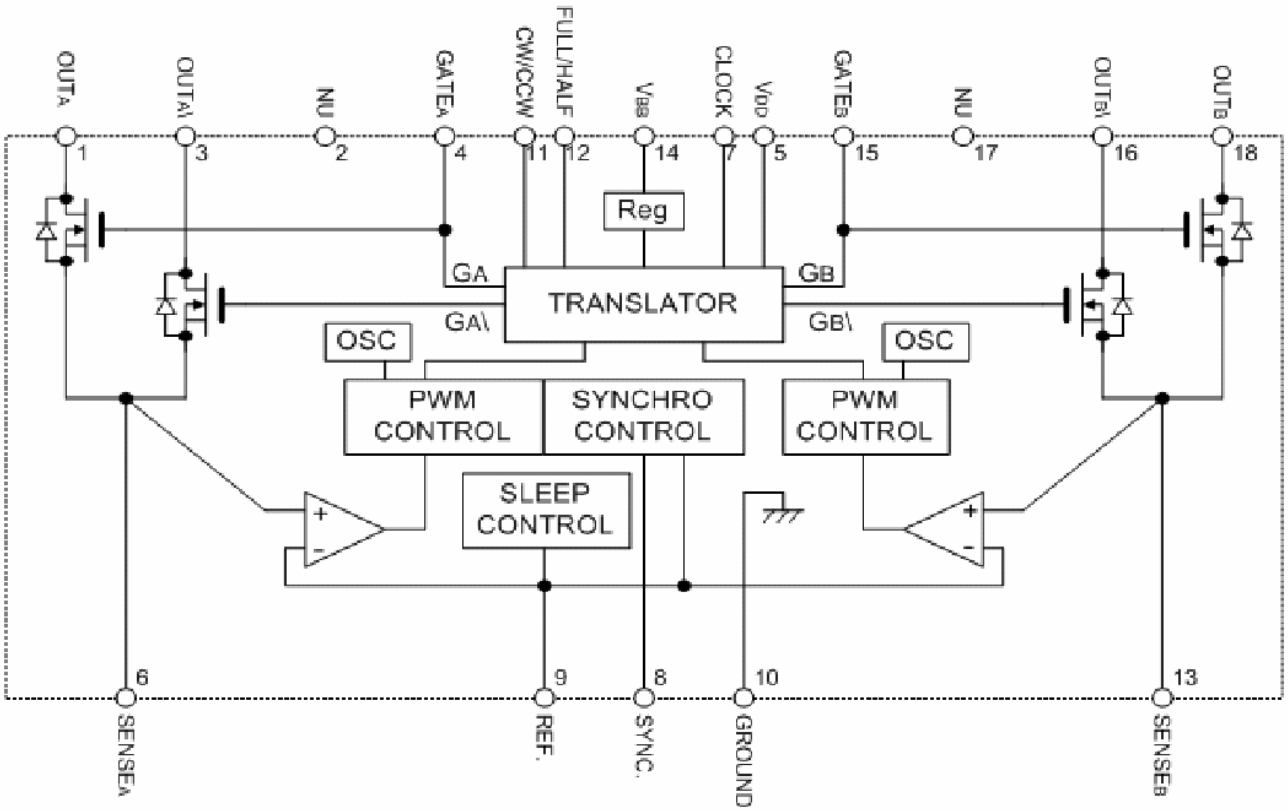
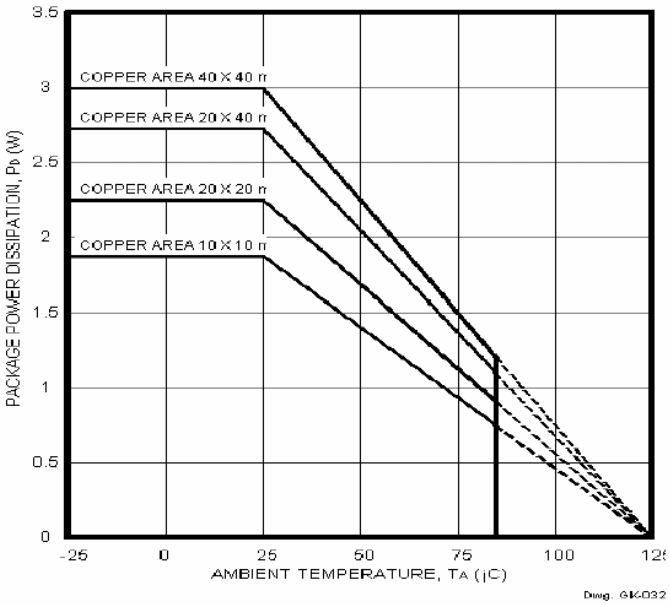
Functional block diagram





Recommended operating conditions

Load Supply Voltage, V_{BB} ..... **10 to 44 V**
Logic Supply Voltage, V_{DD} ..... **3.0 V to 5.5 V**
Reference Input Voltage, V_{REF} ..... **0.1 V to 1.0 V**
Tab Temperature (no heat sink), T_T ..... **<100°C**

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Electrical characteristics: unless otherwise noted at T_A = +25°C, V_{BB} = 24 V, V_{DD} = 5.0 V.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output drivers						
Driver Supply Volt. Range	V_{BB}	Operating	10	—	44	V
Drain-Source Breakdown	$V_{(BR)DS}$	V_{BB} = 44 V, I_D = 1 mA	100	—	—	V
Output On Resistance	$r_{DS(on)}$	I_O = 1.0 A	—	300	500	mΩ
Body Diode Forward Volt.	V_F	I_F = 1.0 A	—	0.8	1.1	V
Driver Supply Current	I_{BB}		—	—	15	mA
		V_{REF} > 2.0 V (sleep mode)	—	—	100	µA
Control logic						
Logic Supply Volt. Range	V_{DD}	Operating	3.0	5.0	5.5	V
Logic Input Voltage	V_{IH}		$0.75V_{DD}$	—	—	V
	V_{IL}		—	—	$0.25V_{DD}$	V
Logic Input Current	I_{IH}		—	±1.0	—	µA
	I_{IL}		—	±1.0	—	µA
Max. Clock Frequency	f_{clk}		100*	—	—	kHz
PWM Off Time	t_{off}		—	12	—	µs
PWM Min. On Time	$t_{on(min)}$		—	5.0	—	µs
Ref. Input Voltage Range	V_{REF}	Operating	0.0	—	1.5	V
		Sleep mode	2.0	—	—	V
Ref. Input Current	I_{REF}		—	±10	—	µA
Sense Voltage	V_S	Trip point	—	V_{REF}	—	V
Propagation Delay Time	t_{PLH}	Clock rising edge to output on	—	2.5	—	µs
	t_{PHL}	Clock rising edge to output off	—	2.0	—	µs
Logic Supply Current	I_{DD}		—	—	3.0	mA

Typical values are given for circuit design information only.
*Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

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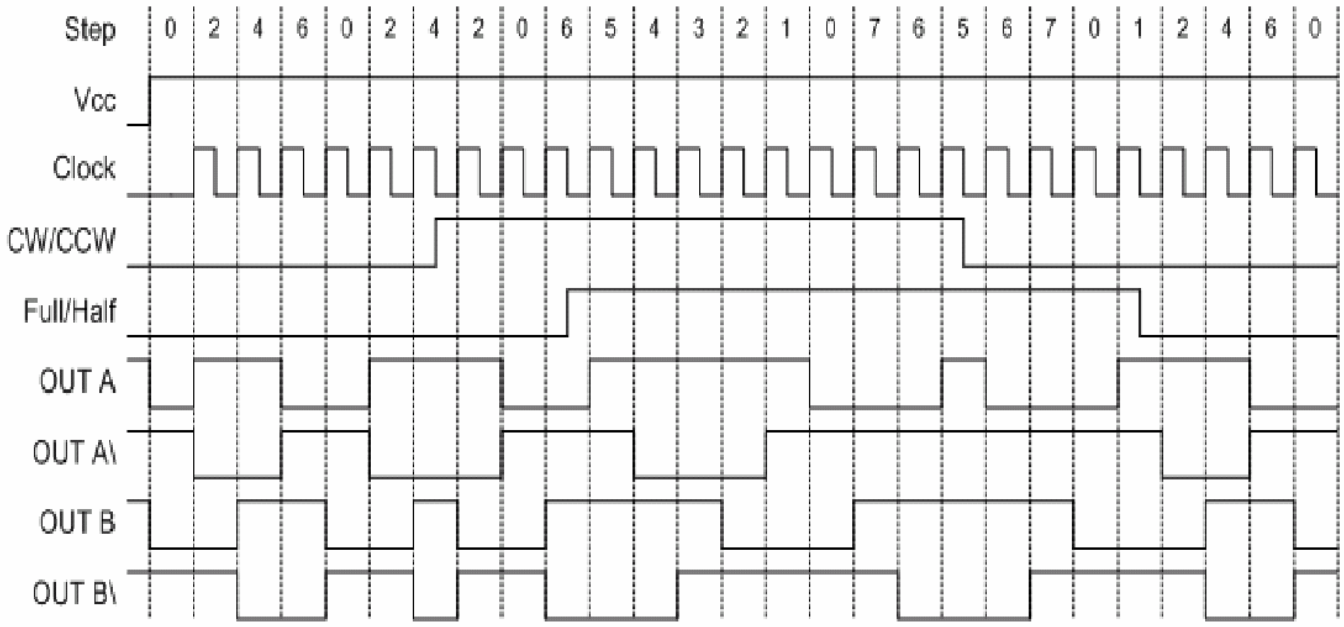
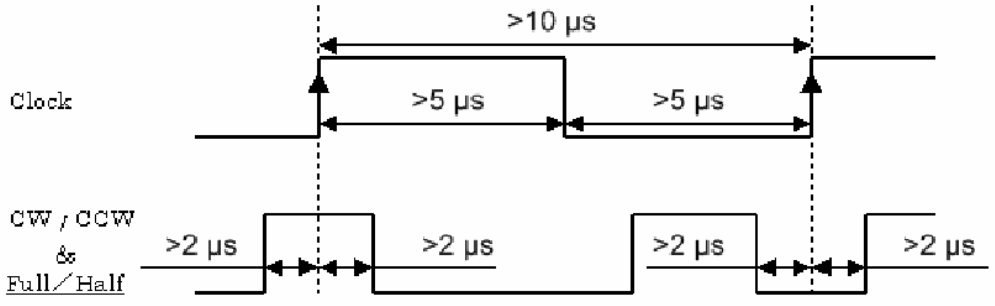


Timing chart



Logic input timing

Functional description

Device operation. The SLA7051M is a complete stepper-motor driver with built-in translator for easy operation with minimal control lines. It is designed to operate unipolar stepper motors in full-step or half-step modes. The current in each pair of outputs, all n-channel MOSFETs, is regulated with internal fixed off-time pulse-width modulated (PWM) control circuitry.

When a step command signal occurs on the clock input the translator automatically sequences to the next step.

Clock (step) input. A low-to-high transition on the clock input sequences the translator and advances the motor one increment. The hold state is done by stopping the CLOCK input regardless of the input level

Full/half-step select. This logic-level input sets the translator step mode. A logic low is two-phase, full step; a logic high is half step. Changes to this input do not take effect until the rising edge of the clock input.

CW/CCW (direction) input. This logic-level input sets the translator step direction. Changes to this input do not take effect until the rising edge of the clock input.

Internal PWM current control. Each pair of outputs is controlled by a fixed off-time PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, an output is enabled and current flows through the motor winding and R_S. When the voltage across the current-sense resistor equals the reference voltage, the current-sense comparator resets the PWM latch, which turns off the driver for the fixed off time during which the load inductance causes the current to recirculate for the off time period. The driver is then re-enabled and the cycle repeats.

Synchronous operation mode. This function prevents occasional motor noise during a "hold" state, which normally results from asynchronous PWM operation of both motor phases. A logic high at the SYNC input is synchronous operation; a logic low is asynchronous operation. The use of synchronous operation during normal stepping is not recommended because it produces less motor torque and can cause motor vibration due to stair-case current.

Sleep mode. Applying a voltage greater than 2 V to the REF pin disables the outputs and puts the motor in a free state (coast). This function is used to minimize power consumption when not in use. It disables much of the internal circuitry including the output MOSFETs and regulator. When coming out of sleep mode, wait 100 µs before issuing a step command to allow the internal circuitry to stabilize.

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Applications information

Layout.

The printed wirting board should use a heavy ground plane.

For optimum electrical and thermal performance, the driver should be soldered directly into the board.

The driver supply terminal, VBB, should be decoupled with an electrolytic capacitor placed as close to the device as possible.

To avoid problems due to capacitive coupling of the high dv/dt switching transients, route the high-level, output traces away from the sensitive, low-level logic traces. Always drive the logic inputs with a low source impedance to increase noise immunity.

Grounding. A star ground system located close to the driver is recommended. The logic supply return and the driver supply return should be connected together at only a single point — the star ground.

Logic supply voltage, V_{DD}. Transients at this terminal should be held to less than 0.5 V to avoid malfunctioning operation. Both V_{BB} and V_{DD} may be turned on or off separately.

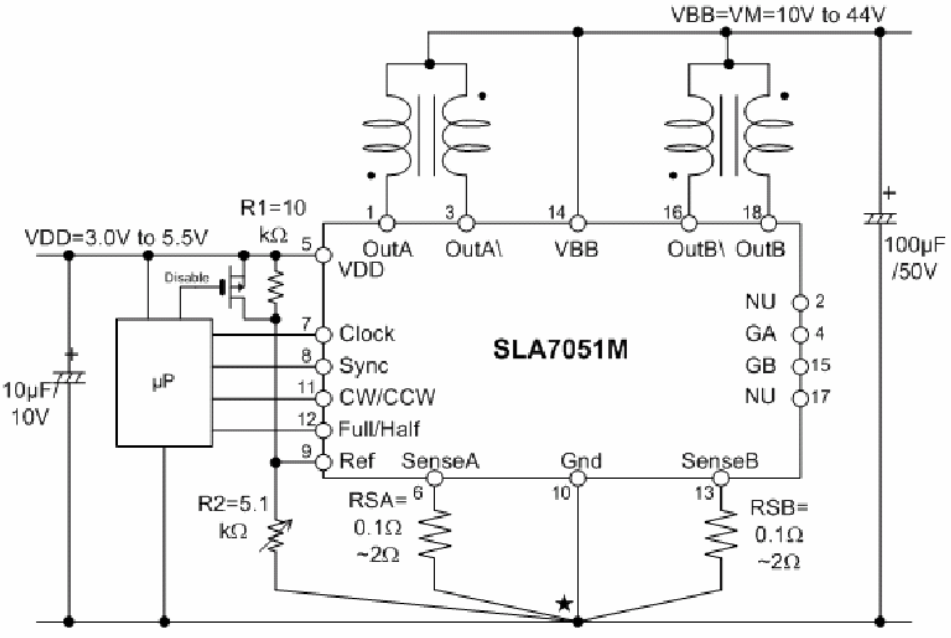
Logic inputs. Unused logic inputs (CW/CCW, FULL/HALF, or SYNC) must be connected to either ground or the logic supply voltage.

Current sensing. To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistor, R_S, should have an independent ground return to the star ground of the device. This path should be as short as possible. For low-value sense resistors, the IR drops in the printed wiring board sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

PWM current control. The maximum value of current limiting (I_{TRIP}) is set by the selection of R_S and the voltage at the REF input with a transconductance function approximated by:

$$I_{TRIP} = V_{REF}/R_S$$

The required V_{REF} should not be less than 0.1 V. If it is, R_S should be increased for a proportionate increase in V_{REF}.



Typical application

Applications Information (cont'd)

Reference voltage. In the Typical Application shown, resistors R_1 and R_2 set the reference voltage as:

$$V_{REF} = (V_{DD} \times R_2)/(R_1 + R_2)$$

The trimming of R_2 allows for the resistor tolerances and REF input current. The sum of R_1+R_2 should be less than 50 kΩ to minimize the effect of I_{REF}.

Minimum output current. The SLA7051M uses fixed off-time PWM current control. Due to internal logic and switching delays, the actual load current peak will be slightly higher than the calculated I_{TRIP} value (especially for low-inductance loads). These delays, plus the minimum recommended V_{REF}, limit the minimum value the current-control circuitry can regulate. An application with this device should maintain continuous PWM control in order to obtain optimum torque out of the motor. The boundary of the load current ($I_{O(min)}$) between continuous and discontinuous operation is:

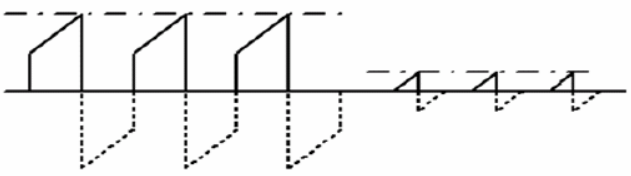
$$I_{O(min)} = [(V_M + V_{SD})/R_m] \times [(1/e^{t_{off}/[R_m \times L_m]}) - 1]$$

where V_M = load supply voltage
V_F = body diode forward voltage
R_m = motor winding resistance
t_{off} = PWM off time
L_m = motor winding inductance

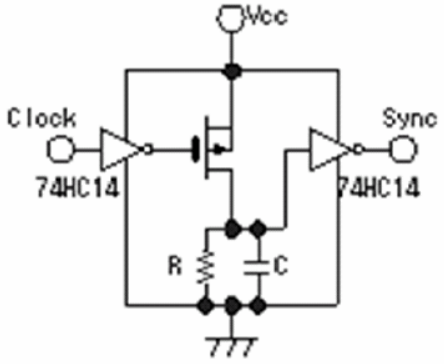
To produce zero current in a motor, the REF input should be pulled above 2 V, turning off all drivers.

Synchronous operation mode. If an external signal is not available to control the synchronous operation mode, a simple circuit can keep the SYNC input low while the CLOCK input is active; the SYNC input will go high (synchronous operation) when the CLOCK input stays low ("hold"). The RC time constant determines the sync trransition timing.

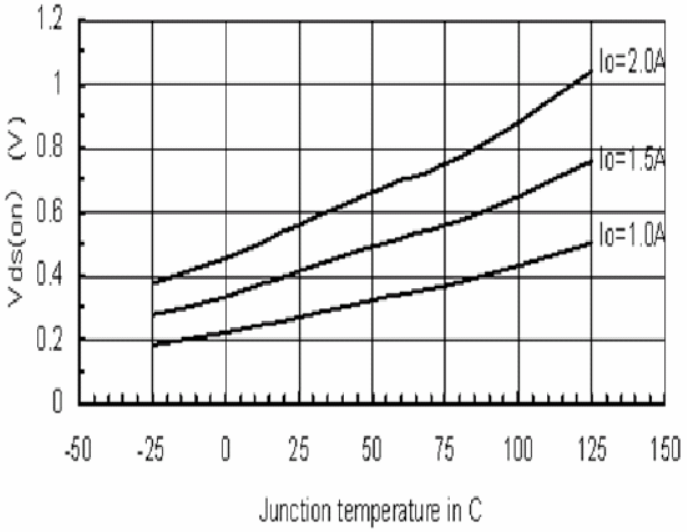
Temperature effects on FET outputs. Analyzing safe, reliable operation includes a concern for the relationship of NMOS on resistance to junction temperature. Device package power calculations must include the increase in on resistance (producing higher on voltages) caused by increased operating junction temperatures. The figure provides a normalized on-resistance curve, and all thermal calculations should consider increases from the



Continuous mode — Discontinuous mode



Sync. signal generator



Normalized FET on resistance

Applications Information (cont'd)

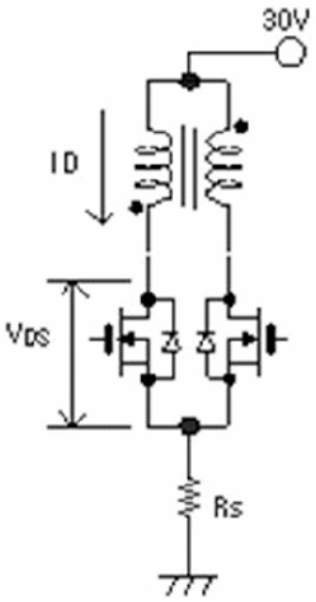
given +25°C limits, which may be caused by internal heating during normal operation.

These power MOSFET outputs feature an excellent combination of fast switching, ruggedized device design, low on resistance, and cost effectiveness.

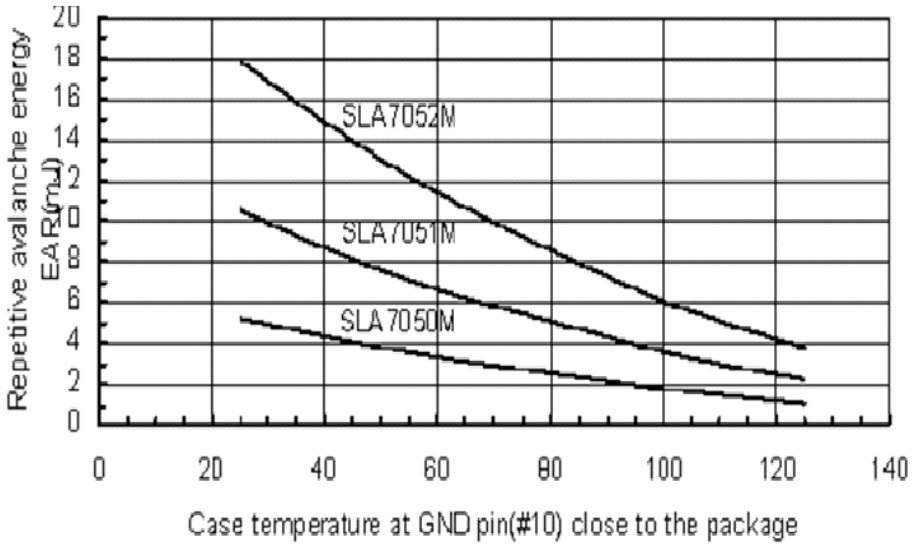
Avalanche energy capability. There is a surge voltage expected when the output MOSFET turns off, and this voltage may exceed the MOSFET breakdown voltage ($V_{(BR)DS}$). However, the MOSFETs are avalanche type and as long as the energy ($E_{(AV)}$), which is imposed on the MOSFET by the surge voltage, is less than the maximum allowable value, it is considered to be within its safe operating area. Note that the maximum allowable avalanche energy is reduced as a function of temperature.

In application, the avalanche energy ($E_{(AV)}$) dissipated by the MOSFET is approximated as

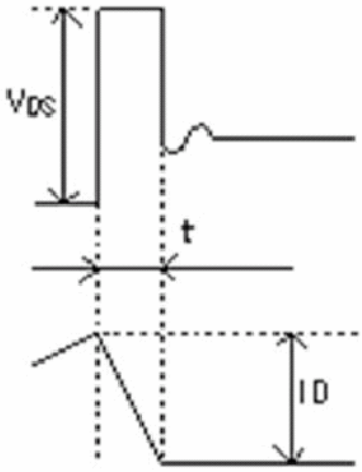
$$E_{(AV)} = V_{DS(AV)} \times 1/2 \times I_D \times t$$



Output circuit for avalanche energy calculations



Allowable avalanche energy



Waveforms during avalanche breakdown

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Terminal list

Pin	Terminal Name	Terminal Description
1	OUTA	Driver output for phase A
2	NU	Not usable
3	OUTA\	Driver output for phase A\
4	GATEA	Phase A MOSFET gate
5	VDD	Logic power supply
6	SENSEA	Phase A current sense
7	CLOCK	Step clock input
8	SYNC	Synchronous PWM control input
9	REF	Current set & “sleep” control
10	GND	Supply negative return
11	CW/CCW	Forward/reverse logic control input
12	FULL/HALF	Full step/half step logic control input
13	SENSEB	Phase B current sense
14	VBB	Driver power supply
15	GATEB	Phase B MOSFET gate
16	OUTB\	Driver output for phase B\
17	NU	Not usable
18	OUTB	Driver output for phase B

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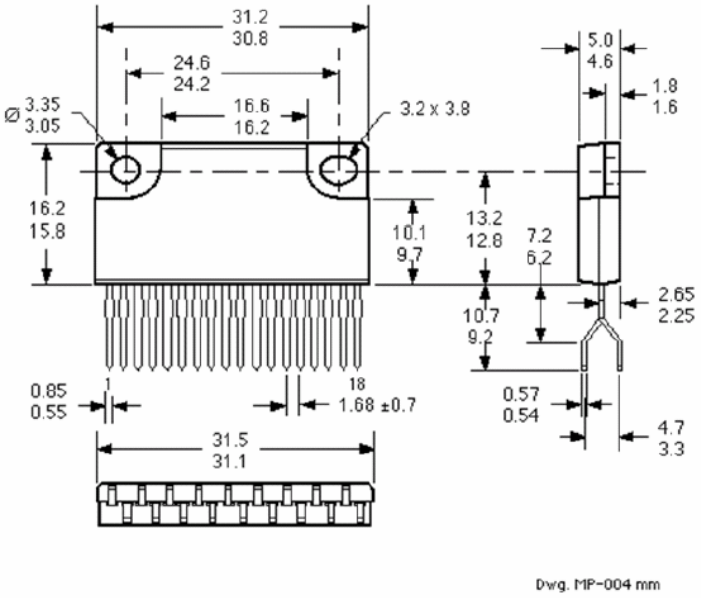
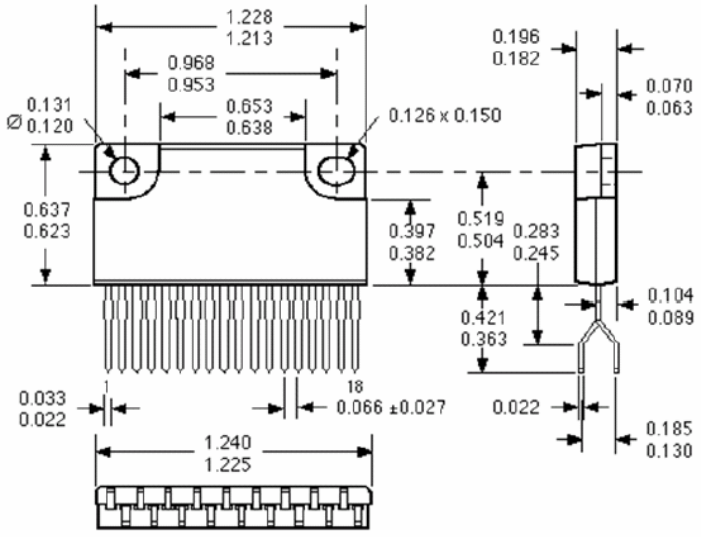


Dwg. MP-004 mm

Dimensions in millimeters
(controlling dimensions)



Dwg. MP-004 in

Dimensions in inches
(for reference only)

NOTES:
1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. The shaded area is exposed heat spreader.
3. Recommended mounting hardware torque: 0.490 - 0.822 Nm.
4. Recommended use of metal-oxide-filled, alkyl-degenerated oil-base silicone grease: Dow Corning SC102, Toshiba YG6260, Shin-Etsu G746, or equivalent.

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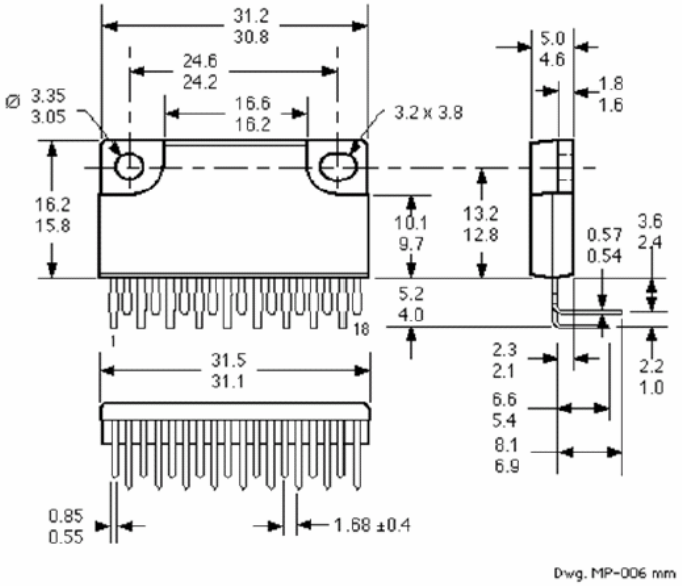
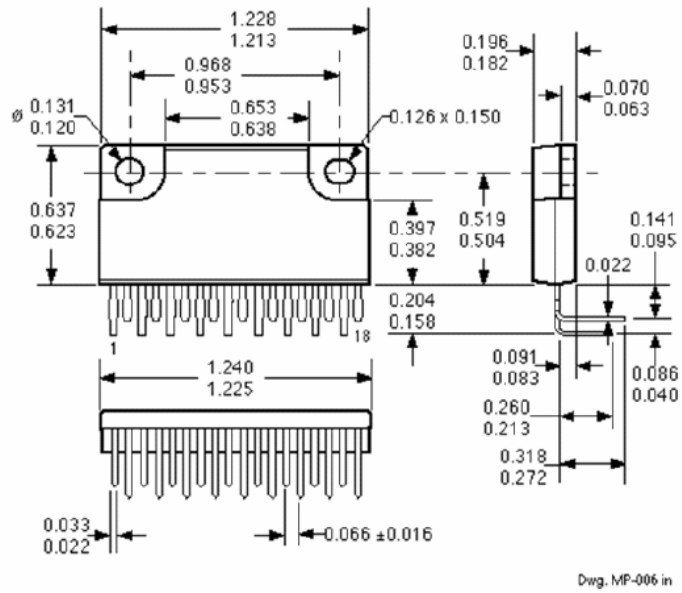
SLA7051MLF872



Dimensions in millimeters
(controlling dimensions)



Dimensions in inches
(for reference only)

NOTES:
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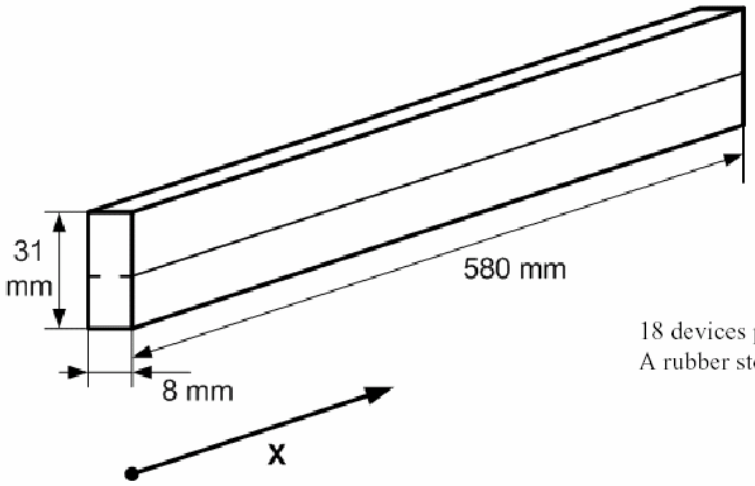
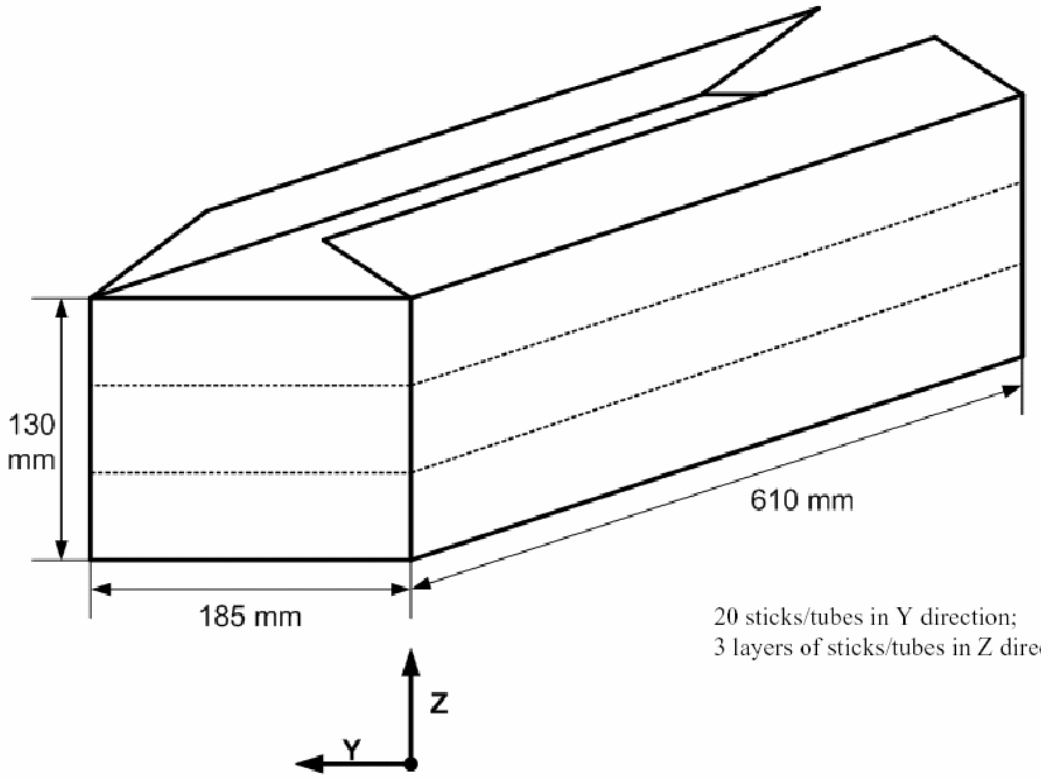
Packing information



18 devices per stick/tube.
A rubber stopper is provided at each end of the stick/tube.



20 sticks/tubes in Y direction;
3 layers of sticks/tubes in Z direction = 1080 devices per box.

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