

### 64K x 18 Fast CMOS Synchronous Static RAM with Interleaved Burst Counter and Output Register

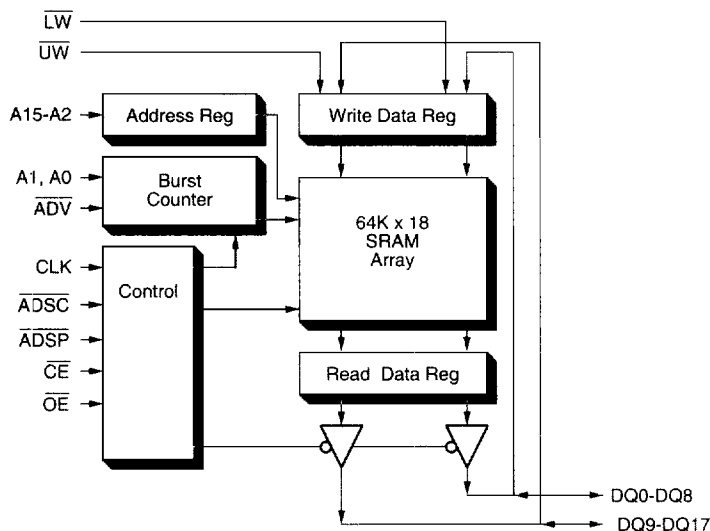
#### Features

- Interfaces directly with the x86 and Pentium™ microprocessors (100, 80, 66, 60, 50 MHz)
- High-speed access times
  - Clock to data valid times: 4.5, 5, 6, 7, 8 ns
  - Cycle times: 8, 10, 13, 15 ns
- High-density 64K x 18 architecture
- Output register for pipelined designs
- Choice of 5V or 3V ( $\pm 10\%$ ) output Vcc for output level compatibility
- High-output drive: 30 pF at rated T<sub>A</sub>
- Asynchronous output enable
- Self-timed write cycle
- Byte writable via dual write strobes
- Internal interleaved burst read/write address counter
- Internal registers for address, data, controls
- Packages: 52-pin PLCC - J

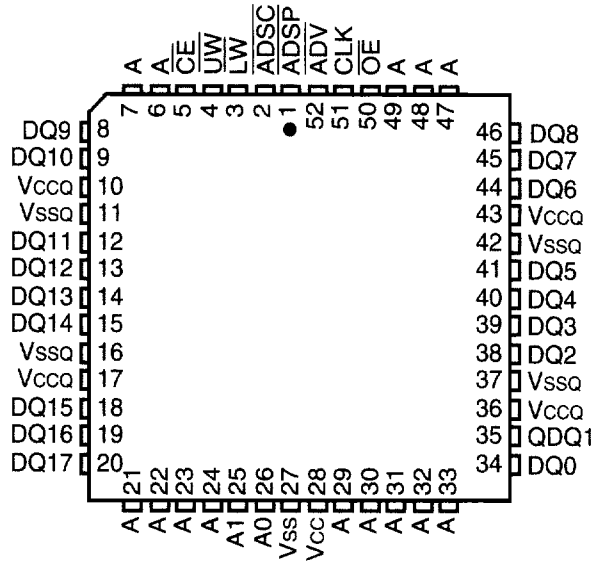
#### Description

The PDM44058 is a 1,179,648 bit synchronous random access memory organized as 65,536 x 18 bits. It has burst mode capability, an output register and interface controls designed to provide high-performance in second level cache designs for x86 and Pentium microprocessors. Addresses, write data and all control signals except output enable are controlled through positive edge-triggered registers. Write cycles are self-timed and are also initiated by the rising edge of the clock. Controls are provided to allow burst reads and writes of up to four words in length. A 2-bit burst address counter controls the two least-significant bits of the address during burst reads and writes. The burst address counter uses the 2-bit counting scheme required by the x86 and Pentium microprocessors. Individual write strobes provide byte write for the upper and lower 9-bit bytes of data. An asynchronous output enable simplifies interface to high-speed buses. Separate output Vcc pins provide user-controlled 5V or 3.3V TTL-compatible output levels.

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Pin Assignment



Pinout

Name	I/O	Description	Name	I/O	Description
A	I	Address Inputs A15-A2	LW	I	Low Byte Write Enable, DQ0-DQ8
A1, A0	I	Address Inputs A1 & A0	UW	I	Upper Byte Write Enable, DQ8-DQ17
DQ0-DQ17	I/O	Read/Write Data	OE	I	Output Enable
CLK	I	Clock	V <sub>CC</sub>	—	Array Power (+5V)
ADV	I	Burst Counter Advance	V <sub>CCQ</sub>	—	Output Power for DQ's (+3.3V or +5V)
ADSC	I	Controller Address Status	V <sub>SS</sub>	—	Array Ground
ADSP	I	Processor Address Status	V <sub>SSQ</sub>	—	Output Ground for DQ's
CE	I	Chip Enable			

Asynchronous Truth Table

Operation	OE	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z: Write Data In
Deselected	X	High-Z

Burst Sequence Table

Sequence	A15-A2	A1	A0
Start Address	XXXX	A1	A0
1st Burst Address	XXXX	A1	A0
2nd Burst Address	XXXX	A1	A0
3rd Burst Address	XXXX	A1	A0

NOTE: 1. L = Low, H = High, X = Don't Care.  
 2. For a write operation following a read operation, OE must be high before the input data required setup time and held high through the input data hold time.

**Synchronous Truth Table** (See Notes 1 through 4)

$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	CLK	Address	Operation
H	X	L	X	X	↑	N/A	Deselected
L	L	X	X	X	↑	External	Read Cycle, Begin Burst
L	H	L	X	L	↑	External	Write Cycle, Begin Burst
L	H	L	X	H	↑	External	Read Cycle, Begin Burst
X	H	H	L	L	↑	Next	Write Cycle, Continue Burst
X	H	H	L	H	↑	Next	Read Cycle, Continue Burst
X	H	H	H	L	↑	Current	Write Cycle, Suspend Burst
X	H	H	H	H	↑	Current	Read Cycle, Suspend Burst
H	X	H	L	L	↑	Next	Write Cycle, Continue Burst
H	X	H	L	H	↑	Next	Read Cycle, Continue Burst
H	X	H	H	L	↑	Current	Write Cycle, Suspend Burst
H	X	H	H	H	↑	Current	Read Cycle, Suspend Burst

- NOTE:
1. L = Low, H = High, X = Don't Care, ↑ = Low-to-High transition.
  2. All inputs except  $\overline{CE}$  must meet setup and hold times relative low-to-high transition of clock, CLK.
  3. Wait states are inserted by suspending burst.
  4.  $\overline{ADSP}$  is gated by  $\overline{CE}$ . Both  $\overline{ADSP}$  and  $\overline{CE}$  must be valid for  $\overline{ADSP}$  to load the address-register and force a read.

### Burst Mode Operation

This is a synchronous part. All activities are initiated by the positive, low-to-high edge of the clock (CLK). This part can perform burst reads and writes with burst lengths of up to four words. The four word burst is created by using a burst counter to drive the two least-significant bits of the internal RAM address. The burst counter is loaded at the start of the burst and is incremented for each word of the burst. The burst counter uses a modified binary sequence compatible with the cache line burst reload sequence of x86 microprocessors. This sequence is given in the Burst Sequence Table.

Burst transfers are initiated by the  $\overline{ADSC}$  or  $\overline{ADSP}$  signals. When the  $\overline{ADSP}$  and  $\overline{CE}$  signals are sampled low, a read cycle is started (independent of  $\overline{UW}$ ,  $\overline{LW}$  and  $\overline{ADSC}$ ), and prior burst activity is terminated.  $\overline{ADSP}$  is gated by  $\overline{CE}$ , so both must be active for  $\overline{ADSP}$  to load the address register and to initiate a read cycle. The address and the chip enable input ( $\overline{CE}$ ) are sampled by the same edge that samples  $\overline{ADSP}$ . Read data is valid at the output after the specified delay from the clock edge.

When  $\overline{ADSC}$  is sampled low and  $\overline{ADSP}$  is sampled high, a read or write cycle is started depending on the state of  $\overline{UW}$  or  $\overline{LW}$ . If  $\overline{UW}$  and  $\overline{LW}$  are both sampled high, a read cycle is started, as described above. If  $\overline{UW}$  or  $\overline{LW}$  is sampled low, a write cycle is begun. The address, write data, and the chip enable input ( $\overline{CE}$ ) are sampled by the same edge that samples  $\overline{ADSC}$  and  $\overline{UW}$  or  $\overline{LW}$ . The  $\overline{ADV}$  line is held high for this clock edge to maintain the correct address for the internal write operation which will follow this second clock edge.

After the first cycle of the write burst, the state of  $\overline{UW}$  and  $\overline{LW}$  determines whether the next cycle is a read or write cycle, and  $\overline{ADV}$  controls the advance of the address counter. The address counter is advanced by the  $\overline{ADV}$  signal. This increments the address to the next available RAM address. You write the next word in the burst by taking  $\overline{ADV}$  low and presenting the write data at the positive edge of the clock. If  $\overline{ADV}$  is sampled low, the burst counter advances and the write data, which is sampled by the same clock, is written into the internal RAM during the time following the clock edge.

This part has an output register. Output read data is available one cycle after the address register and burst counter have been loaded or incremented.

**Absolute Maximum Ratings <sup>(1)</sup>**

Symbol	Rating	Com'l.	Ind.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to V <sub>SS</sub>	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.5	1.5	W
I <sub>OUT</sub>	DC Output Current	50	50	mA
T <sub>j</sub>	Maximum Junction Temperature <sup>(2)</sup>	125	125	°C

- NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form:  $T_j = T_a + P \cdot \theta_{ja}$  where  $T_a$  is the ambient temperature, P is average operating power and  $\theta_{ja}$  the thermal resistance of the package. For this product, use the following  $\theta_{ja}$  value:

PLCC-J: 45° C/W

**Recommended DC Operating Conditions**

Symbol	Description	Min.	Typ.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V	
V <sub>CCQ</sub>		5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V	
Industrial	Ambient Temperature	-40	25	85	°C	
Commercial	Ambient Temperature	0	25	70	°C	

**DC Electrical Characteristics** ( $V_{CC} = 5.0V \pm 5\%$ , All Temperature Ranges)

Symbol	Description	Test Conditions	Min.	Max.	Unit
$I_{L I}$	Input Leakage Current	$V_{CC} = MAX., V_{IN} = V_{SS} \text{ to } V_{CC}$	---	1	$\mu A$
$I_{L O}$	Output Leakage Current	$V_{CC} = MAX., V_{OUT} = V_{SS} \text{ to } V_{CC}$	---	1	$\mu A$
$V_{OL}$	Output Low Voltage	$V_{CC} = Min., I_{OL} = 8 \text{ mA}$	0	0.4	V
$V_{OH}$	Output High Voltage	$V_{CC} = Min., I_{OH} = -4 \text{ mA}$	2.4	$V_{CCQ}$	V
$V_{IH}$	Input HIGH Voltage		2.2	6	V
$V_{IL}$	Input LOW Voltage <sup>(1)</sup>		-0.5	0.8	V

NOTE: 1. Undershoots to -1.5 for 10 ns are allowed once per cycle.

**Power Supply Characteristics**

Symbol	Description	Test Conditions	-4.5	-5 ns	-6 ns	-7 ns	-8 ns	Unit
$I_{CC1}$	Active Supply Current: Outputs Open	$V_{CC} = Max.,$ Inputs @ 0.0V or 3.0V $f = 1/t_{CYC}$ on Rclk & Wclk	390	380	370	360	360	mA
$I_{SB}$	Standby Current: Outputs Open	$V_{CC} = Max.,$ Inputs @ 0.0V or 3.0V $f = 1/t_{CYC}, \overline{CE} = V_{IH}$	135	130	125	120	120	mA

SHADED AREA = PRELIMINARY DATA

NOTE: All values are maximum guaranteed values.

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**Capacitance** ( $T_A = +25^\circ C, f = 1.0 \text{ MHz}$ )

Symbol	Parameter	Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	8	pF

NOTES: 1. This parameter is determined by device characterization, but is not production tested.

**AC Test Conditions**

Input pulse levels	V <sub>SS</sub> to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

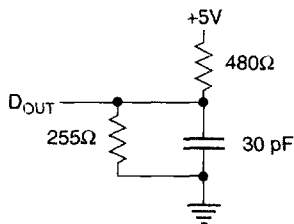


Figure 1. Output Load Equivalent

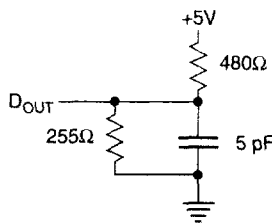


Figure 2. Output Load Equivalent  
(for t<sub>LZCE</sub>, t<sub>HZCE</sub>, t<sub>LZWE</sub>, t<sub>HZWE</sub>, t<sub>LZOE</sub>, t<sub>HZOE</sub>)

**AC Electrical Characteristics**

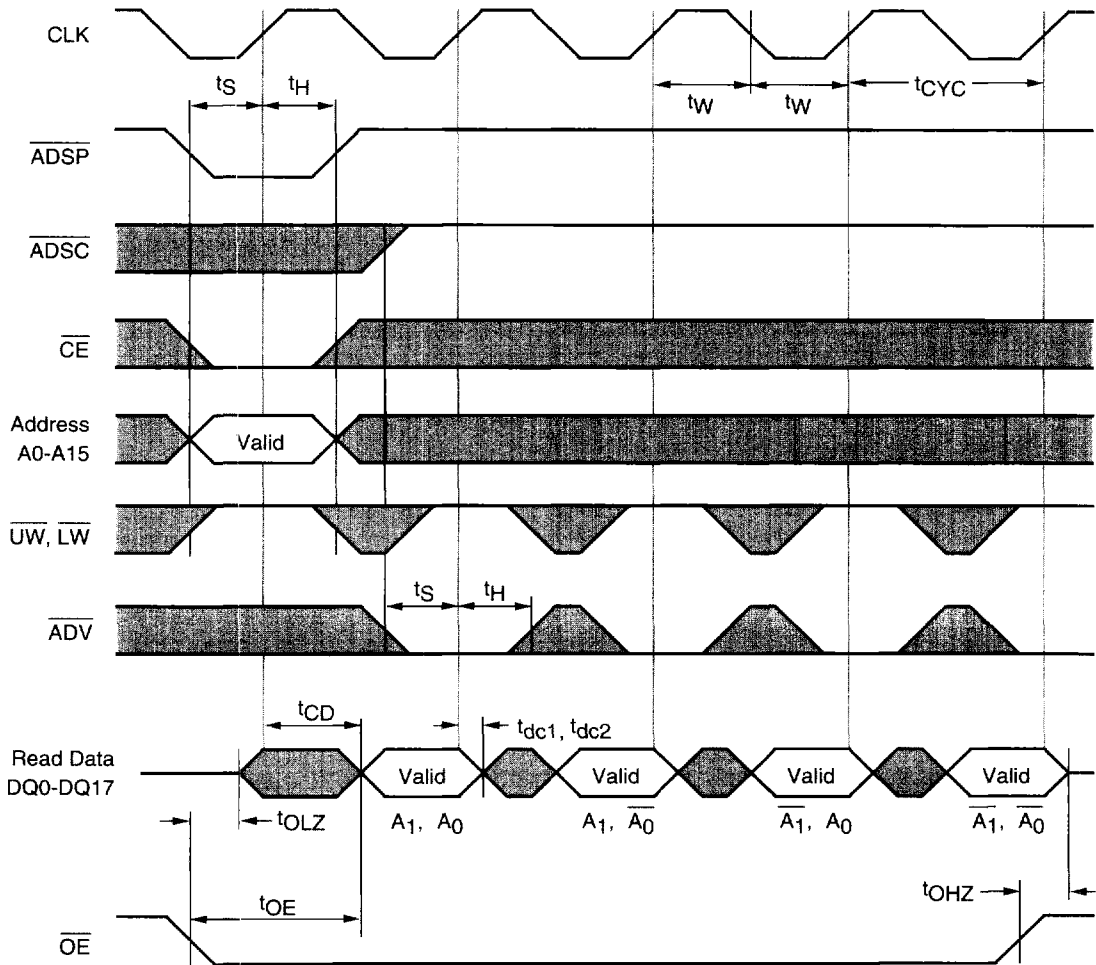
Parameter	Symbol	-4.5	-5	-6	-7	-8	Type	Units
Clock cycle time	t <sub>CYC</sub>	8	10	13	15	15	Min.	ns
Clock to data valid (std. load) <sup>(5)</sup>	t <sub>CD</sub>	4.5	5	6	7	8	Max.	ns
Clock to data valid (0 pF load)	t <sub>CD0</sub>	4	4	5	6	7	Min.	ns
Output enable	t <sub>OE</sub>	4.5	5	5	5	5	Max.	ns
Clock to data low-Z	t <sub>dc1</sub>	2	3	3	3	3	Min.	ns
Clock to data hold time	t <sub>dc2</sub>	2	3	3	3	3	Min.	ns
Output enable to output low-Z <sup>(1)</sup>	t <sub>OLZ</sub>	0	0	0	0	0	Min.	ns
Output enable to output high-Z <sup>(1,6)</sup>	t <sub>OHZ</sub>	2	2	2	2	2	Min.	ns
		3	4	5	5	5	Max.	ns
Clock to data high-Z <sup>(1,6)</sup>	t <sub>CHZ</sub>	4	5	6	6	6	Max.	ns
Clock high/low	t <sub>W</sub>	3	4	4.5	5	5	Min.	ns
Setup time <sup>(7)</sup>	t <sub>S</sub>	2.5	2.5	2.5	2.5	2.5	Min.	ns
Hold time <sup>(7)</sup>	t <sub>H</sub>	0.5	0.5	0.5	0.5	0.5	Min.	ns

SHADED AREA = PRELIMINARY DATA

NOTES:

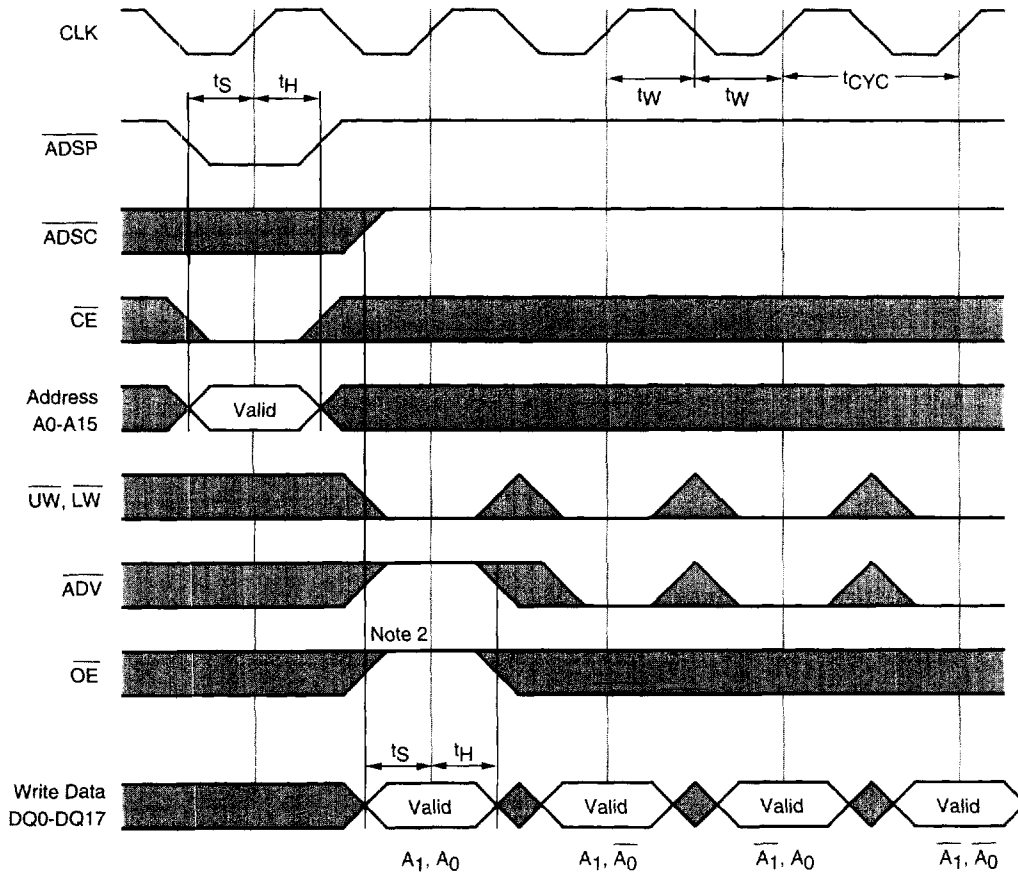
1. Values characterized and guaranteed by design, not currently tested.
2. A read cycle is defined by  $\overline{UW}$  and  $\overline{LW}$  high or  $\overline{ADSP}$  low for the setup and hold times. A write cycle is defined by  $\overline{LW}$  or  $\overline{UW}$  low and  $\overline{ADSP}$  high for the setup and hold times.
3. All read and write cycle timings are referenced from CLK or  $\overline{OE}$ .
4.  $\overline{OE}$  is a "don't care" when  $\overline{UW}$  or  $\overline{LW}$  is sampled low.
5. Maximum access times are guaranteed for all possible x86 external bus cycles.
6. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 2. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t<sub>CHZ</sub> max is less than t<sub>dc1</sub> min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ALL rising edges of CLK whenever  $\overline{ADSP}$  or  $\overline{ADSC}$  is low, and the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when  $\overline{ADSP}$  or  $\overline{ADSC}$  is low) to remain enabled.
8. This device has an output data register. Read data is available one clock cycle after the address register and burst counter have been loaded or the burst counter has been incremented.

ADSP Read Timing Diagram



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**ADSP Write Timing Diagram**

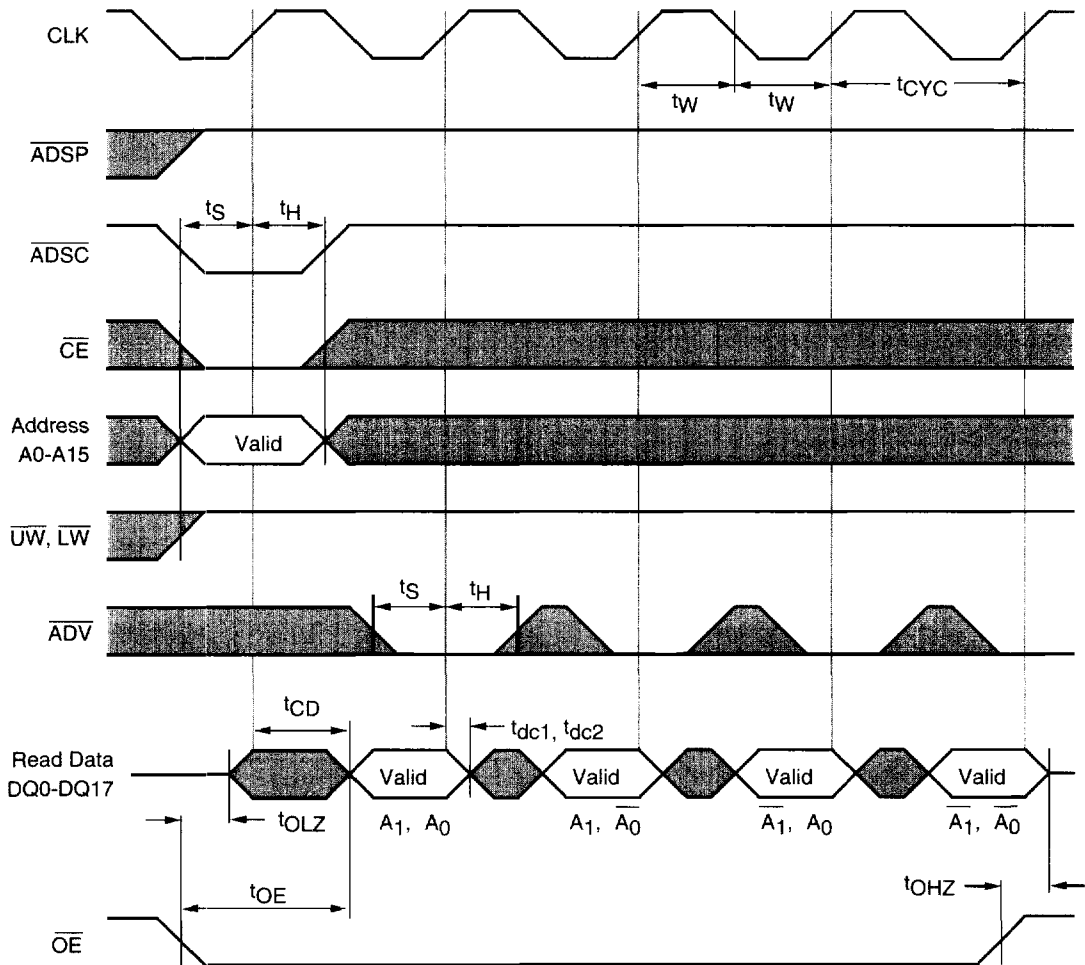


**NOTES:**

1.  $\overline{UW}$  and  $\overline{LW}$  are ignored for the first cycle when  $\overline{ADSP}$  initiates the burst.  $\overline{ADSP}$  active loads a new address into the address counter and forces the first cycle to be a read cycle.
2.  $\overline{OE}$  is high before data in setup.

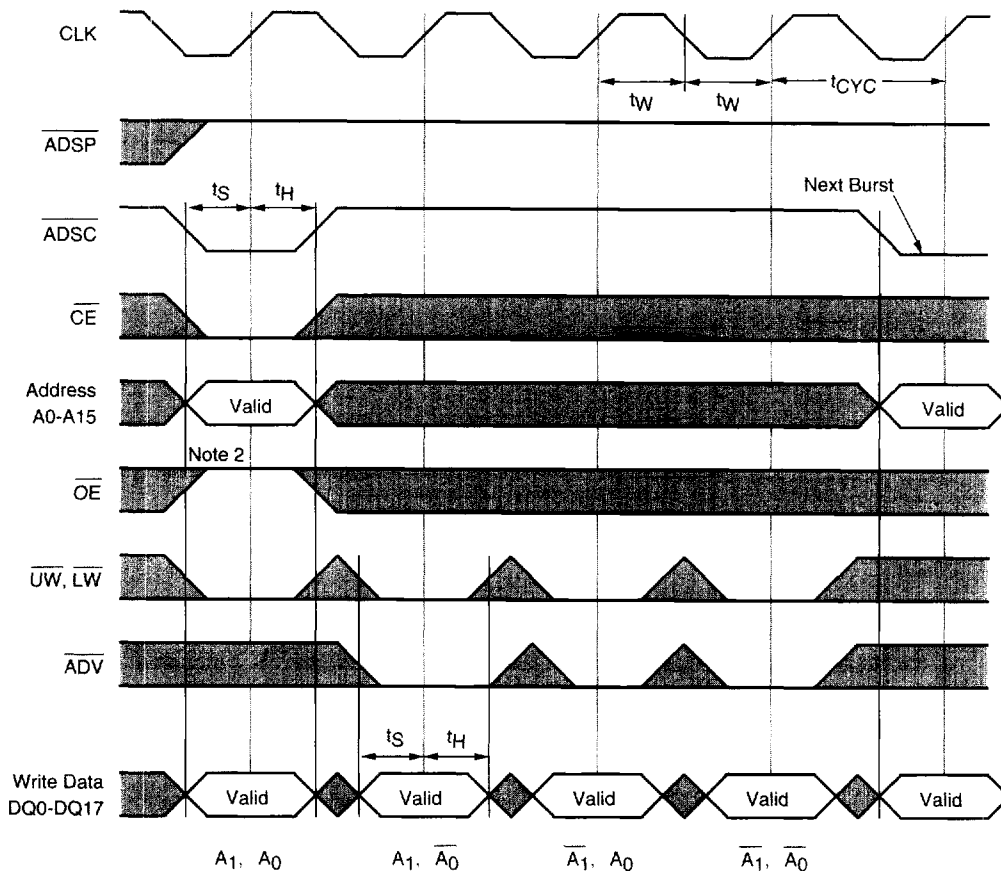


ADSC Read Timing Diagram



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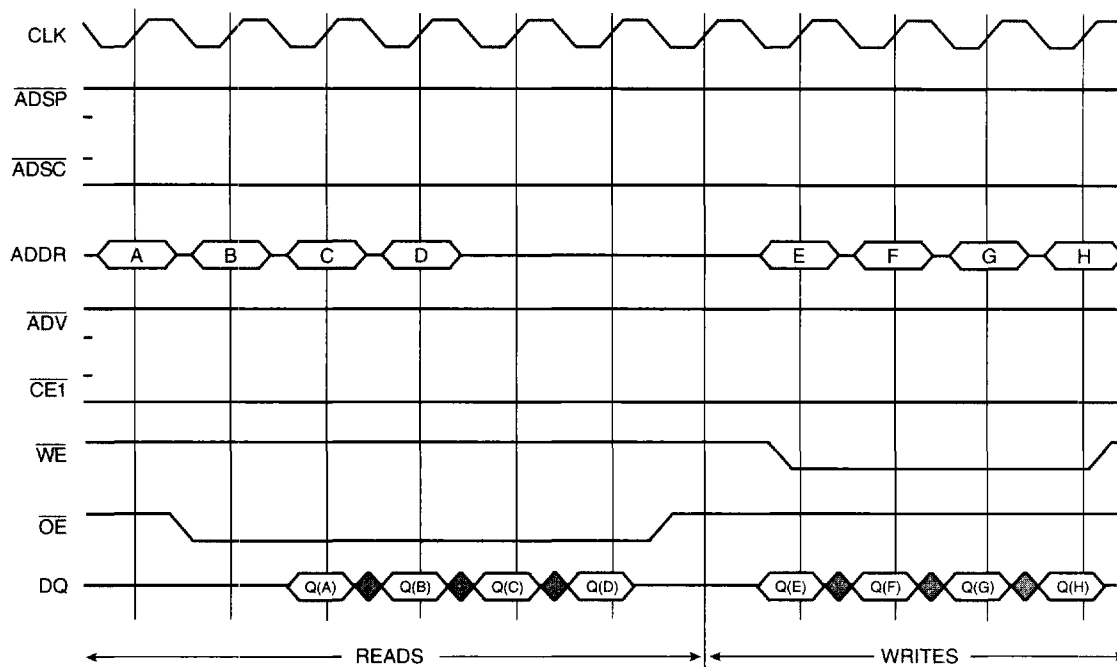
**ADSC Write Timing Diagram**



**NOTES:**

1.  $\overline{UW}$  and  $\overline{LW}$  are ignored for the first cycle when  $\overline{ADSP}$  initiates the burst.  $\overline{ADSP}$  active loads a new address into the address counter and forces the first cycle to be a read cycle.
2.  $\overline{OE}$  is high before data in setup.

Sequential Non-burst Read and Write Timing Diagram



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NOTES:

1.  $\overline{ADSP} = \text{high}$ ,  $\overline{ADSC} = \text{low}$ ,  $\overline{ADV} = \text{high}$ ,  $\overline{CE1} = \text{low}$ .
2.  $H \geq V_{IH}$ ,  $L \leq V_{IL}$ .

Ordering Information

