32M/64M/128M [x8/x16] SINGLE 3V PAGE MODE FLASH MEMORY

FEATURES

- 2.7V to 3.6V operation voltage
- Block Structure
  - 32 x 128Kbyte Erase Blocks (32M)
  - 64 x 128Kbyte Erase Blocks (64M)
  - 128 x 128Kbyte Erase Blocks (128M)
- Fast random / page mode access time
  - 120/25 ns Read Access Time (32M)
  - 120/25 ns Read Access Time (64M)
  - 150/25 ns Read Access Time (128M)
- 128-bit Protection Register
  - 64-bit Unique Device Identifier
  - 64-bit User Programmable OTP Cells
- 32-Byte Write Buffer
  - 6 us/byte Effective Programming Time
- Enhanced Data Protection Features Absolute Protection with VPEN = GND
  - Flexible Block Locking
  - Block Erase/Program Lockout during Power Transitions

Performance

- Low power dissipation
  - typical 15mA active current for page mode read
  - 80uA/(max.) standby current
  - Deep power-down current: 5uA
- High Performance
  - Block erase time: 2s typ.
  - Byte programming time: 210us typ.
  - Block programming time: 0.8s typ. (using Write to Buffer Command)
- Program/Erase Endurance cycles:
  five grades-- "C1" stands for 10 cycles
  　　　　　　 "C2" stands for 100 cycles
  　　　　　　 "C3" stands for 1,000 cycles
  　　　　　　 "C4" stands for 10,000 cycles
  　　　　　　 "C5" stands for 100,000 cycles
  (please refer to Ordering Information of page 47)

Software Feature

- Support Common Flash Interface (CFI)
  - Flash device parameters stored on the device and provide the host system to access.
- Automation Suspend Options
  - Block Erase Suspend to Read
  - Block Erase Suspend to Program
  - Program Suspend to Read

Hardware Feature(Not for 48-TSOP/48-RTSOP)

- A0 pin
  - Select low byte address when device is in byte mode. Not used in word mode.
- STS pin
  - Indicates the status of the internal state machine.
- VPEN pin
  - For Erase /Program/ Block Lock enable.
- VCCQ Pin
  - The output buffer power supply, control the device 's output voltage.

Packaging

- 48-Lead TSOP (for MX28F128J3)
- 48-Lead RTSOP (for MX28F128J3)
- 56-Lead TSOP
- 48-ball Flip Chip CSP (for MX28F320J3/640J3)
- 64-ball CSP

Technology

- MX28F128J3 using Nbit (0.25u) Flash Technology
- MX28F320J3/640J3 using Nbit (0.35u) Flash Technology

GENERAL DESCRIPTION

The MXIC's MX28F320J3/640J3/128J3 series Flash use the most advance 2 bits/cell Nbit technology, double the storage capacity of memory cell. The device provide the high density Flash memory solution with reliable performance and most cost-effective.

The device organized as by 8 bits or by 16 bits of output bus. The device is packaged in 48-Lead TSOP, 48-Lead RTSOP, 56-Lead TSOP, 48-ball Flip Chip CSP and 64-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The device offers fast access time and allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the device has separate chip enable (CE0, CE1, CE2) and output enable ($\overline{OE}$) controls. The device augment EPROM functionality with in-circuit electrical erasure and programming. The device uses a command register to manage this functionality.

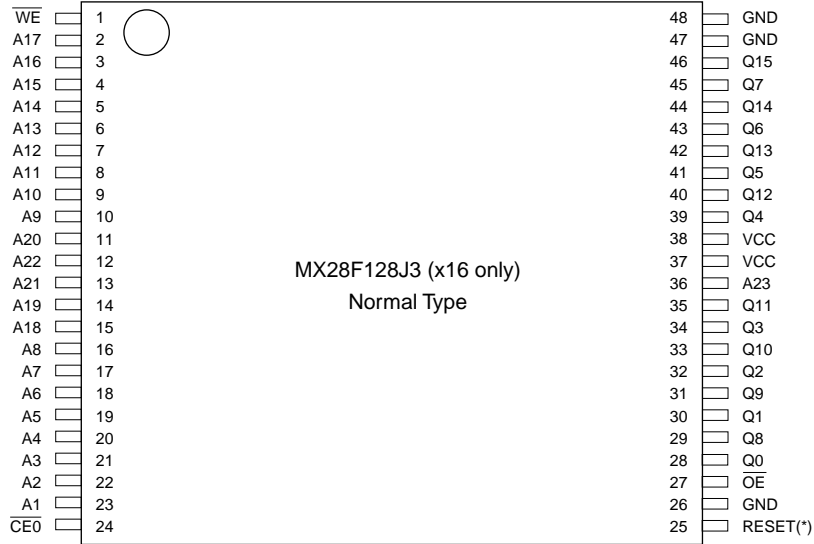The MXIC's Nbit technology reliably stores memory contents even after the specific erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms by utilizing the dielectric's character to trap or release charges from ONO layer.

The device uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

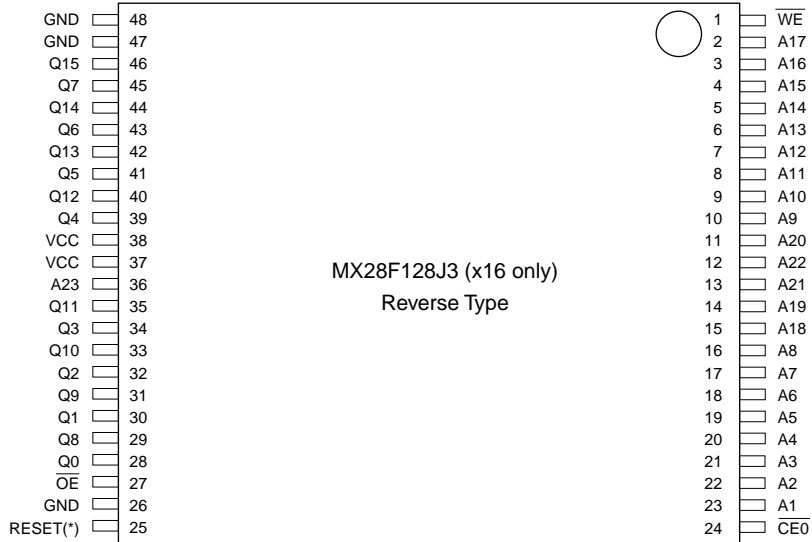The highest degree of latch-up protection is achieved

PIN CONFIGURATION
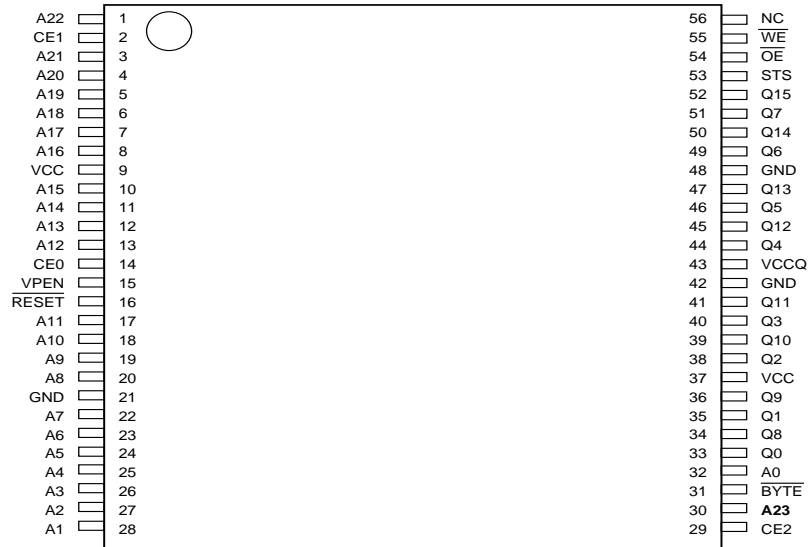
48-TSOP (12mm x 20mm) (for MX28F128J3 word mode only)

Left Pin	#		#	Right Pin
WE	1		48	GND
A17	2		47	GND
A16	3		46	Q15
A15	4		45	Q7
A14	5		44	Q14
A13	6		43	Q6
A12	7		42	Q13
A11	8		41	Q5
A10	9		40	Q12
A9	10		39	Q4
A20	11		38	VCC
A22	12	MX28F128J3 (x16 only)	37	VCC
A21	13	Normal Type	36	A23
A19	14		35	Q11
A18	15		34	Q3
A8	16		33	Q10
A7	17		32	Q2
A6	18		31	Q9
A5	19		30	Q1
A4	20		29	Q8
A3	21		28	Q0
A2	22		27	OE
A1	23		26	GND
CE0	24		25	RESET(*)

(* RESET pin : high enable)

48-RTSOP (12mm x 20mm) (for MX28F128J3 word mode only)

Left Pin	#		#	Right Pin
GND	48		1	WE
GND	47		2	A17
Q15	46		3	A16
Q7	45		4	A15
Q14	44		5	A14
Q6	43		6	A13
Q13	42		7	A12
Q5	41		8	A11
Q12	40		9	A10
Q4	39		10	A9
VCC	38		11	A20
VCC	37	MX28F128J3 (x16 only)	12	A22
A23	36	Reverse Type	13	A21
Q11	35		14	A19
Q3	34		15	A18
Q10	33		16	A8
Q2	32		17	A7
Q9	31		18	A6
Q1	30		19	A5
Q8	29		20	A4
Q0	28		21	A3
OE	27		22	A2
GND	26		23	A1
RESET(*)	25		24	CE0

(* RESET pin : high enable)

56 TSOP (14mm x 20mm)

Pin	Signal		Pin	Signal
1	A22		56	NC
2	CE1		55	$\overline{WE}$
3	A21		54	$\overline{OE}$
4	A20		53	STS
5	A19		52	Q15
6	A18		51	Q7
7	A17		50	Q14
8	A16		49	Q6
9	VCC		48	GND
10	A15		47	Q13
11	A14		46	Q5
12	A13		45	Q12
13	A12		44	Q4
14	CE0		43	VCCQ
15	VPEN		42	GND
16	$\overline{RESET}$		41	Q11
17	A11		40	Q3
18	A10		39	Q10
19	A9		38	Q2
20	A8		37	VCC
21	GND		36	Q9
22	A7		35	Q1
23	A6		34	Q8
24	A5		33	Q0
25	A4		32	A0
26	A3		31	$\overline{BYTE}$
27	A2		30	**A23**
28	A1		29	CE2

Notes:
1. A22 exists on 64M, 128M densities. On 32M densities this pin is a no connect (NC).
2. A23 exists on 128M densities. On 32M and 64M densities this pin is a no connect (NC).

48 Flip Chip CSP (for MX28F320J3/640J3)

	1	2	3	4	5	6	7	8
A	A14	A12	A9	VPEN	VCC	A20	A8	A5
B	A15	A11	$\overline{WE}$	RESET	A19	A18	A6	A3
C	A16	A13	A10	A22	A21	A7	A4	A2
D	A17	Q14	Q5	Q11	Q2	Q8	$\overline{CEO}$	A1
E	VCCQ	Q15	Q6	Q12	Q3	Q9	Q0	GND
F	GND	Q7	Q13	Q4	VCC	Q10	Q1	$\overline{OE}$

13 mm

8mm
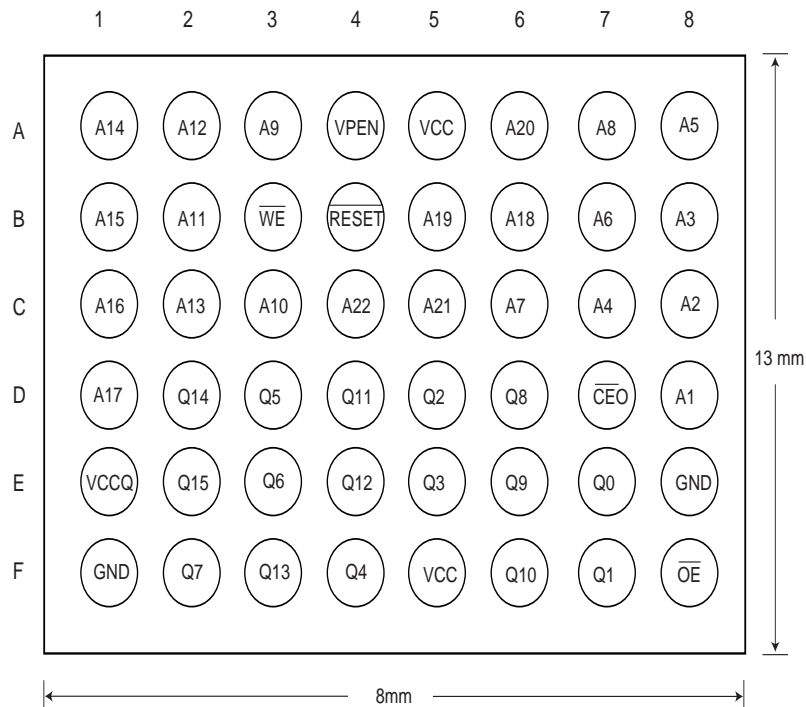
64 Ball CSP (10x13x1.2mm, 1.0mm-ball pitch)

	1	2	3	4	5	6	7	8
A	A1	A6	A8	VPEN	A13	VCC	A18	A22
B	A2	GND	A9	CE0	A14	DU	A19	CE1
C	A3	A7	A10	A12	A15	DU	A20	A21
D	A4	A5	A11	$\overline{\text{RESET}}$	DU	DU	A16	A17
E	Q8	Q1	Q9	Q3	Q4	DU	Q15	STS
F	$\overline{\text{BYTE}}$	Q0	Q10	Q11	Q12	DU	DU	$\overline{\text{OE}}$
G	A23	A0	Q2	VCCQ	Q5	Q6	Q14	$\overline{\text{WE}}$
H	$\overline{\text{CE2}}$	DU	VCC	GND	Q13	GND	Q7	NC

13 mm

10mm

Notes:
1. Address A22 is only valid on 64M and 128M densities. Otherwise, it is a no connect (NC).
2. Address A23 is only valid on 128M densities. Otherwise, it is a no connect (NC).
3. Don't Use (DU) pins refer to pins that should not be connected.

PIN DESCRIPTION

SYMBOL	PIN NAME
A0	Byte Select Address
A1~A23	Address Input (32M:A0~A21, 64M:A0~A22, 128M:A0~A23)
Q0~Q15	Data Inputs/Outputs
CE0, CE1, CE2	Chip Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{RESET}}$	Reset/Deep Power Down mode (low enable for 56-TSOP & 64-CSP)
RESET	Reset/Deep Power Down mode (high enable for 48-TSOP & 48-RTSOP)

SYMBOL	PIN NAME
STS	STATUS Pin
$\overline{\text{BYTE}}$	Byte Mode Enable
VPEN	ERASE/PROGRAM/BLOCK Lock Enable
VCCQ	Output Buffer Power Supply
VCC	Device Power Supply
GND	Device Ground
NC	Pin Not Connected Internally
DU	Don't Use

BLOCK DIAGRAM
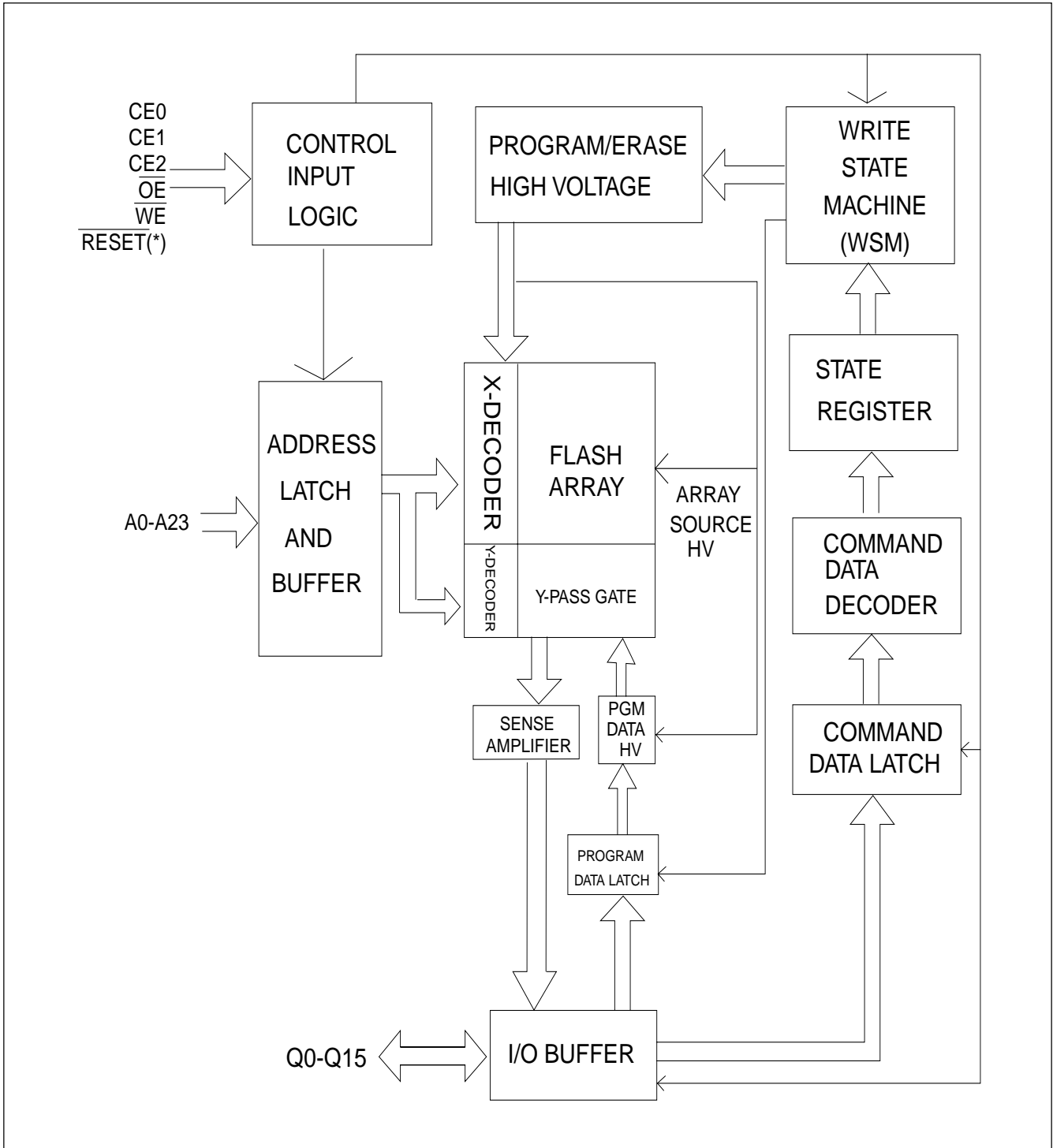
* : $\overline{RESET}$ pin for 56-TSOP & 64-CSP; RESET pin for 48-TSOP & 48-RTSOP.

Figure 1. Block Architecture

Flash memory reads erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.
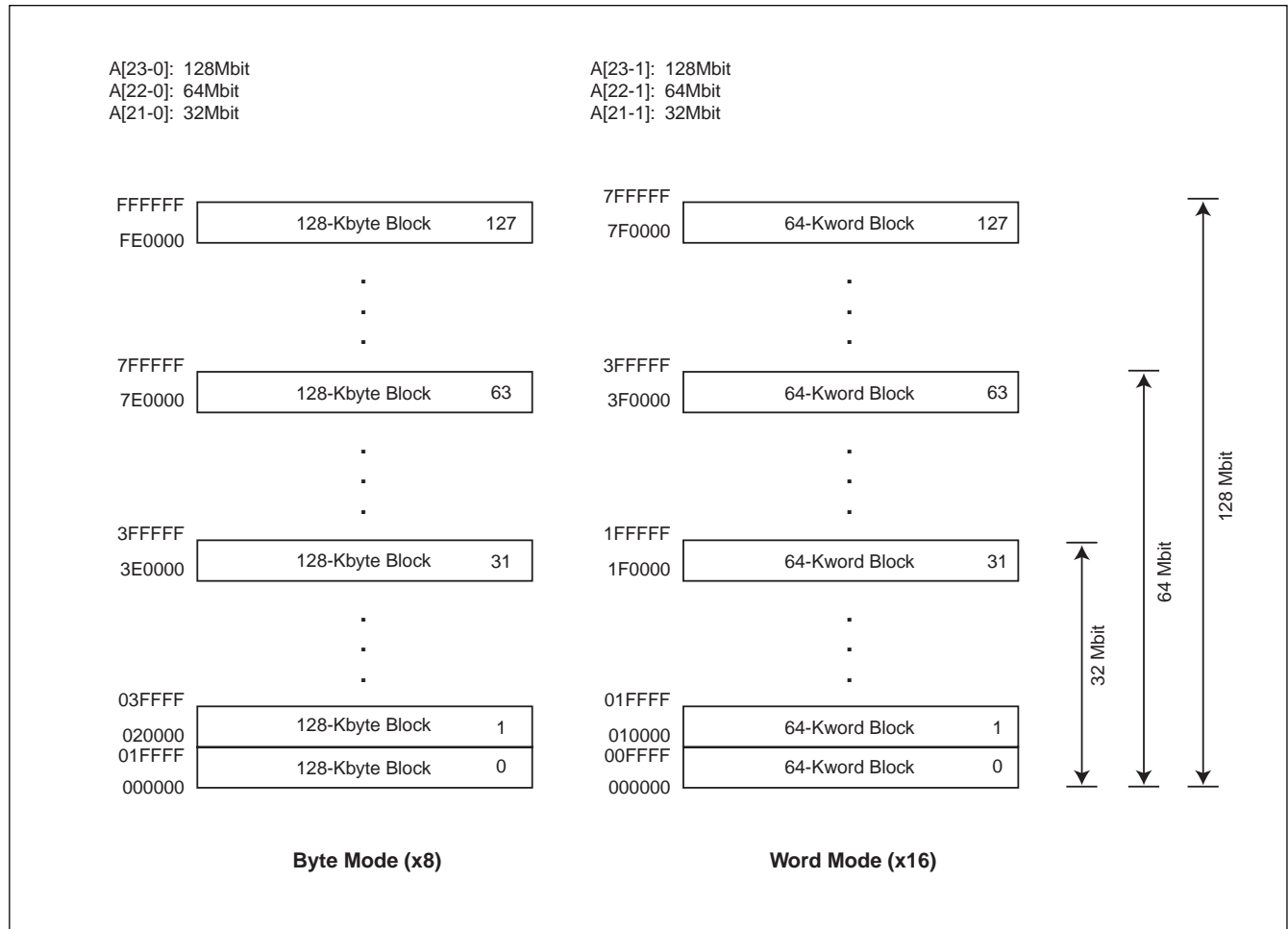
Table 1. Chip Enable Truth Table

CE2	CE1	CE0	DEVICE
VIL	VIL	VIL	Enabled
VIL	VIL	VIH	Disabled
VIL	VIH	VIL	Disabled
VIL	VIH	VIH	Disabled
VIH	VIL	VIL	Enabled
VIH	VIL	VIH	Enabled
VIH	VIH	VIL	Enabled
VIH	VIH	VIH	Disabled

NOTE: For Single-chip applications, CE2 and CE1 can be strapped to GND.

Table 2. Bus Operations

Command Sequence	Read Array	Output Disable	Standby	RESET Mode/ Deep Power Down Mode	Read ID	Read Query	Read Status (WSM off)	Read Status (WSM on)	Write
Notes	4,5,6								6,10,11
$\overline{\text{RESET}}$ (12)	VIH	VIH	VIH	VIL (12)	VIH	VIH	VIH	VIH	VIH
CE0,CE1,CE2(1)	Enabled	Enabled	Disabled	X	Enabled	Enabled	Enabled	Enabled	Enabled
$\overline{\text{OE}}$ (2)	VIL	VIH	X	X	VIL	VIL	VIL	VIL	VIH
$\overline{\text{WE}}$ (2)	VIH	VIH	X	X	VIH	VIH	VIH	VIH	VIL
Address	X	X	X	X	See Figure 2	See Table 6	X	X	X
VPEN	X	X	X	X	X	X	X	X	VPENH
Q (3)	Data out	High Z	High Z	High Z	Note 8	Note 9	Data out	Q7=Data out Q15-8=High Z Q6-0=High Z	Data in
STS (default mode)	High Z (7)	X	X	High Z (7)	High Z (7)	High Z (7)			X

NOTES:
1. See Table 1 on page 7 for valid $\overline{\text{CE}}$ configurations.
2. $\overline{\text{OE}}$ and $\overline{\text{WE}}$ should never be enabled simultaneously.
3. DQ refers to Q0-Q7 if $\overline{\text{BYTE}}$ is low and Q0-Q15 if $\overline{\text{BYTE}}$ is high.
4. Refer to DC Characteristics. When VPEN ≤ VPENLK , memory contents can be read, but not altered.
5. X can be VIL or VIH for control and address pins, and VPENLK or VPENH for VPEN . See DC Characteristics for VPENLK and VPENH voltages.
6. In default mode, STS is VOL when the WSM is executing internal block erase, program, or lock-bit configuration algorithms. It is VOH when the WSM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or reset/deep power-down mode.
7. High Z will be VOH with an external pull-up resistor.
8. See Section , "Read Identifier Codes" for read identifier code data.
9. See Section , "Read Query Mode Command" for read query data.
10. Command writes involving block erase, program, or lock-bit configuration are reliably executed when VPEN= VPENH and VCC is within specification.
11. Refer to Table 3 on page 10 for valid DIN during a write operation.
12. RESET mode of 48-TSOP & 48-RTSOP types is high enabled to entering deep power down mode.

FUNCTION

The device includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and byte/word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Powerdown mode is enabled when the $\overline{\text{RESET}}$ pin of 56-TSOP & 64-CSP types is at GND or RESET pin of 48-TSOP & 48-RTSOP is at VIH, minimizing power consumption.

READ

The device has three read modes, which accesses to the memory array, the Device Identifier or the Status Register independent of the VPEN voltage. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the device automatically resets to read array mode. In the read array mode, low level input to CE0, CE1, CE2 and $\overline{\text{OE}}$, high level input to $\overline{\text{WE}}$ and $\overline{\text{RESET}}$ or low level input to RESET, and address signals to the address inputs (A23-A0) output the data of the addressed location to the data input/output (Q15~Q0).

When reading information in read array mode, the device defaults to asynchronous page mode. In this state, data is internally read and stored in a high-speed page buffer. A2:0 addresses data in the page buffer. The page size is 4 words or 8 bytes. Asynchronous word/byte mode is supported with no additional commands required.

WRITE

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register and when VPEN=VPENH block erasure program and lock-bit configuration. The CUI is written when the device is enable, $\overline{\text{WE}}$ is active and $\overline{\text{OE}}$ is at high level. Address and data are latched on the earlier rising edge of $\overline{\text{WE}}$ and $\overline{\text{CE}}$. Standard micro-processor write timings are used.

OUTPUT DISABLE

When $\overline{\text{OE}}$ is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

STANDBY

When CE0, CE1 and CE2 disable the device (see table1) and place it in standby mode. The power consumption of this device is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase, program or lock-bit configuration, the internal control circuits remain active and the device consume normal active power until the operation completes.

DEEP POWER-DOWN

When $\overline{\text{RESET}}$ pin of 56-TSOP & 64-CSP types is at VIL or RESET pin of 48-TSOP & 48-RTSOP types is at VIH, the device is in the deep power-down mode and its power consumption is substantially low around 5uA. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. To return from deep power down mode requires $\overline{\text{RESET}}$ pin of 56-TSOP & 64-CSP types at VIH or RESET pin of 48-RTSOP & 48-RTSOP types at VIL. After return from powerdown, the CUI is reset to Read Array , and the Status Register is set to value 80H.

During block erase program or lock-bit configuration modes, $\overline{\text{RESET}}$ pin of 56-TSOP & 64-CSP types at VIL or RESET pin of 48-TSOP & 48-RTSOP types at VIH will abort either operation. Memory array data of the block being altered become invalid.

In default mode, STS transitions low and remains low for a maximum time of tPLPH+tPHRH until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after a program or partially altered after an erase or lock-bit configuration. Time tPHWL is required after $\overline{\text{RESET}}$ goes to logic-high (VIH) or RESET goes to VIL before another command can be written.

READ QUERY

The read query operation outputs block status information, CFI (Common Flash Interface) ID string, system interface information, device geometry information and MXIC extended query information.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the CUI. Table 3 defines the valid register command sequences.

When VPEN≤VPENLK only read operations from the status register, query, indentifier code or blocks are enabled. When VPEN=VPENH enables block erase program and lock-bit configuration operations.

Table 3. Command Definitions

| Command Sequence		Read Array	Read ID	Read Query	Read Status Register	Clear Status Register	Write to Buffer	Word/byte Program	Sector Erase
Notes			5		6		7,8,9	10,11	9,10
Bus Write Cycles Req'd		1	≥ 2	≥ 2	2	1	> 2	2	2
First Bus Write Cycles	Operation(2)	Write	Write	Write	Write	Write	Write	Write	Write
	Address(3)	X	X	X	X	X	BA	X	BA
	Data(4,5)	FFH	90H	98H	70H	50H	E8H	40H/10H	20H
Second Bus Read Query	Operation(2)		Read	Read	Read		Write	Write	Write
	Address(3)		IA	QA	X		BA	PA	BA
	Data(4,5)		ID	QD	SRD		N	PD	D0H

Command Sequence		Sector Erase, Program Suspend	Sector Erase, Program Resume	Configur-ation	Set Sector Lock-Bit	Clear Sector Lock-Bit	Protection Program
Notes		10,12	10			13	
Bus Write Cycles Req'd		1	1	2	2	2	2
First Bus Write Cycle	Operation(2)	Write	Write	Write	Write	Write	Write
	Address(3)	X	X	X	X	X	X
	Data(4,5)	B0H	D0H	B8H	60H	60H	C0H
Second Bus Write Cycle	Operation(2)			Write	Write	Write	Write
	Address(3)			X	BA	X	PA
	Data(4,5)			CC	01H	D0H	PD

NOTES:

1. Bus operations are defined in Table 2.
2. X = Any valid address within the device.
    BA = Address within the block.
    IA = Identifier Code Address: see Figure 2 and Table 14.
    QA = Query database Address.
    PA = Address of memory location to be programmed.
    RCD = Data to be written to the read configuration register. This data is presented to the device on A 16-1 ; all other address inputs are ignored.
3. ID = Data read from Identifier Codes.
    QD = Data read from Query database.
    SRD = Data read from status register. See Table 15 for a description of the status register bits.
    PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
    CC = Configuration Code.
4. The upper byte of the data bus (Q8-Q15) during command writes is a "Don't Care" in x16 operation.
5. Following the Read Identifier Codes command, read operations access manufacturer, device and block lock codes. See Section 4.3 for read identifier code data.
6. If the WSM is running, only Q7 is valid; Q15-Q8 and Q6-Q0 float, which places them in a high impedance state.
7. After the Write to Buffer command is issued check the XSR to make sure a buffer is available for writing.
8. The number of bytes/words to be written to the Write Buffer = N + 1, where N = byte/word count argument.
    Count ranges on this device for byte mode are N = 00H to N = 1FH and for word mode are N = 0000H to N =000FH.
    The third and consecutive bus cycles, as determined by N, are for writing data into the Write Buffer.
    The Confirm command (D0H) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the write to buffer operation. Please see Figure 4. "Write to Buffer Flowchart" for additional information.
9. The write to buffer or erase operation does not begin until a Confirm command (D0h) is issued.
10. Attempts to issue a block erase or program to a locked block.
11. Either 40H or 10H are recognized by the WSM as the byte/word program setup.
12. Program suspends can be issued after either the Write-to-Buffer or Word-/Byte-Program operation is initiated.
13. The clear block lock-bits operation simultaneously clears all block lock-bits.

Figure 2. Device Identifier Code Memory Map
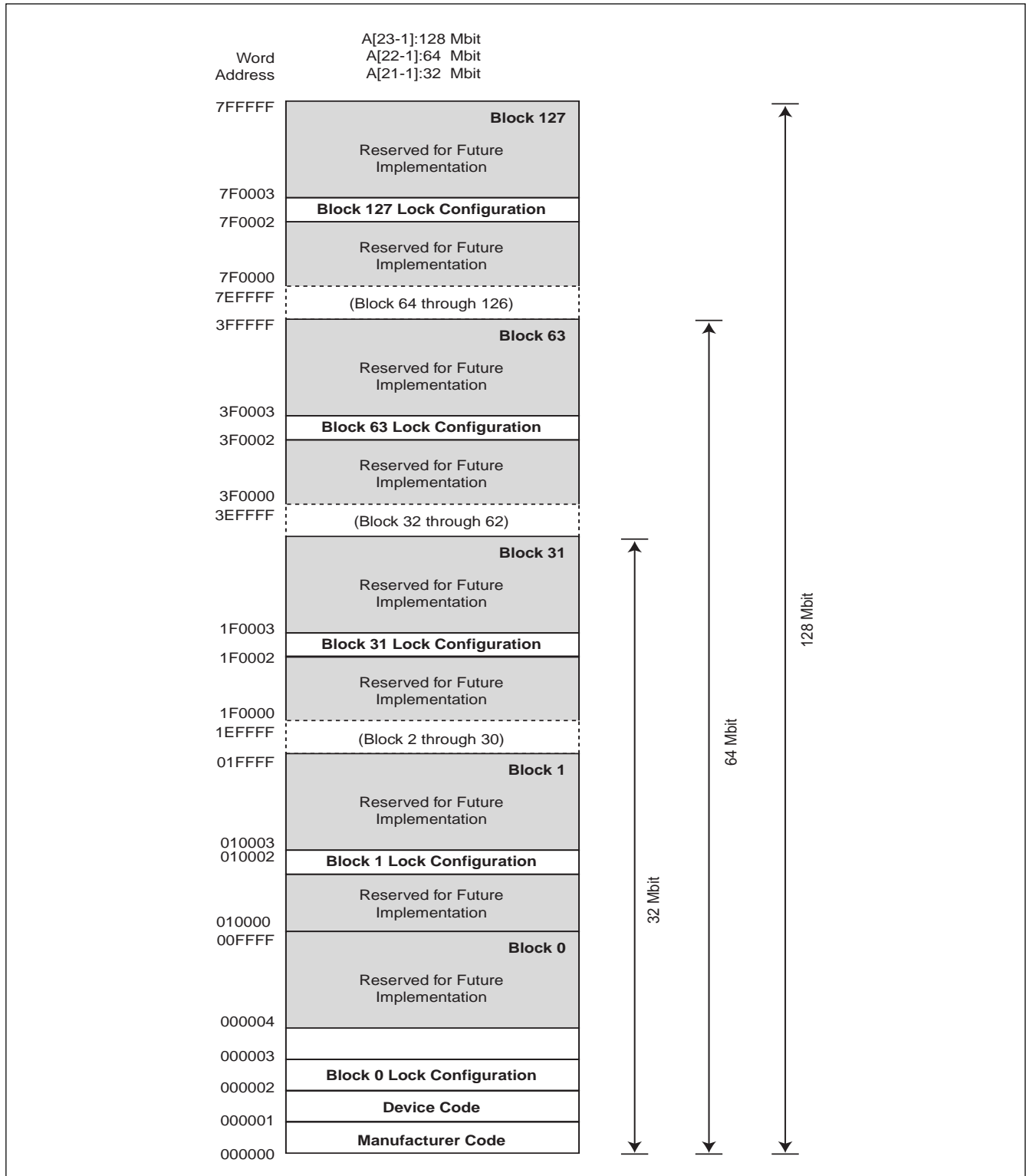
NOTE: A0 is not used in either x8 or x16 mode when obtaining these identifier codes. Data is always given on the low byte in x16 mode (upper byte contains 00h).

Read Array Command

The device is in Read Array mode on initial device power up and after exit from deep power down, or by writing FFH to the Command User Interface. The read configuration register defaults to asynchronous read page mode. The device remains enabled for reads until another command is written. The Read Array command functions independently of the VPEN voltage.

Read Query Mode Command

This section defines the data structure or "Database" returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component.

Query Structure Output

The Query Database allows system software to gain information for controlling the flash component. This section describes the device CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest-order data outputs (DQ 0-7) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two bytes of the Query structure, "Q" and "R" in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII "Q" in the low byte (DQ 0-7) and 00h in the high byte (DQ 8-15).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide devices is always "00h"," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table 4. Summary of Query Structure Output as a Function of Device and Mode

Device Type/Mode	Query start location in maximum device bus width addresses	Query data with maximum device bus width addressing			Query data with byte addressing		
		Hex Offset	Hex Code	ASCII Value	Hex Offset	Hex Code	ASCII Value
x16 device x16 mode	10h	10:	0051	"Q"	20:	51	"Q"
		11:	0052	"R"	21:	00	"Null"
		12:	0059	"Y"	22:	52	"R"
x16 device x8 mode	N/A (1)	N/A (1)			20:	51	"Q"
					21:	51	"Q"
					22:	52	"R"

NOTE:
1. The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing, where these lower addresses are not toggled by the system, is "Not Applicable" for x8-configured devices.

Table 5. Example of Query Structure Output of a x16- and x8-Capable Device

Word Addressing			Byte Addressing		
Offset	Hex Code	Value	Offset	Hex Code	Value
A15-A0	D15 - D0		A7-A0	D7 - D0	
0010h	0051	"Q"	20h	51	"Q"
0011h	0052	"R"	21h	51	"Q"
0012h	0059	"Y"	22h	52	"R"
0013h	P_ID_{LO}	PrVendor	23h	52	"R"
0014h	P_ID_{HI}	ID#	24h	59	"Y"
0015h	PLO	PrVendor	25h	59	"Y"
0016h	PHI	TblAdr	26h	P_ID_{LO}	PrVendor
0017h	A_ID_{LO}	AltVendor	27h	P_ID_{LO}	ID#
0018h	A_ID_{HI}	ID#	28h	P_ID_{HI}	ID#
…	…	…	…	…	…

Query Structure Overview

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or "database". The structure sub-sections and address locations are summarized below.

Table 6. Query Structure (1)

Offset	Sub-Section	Name Description
00h		Manufacturer Code
01h		Device Code
(BA+2)h (2)	Block Status Register	Block-Specific Information
04-0Fh	Reserved	*Reserved for Vendor-Specific Information*
10h	CFI Query Identification String	*Reserved for Vendor-Specific Information*
1Bh	System Interface Information	Command Set ID and Vendor Data Offset
27h	Device Geometry Definition	Flash Device Layout
P (3)	Primary MXIC-Specific Extended Query Table	Vendor-Defined Additional Information Specific to the Primary Vendor Algorithm

NOTES:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = Block Address beginning location (i.e., 02000h is block 2s beginning location when the block size is 128 Kbyte).
3. Offset 15 defines "P" which points to the *Primary Intel-Specific Extended Query* Table.

Block Status Register

The block status register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Table 7. Block Status Register

Offset	Length	Description	Address	Value
(BA+2)h (1)	1	Block Lock Status Register	BA+2:	--00 or --01
		BSR.0 Block Lock Status 0 = Unlocked 1 = Locked	BA+2:	(bit 0): 0 or 1
		BSR 1-7: *Reserved for Future Use*	BA+2:	(bit 1-7): 0

NOTE:
1. BA = The beginning location of a Block Address (i.e., 008000h is block 1s (64-KB block) beginning location in word mode).

CFI Query Identification String

The CFI Query Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 8. CFI Identification

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string "QRY"	10	--51	"Q"
			11:	--52	"R"
			12:	--59	"Y"
13h	2	Primary vendor command set and control interface ID code.	13:	--01	
		16-bit ID code for vendor-specified algorithms	14:	--00	
15h	2	Extended Query Table primary algorithm address	15:	--31	
			16:	--00	
17h	2	Alternate vendor command set and control interface ID code.	17:	--00	
		0000h means no second vendor-specified algorithm exists	18:	--00	
19h	2	Secondary algorithm Extended Query Table address.	19:	--00	
		0000h means none exists	1A:	--00	

System Interface Information

The following device information can optimize system interface software.

Table 9. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	VCC logic supply minimum program/erase voltage bits 0-3 BCD 100 mV bits 4-7 BCD volts	1B:	--27	2.7 V
1Ch	1	VCC logic supply maximum program/erase voltage bits 0-3 BCD 100 mV bits 4-7 BCD volts	1C:	--36	3.6 V
1Dh	1	VPP [programming] supply minimum program/erase voltage bits 0-3 BCD 100 mV bits 4-7 HEX volts	1D:	--00	0.0V
1Eh	1	VPP [programming] supply maximum program/erase voltage bits 0-3 BCD 100 mV bits 4-7 HEX volts	1E:	--00	0.0V
1Fh	1	"n" such that typical single word program time-out = 2us	1F:	--07	128us
20h	1	"n" such that typical max. buffer write time-out = 2us	20:	--07	128us
21h	1	"n" such that typical block erase time-out = 2ms	21:	--0A	1s
22h	1	"n" such that typical full chip erase time-out = 2ms	22:	--00	NA
23h	1	"n" such that maximum word program time-out = 2 times typical	23:	--04	2ms
24h	1	"n" such that maximum buffer write time-out = 2 times typical	24:	--04	2ms
25h	1	"n" such that maximum block erase time-out = 2 times typical	25:	--04	16s
26h	1	"n" such that maximum chip erase time-out = 2 times typical	26:	--00	NA

Device Geometry Definition

This field provides critical details of the flash device geometry.

Table 10. Device Geometry Definition

Offset	Length	Description	Code See Table Below		
27h	1	"n" such that device size = 2^n in number of bytes	27:		
28h	2	Flash device interface: x8 async(28:00,29:00), x16 async(28:01,29:00), x8/x16 async(28:02,29:00)	28: 29:	--02 --00	x8/x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--05 --00	32
2Ch	1	Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in "bulk" 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size)	2C:	--01	1
2Dh	4	Erase Block Region 1 Information bits 0-15 = y, y+1 = number of identical-size erase blocks bits 16-31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:		

Device Geometry Definition

Address	32M	64M	128M
27:	--16	--17	--18
28:	--02	--02	--02
29:	--00	--00	--00
2A:	--05	--05	--05
2B:	--00	--00	--00
2C:	--01	--01	--01
2D:	--1F	--3F	--7F
2E:	--00	--00	--00
2F:	--00	--00	--00
30:	--02	--02	--02

Primary-Vendor Specific Extended Query Table

Certain flash features and commands are optional. The *Primary Vendor-Specific Extended Query* table specifies this and other similar information.

Table 11. Primary Vendor-Specific Extended Query

Offset(1) P=31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	31:	--50	"P"
(P+1)h		Unique ASCII string "PRI"	32:	--52	"R"
(P+2)h			33:	--49	"I"
(P+3)h	1	Major version number, ASCII	34:	--31	"1"
(P+4)h	1	Minor version number, ASCII	35:	--31	"1"
(P+5)h		Optional feature and command support (1=yes, 0=no)	36:	--0A	
(P+6)h		bits 9-31 are reserved; undefined bits are "0". If bit 31 is	37:	--00	
(P+7)h		"1" then another 31 bit field of optional features follows at	38:	--00	
(P+8)h		the end of the bit-30 field.	39:	--00	
		bit 0 Chip erase supported	bit 0 = 0		No
	4	bit 1 Suspend erase supported	bit 1 = 1		Yes
		bit 2 Suspend program supported	bit 2 = 1		Yes
		bit 3 Legacy lock/unlock supported	bit 3 = 1(1)		Yes(1)
		bit 4 Queued erase supported	bit 4 = 0		No
		bit 5 Instant Individual block locking supported	bit 5 = 0		No
		bit 6 Protection bits supported	bit 6 = 1		Yes
		bit 7 Page-mode read supported	bit 7 = 1		Yes
		bit 8 Synchronous read supported	bit 8 = 0		No
(P+9)h	1	Supported functions after suspend: read Array, Status,Query Other supported operations are: bits 1-7 reserved; undefined bits are "0"	3A:	--01	
		bit 0 Program supported after erase suspend	bit 0 = 1		Yes
(P+A)h	2	Block status register mask	3B:	--01	
(P+B)h		bits 2-15 are Reserved; undefined bits are "0"	3C:	--00	
		bit 0 Block Lock-Bit Status register active	bit 0 = 1		Yes
		bit 1 Block Lock-Down Bit Status active	bit 1 = 0		No
(P+C)h	1	VCC logic supply highest performance program/erase voltage bits 0-3 BCD value in 100 mV bits 4-7 BCD value in volts	3D:	--33	3.3V
(P+D)h	1	VPP optimum program/erase supply voltage bits 0-3 BCD value in 100 mV bits 4-7 HEX value in volts	3E:	--00	0.0V

NOTE:
1. Future devices may not support the described "Legacy Lock/Unlock" function. Thus bit 3 would have a value of "0".

Table 12. Protection Register Information

Offset(1) P=31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection bytes are available	3F:	--01	01
(P+F)h (P+10)h (P+11)h (P+12)h		Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) protection register bytes. Some are pre-programmed with device-unique serial numbers. Others are user-programmable. Bits 0-15 point to the protection register lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0-7 = Lock/bytes JEDEC-plane physical low address bits 8-15 = Lock/bytes JEDEC-plane physical high address bits 16-23 = "n" such that 2^n = factory pre-programmed bytes bits 24-31 = "n" such that 2^n = user-programmable bytes	40:	--00	00h

NOTE:
1. The variable P is a pointer which is defined at CFI offset 15h.

Table 13. Page Read Information

Offset(1) P=31h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+13)h	1	Page Mode Read capability bits 0-7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	44:	--03	8 byte
(P+14)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	45:	--00	0
(P+15)h		Reserved for future use	46:		

NOTE:
1. The variable P is a pointer which is defined at CFI offset 15h.

DEVICE OPERATION

SILICON ID READ

The Silicon ID Read mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the two cycle "Silicon ID Read" command is requested. (The command sequence is illustrated in Table 14.

During the "Silicon ID Read" Mode, manufacturer's code (MXIC=C2H) can be read out by setting A0=VIL and device identifier can be read out by setting A0=VIH.

To terminate the operation, it is necessary to write the read command. The "Silicon ID Read" command functions independently of the VPEN voltage. This command is valid only when the WSM is off or the device is suspended.

Table 14. MX28F320J3/640J3/128J3 Silicon ID Codes and Verify Sector Protect Code

Type		Address (1)	Code (HEX)	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Manufacture Code		00000	C2H	1	1	0	0	0	0	1	0
Device Code	32M	00001	(00) 72H	0	1	1	1	0	0	1	0
	64M	00001	(00) 73H	0	1	1	1	0	0	1	1
	128M	00001	(00) 74H	0	1	1	1	0	1	0	0
Block Lock Configuration		X0002 (2)									
- Block is Unlocked			DQ0=0								
- Block is Locked			DQ0=1								
- Reserved for Future Use			DQ1-7								

* Outputs C2H at protected sector address, 00H at unprotected sector address.
** Only the top and the bottom sectors have protect-bit feature. Sector address = (A20, A19, A18,A17,A16) = 00000B or 11111B

Table 15. Status Register Definitions

Symbol	High Z When Busy?	Status	Definition "1"	Definition "0"	Notes
SR.7	No	WRITE STATE MACHINE STATUS	Ready	Busy	1
SR.6	Yes	ERASE SUSPEND STATUS	Block Erase Suspended	Block Erase in Progress/Completed	
SR.5	Yes	ERASE AND CLEAR LOCK-BITS STATUS	Error in Block Erasure or Clear Lock-Bits	Successful Block Erase or Clear Lock-Bits	2
SR.4	Yes	PROGRAM AND SET LOCK-BIT STATUS	Error in Setting Lock-Bit	Successful Set Block Lock Bit	
SR.3	Yes	PROGRAMMING VOLTAGE STATUS	Low Programming Voltage Detected, Operation Aborted	Programming Voltage OK	3
SR.2	Yes	PROGRAM SUSPEND STATUS	Program suspended	Program in progress/completed	
SR.1	Yes	DEVICE PROTECT STATUS	Block Lock-Bit Detected, Operation Abort	Unlock	4
SR.0	Yes	RESERVED			5

Notes

1. Check STS or SR.7 to determine block erase, program, or lock-bit configuration completion. SR.6-SR.0 are not driven while SR.7 = 0

2. If both SR.5 and SR.4 are "1" after a block erase or lock-bit configuration attempt, an improper command sequence was entered.

3. SR.3 does not provide a continuous programming voltage level indication. The WSM interrogates and indicates the programming voltage level only after Block Erase, Program, Set Block Lock-Bit, or Clear Block Lock-Bits command sequences.

4. SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bits only after Block Erase, Program, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set. Read the block lock configuration codes using the Read Identifier Codes command to determine block lock-bit status.

5. SR.0 is reserved for future use and should be masked when polling the status register.

Table 16 . Extended Status Register Definitions

Symbol	High Z When Busy?	Status	Definition "1"	Definition "0"	Notes
XSR.7	No	WRITE BUFFER STATUS	Write buffer available	Write buffer not available	1
XSR.6-XSR.0	Yes	RESERVED			2

Notes:

1. After a Buffer-Write command, XSR.7 = 1 indicates that a Write Buffer is available.

2. XSR.6-XSR.0 are reserved for future use and should be masked when polling the status register.

READ STATUS REGISTER COMMAND

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of $\overline{OE}$ or the first edge of CE0, CE1, CE2 that enables the device $\overline{OE}$ must be toggle to VIH or the device must be disable before further reads to update the status register latch. The Read Status Register command functions independently of the VPEN voltage.

CLEAR STATUS REGISTER COMMAND

The Erase Status, Program Status, Block Status bits and protect status are set to "1" by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

BLOCK ERASE COMMAND

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required (erase changes all block data to FFH).

Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). The CPU can detect block erase completion by analyzing the output of the STS pin or status register bit SR.7. Toggle $\overline{OE}$, CE0 , CE1 , or CE2 to update the status register. The CUI remains in read status register mode until a new command is issued. Also, reliable block erasure can only occur when VCC is valid and VPEN = VPENH .

BLOCK ERASE SUSPEND COMMAND

This command only has meaning while the WSM is executing Block erase operation, and therefore will only be responded to during Block erase operation. After this command has been executed, the WSM suspend the erase operations, and then return to Read Status Register mode. The WSM will set the Q6 bit to a "1". Once the WSM has reached the Suspend state, the WSM will set

the Q7 bit to a "1". In default mode, STS will also transition to VOH.

At this time, A read array/program command sequence can also be issued during erase suspend to read or program data in other blocks. During a program operation with block erase suspended, status register bit SR.7 will return to "0" and STS output (in default mode) will transition to VOL The WSM will continue to run, idling in the SUSPEND state, regardless of the state of all input control pins.

The only other valid commands while block erase is suspended are Read Query, Read Status Register, Clear Status Register, Configure, and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS (in default mode) will return to VOL. VPEN must remain at VPENH (the same VPEN level used for block erase) while block erase is suspended. Block erase cannot resume until program operations initiated during block erase suspend have completed.

WRITE TO BUFFER COMMAND

To program the device, a Write to Buffer command is issue first. A variable number of bytes, up to the buffer size, can be loaded into the buffer and written to the flash device. First, the Write to Buffer Setup command is issued along with the Block Address (see Figure , Write to Buffer Flowchart" on page). After the command is issued, the extended Status Register (XSR) can be read when $\overline{CE}$ is VIL. XSR.7 indicates if the Write Buffer is available.

If the buffer is available, the number of words/bytes to be program is written to the device. Next, the start address is given along with the write buffer data. Subsequent writes provide additional device addresses and data, depending on the count. After the last buffer data is given, a Write Confirm command must be issued. The WSM beginning copy the buffer data to the flash array.

If an error occurs while writing, the device will stop writing, and status register bit SR.4 will be set to a "1" to indicate a program failure. The internal WSM verify only detects errors for "1" that do not successfully program to "0" . If a program error is detected, the status register should be cleared. Any time SR.4 and/or SR.5 is set, the

device will not accept any more Write to Buffer commands. Reliable buffered writes can only occur when VCC is valid and VPEN = VPENH. Also, successful programming requires that the corresponding block lock-bit be reset.

BYTE/WORD PROGRAM COMMANDS

Byte/Word program is executed by a two-command sequence. The Byte/Word Program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation. The CPU can detect the completion of the program event by analyzing the STS pin or status register bit SR.7.

If a byte/word program is attempted while VPEN_V PENLK, status register bits SR.4 and SR.3 will be set to "1". Successful byte/word programs require that the corresponding block lock-bit be cleared. If a byte/ word program is attempted when the corresponding block lock-bit is set, SR.1 and SR.4 will be set to "1".

SUSPEND/RESUME COMMAND

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Block address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. When SR.7 = 1, SR.2 should also be set to "1", indicating that the device is in the program suspend mode. STS in level RY/$\overline{BY}$ mode will also transition to VOH.

At this time, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. The only other valid commands while programming is suspended are Read Query, Read Status Register, Clear Status Register, Configure, and Program Resume. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes. Status register bits SR.2 and SR.7 will automatically clear and STS in RY/$\overline{BY}$ mode will return to VOL.

Read Configuration

The device will support both asynchronous page mode and standard word/byte reads. No configuration is required. Status register and identifier only support standard word/byte single read operations.

Table 17. Read Configuration Register Definition

RM	R	R	R	R	R	R	R
16(A16)	15	14	13	12	11	10	9
R	R	R	R	R	R	R	R
8	7	6	5	4	3	2	1
				Notes			
RCR.16 = READ MODE (RM) 0 = Standard Word/Byte Reads Enabled (Default) 1 = Page-Mode Reads Enabled				Read mode configuration effects reads from the flash array. Status register, query, and identifier reads support standard word/byte read cycles.			
RCR.15-1= RESERVED FOR FUTURE ENHANCEMENTS (R)				These bits are reserved for future use. Set these bits to "0".			

Configuration Command

The Status (STS) pin can be configured to different states using the Configuration command. Once the STS pin has been configured, it remains in that configuration until another configuration command is issued or $\overline{RP}$ is asserted low. Initially, the STS pin defaults to RY/$\overline{BY}$ operation where RY/$\overline{BY}$ low indicates that the state machine is busy. RY/$\overline{BY}$ high indicates that the state machine is ready for a new operation or suspended. Table 19, "Configuration Coding Definitions" on page 28 displays the possible STS configurations.

To reconfigure the Status (STS) pin to other modes, the Configuration command is given followed by the desired configuration code. The three alternate configurations are all pulse mode for use as a system interrupt as described below. For these configurations, bit 0 controls Erase Complete interrupt pulse, and bit 1 controls Program Complete interrupt pulse. Supplying the 00h configuration code with the Configuration command resets the STS pin to the default RY/$\overline{BY}$ level mode. The possible configurations and their usage are described in Table 19, "Configuration Coding Definitions" on page 28. The Configuration command may only be given when the device is not busy or suspended. Check SR.7 for device status. An invalid configuration code will result in both status register bits SR.4 and SR.5 being set to "1"." When configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns.

Table 18. Configuration Coding Definitions

Reserved		Pulse on Program Complete (1)	Pulse on Erase Compete (1)
bits7-2		**bit 1**	**bit 0**

Q7 - Q2 = Reserved
Q1 - Q0 = STS Pin Configuration Codes
00 = default, level mode RY/BY
(device ready) indication
01 = pulse on Erase complete
10 = pulse on Program complete
11 = pulse on Erase or Program Complete
Configuration Codes 01b, 10b, and 11b are all pulse mode such that the STS pin pulses low then high when the operation indicated by the given configuration is completed.
Configuration Command Sequences for STS pin configuration (masking bits Q7- Q 2 to 00h) are as follows:
Default RY/BY level mode: B8h, 00h
ER INT (Erase Interrupt): B8h, 01h
Pulse-on-Erase Complete
PR INT (Program Interrupt): B8h, 02h
Pulse-on-Program Complete
ER/PR INT (Erase or Program Interrupt): B8h, 03h
Pulse-on-Erase or Program Complete

Q7 - Q2 are reserved for future use.
default (Q1-Q 0 = 00) RY/BY, level mode
- used to control HOLD to a memory controller to prevent accessing a flash memory subsystem while any flash device's WSM is busy.
configuration 01 ER INT, pulse mode
- used to generate a system interrupt pulse when any flash device in an array has completed a Block Erase. Helpful for reformatting blocks after file system free space reclamation or "cleanup"
configuration 10 PR INT, pulse mode
-used to generate a system interrupt pulse when any flash device in an array has complete a Program operation. Provides highest performance for servicing continuous buffer write operations.
configuration 11 ER/PR INT, pulse mode
-used to generate system interrupts to trigger servicing of flash arrays when either erase or program operations are completed when a common interrupt service routine is desired.

NOTE: 1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns.

Set Block Lock-Bit Commands

This device provided the block lock-bits, to lock and unlock the individual block. To set the block lock-bit, the two cycle Set Block Lock-Bit command is requested. This command is invalid while the WSM is running or the device is suspended. Writing the set block lock-bit command of 60H followed by confirm command and an appropriate block address. After the command is written, the device automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing the STS pin output or status register bit SR.7. Also, reliable operations occur only when VCC and VPEN are valid. With VPEN _VPENLK , lock-bit contents are protected against alteration.

Clear Block Lock-Bits Command

All set block lock-bits can clear by the Clear Block Lock-Bits command. This command is invalid while the WSM is running or the device is suspended. To Clear the block lock-bits, two cycle command is requested . The device automatically outputs status register data when read. The CPU can detect completion of the clear block lock-bits event by analyzing the STS pin output or status register bit SR.7. If a clear block lock-bits operation is aborted due to V PEN or V CC transitioning out of valid range, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

Protection Register Program Command

The device offer a 128-bit protection register to increase the security of a system design. The 128-bits protection register are divided into two 64-bit segments. One is programmed in the factory with a unique 64-bit number, which is unchangeable. The other one is left blank for customer designers to program as desired. Once the customer segment is programmed, it can be locked to prevent reprogramming.

Reading the Protection Register

The protection register is read in the identification read mode. The device is switched to this mode by writing the Read Identifier command 90H. Once in this mode, read cycles from addresses retrieve the specified informa-tion. To return to read array mode, write the Read Array command (FFH).

Programming the Protection Register

The protection register bits are programmed using the two-cycle Protection Program command. The 64-bit number is programmed 16 bits at a time for word-wide parts and eight bits at a time for byte-wide parts. First write the Protection Program Setup command, C0H. The next write to the device will latch in address and data and program the specified location.

Any attempt to address Protection Program commands outside the defined protection register address space will result in a status register error. Attempting to program a locked protection register segment will result in a status register error.

Locking the Protection Register

The user-programmable segment of the protection register is lockable by programming Bit 1 of the PR-LOCK location to 0. Bit 0 of this location is programmed to 0 at the Intel factory to protect the unique device number. Bit 1 is set using the Protection Program command to program "FFFD" to the PR-LOCK location. After these bits have been programmed, no further changes can be made to the values stored in the protection register. Protection Program commands to a locked section will result in a status register error. Protection register lockout state is not reversible.

Figure 3. Protection Register Memory Map

Word Address

A[23 -1]: 128 Mbit
A[22 -1]: 64 Mbit
A[21 -1]: 32 Mbit

88H

4 Words
User Programmed

85H
84H

4 Words
Factory Programmed

81H

1 Word Lock

80H
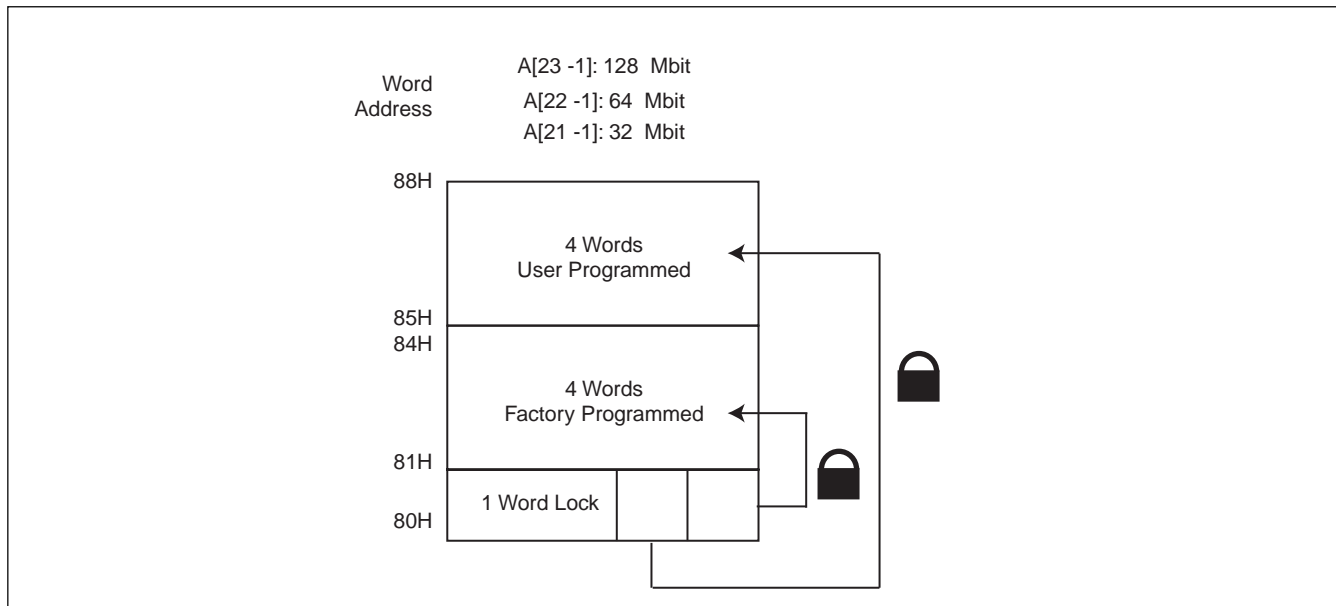
NOTE: A 0 is not used in x16 mode when accessing the protection register map (See Table 20 for x16 addressing). For x8 mode A 0 is used (See Table 21 for x8 addressing).

Table 20. Word-Wide Protection Register Addressing

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
LOCK	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	1	0
2	Factory	1	0	0	0	0	0	1	1
3	Factory	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

NOTE: 1. All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., A23-A9 = 0.

Table 21. Byte-Wide Protection Register Addressing

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
LOCK	Both	1	0	0	0	0	0	0	0
LOCK	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	0	1
2	Factory	1	0	0	0	0	0	1	0
3	Factory	1	0	0	0	0	0	1	0
4	Factory	1	0	0	0	0	0	1	1
5	Factory	1	0	0	0	0	0	1	1
6	Factory	1	0	0	0	0	1	0	0
7	Factory	1	0	0	0	0	1	0	0
8	User	1	0	0	0	0	1	0	1
9	User	1	0	0	0	0	1	0	1
A	User	1	0	0	0	0	1	1	0
B	User	1	0	0	0	0	1	1	0
C	User	1	0	0	0	0	1	1	1
D	User	1	0	0	0	0	1	1	1
E	User	1	0	0	0	1	0	0	0
F	User	1	0	0	0	1	0	0	0

NOTE: 1. All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., A23-A9 = 0.
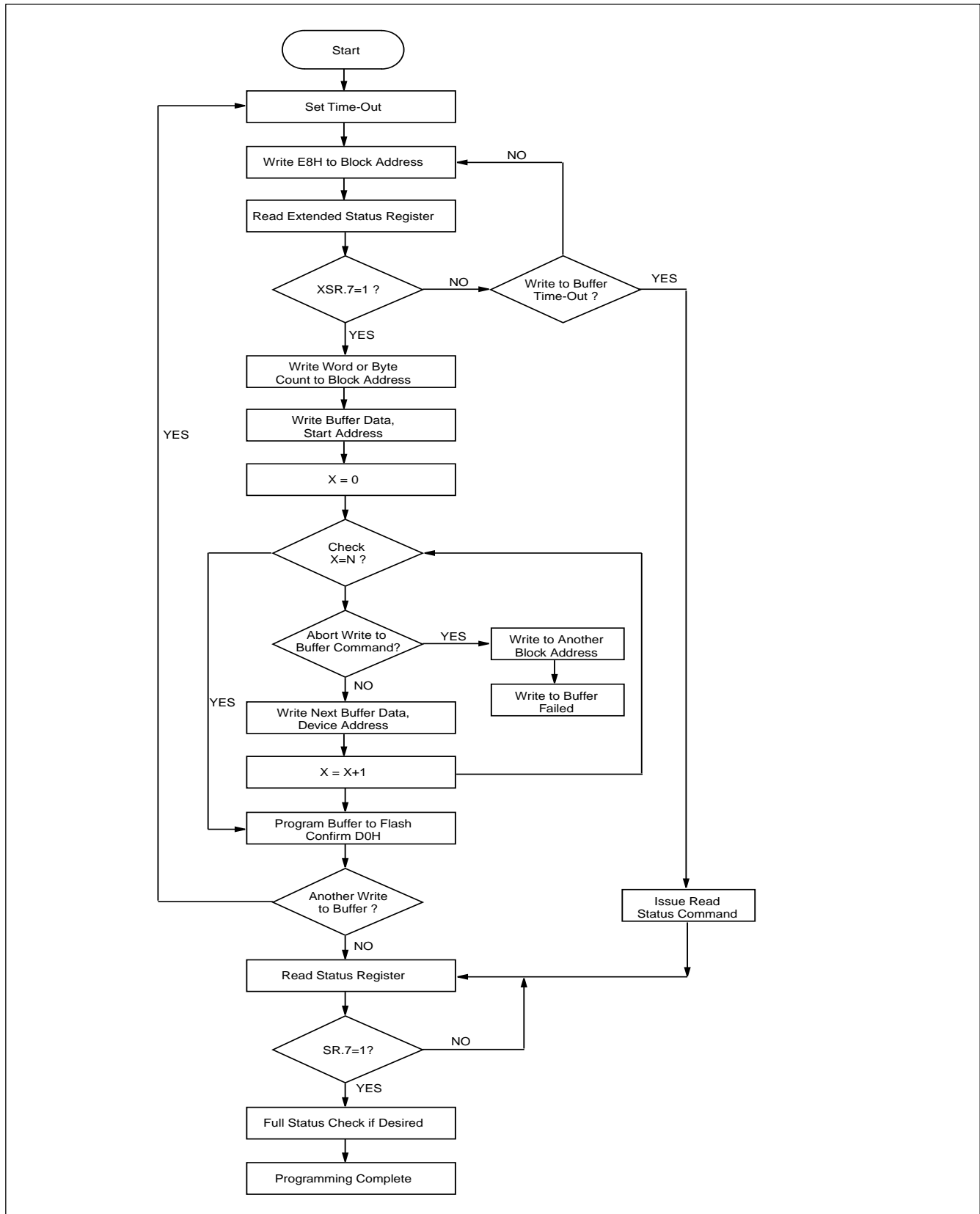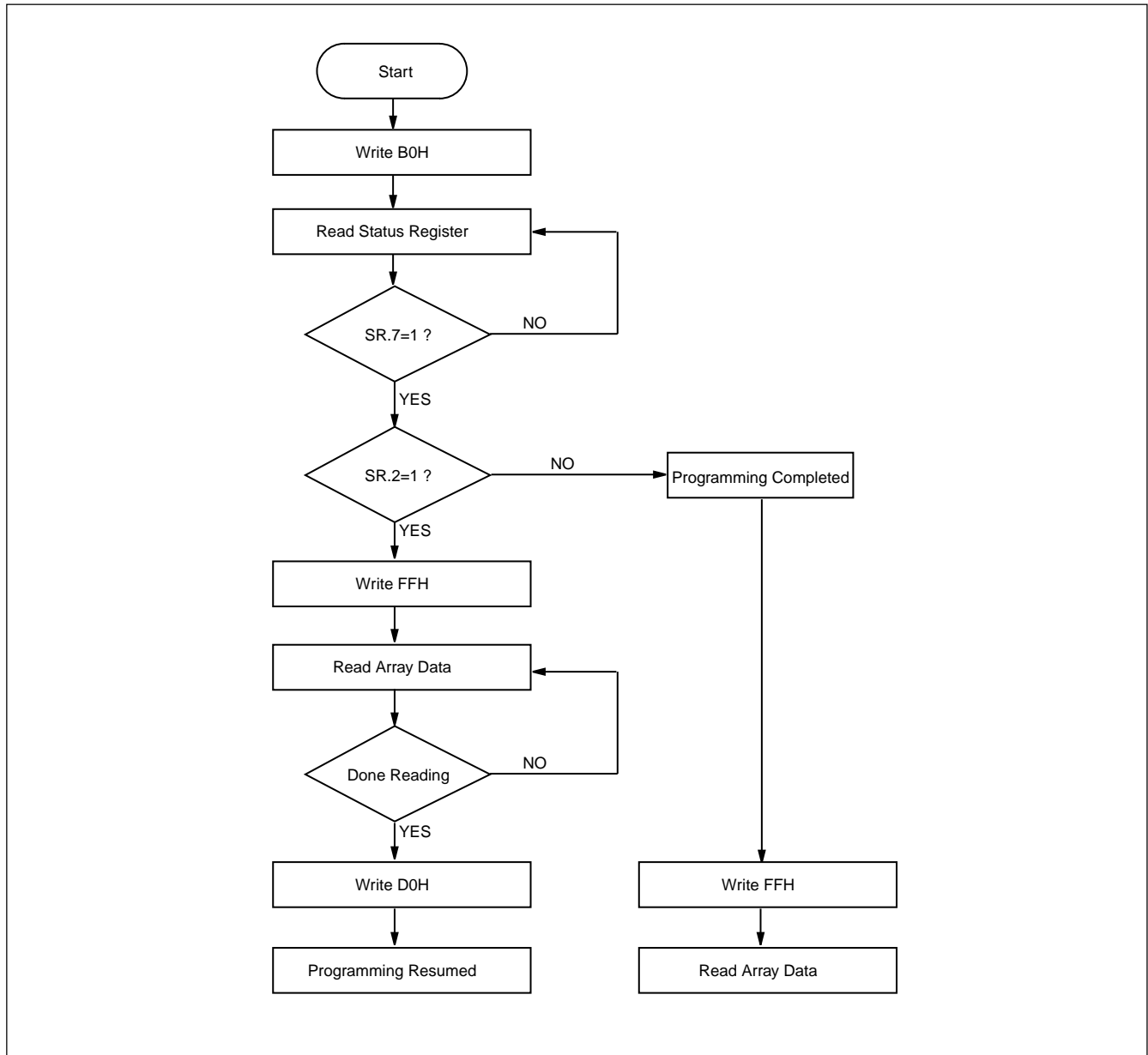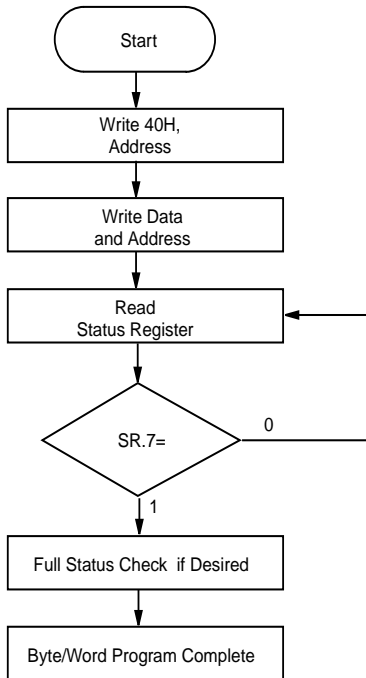
Figure 4. Write to Buffer Flowchart

Figure 5. Program Suspend/Resume Flowchart

Figure 6. Byte/Word Programming Flowchart

FULL STATUS CHECK PROCEDURE

Bus Operation	Command	Comments
Write	Setup Byte/ Word Program	Data=40H Addr=Location to Be Programmed
Write	Byte/Word Program	Data=Data to Be Programmed Addr=Location to Be Programmed
Read (Note 1)		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

1. Toggling $\overline{OE}$ (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR full status check can be done after each program operation, or after a sequence of programming operations.

Write FFH after the last program operation to place device in read array mode.
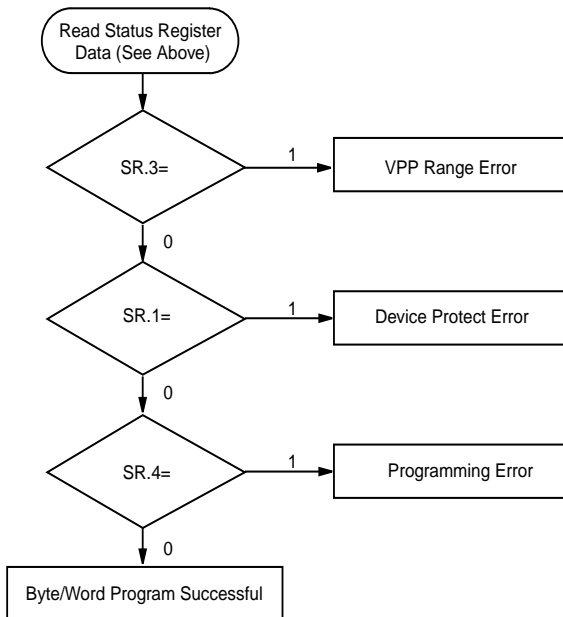
Bus Operation	Command	Comments
Standby		Check SR.3 1=Programming to Voltage Error Detect
Standby		Check SR.1 1=Device Protect Detect $\overline{RP}$=VIH, Block Lock-Bit is Set Only required for systems
Standby		Check SR.4 1=Programming Error

Toggling $\overline{OE}$ (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.

SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register Command in cases where multiple location are programmed before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 7. Block Erase Flowchart
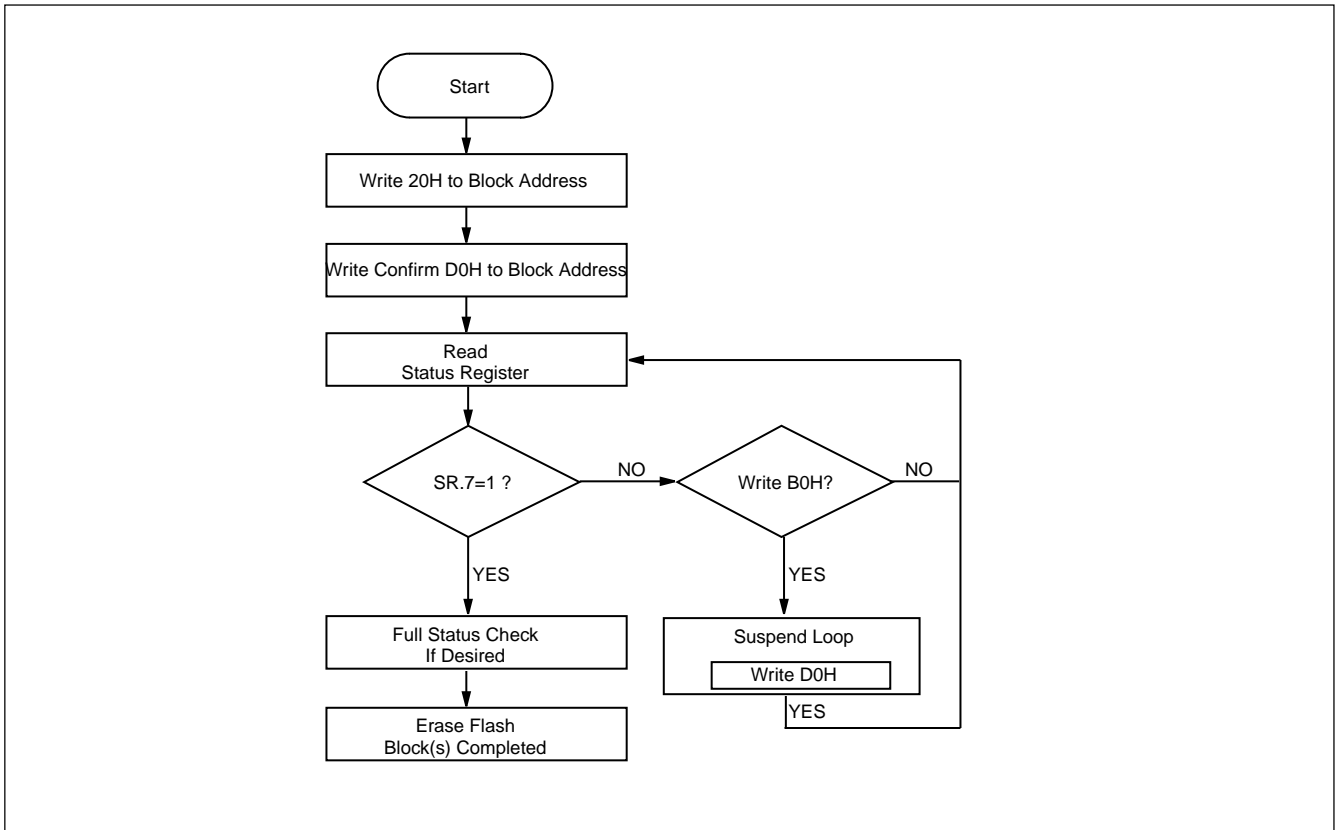
Figure 8. Block Erase Suspend/Resume Flowchart
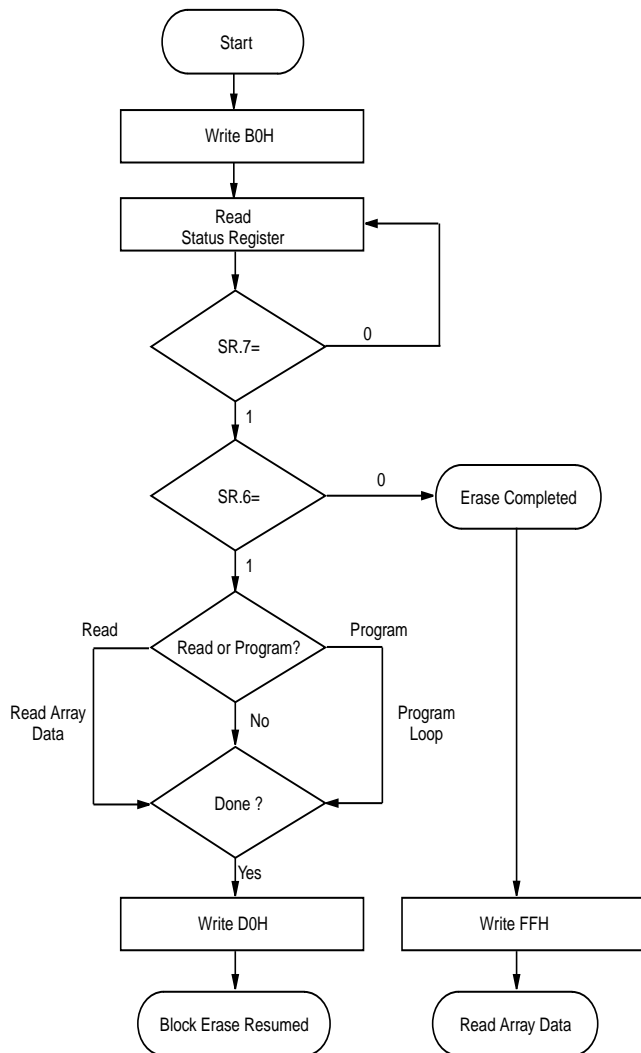
Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspend 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 9. Set Block Lock-Bit Flowchart
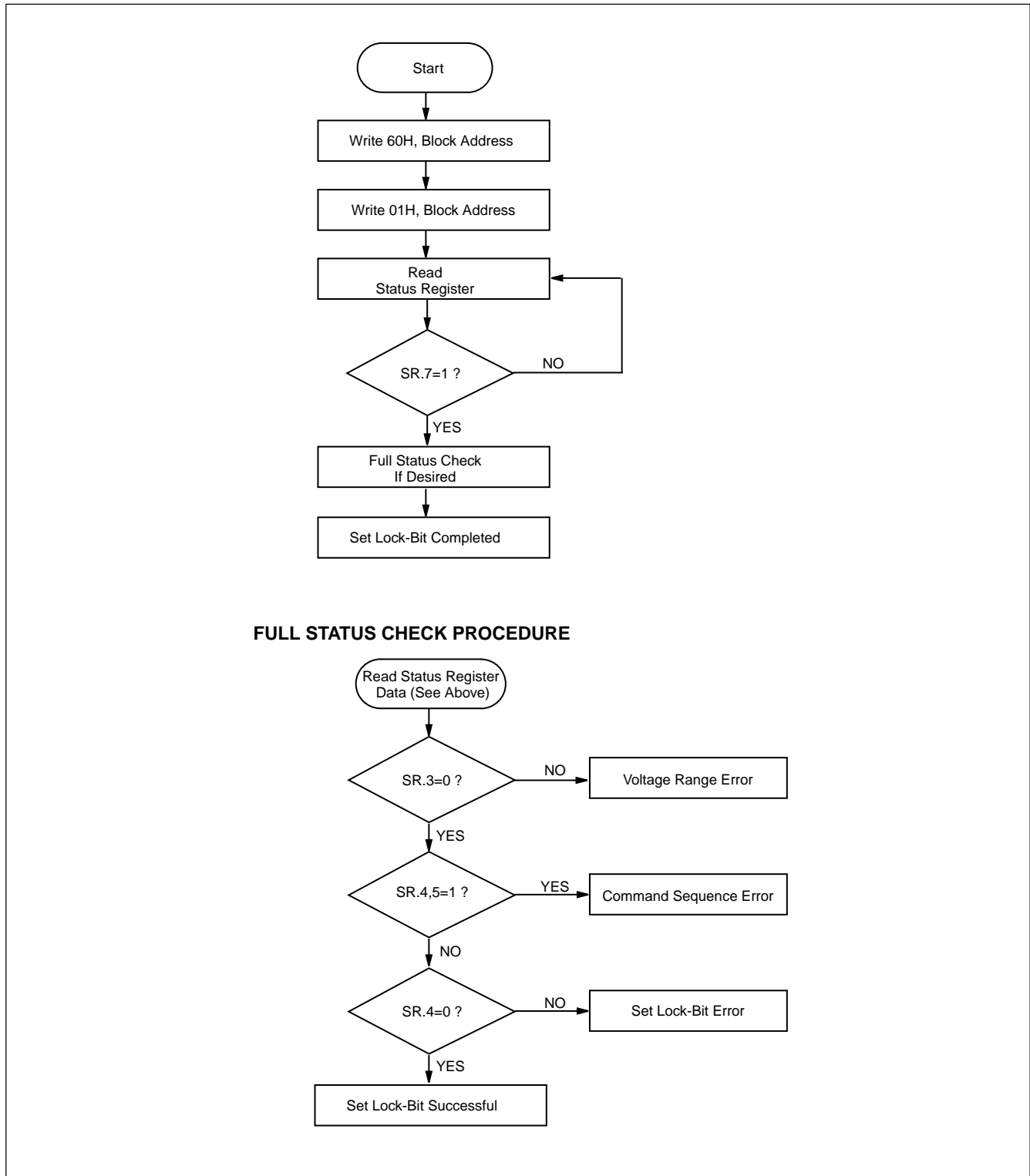
Figure 10. Clear Lock-Bit Flowchart

FULL STATUS CHECK PROCEDURE
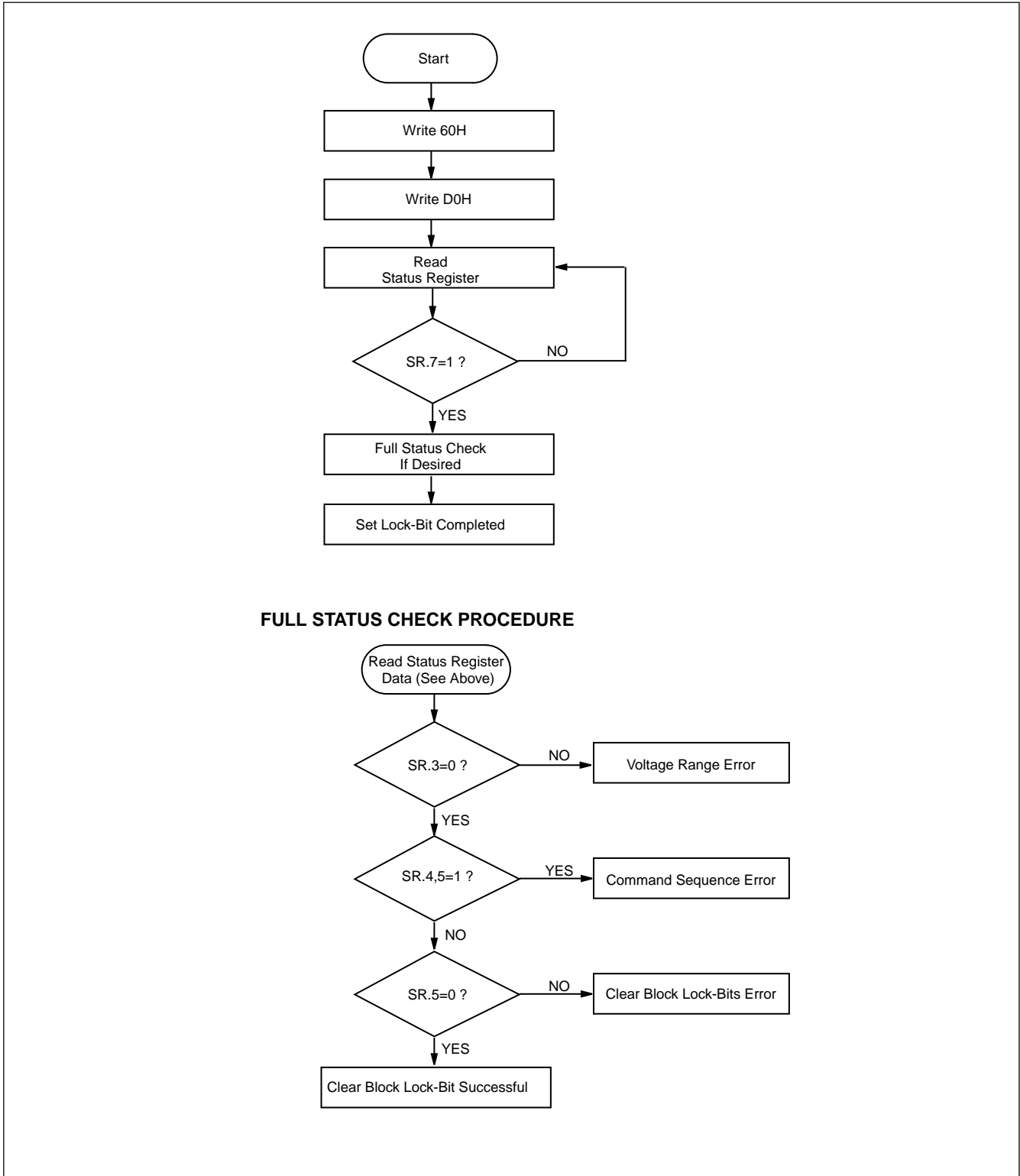
Figure 11. Protection Register Programming Flowchart
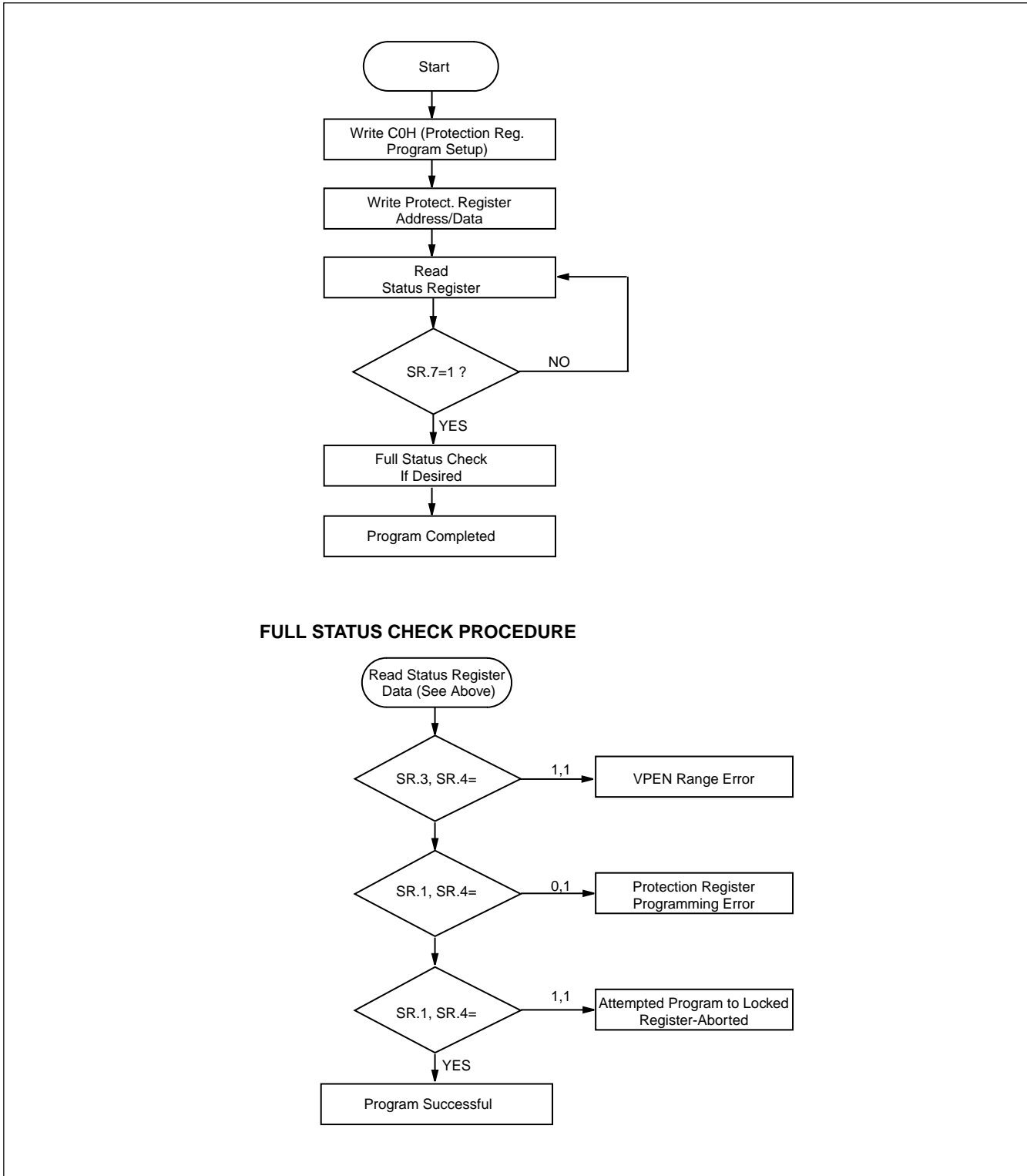
ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

   VCC (Note 1) . . . . -0.5 V to +4.0 V

   A9, $\overline{OE}$, and

   $\overline{RESET}$ or RESET(Note 2) . . . .-0.5 V to +12.5 V

   All other pins (Note 1) . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20 ns. See Figure 7.

2. Minimum DC input voltage on pins A9, $\overline{OE}$, and RESET or $\overline{RESET}$ is -0.5 V. During voltage transitions, A9, $\overline{OE}$, and RESET or $\overline{RESET}$ may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Rat-ings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those in-dicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maxi-mum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices

Ambient Temperature (T$_A$). . . . . 0°C to +70°C

Vcc Supply Voltages

Vcc for full voltage range. . . . . +2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

Symbol	Parameter	Notes	Typ	Max	Unit	Test Conditions
ILI	Input and V PEN Load Current	1		±1	uA	VCC = VCC Max; VCCQ = VCCQ Max VIN = VCCQ or GND
ILO	Output Leakage Current	1		±10	uA	VCC = VCC Max; VCCQ = VCCQ Max VIN = VCCQ or GND
ICC1	VCC Standby Current	1,2,3	25	80	uA	CMOS Inputs, VCC = VCC Max, Device is disabled (see table 2) $\overline{RESET}$=VCCQ±0.2V or RESET=VIL
			0.71	2	mA	TTL Inputs, VCC=VCC max, Device is disable (see table 2), $\overline{RESET}$=VIH or RESET=VIL
ICC2	VCC Power-Down Current		2	5	uA	$\overline{RESET}$=GND±0.2V, or RESET=VIH IOUT(STS)=0mA
ICC3	VCC Page Mode Read Current	1,3	15	20	mA	CMOS Inputs, VCC=VCC Max, VCCQ=VCCQ Max Device is enabled (see Table 2) f=5MHz, IOUT=0mA
			24	29	mA	CMOS Inputs, VCC=VCC Max, VCCQ=VCCQ Max Device is enabled (see Table 2) f=33MHz, IOUT=0mA
ICC4	VCC Word Mode Read Current	1,3	40	50	mA	CMOS Inputs, VCC=VCC Max, VCCQ=VCCQ Max Device is enabled (see Table 2) f=5MHz, IOUT=0MA
ICC5	VCC Program or Set Lock-Bit Current	1,4	35	60	mA	CMOS Inputs, VPEN=VCC
			40	70	mA	TTL Inputs, VPEN=VCC
ICC6	VCC Block Erase or Clear Block Lock-Bits Current	1,4	35	70	mA	CMOS Inputs, VPEN=VCC
			40	80	mA	TTL Inputs, VPEN=VCC
ICC7	VCC Program Suspend or Block Erase Suspend Current	1,5		10	mA	Device is disabled (see Table 2)

DC Characteristics, Continued

Symbol	Parameter	Notes	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	4	-0.5	0.8	V	
VIH	Input High Voltage	4	2.0	VCCQ+0.5	V	
VOL	Output Low Voltage	2,4		0.4	V	VCCQ=VCCQ2/3 Min IOL=2mA
				0.2	V	VCCQ=VCCQ2/3 Min IOL=100uA
VOH	Output High Voltage	2,4	0.85 x VCCQ		V	VCCQ=VCCQ Min IOH=-2.5mA
			VCCQ-0.2		V	VCCQ=VCCQ Min IOH=-100uA
VPENLK	VPEN Lockout during Program, Erase and Lock-Bit Operations	4,6,7		2.2	V	
VPENH	VPEN during Block Erase, Program, or Lock-Bit Operations	6,7	2.7	3.6	V	
VLKO	VCC Lockout Voltage	8	2.2		V	

NOTES:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds).

2. Includes STS.

3. CMOS inputs are either VCC ± 0.2 V or GND ± 0.2 V. TTL inputs are either VIL or VIH .

4. Sampled, not 100% tested.

5. ICCWS and ICCES are specified with the device de-selected. If the device is read or written while in erase suspend mode, the device's current draw is I CCR or I CCW .

6. Block erases, programming, and lock-bit configurations are inhibited when V PEN ˆ V PENLK , and not guaranteed in the range between VPENLK (max) and VPENH (min), and above VPENH (max).

7. Typically, VPEN is connected to VCC (2.7 V - 3.6 V).

8. Block erases, programming, and lock-bit configurations are inhibited when VCC < VLKO , and not guaranteed in the range between VLKO (min) and VCC (min), and above VCC (max).

Figure 12. Transient Input/Output Reference Waveform for VCCQ=3.0V-3.6V or VCCQ=2.7V-3.6 V

VCCQ

Input VCCQ/2 — — — — — TEST POINTS — — — — VCCQ/2 Output

0.0

Note:AC test inputs are driven at VCCQ for a Logic "1" and 0.0V for a Logic "0".
Input timing being, and output timing ends, at VCCQ/2V (50% of VCCQ).
Input rise and fall times (10% tp 90%)<5ns.
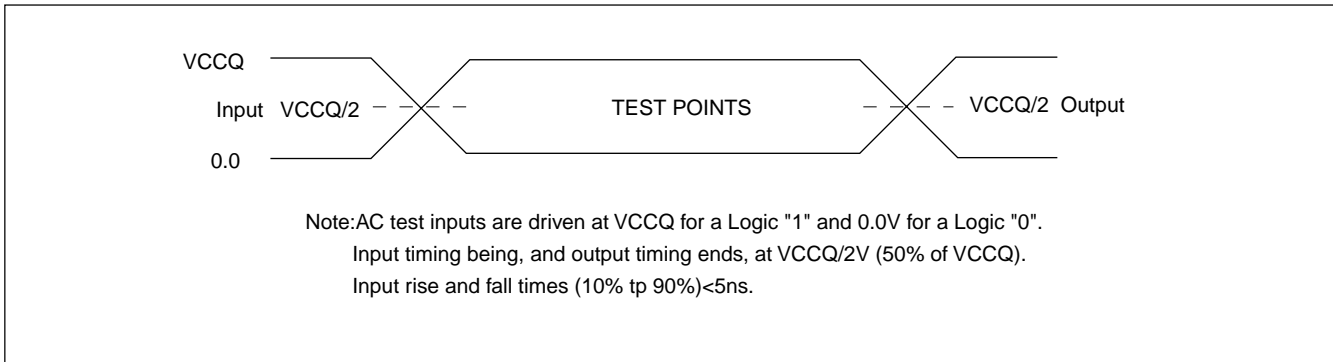
Figure 13. Transient Equivalent Testing Load Circuit

1.3V

1N914

RL=3.3K ohm

Device
Under Test

Out

CL
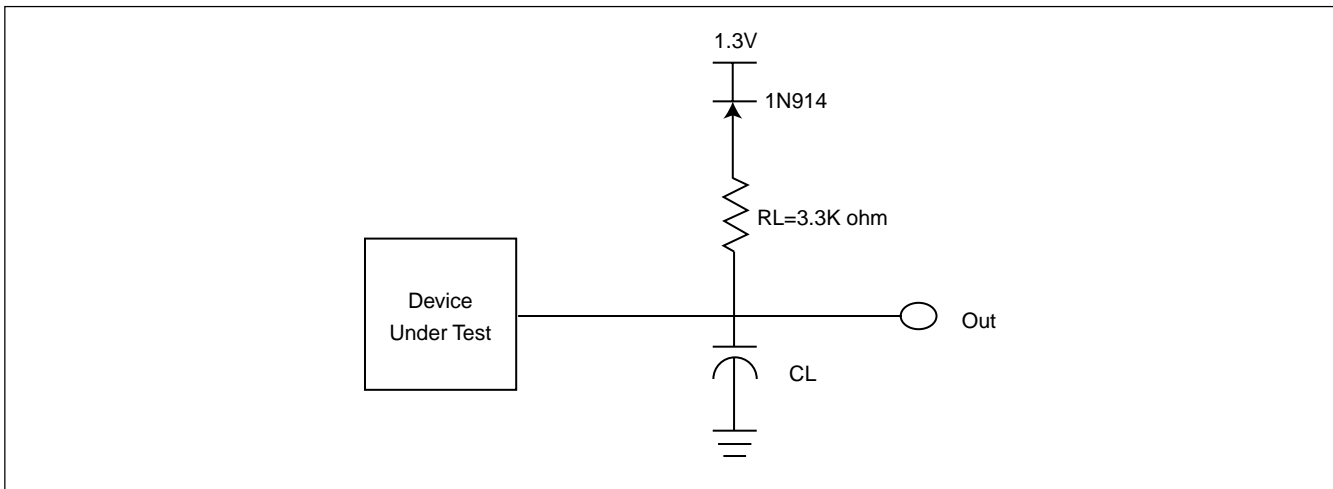
NOTE: CL Includes Jig Capacitance

Test Configuration	C L (pF)
VCCQ = VCC = 3.0 V-3.6 V	30
VCCQ = VCC = 2.7 V-3.6 V	30

AC Characteristics --Read-Only Operations (1,2)

Versions			VCC	3.0V-3.6V(3)		2.7V-3.6V(3)	
(All units in ns unless otherwise noted)			VCCQ	3.0V-3.6V(3)		2.7V-3.6V(3)	
Sym	Parameter		Notes	Min	Max	Min	Max
tAVAV	Read/Write Cycle Time	32M		120		120	
		64M	7	120		120	
		128M		150		150	
tAVQV	Address to Output Delay	32M			120		120
		64M			120		120
		128M			150		150
tELQV	CEX to Output Delay	32M	2		120		120
		64M	2, 7		120		120
		128M	2		150		150
tGLQV	$\overline{OE}$ to Non-Array Output Delay		2, 4		50		50
tPHQV	$\overline{RESET}$ High to Output Delay	32M			180		180
		64M			180		180
		128M	8		210		210
tELQX	CEX to Output in Low Z		5	0		0	
tGLQX	$\overline{OE}$ to Output in Low Z		5	0		0	
tEHQZ	CEX High to Output in High Z		5		35		35
tGHQZ	$\overline{OE}$ High to Output in High Z		5		15		15
tOH	Output Hold from Address, CEX, or $\overline{OE}$ Change, Whichever Occurs First		5	0		0	
tELFL/tELFH	CEX Low to $\overline{BYTE}$ High or Low		5		10		10
tFLQV/tFHQV	$\overline{BYTE}$ to Output Delay				1000		1000
tFLQZ	$\overline{BYTE}$ to Output in High Z		5		1000		1000
tEHEL	CEx High to CEx Low		5	0		0	
tAPA	Page Address Access Time		5, 6		25		30
tGLQV	$\overline{OE}$ to Array Output Delay		4		25		30

NOTES:CEX low is defined as the first edge of CE0 , CE1 , or CE2 that enables the device. CEX high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 2).

1. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.

2. $\overline{OE}$ may be delayed up to t ELQV -t GLQV after the first edge of CE0, CE1, or CE2 that enables the device (see Table 2) without impact on t ELQV .

3. See Figures 14-16, Transient Input/Output Reference Waveform for VCCQ = 3.0V - 3.6V or VCCQ = 2.7V-3.6 V, and Transient Equivalent Testing Load Circuit for testing characteristics.

4. When reading the flash array a faster tGLQV (R16) applies. Non-array reads refer to status register reads, query reads, or device identifier reads.

5. Sampled, not 100% tested.

6. For devices configured to standard word/byte read mode, R15 (tAPA) will equal R2 (tAVQV).

7. The performance of 64Mb depends on 120ns speed grade or 150ns speed grades.

8. tPHQV is RESET low to output delay for 48-TSOP & 48-RTSOP package types.

Figure 14. AC Waveform for Both Page-Mode and Standard Word/Byte Read Operations (for 56-TSOP & 64-CSP)
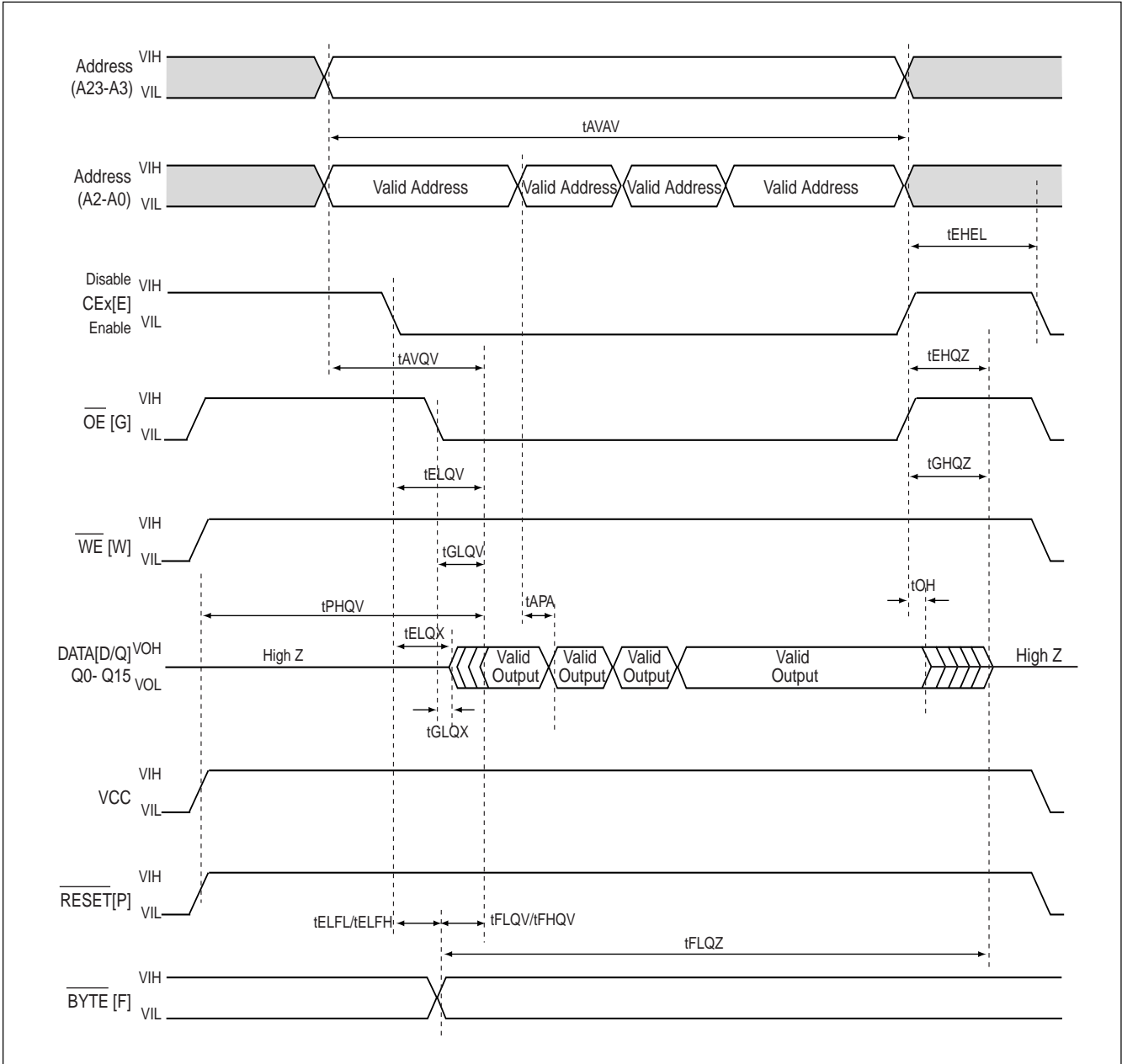
NOTE:

1. CE_X low is defined as the first edge of CE0 , CE1 , or CE2 that enables the device. CE_X high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 2).
2. For standard word/byte read operations, tAPA will equal tAVQV.
3. When reading the flash array a faster tGLQV applies. Non-array reads refer to status register reads, query reads, or device identifier reads.

Figure 15. AC Waveform for Both Page-Mode and Standard Word Read Operations (for 48-TSOP & 48-RTSOP)
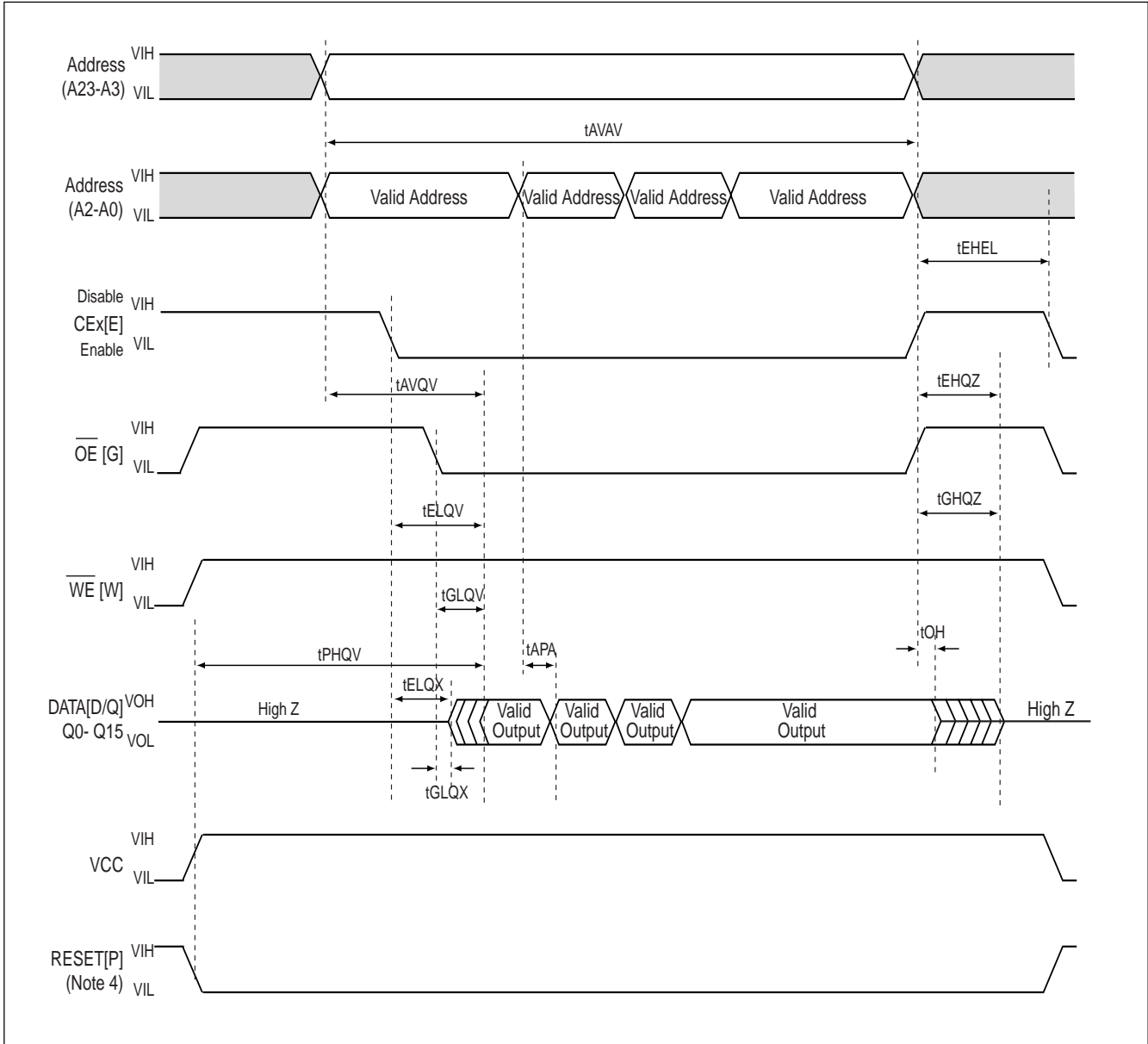
NOTE:
1. CE_x low is defined as the first edge of CE0 , CE1 , or CE2 that enables the device. CE_x high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 2).
2. For standard word/byte read operations, tAPA will equal tAVQV.
3. When reading the flash array a faster tGLQV applies. Non-array reads refer to status register reads, query reads, or device identifier reads.
4. For 48-TSOP & 48-RTSOP the RESET pin is high enable.

AC Characteristics--Write Operations (1,2)

Versions			Valid for All Speeds		Unit
Symbol	Parameter	Notes	Min	Max	
tPHWL (tPHEL)	RESET High Recovery to WE(CEX) Going Low	3,10	2		us
tELWL (tWLEL)	CEX (WE) Low to WE(CEX) Going Low	4	0		ns
tWP	Write Pulse Width	4	70		ns
tDVWH (tDVEH)	Data Setup to WE(CEX) Going High	5	50		ns
tAVWH (tAVEH)	Address Setup to WE(CEX) Going High	5	55		ns
tWHEH (tEHWH)	CEX (WE) Hold from WE(CEX) High		0		ns
tWHDX (tEHDX)	Data Hold from WE(CEX) High		0		ns
tWHAX (tEHAX)	Address Hold from WE(CEX) High		0		ns
tWPH	Write Pulse Width High	6	30		ns
tVPWH (tVPEH)	VPEN Setup to WE(CEX) Going High	3	0		ns
tWHGL (tEHGL)	Write Recovery before Read	7	35		ns
tWHRL (tEHRL)	WE(CEX) High to STS Going Low	8		500	ns
tQVVL	VPEN Hold from Valid SRD, STS Going High	3,8,9	0		ns
tWHQV5 (tEHQV5)	Set Lock-Bit Time	4,9	64	75/85	us
tWHQV6 (tEHQV6)	Clear Block Lock-Bits Time	4	0.5	0.70	sec
tWHRH1 (tEHRH1)	Program Suspend Latency Time to Read	9	25	75/90	us
tWHRH (tEHRH)	Erase Suspend Latency Time to Read	9	26	35/40	us

NOTES:

CEX low is defined as the first edge of CE0, CE1, or CE2 that enables the device. CEX high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 2).

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics-Read-Only Operations.
2. A write operation can be initiated and terminated with either CE X or WE.
3. Sampled, not 100% tested.
4. Write pulse width (tWP) is defined from CEX or WE going low (whichever goes low last) to CEX or WE going high (whichever goes high first). Hence, tWP = tWLWH = tELEH = tWLEH = tELWH.
5. Refer to Table 4 for valid A IN and D IN for block erase, program, or lock-bit configuration.
6. Write pulse width high (t WPH) is defined from CEX or WE going high (whichever goes high first) to CEX or WE going low (whichever goes low first). Hence, tWPH = tWHWL = tEHEL = tWHEL = tEHWL .
7. For array access, tAVQV is required in addition to tWHGL for any accesses after a write.
8. STS timings are based on STS configured in its RY/BY default mode.
9. VPEN should be held at VPENH until determination of block erase, program, or lock-bit configuration success (SR.1/3/4/5=0).
10. For 48-TSOP & 48-RTSOP, the RESET pin is high enable.

Figure 16. AC Waveform for Write Operations (for 56-TSOP & 64-CSP)

NOTES:
1. CEX low is defined as the first edge of CE0 , CE1 , or CE2 that enables the device. CEX high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 2).

STS is shown in its default mode (RY/$\overline{BY}$).

a. VCC power-up and standby.

b. Write block erase, write buffer, or program setup.

c. Write block erase or write buffer confirm, or valid address and data.

d. Automated erase delay.

e. Read status register or query data.

f. Write Read Array command.

Figure 17. AC Waveform for Write Operations (for 48-TSOP & 48-RSOP)

NOTES:
1. CEX low is defined as the first edge of CE0 , CE1 , or CE2 that enables the device. CEX high is defined at the first edge of CE0, CE1, or CE2 that disables the device (see Table 2).
   STS is shown in its default mode (RY/$\overline{BY}$).
   a. VCC power-up and standby.
   b. Write block erase, write buffer, or program setup.
   c. Write block erase or write buffer confirm, or valid address and data.
   d. Automated erase delay.
   e. Read status register or query data.
   f. Write Read Array command.
2. For 48-TSOP & 48-RTSOP, the RESET pin is high enable.

Figure 18. AC Waveform for Reset Operation (for 56-TSOP & 64-CSP)
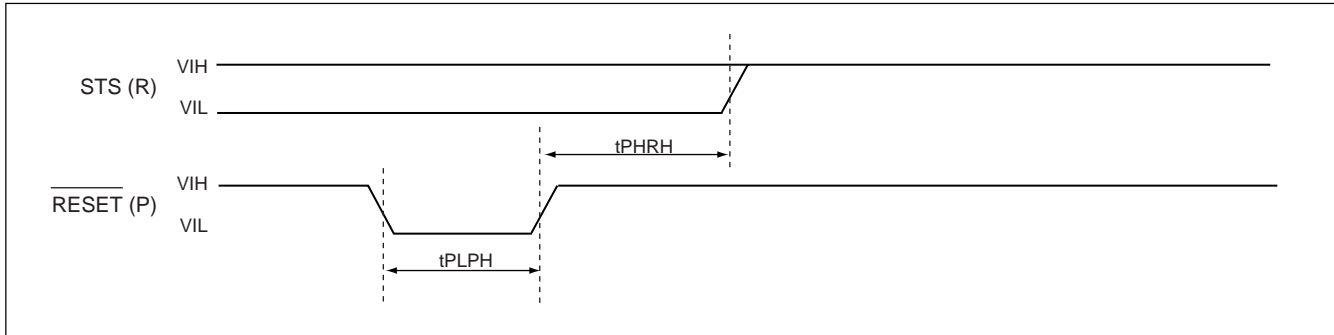
NOTE:
1. STS is shown in its default mode (RY/BY).

Figure 19. AC Waveform for Reset Operation (for 48-TSOP & 48-RTSOP)
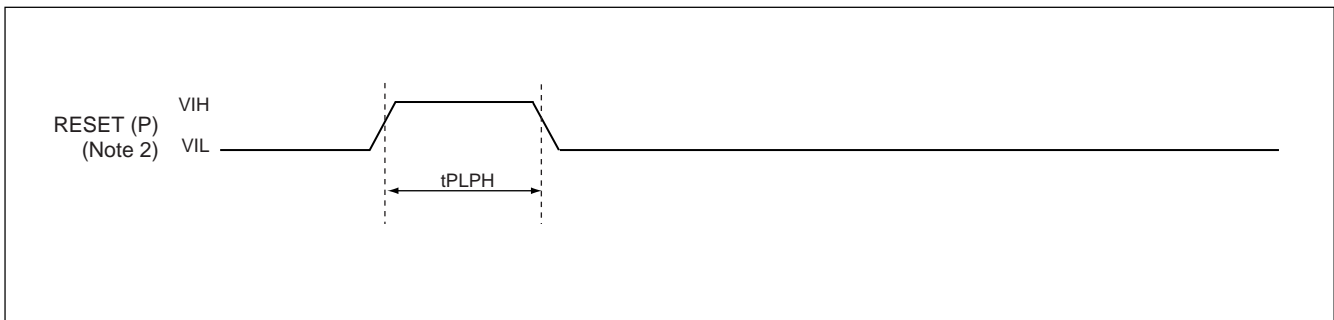
NOTE:
1. STS is shown in its default mode (RY/BY).
2. For 48-TSOP & 48-RTSOP, the RESET pin is high enable.

Reset Specifications (1)

Sym	Parameter	Notes	Min	Max	Unit
tPLPH	RESET Pulse Low Time	2	35		us
	(If RESET is tied to VCC , this specification is not applicable)				
	(for 48-TSOP & 48-RSTOP, the tPLPH indicates the RESET				
	Pulse High Time)				
tPHRH	RESET High to Reset during Block Erase, Program, or	3		2	us
	Lock-Bit Configuration				

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. If RESET is asserted while a block erase, program, or lock-bit configuration operation is not executing then the minimum required RESET Pulse Low Time is 100ns.
3. A reset time, tPHQV, is required from the latter of STS (in RY/BY mode) or RESET going high until outputs are valid.

ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER		MIN.	TYP.(2)	MAX.	UNITS
			LIMITS		
Block Erase Time			2.0	15.0	sec
Write Buffer Byte Program Time (Time to Program 32 bytes/16 words)			218	654	us
Byte Program Time (Using Word/Byte Program Command)			210	630	us
Block Program Time (Using Write to Buffer Command)			0.8	2.4	sec
Block Erase/Program Cycles	C1	10			Cycles
	C2	100			
	C3	1,000			
	C4	10,000			

Note: 1. Not 100% Tested, Excludes external system level over head.
2. Typical values measured at 25°C, 3.3V. Additionally programming typically assume checkerboard pattern.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

CAPACITANCE   TA=0°C to 70°C, VCC=2.7V~3.6V

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN	Input Capacitance	VIN=0	6	8	pF
COUT	Output Capacitance	VOUT=0	8	12	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA=25°C, f=1.0MHz

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150	10	Years
	125	20	Years

ORDERING INFORMATION

PLASTIC PACKAGE

Part NO.	Access Time (ns)	Package type	Cycles
MX28F128J3TBC-15C1	150/25	48-TSOP	10
MX28F128J3RBC-15C1	150/25	48-RTSOP	10
MX28F128J3TC-15C3	150/25	56-TSOP	1,000
MX28F128J3TBC-15C3	150/25	48-TSOP	1,000
MX28F128J3RBC-15C3	150/25	48-RTSOP	1,000
MX28F128J3XCC-15C3	150/25	64-CSP	1,000
MX28F128J3TC-15C4	150/25	56-TSOP	10,000
MX28F128J3TBC-15C4	150/25	48-TSOP	10,000
MX28F128J3RBC-15C4	150/25	48-RTSOP	10,000
MX28F128J3XCC-15C1	150/25	64-CSP	10
MX28F128J3XCC-15C4	150/25	64-CSP	10,000
MX28F640J3TC-12C3	120/25	56-TSOP	1,000
MX28F640J3IAC-12C3	120/25	48-FCCSP	1,000
MX28F640J3XCC-12C3	120/25	64-CSP	1,000
MX28F640J3TC-15C4	150/25	56-TSOP	10,000
MX28F640J3IAC-15C4	150/25	48-FCCSP	10,000
MX28F640J3XCC-15C4	150/25	64-CSP	10,000
MX28F320J3TC-12C3	120/25	56-TSOP	1,000
MX28F320J3IAC-12C3	120/25	48-FCCSP	1,000
MX28F320J3XCC-12C3	120/25	64-CSP	1,000
MX28F320J3TC-12C4	120/25	56-TSOP	10,000
MX28F320J3IAC-12C4	120/25	48-FCCSP	10,000
MX28F320J3XCC-12C4	120/25	64-CSP	10,000

PACKAGE INFORMATION

48-Ball Flip Chip CSP
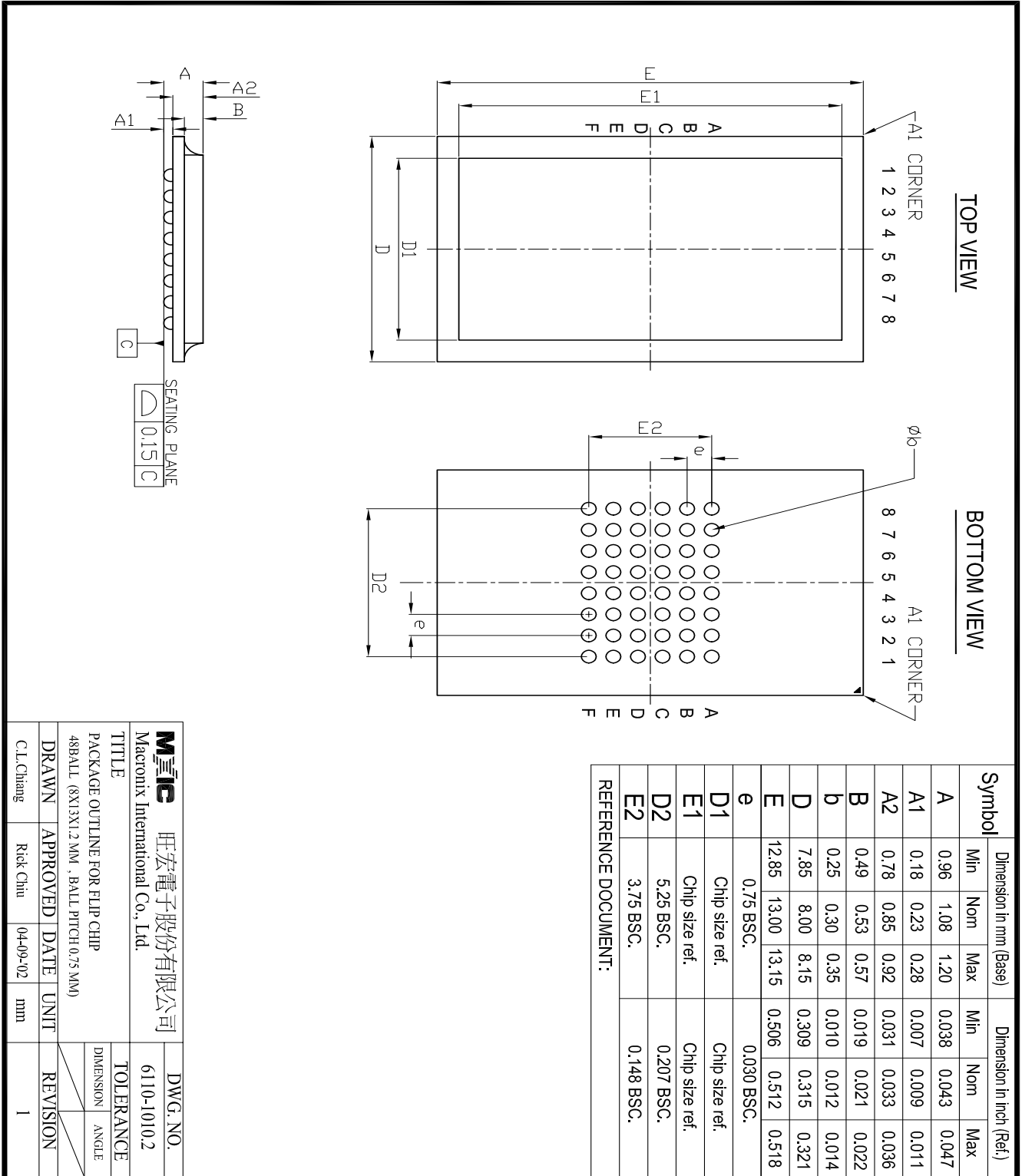
Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	0.96	1.08	1.20	0.038	0.043	0.047
A1	0.18	0.23	0.28	0.007	0.009	0.011
A2	0.78	0.85	0.92	0.031	0.033	0.036
B	0.49	0.53	0.57	0.019	0.021	0.022
b	0.25	0.30	0.35	0.010	0.012	0.014
D	7.85	8.00	8.15	0.309	0.315	0.321
E	12.85	13.00	13.15	0.506	0.512	0.518
e	0.75 BSC.			0.030 BSC.		
D1	Chip size ref.			Chip size ref.		
E1	Chip size ref.			Chip size ref.		
D2	5.25 BSC.			0.207 BSC.		
E2	3.75 BSC.			0.148 BSC.		

REFERENCE DOCUMENT:

TOP VIEW

A1 CORNER

SEATING PLANE
0.15 C

BOTTOM VIEW

A1 CORNER

Macronix International Co., Ltd.
旺宏電子股份有限公司

TITLE	PACKAGE OUTLINE FOR FLIP CHIP 48BALL (8X13X1.2 MM , BALL PITCH 0.75 MM)		DWG. NO. 6110-1010.2	
DRAWN C.L.Chiang	APPROVED Rick Chiu	DATE 04-09-'02	UNIT mm	TOLERANCE DIMENSION / ANGLE
				REVISION 1

56 TSOP

Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.22	0.27
b1	0.007	0.008	0.011	0.17	0.20	0.23
c	0.004	0.005	0.008	0.10	—	0.21
c1	0.004	0.005	0.006	0.10	0.13	0.16
D		0.787 BSC			20.00 BSC	
D1		0.724 BSC			18.40 BSC	
E		0.551 BSC			14.00 BSC	
L	0.020	0.024	0.028	0.50	0.60	0.70
L1		0.010 BSC			0.25 BSC	
e		0.020 BSC			0.5 BSC	
R1	0.003	0.006	—	0.08	0.15	—
R2	0.003	0.006	0.008	0.08	0.15	0.20
θ	0°	3°	5°	0°	3°	5°
θ1	0°	—	—	0°	—	—
θ2		15° REF			15° REF	
θ3		15° REF			15° REF	

DETAIL "A"

DETAIL "B"

TITLE			
PACKAGE OUTLINE FOR TSOP(I) 56L(14X20 MM)		DWG. NO. 6110-0241	
DRAWN	APPROVED	DATE	UNIT	REVISION
C.L.Chiang	Dennis Chang	06-12-'01		0

Macronix International Co., Ltd.
旺宏電子股份有限公司

TOLERANCE
.X ±
.XX ±.01
.XXX±.002
ANGLE

64 CSP

TOP VIEW

BOTTOM VIEW

Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.010	0.012	0.014	0.25	0.30	0.35
b	0.014	0.016	0.018	0.35	0.40	0.45
D	0.392	0.394	0.396	9.95	10.00	10.05
D1		0.276 BSC.			7.00 BSC.	
e	—	0.039	—	—	1.00	—
E	0.510	0.512	0.514	12.95	13.00	13.05
E1		0.276			7.00 BSC.	

REFERENCE DOCUMENT:

Macronix International Co., Ltd. 旺宏電子股份有限公司		DWG. NO. 6110-1003.22
TITLE PACKAGE OUTLINE FOR CSP 64BALL (10X13X1.2 MM , BALL PITCH 1.00 MM)		TOLERANCE
		DIMENSION	ANGLE
DRAWN	APPROVED	DATE	UNIT	REVISION
C.L.Chiang	Rick Chiu	03-05-'02	mm	0

48 TSOP

DETAIL F

SECTION B-B

Symbol	Dimension in Inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
c	0.004	—	0.008	0.10	—	0.21
c1	0.004	—	0.006	0.10	—	0.16
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	0.465	0.472	0.480	11.80	12.00	12.20
[e]	0.020BSC			0.50BSC		
L	0.016	0.020	0.024	0.40	0.50	0.60
y	—	—	0.003	—	—	0.076
θ	0°	5°	8°	0°	5°	8°

Macronix International Co., Ltd.
旺宏電子股份有限公司

TITLE
PACKAGE OUTLINE FOR
TSOP(I) 48L (12X20MM) NORMAL FORM

DRAWN C.L.Chiang
APPROVED Leo Lee
DATE 05-04-00
UNIT

TOLERANCE
.X ±
.XX ±.01
.XXX±.002
ANGLE

DWG. NO. 6110-0214

REVISION 4

48 TSOP (Reverse)

Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
c	0.004	—	0.008	0.10	—	0.21
c1	0.004	—	0.006	0.10	—	0.16
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	0.465	0.472	0.480	11.80	12.00	12.20
e	0.020BSC			0.50BSC		
L	0.016	0.020	0.024	0.40	0.50	0.60
y	—	—	0.003	—	—	0.076
θ	0°	5°	8°	0°	5°	8°

DETAIL F

SECTION B-B

TITLE	PACKAGE OUTLINE FOR TSOP(I) 48L (12X20MM) REVERSE FORM	DWG. NO. 6110-0214.1
DRAWN	C.L.Chiang	REVISION 4
APPROVED	Leo Lee	
DATE	05-04-'00	
UNIT		

Macronix International Co., Ltd.
旺宏電子股份有限公司

TOLERANCE
.X ±
.XX ±.01
.XXX ±.002
ANGLE

REVISION HISTORY

Revision No.	Description	Page	Date
0.1	1. To add 32M/128M information	All	JAN/17/2002
	2. To modify the CSP package size from 13x10mm to 10x13mm	P3	
0.2	1. Add 48-TSOP	P1	APR/04/2002
	2. Technology name is changed from MXVAND to Nbit	P1	
	3. 48-ball CSP name is added "Flip Chip" wording	P1	
	4. 64-ball CSP naming is changed	P1,4	
	5. Mis-tying : removing verify sector		
	5-1 Protection code from Table 14	P8,19	
	5-2 Correct Program Suspend/Resume flowchart	P30	
	5-3 Correct Block Erase Suspend/Resume flowchart	P31	
0.3	1. Added 48-RTSOP	P1,3,47	MAY/28/2002
	2. Added deep power-down spec:5uA(max.)	P1,9,11,38	
	3. Changed standby current from 120uA(max.) to 80uA(max.)	P38	
	4. Added "Cx" on part number to distinguish different program	P1,3,46,47	
	5. Changed spec of tPHWL(tPHEL) from 1us to 2us	P43	
	6. Changed spec of tPHRH from 100ns to 2us	P45	
	7. Changed speed spec of 32Mb from 110ns-->120ns	P1,41,47	
0.4	Deep power down mode is entering by RESET pin at VIH of 48-TSOP & 48-RTSOP types. 64-CSP & 56-TSOP is still kept RESET=VIL for entering deep power down mode.	P3,5,6,8,9,20, P37,38,41~47	JUN/07/2002
	Removed reset command	P10,11	

MACRONIX INTERNATIONAL CO., LTD.