

# OKI semiconductor

## MSM511000A

1,048,576-WORD x 1-BIT DYNAMIC RAM

### GENERAL DESCRIPTION

The MSM511000A is a new generation dynamic RAM organized as 1,048,576 words x 1 bit. The technology used to fabricate the MSM511000A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

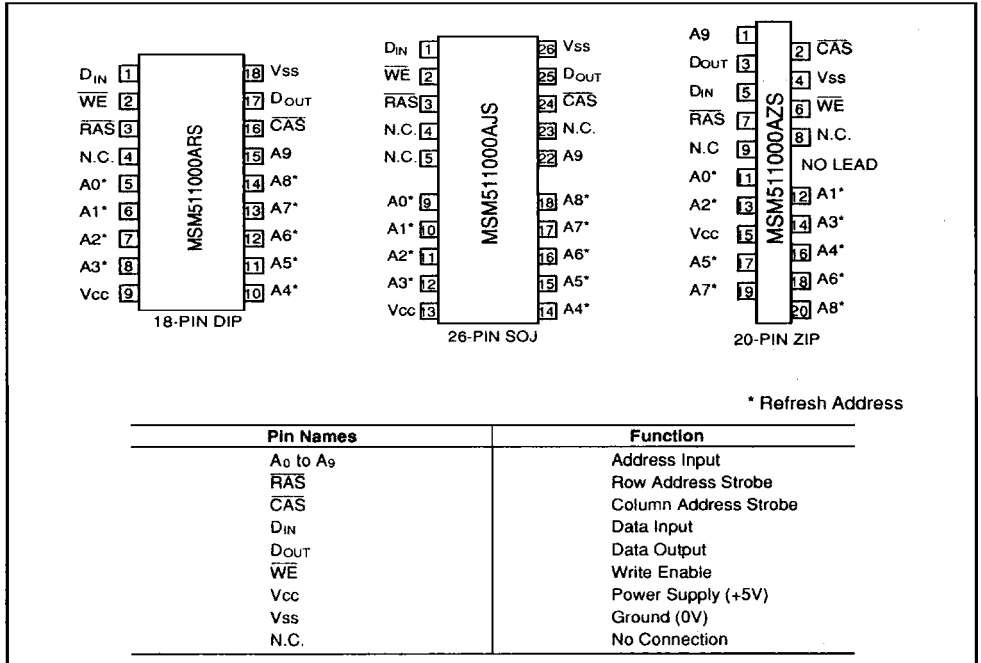
### FEATURES

- Silicon gate, triple polysilicon CMOS, 1-transistor memory cell
- Single +5V power supply,  $\pm 10\%$  tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using Early Write operation
- 1,048,576-word x 1-bit organization
- Fast page mode, read/write capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, Hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
- Gated  $\overline{\text{CAS}}$
- Built-in  $V_{\text{bb}}$  generator circuit

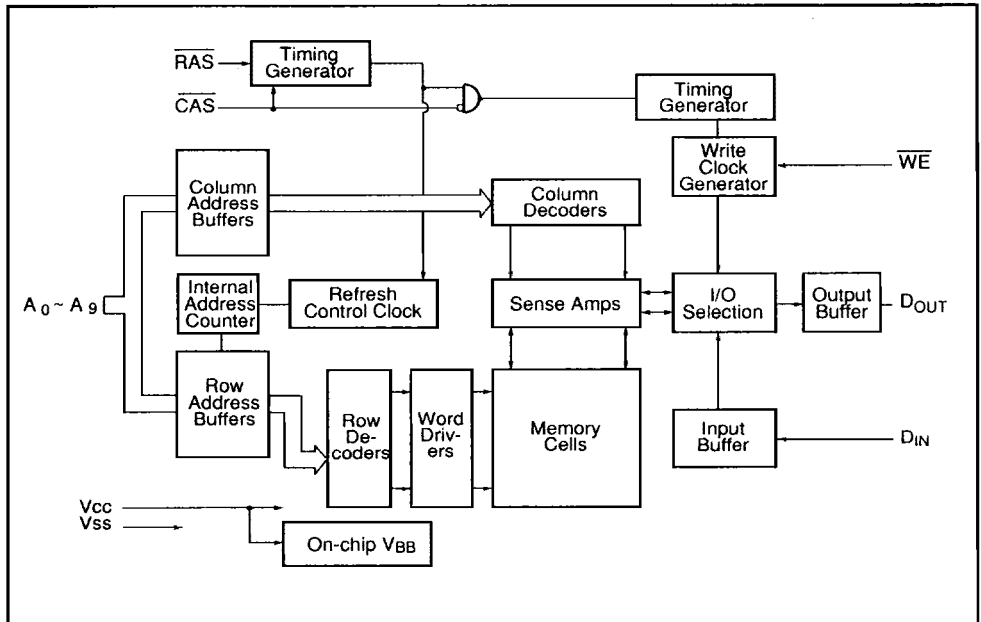
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Family	Access Time (Max.)	Cycle Time (Min.)	Power Dissipation	
			Operating (Max.)	Standby (Max.)
MSM511000A-70	70ns	140ns	468mW	5.5mW
MSM511000A-80	80ns	160ns	413mW	
MSM511000A-10	100ns	190ns	358mW	

**PIN CONFIGURATION (TOP VIEW)**



**FUNCTIONAL BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS**  
**ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	$T_a = 25^\circ\text{C}$	-1.0 to +7.0	V
Short circuit output current	$I_{OS}$	$T_a = 25^\circ\text{C}$	50	mA
Power dissipation	$P_D$	$T_a = 25^\circ\text{C}$	1	W
Operating temperature	$T_{opr}$	-	0 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-	-55 to +150	$^\circ\text{C}$

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Conditions	Value			Unit	Operating Temperature
			Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	-	4.5	5.0	5.5	V	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$
	$V_{SS}$	-	0	0	0	V	
Input high voltage	$V_{IH}$	-	2.4	-	6.5	V	
Input low voltage	$V_{IL}$	-	-1.0	-	0.8	V	

**DC CHARACTERISTICS**

( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0$  to  $+70^\circ C$ )

Parameter	Symbol	Conditions	MSM 511000A-70		MSM 511000A-80		MSM 511000A-10		Unit	Note	
			Min.	Max.	Min.	Max.	Min.	Max.			
Output high voltage	$V_{OH}$	$I_{OH} = -5.0mA$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	—	
Output low voltage	$V_{OL}$	$I_{OL} = 4.2mA$	0	0.4	0	0.4	0	0.4	V	—	
Input leakage current	$I_{LI}$	$0V \leq V_I \leq 6.5V$ ; all other pins not under test = 0V	-10	10	-10	10	-10	10	$\mu A$	—	
Output leakage current	$I_{LO}$	$\overline{D_{OUT}}$ disable $0V \leq V_O \leq 5.5V$	-10	10	-10	10	-10	10	$\mu A$	—	
Average power supply current* (Operating)	$I_{CC1}$	$\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = \min$	—	85	—	75	—	65	mA	—	
Power supply current* (Standby)	$I_{CC2}$	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IH}$ $D_{OUT} = Hz$	TTL	—	2	—	2	—	2	mA	—
		MOS	—	1	—	1	—	1			
Average power supply current* (RAS only refresh)	$I_{CC3}$	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ $t_{RC} = \min$	—	85	—	75	—	65	mA	—	
Average power supply current* (CAS before $\overline{RAS}$ refresh)	$I_{CC6}$	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	—	85	—	75	—	65	mA	—	
Average power supply current* (Fast page mode)	$I_{CC7}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling $t_{PC} = \min$	—	70	—	60	—	55	mA	—	

$I_{CC}$  depends on output loading and cycle rates. Specified values are obtained with the output open.

**CAPACITANCE**

( $T_a = 25^\circ C$ ,  $f = 1$  MHz)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Input capacitance ( $A_0$ to $A_9, D_{IN}$ )	$C_{IN1}$	—	—	6	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	$C_{IN2}$	—	—	7	pF
Output capacitance ( $D_{OUT}$ )	$C_{OUT}$	—	—	7	pF

**AC CHARACTERISTICS**

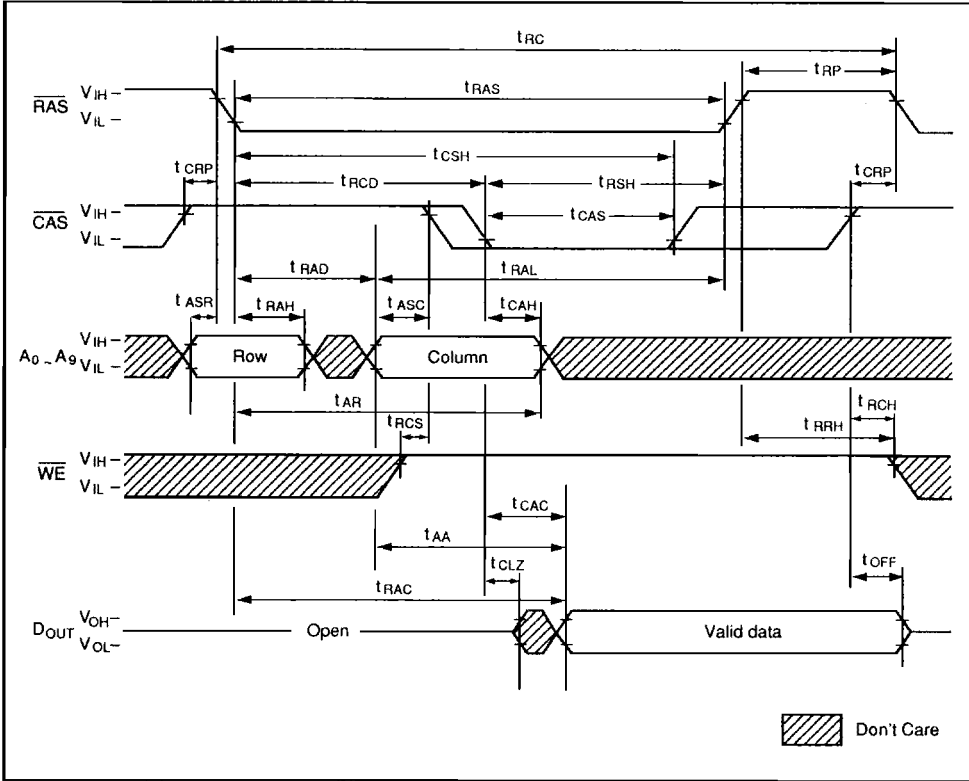
(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to +70°C) Notes 1,2,3

Parameter	Symbol	MSM 511000A-70		MSM 511000A-80		MSM 511000A-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Refresh period	t <sub>REF</sub>	–	8	–	8	–	8	ms	–
Random read or write cycle time	t <sub>RC</sub>	140	–	160	–	190	–	ns	–
Read/write cycle time	t <sub>RWC</sub>	165	–	185	–	220	–	ns	–
Fast page mode cycle time	t <sub>PC</sub>	45	–	50	–	55	–	ns	–
Fast page mode read/write cycle time	t <sub>PRWC</sub>	70	–	75	–	85	–	ns	–
Access time from RAS	t <sub>RAC</sub>	–	70	–	80	–	100	ns	4,5,6
Access time from CAS	t <sub>CAC</sub>	–	20	–	20	–	25	ns	4,5
Access time from column address	t <sub>AA</sub>	–	35	–	40	–	50	ns	4,6
Access time from CAS precharge	t <sub>CPA</sub>	–	40	–	45	–	50	ns	4
Output low impedance time from CAS	t <sub>CLZ</sub>	0	–	0	–	0	–	ns	4
Output buffer turn-off delay time	t <sub>OFF</sub>	0	20	0	20	0	20	ns	–
Transition time	t <sub>T</sub>	3	50	3	50	3	50	ns	3
RAS precharge time	t <sub>RP</sub>	60	–	70	–	80	–	ns	–
RAS pulse width	t <sub>RAS</sub>	70	10,000	80	10,000	100	10,000	ns	–
RAS pulse width (Fast page mode)	t <sub>RASP</sub>	70	100,000	80	100,000	100	100,000	ns	–
RAS hold time	t <sub>RSH</sub>	20	–	20	–	25	–	ns	–
CAS precharge time (Fast page mode)	t <sub>CP</sub>	10	–	10	–	10	–	ns	–
CAS pulse width	t <sub>CAS</sub>	20	10,000	20	10,000	25	10,000	ns	–
CAS hold time	t <sub>CSH</sub>	70	–	80	–	100	–	ns	–
RAS to CAS delay time	t <sub>RCD</sub>	20	50	22	60	25	75	ns	5
RAS to column address delay time	t <sub>RAD</sub>	15	35	17	40	20	50	ns	6
CAS to RAS precharge time	t <sub>CRP</sub>	10	–	10	–	10	–	ns	–
Row address set-up time	t <sub>ASR</sub>	0	–	0	–	0	–	ns	–
Row address hold time	t <sub>RAH</sub>	10	–	12	–	15	–	ns	–
Column address set-up time	t <sub>ASC</sub>	0	–	0	–	0	–	ns	–
Column address hold time	t <sub>CAH</sub>	15	–	15	–	20	–	ns	–
Column address hold time from RAS	t <sub>AR</sub>	55	–	60	–	75	–	ns	–
Column address to RAS lead time	t <sub>RAL</sub>	35	–	40	–	50	–	ns	–

AC CHARACTERISTICS (CONT.)

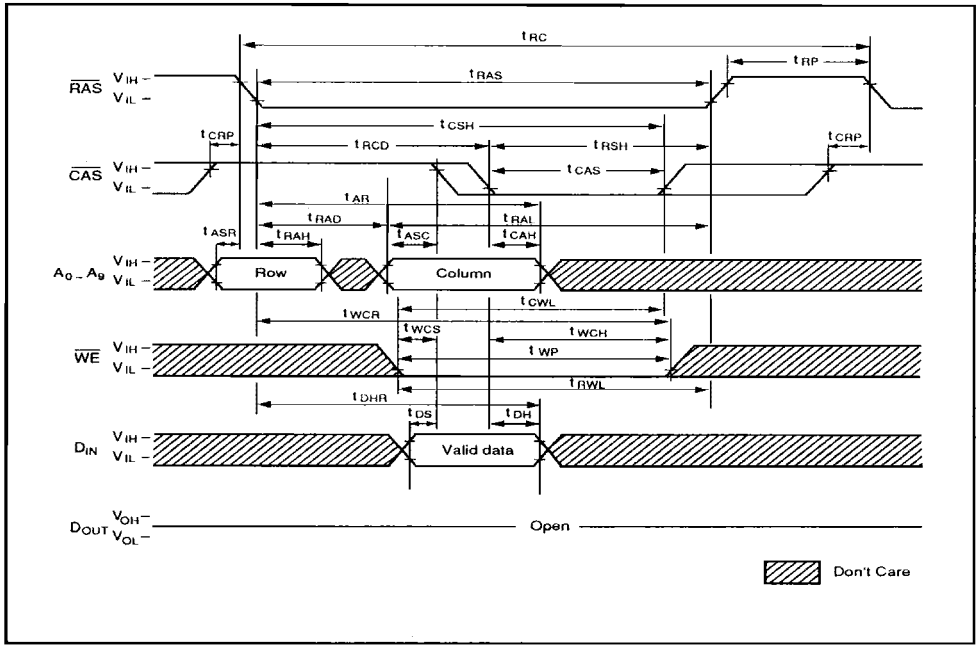
Parameter	Symbol	MSM 511000A- 70		MSM 511000A- 80		MSM 511000A- 10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read command set-up time	$t_{RCS}$	0	—	0	—	0	—	ns	—
Read command hold time	$t_{RCH}$	0	—	0	—	0	—	ns	8
Write command hold time from $\overline{RAS}$	$t_{WCR}$	55	—	60	—	75	—	ns	—
Write command set-up time	$t_{WCS}$	0	—	0	—	0	—	ns	7
Write command hold time	$t_{WCH}$	15	—	15	—	20	—	ns	—
Write command pulse width	$t_{WP}$	15	—	15	—	20	—	ns	—
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	20	—	20	—	25	—	ns	—
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	20	—	20	—	25	—	ns	—
Data-in set-up time	$t_{DS}$	0	—	0	—	0	—	ns	—
Data-in hold time	$t_{DH}$	15	—	15	—	20	—	ns	—
Data-in hold time from $\overline{RAS}$	$t_{DHR}$	55	—	60	—	75	—	ns	—
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	20	—	20	—	25	—	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	70	—	80	—	100	—	ns	7
Column address to $\overline{WE}$ delay time	$t_{AWD}$	35	—	40	—	50	—	ns	7
Read command hold time reference to $\overline{RAS}$	$t_{RRH}$	0	—	10	—	10	—	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ( $\overline{CAS}$ before $\overline{RAS}$ )	$t_{CSR}$	10	—	10	—	10	—	ns	—
$\overline{RAS}$ to $\overline{CAS}$ hold time ( $\overline{CAS}$ before $\overline{RAS}$ )	$t_{CHR}$	30	—	30	—	30	—	ns	—
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	$t_{RPC}$	10	—	10	—	10	—	ns	—
$\overline{CAS}$ precharge time (Refresh counter test)	$t_{CPT}$	40	—	40	—	50	—	ns	—
$\overline{CAS}$ precharge time	$t_{CPN}$	10	—	10	—	15	—	ns	—

READ CYCLE

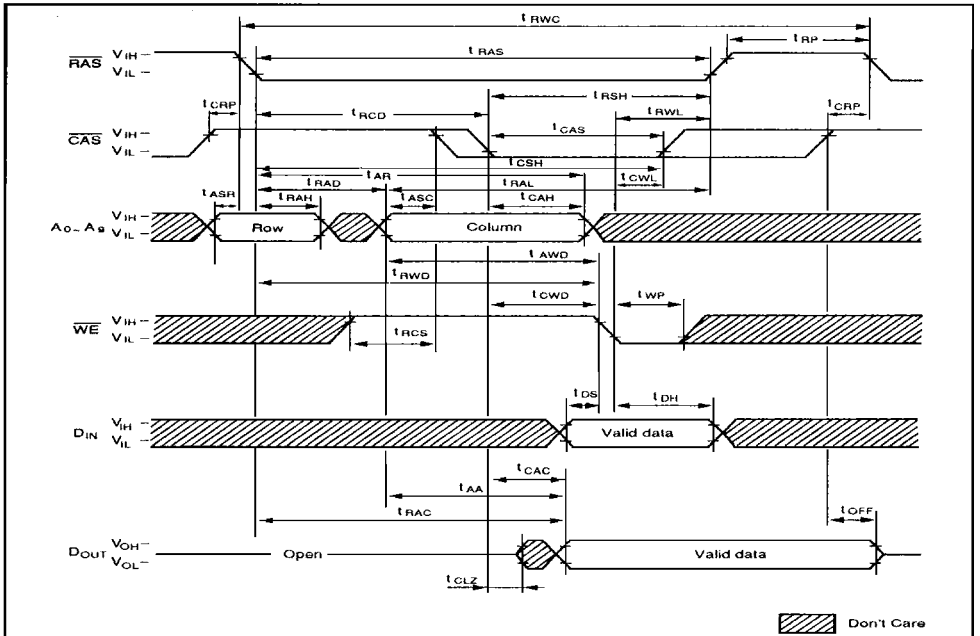


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WRITE CYCLE (EARLY WRITE)

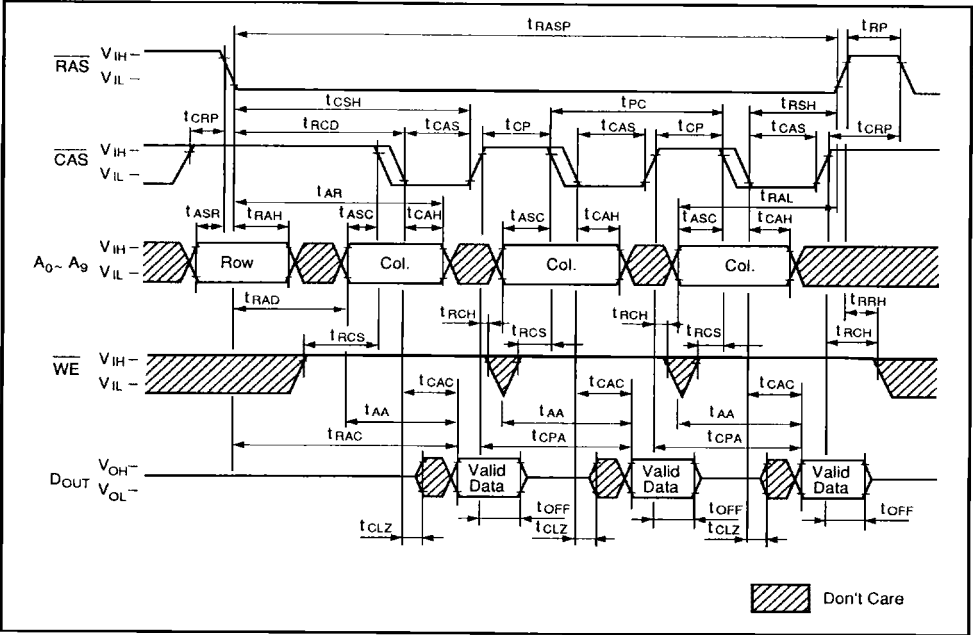


READ/WRITE CYCLE



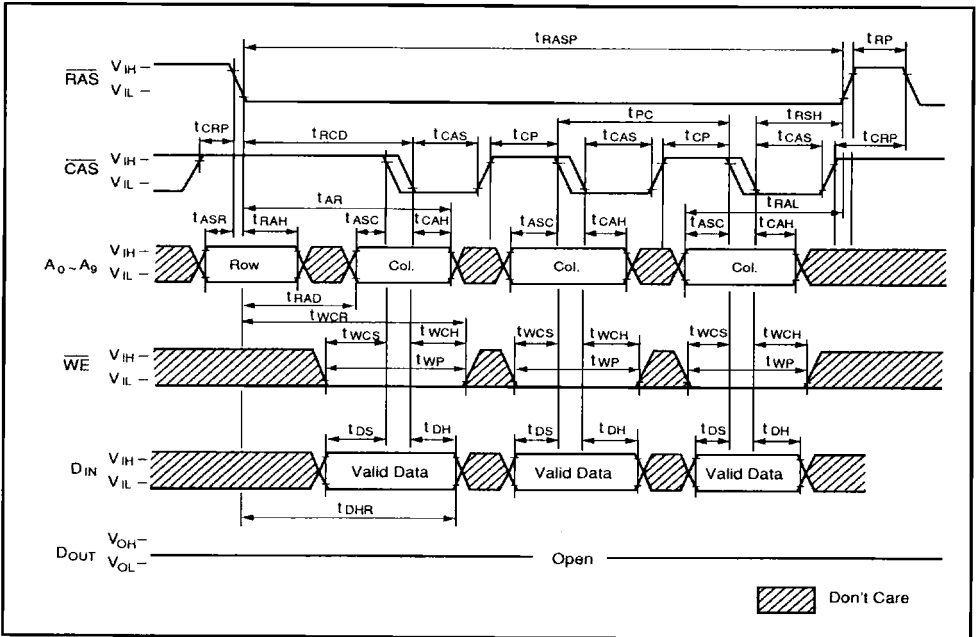


**FAST PAGE MODE READ CYCLE**

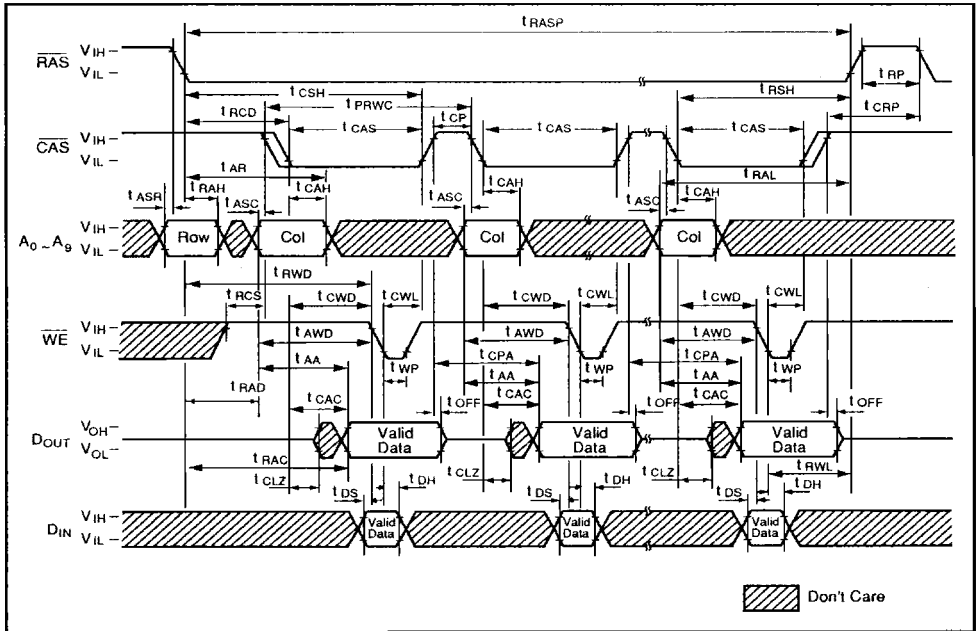


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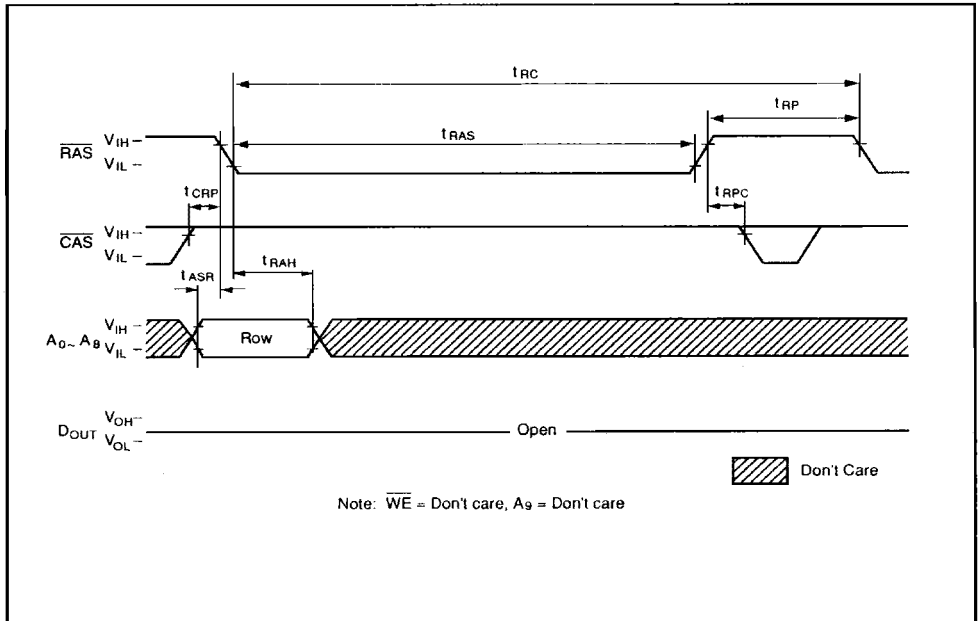
**FAST PAGE MODE WRITE CYCLE (EARLY WRITE)**



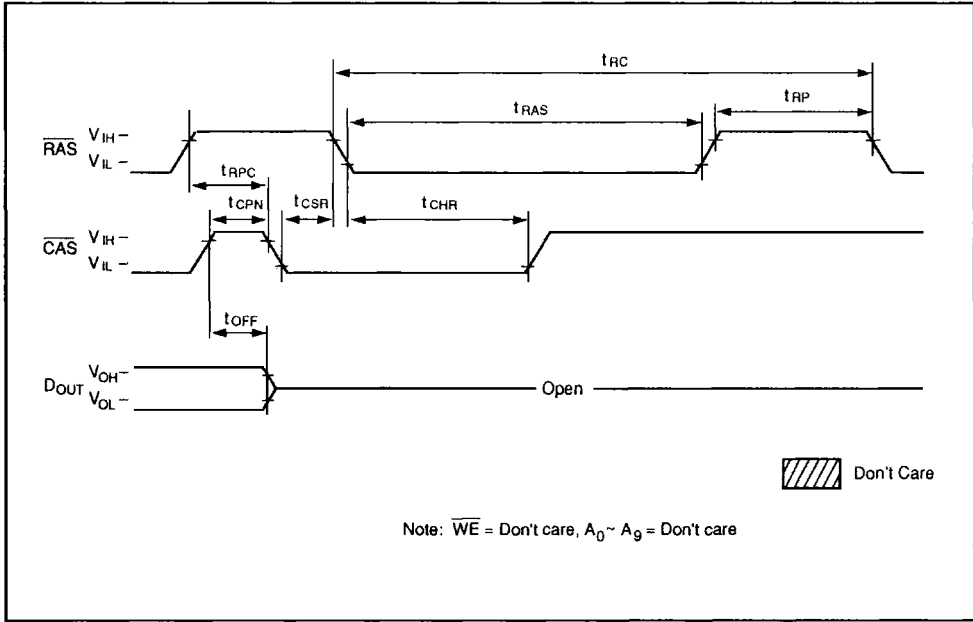
**FAST PAGE MODE READ/WRITE CYCLE**



**RAS-ONLY REFRESH CYCLE**

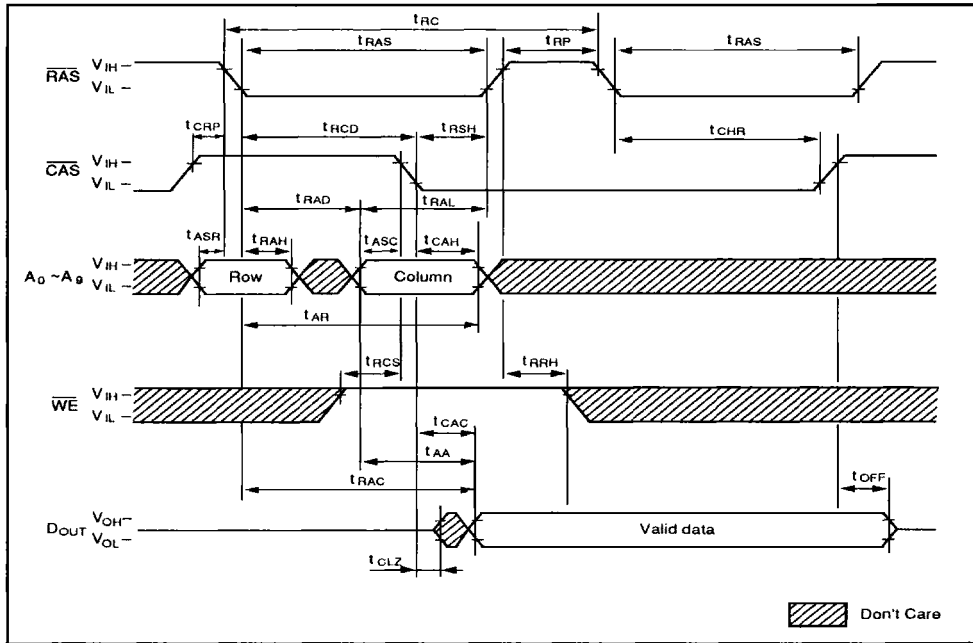


CAS BEFORE RAS AUTO-REFRESH CYCLE

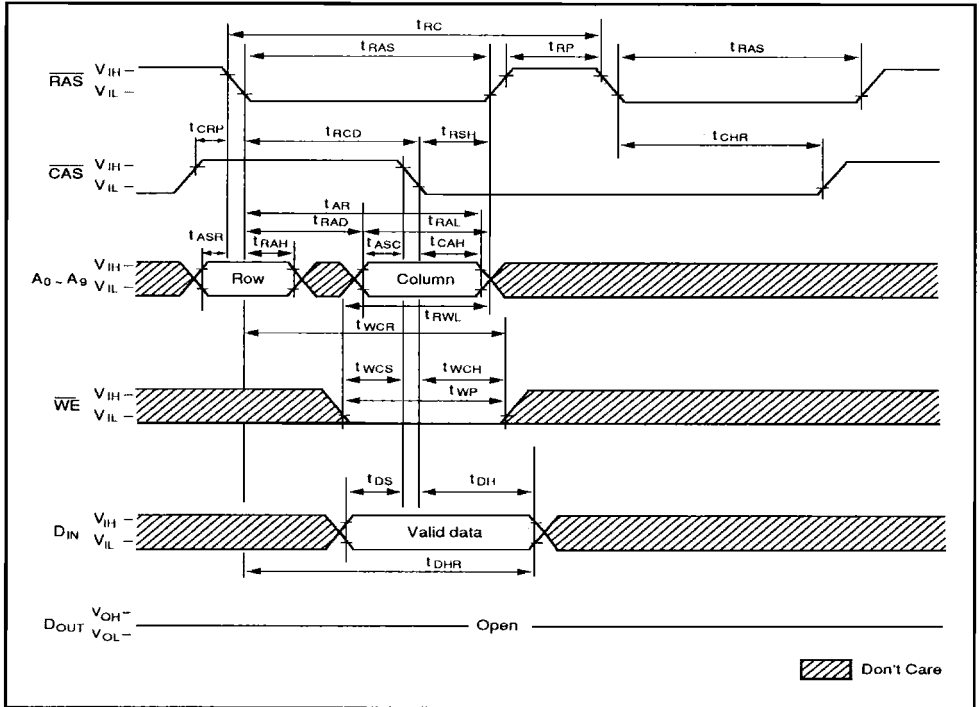


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HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

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