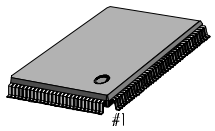
# 1 PRODUCT OVERVIEW

## INTRODUCTION

KS1453 is a data processing IC that can operate in 1x DVDP or 4x CD (audio/ VCD) mode. It receives the sliced output (EFM signals) of the RF signal from the disc and carries out data demodulation and error correction. It includes a buffer control feature that allows the demodulated data to be continuously output in hand shake mode.

128-QFP




## FEATURES

- External plck input
- EFM/EFMPLUS demodulator
- Sync protection/insertion
- CIRC/RS-PC error correction (4/16 erasure correction)
- Cross/row deinterleave
- 4 - 16 Mbits DRAM interface (external component for error correction/track buffering)
- Descramble
- ID error correction
- Main data error detection (EDC)
- Error flag monitoring
- MICOM interface
- MICOM direct memory access feature (DVD/CD)
- DSI detection and DSI data output
- A/V decoder parallel interface
- Built-in CD-DA decoder
- Sub-code data serial output
- Spindle servo control signal generation
- DVD playback
- CD/VCD playback
- CLV/CAV feature
- CD/VCD repeat correcting feature
- Technology
  - Application mode: CD_Player, CD_ROM, Video-CD, DVDP player

## BLOCK DIAGRAM

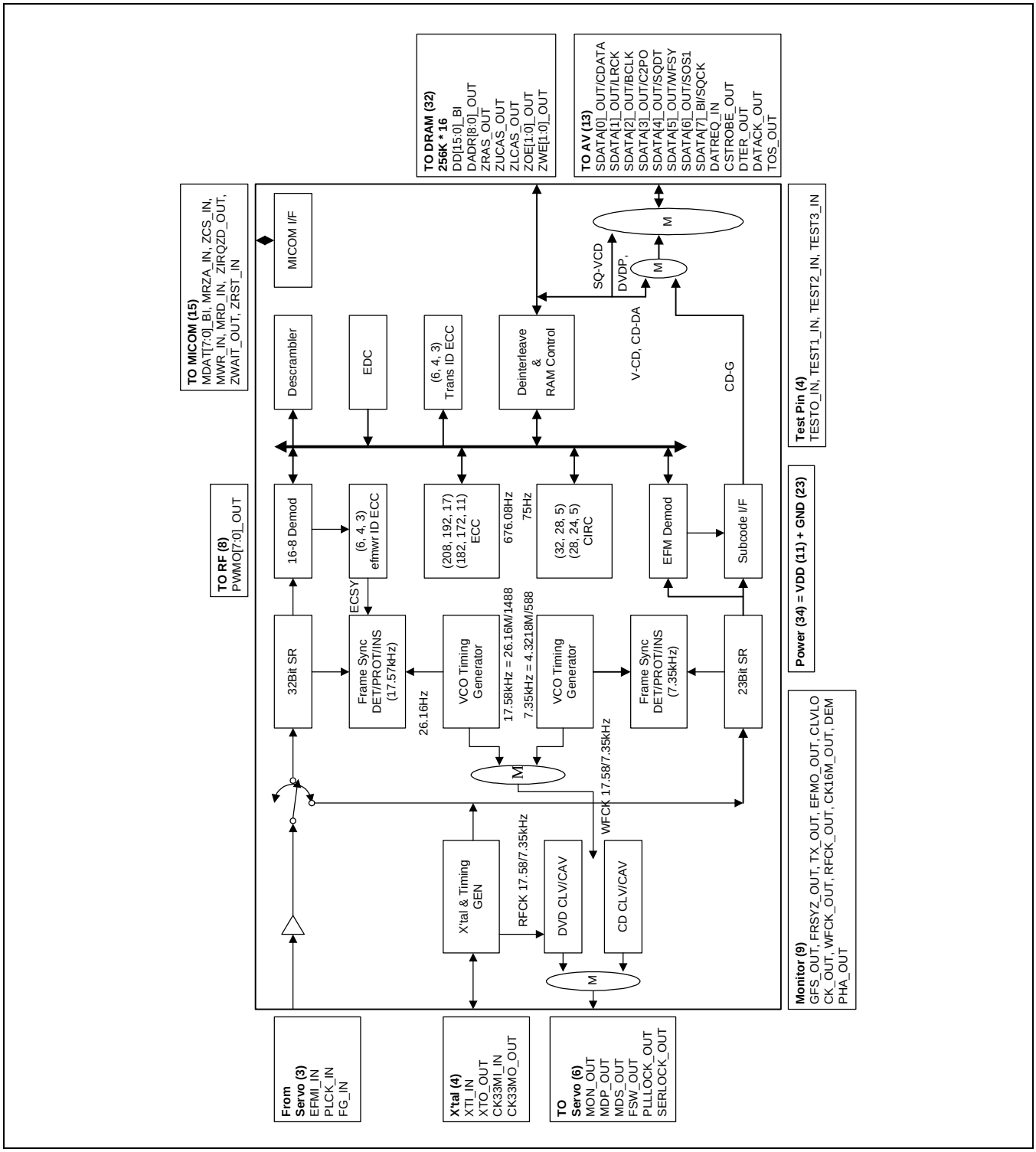



**Figure 1. Block Diagram**

## PIN CONFIGURATION

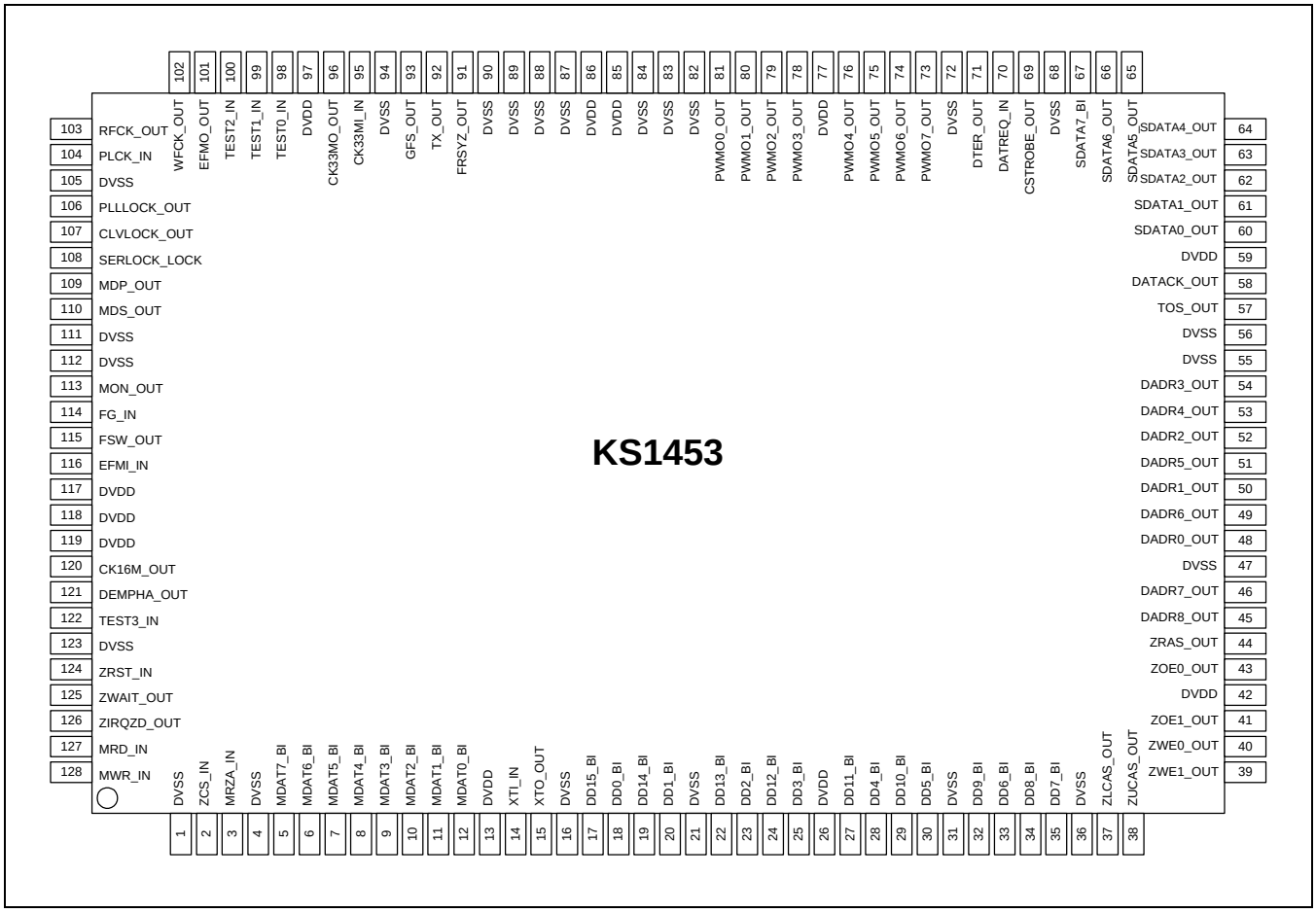



**Figure 2. Pin Configuration**

## PIN DESCRIPTION

**Table 1. Pin Description**

| No | Pin Name | Description | I/O | Note |
|---|---|---|---|---|
| 1 | DVSS | Digital GND (0V) | | |
| 2 | ZCS_IN | Chip select (active low), pull_up pin | I | MICOM |
| 3 | MRZA_IN | MICOM register select, pull_up pin<br>(L → register, H → data) | I | MICOM |
| 4 | DVSS | Digital GND (0V) | | |
| 5 | MDAT7_BI | MICOM data bus | B | MICOM |
| 6 | MDAT6_BI | MICOM data bus | B | MICOM |
| 7 | MDAT5_BI | MICOM data bus | B | MICOM |
| 8 | MDAT4_BI | MICOM data bus | B | MICOM |
| 9 | MDAT3_BI | MICOM data bus | B | MICOM |
| 10 | MDAT2_BI | MICOM data bus | B | MICOM |
| 11 | MDAT1_BI | MICOM data bus | B | MICOM |
| 12 | MDAT0_BI | MICOM data bus | B | MICOM |
| 13 | DVDD | Digital power (+5V) | | |
| 14 | XTI_IN | System clock input for 26.16MHz | I | XTAL |
| 15 | XTO_OUT | System clock output for 26.16MHz | O | XTAL |
| 16 | DVSS | Digital GND (0V) | | |
| 17 | DD15_BI | DRAM data bus | B | DRAM |
| 18 | DD0_BI | DRAM data bus | B | DRAM |
| 19 | DD14_BI | DRAM data bus | B | DRAM |
| 20 | DD1_BI | DRAM data bus | B | DRAM |
| 21 | DVSS | Digital GND (0V) | | |
| 22 | DD13_BI | DRAM data bus | B | DRAM |
| 23 | DD2_BI | DRAM data bus | B | DRAM |
| 24 | DD12_BI | DRAM data bus | B | DRAM |
| 25 | DD3_BI | DRAM data bus | B | DRAM |
| 26 | DVDD | DIGITAL power (+5V) | | |
| 27 | DD11_BI | DRAM data bus | B | DRAM |
| 28 | DD4_BI | DRAM data bus | B | DRAM |
| 29 | DD10_BI | DRAM data bus | B | DRAM |
| 30 | DD5_BI | DRAM data bus | B | DRAM |
| 31 | DVSS | DIGITAL GND (0V) | | |
| 32 | DD9_BI | DRAM data bus | B | DRAM |
| 33 | DD6_BI | DRAM data bus | B | DRAM |
| 34 | DD8_BI | DRAM data bus | B | DRAM |
| 35 | DD7_BI | DRAM data bus | B | DRAM |

**Table 1. Pin Description (Continued)**

| No | Pin Name | Description | I/O | Note |
|---|---|---|---|---|
| 36 | DVSS | Digital GND (0V) | | |
| 37 | ZLCAS_OUT | DRAM low column address strobe | O | DRAM |
| 38 | ZUCAS_OUT | DRAM upper column address strobe | O | DRAM |
| 39 | ZWE1_OUT | DRAM write enable 1 (8M only) | O | DRAM |
| 40 | ZWE0_OUT | DRAM write enable 0 (4M, 8M, 16M) | O | DRAM |
| 41 | ZOE1_OUT | DRAM output enable 1 (DADR9 in 16M mode) | O | DRAM |
| 42 | DVDD | Digital power (+5V) | | |
| 43 | ZOE0_OUT | DRAM output enable 0 | O | DRAM |
| 44 | ZRAS_OUT | DRAM row address strobe | O | DRAM |
| 45 | DADR8_OUT | DRAM address bus | O | DRAM |
| 46 | DADR7_OUT | DRAM address bus | O | DRAM |
| 47 | DVSS | Digital GND (0V) | | |
| 48 | DADR0_OUT | DRAM address bus | O | DRAM |
| 49 | DADR6_OUT | DRAM address bus | O | DRAM |
| 50 | DADR1_OUT | Address bus | O | DRAM |
| 51 | DADR5_OUT | DRAM address bus | O | DRAM |
| 52 | DADR2_OUT | DRAM address bus | O | DRAM |
| 53 | DADR4_OUT | DRAM address bus | O | DRAM |
| 54 | DADR3_OUT | DRAM address bus | O | DRAM |
| 55 | DVSS | Digital GND (0V) | | |
| 56 | DVSS | Digital GND (0V) | | |
| 57 | TOS_OUT | Top of sector | O | AV Decoder |
| 58 | DATACK_OUT | Data acknowledge signal output | O | AV Decoder |
| 59 | DVDD | Digital power (+5V) | | |
| 60 | SDATA0_OUT | DVD data/CD data bit stream (CDATA) | O | AV Decoder |
| 61 | SDATA1_OUT | DVD data/CD data L/R clock (LRCK) | O | AV Decoder |
| 62 | SDATA2_OUT | DVD data/CD data bit clock (BLCK) | O | AV Decoder |
| 63 | SDATA3_OUT | DVD data/CD data error plug (C2PO) | O | AV Decoder |
| 64 | SDATA4_OUT | DVD data/sub-code serial data (SQDT) | O | AV Decoder |
| 65 | SDATA5_OUT | DVD data/sub-code frame sync (WFSY) | O | AV Decoder |
| 66 | SDATA6_OUT | DVD data/sub-code block sync (S0S1) | O | AV Decoder |
| 67 | SDATA7_BI | DVD data/sub-code serial clock (SQCK) | B | AV Decoder |
| 68 | DVSS | Digital GND (0V) | | |
| 69 | CSTROBE_OUT | Data strobe (clock) output | O | AV Decoder |
| 70 | DATREQ_IN | Data request from A/V decoder or ROM Ecuador | I | AV Decoder |
| 71 | DTER_OUT | DVD data error output | O | AV Decoder |
| 72 | DVSS | Digital GND (0V) | | |

**Table 1. Pin Description (Continued)**

| No | Pin Name | Description | I/O | Note |
|---|---|---|---|---|
| 73 | PWMO7_OUT | PWM output signal | O | RF |
| 74 | PWMO6_OUT | PWM output signal | O | RF |
| 75 | PWMO5_OUT | PWM output signal | O | RF |
| 76 | PWMO4_OUT | PWM output signal | O | RF |
| 77 | DVDD | Digital power (+5V) | | |
| 78 | PWMO3_OUT | PWM output signal | O | RF |
| 79 | PWMO2_OUT | PWM output signal | O | RF |
| 80 | PWMO1_OUT | PWM output signal | O | RF |
| 81 | PWMO0_OUT | PWM output signal | O | RF |
| 82 | DVSS | Digital GND (0V) | | |
| 83 | DVSS | Digital GND (0V) | | |
| 84 | DVSS | Digital GND (0V) | | |
| 85 | DVDD | Digital power (+5V) | | |
| 86 | DVDD | Digital power (+5V) | | |
| 87 | DVSS | Digital GND (0V) | | |
| 88 | DVSS | Digital GND (0V) | | |
| 89 | DVSS | Digital GND (0V) | | |
| 90 | DVSS | Digital GND (0V) | | |
| 91 | FRSYZ_OUT | Frame sync out | O | Monitor |
| 92 | TX_OUT | Digital out (3-state) | O | Monitor |
| 93 | GFS_OUT | Good frame sync detection status output (OK at H) | O | Monitor |
| 94 | DVSS | Digital GND (0V) | | |
| 95 | CK33MI_IN | System clock input for 33.8688MHz | I | XTAL |
| 96 | CK33MO_OUT | System clock output for 33.8688MHz | O | XTAL |
| 97 | DVDD | Digital power (+5V) | | |
| 98 | TEST0_IN | Test mode select signal, pull_down pin | I | |
| 99 | TEST1_IN | Test mode select signal, pull_down pin | I | |
| 100 | TEST2_IN | Test mode select signal, pull_down pin | I | |
| 101 | EFMO_OUT | EFM out | O | Monitor |
| 102 | WFCK_OUT | Write frame pulse | O | Monitor |
| 103 | RFCK_OUT | Reference frame pulse | O | Monitor |
| 104 | PLCK_IN | Phase locked clock | I | Servo |
| 105 | DVSS | Digital GND (0V) | | |
| 106 | PLLLOCK_OUT | Lock signal for pll | O | Servo |
| 107 | CLVLOCK_OUT | Lock signal for CLV | O | Monitor |
| 108 | SERLOCK_OUT | Lock signal for servo | O | Servo |
| 109 | MDP_OUT | Spindle motor phase control signal (3-state) | O | Servo |

**Table 1. Pin Description (Continued)**

| No | Pin Name | Description | I/O | Note |
|---|---|---|---|---|
| 110 | MDS_OUT | Spindle motor speed control signal (3-state) | O | Servo |
| 111 | DVSS | Digital GND (0V) | | |
| 112 | DVSS | Digital GND (0V) | | |
| 113 | MON_OUT | Spindle motor on/off control output | O | Servo |
| 114 | FG_IN | Reference signal for CAV | I | Servo |
| 115 | FSW_OUT | Spindle motor output filter conversion output (3-state) | O | Servo |
| 116 | EFMI_IN | EFM/EFM + signal input | I | Servo |
| 117 | DVDD | Digital power (+5V) | | |
| 118 | DVDD | Digital power (+5V) | | |
| 119 | DVDD | Digital power (+5V) | | |
| 120 | CK16M_OUT | CK33M's 1/2 clock/16.9344MHz | O | Monitor |
| 121 | DEMPHA_OUT | Deemphasis on when "high" | O | Monitor |
| 122 | TEST3_IN | Test mode select signal, pull_down in | I | |
| 123 | DVSS | Digital GND (0V) | | |
| 124 | ZRST_IN | Hardware reset (active low) pull_up pin | I | MICOM |
| 125 | ZWAIT_OUT | MICOM read/write access wait (wait at L) | O | MICOM |
| 126 | ZIRQZD_OUT | Interrupt request to MICOM | O | MICOM |
| 127 | MRD_IN | MICOM read strobe (active low) pull_up pin | I | MICOM |
| 128 | MWR_IN | MICOM write strobe (active low) pull_up pin | I | MICOM |

# 2 ELECTRICAL CHARACTERISTICS

## DC CHARACTERISTICS

($V_{DD}$ = 5.0V ± 5%, $V_{SS}$ = 0V, Ta = 0 - +70°C)

| Item | | | Conditions | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input voltage | Input voltage "H" level | VIH | - | $0.7V_{DD}$ | - | V | 1 |
| | Input voltage "L" level | VIL | - | - | $0.3V_{DD}$ | V | |
| Output voltage | Output voltage "H" level | VOH | IOH = -2, -4mA | 2.4 | $V_{DD}$ | V | 2 |
| | Output voltage "L" level | VOL | IOL = 2, 4mA | 0 | 0.4 | V | |
| Input voltage | Input voltage "H" level | IIH1 | Vin = $V_{DD}$ | -10 | 10 | µA | 3 |
| | Input voltage "L" level | IIL1 | Vin = $V_{SS}$ | -10 | 10 | µA | |
| Input voltage | Input voltage "H" level | IIH2 | Vin = $V_{DD}$ | 10 | 100 | µA | 4 |
| | Input voltage "L" level | IIL2 | Vin = $V_{SS}$ | -100 | -10 | µA | 5 |
| Input current leak | | $I_{LI}$ | $V_I$ = 0 - 5.25V | -10 | 10 | µA | 1 |

**NOTES:**

1. All CMOS input signals, BIDIR PAD's input mode signals
2. All output signals
3. All CMOS input signals, BIDIR PAD's input mode signals
4. All input signals with pull-down
5. All input signals with pull-up

## ABSOLUTE MAXIMUM RATINGS

| No | Item | Symbol | Spec | Unit |
|---|---|---|---|---|
| 1 | DC input voltage | Vin | -0.3 - $V_{DD}$ + 0.3 | V |
| 2 | C supply voltage | $V_{DDmax}$ | -0.3 - +7.0 | V |
| 3 | C input current | Lin | 10 | mA |
| 4 | Storage temperature | Tstg | -40 - 125 | °C |

## RECOMMENDED OPERATING CONDITIONS

| No | Item | Symbol | Spec | Unit |
|---|---|---|---|---|
| 1 | Operating temperature | Topr | 0 - 70 | |
| 2 | DC supply voltage | $V_{DD}$ | 4.75 - 5.25 | V |

# 3 BLCOK CHARACTERISTICS

## ECC FEATURE

Euclid's algorithm used.

Same circuit used for DVD and CD.

**DVD (PRIMITIVE POLYNOMIAL: X8 + X4 + X3 + X2 + 1)**

: Error correcting ability for DVD data.

- ® PI (182, 172, 11) code: 5 error correct/10 errata correct
- ® PO (208, 192, 17) code: 8 error correct/16 errata correct

38.8688MHz clock: 1X operation (PI+PO+PI)/1 EFM block satisfaction → basic operation

**CD (PRIMITIVE POLYNOMIAL: X8 + X4 + X3 + X2 + 1)**

- ® C1 (32, 28, 5) code: 2 error correct
- ® C2 (28, 24, 4) code: 2 error correct/4 errata correct

Repeat correction carried at for video-CD (C1 → C2 → C1 → C2)

## MEMORY CONTROL FEATURE

CD data processor and DVD data processor has an external 4M or 8M DRAM in common.

EFM data write, ECC data R/W, descrambler R/W, and transfer read addressing feature.

**DVD**

- 33.8688MHz crystal clock used.
- Continuous storage according to input order regardless of data format (PO deinterleave).
- 13 ECC block areas guaranteed in 4M bit DRAM. (EFM, ECC, descrambler, and transfer cyclically processed)
- MICOM user area guaranteed (can use blocks 1 - 8 selectively in units of ECC blocks)
- EFM data Write in units of sectors.
- Data transfer in units of sectors.
- Block copy feature (sector number selection possible)
- MICOM direct access on DRAM

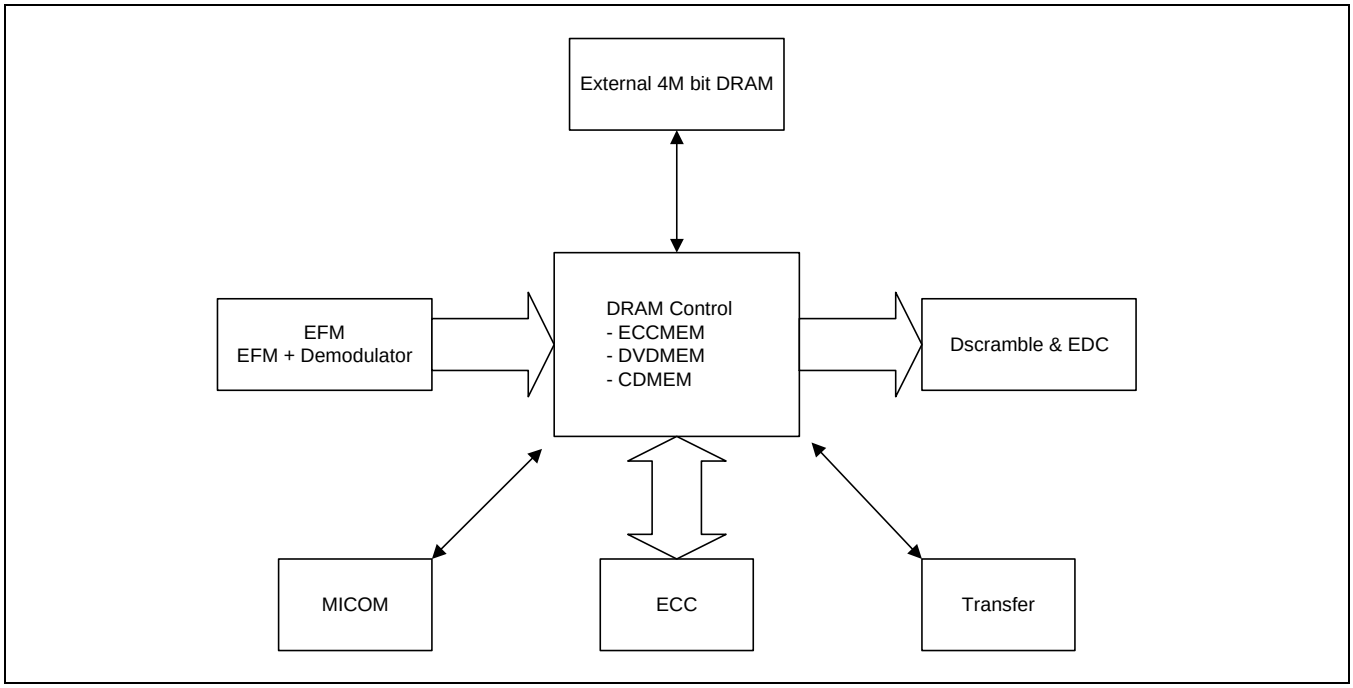



**Figure 3. Block Diagram of Memory Control**

**CD**

- CD-DA, CD-ROM, V-CD: 33.8688MHz crystal clock used.
- Video-CD: Repeat correction possible.
- 8Kbyte memory area used.
- EF M, ECC, transfer feature.
- EFM: referenced by WFCK.
- ECC, transfer: referenced by RFCK.
- MICOM direct access on DRAM.

## DESCRAMBLER & EDC & TRANSFER FEATURE

- Descramble on/off control possible in MICOM
- EDC flag output to MICOM
- 2048-byte or 2064-byte output selection possible
- Transfer sector number selection possible
- Maximum transfer rate: 5.4MBytes/s.
- Parallel synchronous I/F support
- Request, TOS, ACK, DATCLK, and EDCFLG'S active 'L/H" selection possible.

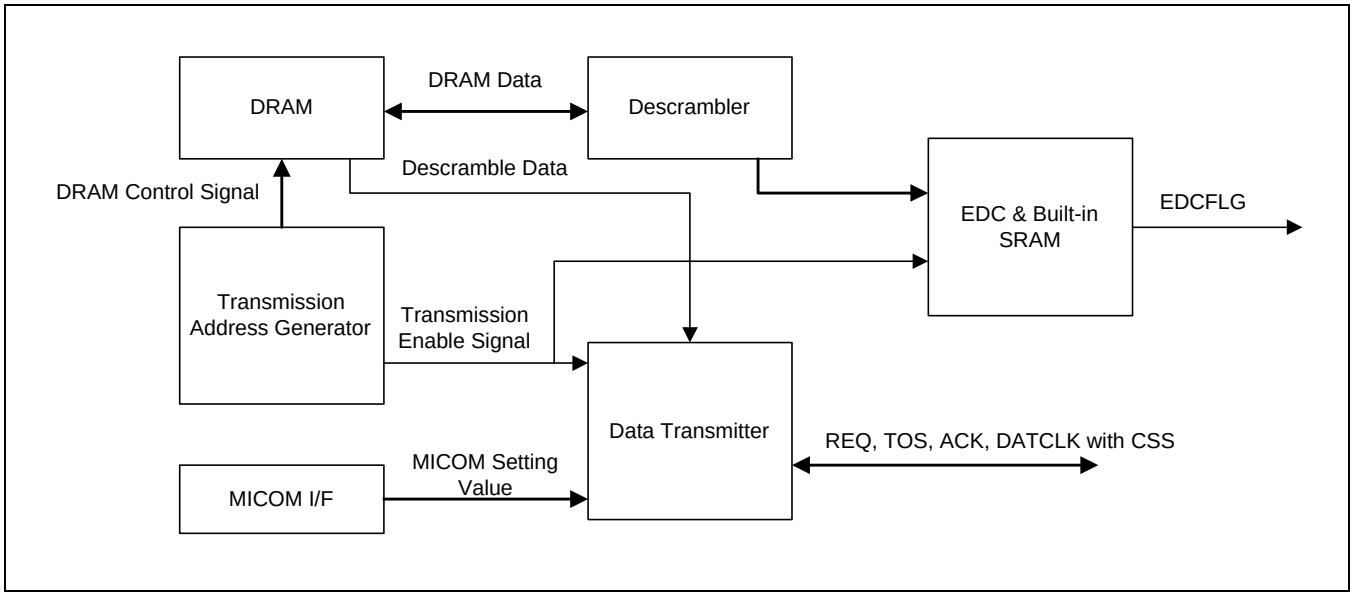



**Figure 4. Block Diagram of the Transfer Part**

## CD AUDIO FEATURE

Receives data that has been completely corrected of errors in units of byte, and outputs it serially.

Interpolation, mute, and attenuation carried out for CD-DA.

## SUBCODE I/F FEATURE

CD graphic processing subcode data (P, Q, R, S, T, U, V, W) is serially output.

Errors existing in the disc controlling subcode data (Q) are checked and output.
(p(x) = x16 + x12 + x5 + 1)

## MICOM I/F FEATURE

Address/command data: 1byte

Write register access
: CS enable → W_reg address write → Command data write → CS disable

Read register access
: CS enable → R_reg address write → R_reg data read → CS disable

## EFM DEMODULATOR FEATURE

CD player, CD-ROM, and DVD player mode

Demodulator
: EFM + demodulation (DVD)
EFM demodulation (CD)

ID sync, frame sync detection/protection/insertion
: 4 step ID sync/frame sync protection window section select
4 step ID sync/ frame sync insertion frame number select

SID error correction

ID (frame) sync continuous check

# 4 MICOM REGISTER

## MICOM WRITE REGISTER & READ/WRITE REGISTER

**Table 2. MICOM Write Register & Read/Write Register Table (R/W unmarked; W)**

| Name | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| **RESERVED (00 - 09)** | | | | | | | | | |
| INTCTL1 | 0A | DVDIEN | DSIEN | TOSEN | TSCMPEN | ECCIEN | EMPTYEN | OVEREN | UNDEREN |
| INTCTL2 | 0B | SBQIEN | MCPEN | - | - | - | - | - | - |
| INTCTL3 | 0C | - | - | - | IFRQ2 | IFRQ1 | IFRQ0 | - | CLRINT |
| SYSCONT1 | 0D | MRESET | - | - | RCF1 | RCF0 | DISC2 | DISC1 | DISC0 |
| USER1CON | 0E | WIDEWIN | GFSPRO | SYNCDEC | ISPROT | FNADJ | RFNCON | - | - |
| USER2CON | OF | ABTH7 | ABTH6 | ABTH5 | AB TH4 | ABTH3 | ABTH2 | ABTH1 | ABTH0 |
| DVDDSET | 10 | - | - | FWSEL1 | FWSEL0 | FGSEL1 | FGSEL0 | IGSEL1 | IGSEL0 |
| DVDCONTROL1 | 11 | DSCREN | STRST | - | - | INSEN | WNDEN | WNDRT | FCLDS |
| DVDCONTROL2 | 12 | WRST | TRST | ECCST | ECNEGLT | ECMOD2 | ECMOD1 | ECMOD0 | MCPST |
| CLVCONTROL1 | 13 | PGAIN1 | PGAIN0 | SGAIN1 | SGAIN0 | - | - | - | - |
| CLVCONTROL2 | 14 | MDSCON1 | MDSCON0 | PLLC1 | PLLC0 | - | MDPC | P_RES1 | P_RES0 |
| CLVCONTROL3 | 15 | FALTHR1 | FALTHR1 | RISTHR1 | RISTHR0 | REFSEL | SERVOC | CLVC1 | CLVC0 |
| CLVMODE | 16 | SDWP | SDWB | - | - | SDCM3 | SDCM2 | SDCM1 | SDCM0 |
| **RESERVED (17 - 18)** | | | | | | | | | |
| TRMODE | 19 | IFMOD2 | IFMOD1 | IFMOD0 | - | CDIF0 | DRATE | - | DVDIF0 |
| CDSPEED | 1A | - | - | - | - | - | CDSPD2 | CDSPD1 | CDSPD0 |
| CDMUTCNT | 1B | CBITIN2 | CBITIN1 | CBITIN0 | DGOEN | DEMPHA | MUTE | ZCMT | ATTN |
| CDCONTROL | 1C | - | - | - | - | BYPASS | INFR | T3_SEL | T3_MODE |
| ECCREG1 | 1D | ERAMODF | ERAMODL | maxmode2f | maxmode2l | c2eccf | c2eccl | c2err onlyf | c2err onlyl |
| ECCREG2 | 1E | - | cdecc | eccmode | c2fgtype [4] | c2fgtype [3] | c2fgtype [2] | c2fgtype [1] | c2fgtype [0] |
| ECCREG3 | 1F | - | - | - | - | SETFLG [3] | SETFLG [2] | SETFLG [1] | SETFLG [0] |
| **Address Setting on MICOM Direct Access Buffer Mode** (Read/Write) | | | | | | | | | |
| WADRH | 20 | - | - | - | ADR20 | ADR19 | ADR18 | ADR17 | ADR16 |
| WADRM | 21 | ADR15 | ADR14 | ADR13 | ADR12 | ADR11 | ADR10 | ADR9 | ADR8 |
| WADRL | 22 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 |
| **Data Write to Buffer (When MDAB = 1)** | | | | | | | | | |

**Table 2. MICOM Write Register & Read/Write Register Table (R/W unmarked; W) (Continued)**

| Name | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| WDATA | 23 | WDT7 | WDT6 | WDT5 | WDT4 | WDT3 | WDT2 | WDT1 | WDT0 |
| **RESERVED (24 - 2F)** | | | | | | | | | |
| **Buffering Start Sector Unit Number** | | | | | | | | | |
| WBAH | 30 | - | - | - | - | - | - | B9 | B8 |
| WBAL | 31 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **ECC Start Block Unit Number** | | | | | | | | | |
| WEAH | 32 | - | - | - | - | - | - | B9 | B8 |
| WEAL | 33 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Transfer Start Sector Unit Number** | | | | | | | | | |
| WTAH | 34 | - | - | - | - | - | - | B9 | B8 |
| WTAL | 35 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Over Threshold Size (Number of Sector Units)** (Read/Write) | | | | | | | | | |
| OTSH | 36 | - | - | - | - | - | - | B9 | B8 |
| OTSL | 37 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Under Threshold Size (Number of Sector Units)** (Read/Write) | | | | | | | | | |
| UTSH | 38 | - | - | - | - | - | - | B9 | B8 |
| UTSL | 39 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Number of Transfer Sectors select** (Read/Write) | | | | | | | | | |
| TNH | 3A | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
| TNL | 3B | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Size of Buffer for MICOM use select** (Read/Write) | | | | | | | | | |
| MBS | 3C | - | - | - | - | B3 | B2 | B1 | B0 |
| **Decoder Direct Data Block Copy Source Sector Address select** | | | | | | | | | |
| BCPSH | 3D | - | - | - | - | - | - | B9 | B8 |
| BCPSL | 3E | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Reserved (3F)** | | | | | | | | | |
| **Decoder Direct Data Block Copy Target Sector Address select** | | | | | | | | | |
| BCPTH | 40 | - | - | - | - | - | - | B9 | B8 |
| BCPTL | 41 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Descramble Start Sector Unit Number** | | | | | | | | | |
| WDAH | 42 | - | - | - | - | - | - | B9 | B8 |
| WDAL | 43 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

**Table 2. MICOM Write Register & Read/Write Register Table (R/W unmarked; W) (Continued)**

| Name | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| **RESERVED (44 - 49)** | | | | | | | | | |
| USERREG | **RESERVED (A0 - A7)** | | | | | | | | |
| | A8 | - | - | TSTWRD | ECTEST | - | - | - | - |
| | **RESERVED (A9)** | | | | | | | | |
| | AA | MONITOR3 | MONITOR2 | MONITOR1 | MONITOR0 | MPRSTZ | TSTENDMUX | TSTPOREND | TSTPIRENED |
| | **RESERVED (AB - AD)** | | | | | | | | |
| | AE | REGEG | ACKEG | STREG | TOSEG | DTREG | - | TSTID | TSTIDSY |
| | **RESERVED (AF - BF)** | | | | | | | | |
| | C0 | PWM07 | PWM06 | PWM05 | PWM04 | PWM03 | PWM02 | PWM01 | PWM00 |
| | C1 | PWM17 | PWM16 | PWM15 | PWM14 | PWM13 | PWM12 | PWM11 | PWM10 |
| | C2 | PWM27 | PWM26 | PWM25 | PWM24 | PWM23 | PWM22 | PWM21 | PWM20 |
| | C3 | PWM37 | PWM36 | PWM35 | PWM34 | PWM33 | PWM32 | PWM31 | PWM30 |
| | C4 | PWM47 | PWM46 | PWM45 | PWM44 | PWM43 | PWM42 | PWM41 | PWM40 |
| | C5 | PWM57 | PWM56 | PWM55 | PWM54 | PWM53 | PWM52 | PWM51 | PWM50 |
| | C6 | PWM67 | PWM66 | PWM65 | PWM64 | PWM63 | PWM62 | PWM61 | PWM60 |
| | C7 | PWM77 | PWM76 | PWM75 | PWM74 | PWM73 | PWM72 | PWM71 | PWM70 |
| | C8 | CAVCKSEL1 | CAVCKSEL0 | - | - | - | CAVVAL10 | CAVVAL9 | CAVVAL8 |
| | C9 | CAVVAL7 | CAVVAL6 | CAVVAL5 | CAVVAL4 | CAVVAL3 | CAVVAL2 | CAVVAL1 | CAVVAL0 |
| | **RESERVED (CA - DF)** | | | | | | | | |
| **RESERVED (E0 - EF)** | | | | | | | | | |

## MICOM READ REGISTER & READ/WRITE REGISTER

**Table 3. MICOM Read Register & Read/Write Register Table (R/W unmarked; R)**

| Name | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| INTSTAT1 | 4A | DVDSINT | DSINT | TOSINT | TRSCMPLT | ECCMPLT | EMPTY | OVER | UNDER |
| INTSTAT2 | 4B | SBQINT | MCPINT | - | - | - | - | - | - |
| ERRSTAT | 4C | EIDERR | DSIERR | IDCONERR | - | ECCERR | EDCFLG | - | SBQERR |
| DVDSTATUS | 4D | - | - | - | - | SYOK | NOSY | ILSY | - |
| DVDSVSTAT | 4E | - | LOCK | GFS | - | - | - | - | - |
| **RESERVED (4F)** | | | | | | | | | |
| CDSUBQ | 50 | SBQ79 | SBQ78 | SBQ77 | SBQ76 | SBQ75 | SBQ74 | SBQ73 | SBQ72 |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| | 59 | SBQ07 | SBQ06 | SBQ05 | SBQ04 | SBQ03 | SBQ02 | SBQ01 | SBQ00 |
| **RESERVED (5A - 5F)** | | | | | | | | | |
| SEEKIDADR | 60 | SID31 | SID30 | SID29 | SID28 | SID27 | SID26 | SID25 | SID24 |
| | 61 | SID23 | SID22 | SID21 | SID20 | SID19 | SID18 | SID17 | SID16 |
| | 62 | SID15 | SID14 | SID13 | SID12 | SID11 | SID10 | SID09 | SID08 |
| | 63 | SID07 | SID06 | SID05 | SID04 | SID03 | SID02 | SID01 | SID00 |
| TRANSIDADR | 64 | TID31 | TID30 | TID29 | TID28 | TID27 | TID26 | TID25 | TID24 |
| | 65 | TID23 | TID22 | TID21 | TID20 | TID19 | TID18 | TID17 | TID16 |
| | 66 | TID15 | TID14 | TID13 | TID12 | TID11 | TID10 | TID09 | TID08 |
| | 67 | TID07 | TID06 | TID05 | TID04 | TID03 | TID02 | TID01 | TID00 |
| **RESERVED (68 - 6F)** | | | | | | | | | |
| **Address Reading on Micom Direct Access Buffer Mode** (Read/Write) | | | | | | | | | |
| RADRH | 70 | - | - | - | ADR20 | ADR19 | ADR18 | ADR17 | ADR16 |
| RADRM | 71 | ADR15 | ADR14 | ADR13 | ADR12 | ADR11 | ADR10 | ADR9 | ADR8 |
| RADRL | 72 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 |
| **Data Read from Buffer** | | | | | | | | | |
| RDATA | 73 | RDT7 | RDT6 | RDT5 | RDT4 | RDT3 | RDT2 | RDT1 | RDT0 |
| **RESERVED (74 - 7F)** | | | | | | | | | |
| **Buffering End Sector Unit Number** | | | | | | | | | |
| RWAH | 80 | - | - | - | - | - | - | B9 | B8 |
| RWAL | 81 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **ECC End Sector Unit Number** | | | | | | | | | |
| REAH | 82 | - | - | - | - | - | - | B9 | B8 |
| REAL | 83 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Transferring End Sector Unit Number** | | | | | | | | | |
| RTAH | 84 | - | - | - | - | - | - | B9 | B8 |
| RTAL | 85 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **DSI Unit Number** | | | | | | | | | |
| DSIH | 86 | - | - | - | - | - | - | B9 | B8 |
| DSIL | 87 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **Descramble End Sector Unit Number** | | | | | | | | | |
| RDAH | 88 | - | - | - | - | - | - | B9 | B8 |
| RDAL | 89 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

**Table 3. MICOM Read Register & Read/Write Register Table (R/W unmarked; R) (Continued)**

| Name | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| **RESERVED (8A - 93)** | | | | | | | | | |
| **ECC End ID Address** | | | | | | | | | |
| EEIDA | 94 | ID31 | ID30 | ID29 | ID28 | ID27 | ID26 | ID25 | ID24 |
| | 95 | ID23 | ID22 | ID21 | ID20 | ID19 | ID18 | ID17 | ID16 |
| | 96 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID09 | ID08 |
| | 97 | ID07 | ID06 | ID05 | ID04 | ID03 | ID02 | ID01 | ID00 |
| **RESERVED (98 - 9B)** | | | | | | | | | |
| **DSI ID Address** | | | | | | | | | |
| DSIDA | 9C | ID31 | ID30 | ID29 | ID28 | ID27 | ID26 | ID25 | ID24 |
| | 9D | ID23 | ID22 | ID21 | ID20 | ID19 | ID18 | ID17 | ID16 |
| | 9E | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID09 | ID08 |
| | 9F | ID07 | ID06 | ID05 | ID04 | ID03 | ID02 | ID01 | ID00 |
| **Remaining Data Size (Number of Sector Units)** | | | | | | | | | |
| RDSH | F0 | - | - | - | - | -- | - | B9 | B8 |
| RDSL | F1 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| **RESERVED (F2 - FF)** | | | | | | | | | |

## MICOM REGISTER DESCRIPTION

### MICOM WRITE REGISTER & READ/WRITE REGISTER (R/W UNMARKED; W)

| INTCTL1: Interrupt Control Register 1 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 0A | DVDIEN | DSIEN | TOSEN | TSCMPTEN | ECCIEN | EMPTYEN | OVEREN | UNDEREN |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

< DVD Interrupt Masking Register >

- DVDIEN: DVD ID-sync interrupt request enable
  Enable/Disable control bit of the ID-sync Interrupt generated in the DVD decoder.
  1: Enable 0: Disable

- DSIEN: DSI interrupt
  1: Enable 0: Disable

- TOSEN: Top of sector interrupt request enable
  Enable/Disable control bit of the interrupt that marks the first data in the sector being transferred from the DVD decoder to the A/V decoder or host.
  1: Enable 0: Disable

- TSCMPTEN: Transfer complete interrupt request enable
  Control bit for Interrupt signal generation when transfer is complete for the number of bytes demanded in DVD ROM application (TNH, L).
  1: Enable 0: Disable

- ECCIEN: ECC complete interrupt request enable
  Enable/Disable control bit of the ECC complete interrupt generated in the DVD decoder.
  1: Enable 0: Disable

- EMPTYEN: Buffer memory empty interrupt (for transfer) request enable
  1: Enable 0: Disable

- OVEREN: Buffer memory over interrupt request enable
  Interrupt request enable generated when the filled area in the buffer memory is more than the over threshold size (OTS) set by MICOM (hysteresis).
  1: Enable 0: Disable

- UNDEREN: Buffer memory under interrupt request enable
  Interrupt request enable generated when the filled area in the buffer memory is less than the under threshold size set by MICOM (hysteresis).
  1: Enable 0: Disable

| INTCTL2: Interrupt Control Register 2 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 0B | SBQIEN | MCPEN | - | - | - | - | - | - |
| Reset Value | 0 | 0 | - | - | - | - | - | - |

< CD interrupt Masking Register >

- SBQIEN: CD subcode-sync interrupt request enable
  Enable/Disable control bit for subcode-sync interrupt generated in the CD decoder.
  1: Enable 0: Disable

- MCPEN: Micom block copy mode
  1: Enable 0: Disable

| INTCTL3: Interrupt Control Register 3 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 0C | - | - | - | IFRQ2 | IFRQ1 | IFRQ0 | - | CLRINT |
| Reset Value | - | - | - | 0 | 0 | 0 | - | 1 |

- IFRQ2 - 0: Interrupt request frequency select register (only applicable to DVDSINT)

| IFRQ2 | IFRQ1 | IFRQ0 | Number of Interrupts/Number of ID Sectors |
|---|---|---|---|
| 0 | 0 | 0 | 1/1 ID sector |
| 0 | 0 | 1 | 1/2 ID sectors |
| 0 | 1 | 0 | 1/4 ID sectors |
| 0 | 1 | 1 | 1/8 ID sectors |
| 1 | 0 | 0 | 1/16 ID sectors |
| Other | | | Reserved |

- CLRINT: Interrupt clear register
  Decides whether or not to clear the interrupt status register after MICOM has read it.
  1: Clear 0: Don't clear

| SYSCONT1: System Control Register 1 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 0D | MRESET | - | - | RCF1 | RCF0 | DISC2 | DISC1 | DISC0 |
| Reset Value | 1 | - | - | 0 | 0 | 1 | 0 | 0 |

- MRESET: Master reset → reset Z-decoder.
  (Setting all registers to predefined reset value. Same as ZRST) the decoder automatically sets to "1" after MICOM turns on the reset.
  0: Reset on, 1: Reset off

- RCF1 - 0: RAM configuration → buffer size select.

| RCF1 | RCF0 | DRAM Configuration |
|---|---|---|
| 0 | 0 | 4Mbits |
| 0 | 1 | 8Mbits |
| 1 | 0 | N.A |
| 1 | 1 | 16Mbits |

- Z-Decoder control register.
  DISC2 - 0: Shows the operating disc type.

| DISC2 | DISC1 | DISC0 | Disc Type |
|---|---|---|---|
| 1 | 0 | 0 | DVD |
| 1 | 1 | 0 | DVD-ROM |
| 0 | 0 | 0 | CD-DA |
| 0 | 0 | 1 | V-CD |
| 0 | 1 | 0 | CD-ROM |
| Other | | | Reserved |

| USERCONT1: User Control Register1 (Sync Control) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 0E | WIDEWIN | GFSPRO | SYNCDEC | ISPROT | FNADJ | RFNCON | - | - |
| Reset Value | 1 | 1 | 1 | 0 | 1 | 1 | - | - |

- WIDEWIN: Sync protection window control
  H → If frame sync doesn't occur for more than the insertion number (N) designated by the protection window, again set the widest protection window for sync detection. If sync is detected, immediately correct to that value and protect to the window with the selected width. If sync isn't detected, immediately cancel window.
  L → Find sync by immediately cancelling the protection window without wide window operating mode.

- GFSPRO: Good frame sync detecting conditions
  H → Complete match between detected sync and inserted sync
  L → A ±1 difference between detected sync and inserted sync

- SYNCDEC: Frame sync detecting conditions
  H → Sync detect by sync code (32bit)
  L → Sync detect using specified pattern (22bit)

- ISPROT: ID sync protection starting conditions
  H → Immediately start ID sync protection when sector sync is detected.
  L → ID Sync protection is started when ID sync is detected in the expected frame after frame sync protection has begun. Frame number (FN) match:/S0 detected in FN0 set to low after system reset.

- FNADJ: Frame number (address) correcting conditions
  H → Correct counter value within a ±5 difference between the detected frame number and frame counter value.
  L → Correct counter value within a ±2 difference.
  Valid conditions: Frame sync continuity must be maintained. If continuity isn't maintained, it is changed to insertion mode.

- RFNCON: Frame number correction to the detected value.
  H → Frame number correction (if detected frame number is continuous for more than 3 times)
  L → Frame number correction (according to FNADJ conditions)
  Valid conditions: Frame sync continuity must be maintained. If continuity isn't maintained, it is changed to insertion mode.

| USERCONT2: User Con. Register2 (Channel Clock PLL Control) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 0F | ABTH7 | ABTH6 | ABTH5 | ABTH4 | ABTH3 | ABTH2 | ABTH1 | ABTH0 |
| Reset Value | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

- BTH[7:0]
  : Flag generated if the absolute value of the input data difference (|L0-L1|) is larger than the set ABTH value during L-ch/ R-ch data serial output.
  : If the flag pattern is

0 0 1 1 0 0 ← Flag

|L0-L1| |L1-L2| |L2-L3| |L3-L4| |L4-L5| |L5-L6| ← Data

→ L3 = (L2+L4)/2

0 0 1 1 1 0 ← Flag

|L0-L1| |L1-L2| |L2-L3| |L3-L4| |L4-L5| |L5-L6| ← Data

→ L3 = (L2+L5)/2, L4 = (L3+L5)/2

| DVDDSET: DVD Decoder Set (Sync Detect Conditions) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 10 | - | - | FWSEL1 | FWSEL0 | FGSEL1 | FGSEL0 | IGSEL1 | IGSEL0 |
| Reset Value | - | - | 0 | 0 | 0 | 0 | 0 | 0 |

- FWSEL1 - 0: Frame sync protection window section select

| FWSEL1 | FWSEL0 | Frame Sync Protection Window (DVD) | Frame Sync Protection Window (CD) |
|---|---|---|---|
| 0 | 0 | ± 6 clocks | ± 3 clocks |
| 0 | 1 | ± 12 clocks | ± 6 clocks |
| 1 | 0 | ± 20 clocks | ± 10 clocks |
| 1 | 1 | ± 24 clocks | ± 12 clocks |

- FGSEL1 - 0: Number of frame sync inserted frames

| FGSEL1 | FGSEL0 | Number of Frame Sync Inserted Frames |
|---|---|---|
| 0 | 0 | 4 Frames |
| 0 | 1 | 13 Frames |
| 1 | 0 | 16 Frames |
| 1 | 1 | 28 Frames |

- IGSEL1 - 0: Number of ID sync inserted sectors

| IGSEL1 | IGSEL0 | Number of ID Sync Inserted Sectors |
|---|---|---|
| 0 | 0 | 1 Sector |
| 0 | 1 | 2 Sectors |
| 1 | 0 | 3 Sectors |
| 1 | 1 | 4 Sectors |

| DVDCONTROL1: DVD Decoder (Sync) Control Register 1 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 11 | DSCREN | STRST | - | - | INSEN | WNDEN | WNDRT | FCLDS |
| Reset value | 1 | 0 | - | - | 1 | 1 | 0 | 1 |

- DSCREN: Descramble on/off
  1: Descramble on
  0: Descramble off

- STRST: Forced TR mode cancellation
  1: Cancel
  0: Normal

- INSEN: Insert enable
  1: Carry out frame, ID sync insertion.
  0: Don't carry out sync insertion.

- WNDEN: Window enable (frame)
  1: Enable sync protection window. Sync detected outside the window is illegal, and isn't used in resets such as insertion timing. If illegal syncs are consecutively found N times, the protection window is reset and opened.
  0: Open the window and make all detected syncs valid.

- WNDRT: Window reset
  Window is opened if this bit is 1. It is used when you want to lock the window quickly by detecting new sync during track jump.

- FCLDS: Frame counter value load conditions
  1: Load the frame counter value continuously detected while continuity was being maintained.
  0: Load the frame counter value detected within the frwin section while continuity was being maintained. In other sections, load the inserted frame counter.

| DVDCONTROL2: DVD Control Register 2 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 12 | WRST | TRST | ECCST | ECNEGLT | ECMOD2 | ECMOD1 | ECMOD0 | MCPST |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

- WRST: Enables/Disables EFM demodulated data write to the buffer.
  1: Buffer write enable
  0: Buffer write disable

- TRST: Data transfer enable/disable from the buffer to the A/V decoder or host.
  1: Transfer enable
  0: Transfer disable

- ECCST: Error correction enable/disable.
  1: Error correction enable
  0: Error correction disable

- ECNEGLT: Disregard error correction (used when error still remains in an ECC completed block, but MICOM decides an ECC retry isn't necessary.)
  1: Repeat error correction (until ECC stop {ECCST = '0'} or {ECNEGLT = '1'})
  0: Disregard error correction (skip current correction block and move to next block.)

- ECMOD2 - 0: Error correction mode select

| ECMOD2 | ECMOD1 | ECMOD0 | Disc Speed |
|---|---|---|---|
| 0 | 0 | 0 | No error correction |
| 0 | 0 | 1 | PI+PO |
| 0 | 1 | 0 | PI+PO+PI (normal) |
| 0 | 1 | 1 | PI+PO+PI+PO |
| 1 | 0 | 0 | Repeat correction (PIPO) |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | X | |

  In repeat correction mode (ECMOD2 = '1'), if errors still exist after correction and there is enough buffer space, ECC is automatically retried until the ECCNEGLT signal is input. (buffer space is determined by MICOM)

- MCPST: MICOM block copy start command
  When it is '1', the decoder automatically moves 1 sector of data in the MICOM-selected address.
  MCPEND is output when the operation is complete, and MICOM resets the MCPST bit to '0'.

| CLVCONTROL1: CLV Control Register 1 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 13 | PGAIN1 | PGAIN0 | SGAIN1 | SGAIN0 | - | - | - | - |
| Reset Value | 0 | 0 | 0 | 0 | - | - | - | - |

- PGAIN(1:0): DVD/CD CLV's MDP gain select

| PGAIN1 | PGAIN0 | MDP Gain |
|---|---|---|
| 0 | 0 | -6dB |
| 0 | 1 | -12dB |
| 1 | 0 | -18dB |
| 1 | 1 | 0dB |

- SGAIN(1:0): DVD/CD CLV's MDS gain select and CAV control's MDS gain select.

| SGAIN1 | SGAIN0 | MDS Gain |
|---|---|---|
| 0 | 0 | -6dB |
| 0 | 1 | -12dB |
| 1 | 0 | -18dB |
| 1 | 1 | 0dB |

| CLVCONTROL2: CLV Control Register 2 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 14 | MDSCON1 | MDSCON0 | PLLC1 | PLLC0 | - | MDPC | PRES1 | PRES0 |
| Reset Value | 0 | 0 | 0 | 0 | - | 0 | 0 | 0 |

- MDSCON(1:0): DVD/CD CLV's MDS linear motion range select

| **MDSCON1** | **MDSCON0** | **Linear Range** | |
|---|---|---|---|
| | | **DVDROM** | **CDROM** |
| 0 | 0 | ±9% | ±4.5% |
| 0 | 1 | ±18% | ±9% |
| 1 | 0 | ±36% | ±18% |
| 1 | 1 | Reserve | ±33% |

- PLLC(1:0): Threshold value select for DVD/CD pll lock signal cancellation

| **PLLC1** | **PLLC0** | **Threshold** |
|---|---|---|
| 0 | 0 | Pll lock falling after WFCK 16 |
| 0 | 1 | Pll lock falling after WFCK 32 |
| 1 | 0 | Pll lock falling after WFCK 64 |
| 1 | 1 | Pll lock falling after WFCK 128 |

- MDPC: MDP output select outside of MDS linear range

| MDPC | Operation |
|---|---|
| 0 | Error signal output outside the MDS linear range |
| 1 | Hi-Z output outside the MDS linear range |

- PRES(1:0): WFCK/RFCK reference signal for MDP select within CLVP mode of DVD/CD CLV

| **PRES1** | **PRES0** | **WFCK Standard** | **RFCK Standard** |
|---|---|---|---|
| 0 | 0 | WFCK/2 | RFCK/2 |
| 0 | 1 | WFCK/4 | RFCK/4 |
| 1 | 0 | WFCK/8 | RFCK/8 |
| 1 | 1 | WFCK/16 | RFCK/16 |

| CLVCONTROL3: CLV Control Register 3 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 15 | FALTHR1 | FALTHR0 | RISTHR1 | RISTHR0 | REFSEL | SERVOC | CLVC1 | CLVC0 |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- FALTHR(1:0): DVD/CD's CLV lock signal falling time select

| FALTHR1 | FALTHR0 | Threshold |
|---|---|---|
| 0 | 0 | CLV lock falling after WFCK/RFCK 32 |
| 0 | 1 | CLV lock falling after WFCK/RFCK 64 |
| 1 | 0 | CLV lock falling after WFCK/RFCK 128 |
| 1 | 1 | CLV lock falling after WFCK/RFCK 256 |

- RISTHR(1:0): DVD/CD's CLV lock signal rising time select

| RISTHR1 | RISTHR0 | Threshold |
|---|---|---|
| 0 | 0 | CLV lock rising after WFCK/RFCK 1 |
| 0 | 1 | CLV lock rising after WFCK/RFCK 2 |
| 1 | 0 | CLV lock rising after WFCK/RFCK 4 |
| 1 | 1 | CLV lock rising after WFCK/RFCK 8 |

- REFSEL: DVD/CD's CLV lock signal generating GFS sample signal select

| REFSEL | CLV Lock Reference Signal |
|---|---|
| 0 | WFCK |
| 1 | RFCK |

- SERVOC: DVD/CD's servo lock signal falling time select
  Rising is carried out if GFS is detected twice in a row in RFCK standard.

| SERVOC | Threshold |
|---|---|
| 0 | Servo lock falling after RFCK 64 |
| 1 | Servo lock falling after RFCK 128 |

- CLVC(1:0): Mode select for DVD/CD's CLV lock on/off
  CLV Lock decision signal in wide mode: GFS
  CLV Lock decision signal in narrow mode: GFS narrow
  The narrow signal means the pll operates within the linear range selected by MDSCON(1:0). Narrow means GFS = high, and the 'not saturated' condition.

| CLVC1 | CLVC2 | CLVLOCK On (Active High) | CLVLOCK Off (Active Low) |
|---|---|---|---|
| 0 | 0 | Wide | Wide |
| 0 | 1 | Wide | Narrow |
| 1 | 0 | Narrow | Wide |
| 1 | 1 | Narrow | Narrow |

| CLVMODE: CLV Mode Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 16 | SDWP | SDWB | - | - | SDCM3 | SDCM2 | SDCM1 | SDCM0 |
| Reset Value | 1 | 1 | - | - | 0 | 0 | 0 | 0 |

- SDWp: Small section sample signal
  0: Sample every RFCK/4
  1: Sample every RFCK/2

- SDWb: Large section sample signal
  0: Sample every RFCK/32
  1: Sample every RFCK/16

- SDCM3 - SDCM0: CLV mode select

| SDCM3 | SDCM2 | SDCM1 | SDCM0 | CLV Mode | MDP Block | MDS Block |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | STOP | Hi-Z | Hi-Z |
| 1 | 0 | 0 | 0 | KICK | H | Hi-Z |
| 1 | 0 | 1 | 0 | BRAK | L | Hi-Z |
| 1 | 1 | 1 | 0 | CLVS | L,Z,H | Hi-Z |
| 1 | 1 | 0 | 0 | CLVH | L,Z,H | Hi-Z |
| 1 | 1 | 1 | 1 | CLVP | L,Z,H | L,H |
| 0 | 1 | 1 | 0 | CLVA | L,Z,H | L,Z,H |
| 1 | 0 | 0 | 1 | CAV | Hi-Z | L,Z,H |
| Other | | | | Reserve | | |

MDP must output to Hi-Z in stop mode.

| TRMODE: Data Transfer Mode Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 19 | IFMOD2 | IFMOD1 | IFMOD0 | - | CDIF0 | DRATE | - | DVDIF0 |
| Reset Value | 0 | 0 | 0 | - | 0 | 1 | - | 1 |

- IFMOD2 - 0: Transfer I/F method to A/V decoder or ROM decoder select

| IFMOD2 | IFMOD1 | IFMOD0 | Transfer I/F Method |
|---|---|---|---|
| 0 | 0 | 0 | C (A/V decoder: Synchronous) |
| - | - | - | Reserved |

- CDIF0: CD Interface format select

| CDIF0 | Transfer Format |
|---|---|
| 0 | Format 1 |
| 1 | Format 2 |

- DRATE: Transfer speed to A/V decoder or ROM decoder select
  1: Byte/240nS
  0: Byte/480nS
  Fixed to byte/240nS in DVD-ROM mode.

- DVDIF0: DVD interface format select

| DVDIF0 | Transfer Format | Transfer Data |
|---|---|---|
| 0 | Mode 1 | 2048 Bytes Main |
| 1 | Mode 2 | 2064 Bytes Sector |

| CDSPEED: CD Speed Control Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 1A | - | - | - | - | - | CDSPD2 | CDSPD1 | CDSPD0 |
| Reset Value | - | - | - | - | - | 0 | 0 | 0 |

- CD speed control register

| CDSPD2 | CDSPD1 | CDSPD0 | DISC Speed |
|---|---|---|---|
| 0 | 0 | 0 | 1x |
| 0 | 0 | 1 | 2x |
| 0 | 1 | 0 | 4x |
| Other | | | Reserved |

| CDMUTCNT: CD Mute Control Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 1B | CBITIN2 | CBITIN1 | CBITIN0 | DGOEN | DEMPHA | MUTE | ZCMT | ATTN |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

- CBITIN(2:0): Digital audio output control mode select
  CBITIN0 = 0: For common use (mode II)
  CBITIN1 = 0: Audio
  CBITIN2 = 0: Digital copy prohibited,
  1: Digital copy possible

- DGOEN: Digital audio output mode select
  0: Hi-Z
  1: Output

- DEMPHA: CD audio's deemphasis control
  0: Deemphasis off
  1: Deemphasis on

- MUTE: CD-DA data mute
  0: Mute off
  1: Mute on

- ZCMT: Zero cross mute control bit
  0: Zero cross mute on
  1: Zero cross mute off

- ATTN: Attenuation on/off
  0: Attenuation off
  1: Attenuation on

| ATTN | MUTE | dB |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | -∞ |
| 1 | 0 | -12 |
| 1 | 1 | -12 |

| CDCONTROL: CD Control Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 1C | - | - | - | - | BYPASS | INFR | T3_SEL | T3_MODE |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

- BYPASS:
  H: Normal L-ch/ R-ch data serial output
  L: Error value correcting circuit application.

- INFR: Decides whether to release the frame window right after the inserted frame number set by FGSEL (1:0), or wait until after seeing a few more frame syncs detected by FWID.

  0: Release frame window right after the inserted frame number set by FGSEL (1:0). Inserted counter is reset by the frame sync detected first, and the frame window is locked again within a regular period.
  1: Don't release frame window right after the inserted frame number set by FGSE (1:0). Lock frame window when detected frame syncs are generated continuously within a regular period, after the inserted counter is reset by the frame sync detected first.

- T3_SEL: When 2T is generated in the EFM input data, and more than 4T of data is maintained before and after, decides the direction change that will increase data by 2T in either direction to change to 3T.
  H: Increase to previous 4T data direction.
  L: Increase to later 4T data direction.

- T3_MODE: Carry out 3T correction using EFM input data
  H: On
  L: Off

| CDCONTROL: CD Control Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 1D | ERAMOF | ERAMOL | maxmode 2f | maxmode 2l | c2eccf | c2eccl | c2erro onlyf | c2erro onlyl |
| Reset Value | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

- [ERAMODF]
  1: Erasure correction mode in DVD mode during max erasure generation
  Erasure correction mode in CD-first-C2 mode during max erasure generation
  0: Erasure correction mode in DVD mode during max erasure generation
  Erasure correction mode in CD-first-C2 mode during max erasure generation

- [ERAMODL] There is no DVD mode.
  1: Erasure correction mode in CD-last-C2 mode during max erasure generation
  0: Erasure correction mode in CD-last-C2 mode during max erasure generation

- [maxmode2f]
  1: Don't error correct max erasure generation in DVD mode
  Don't error correct max erasure generation in CD-first-C2 mode
  0: Error correct max erasure generation in DVD mode
  Error correct max erasure generation in CD-first-C2 mode

- [maxmode2l] There is no DVD mode.
  1: Don't error correct max erasure generation in CD-last-C2 mode
  0: Error correc2eccf] There is no DVD Mode

- [c2eccf] There is no DVD mode
  1: Don't error correct overflow generation in CD-first-C2 mode
  0: Error correct overflow generation in CD-first-C2 mode

- [c2eccl] There is no DVD mode
  1: Don't error correct overflow generation in CD-last-C2 mode
  0: Error correct overflow generation in CD-last-C2 mode

- [c2erronlyf]
  1: Only error correct in CD-first-C2 mode (Ignore flag)
  0: Error correct in CD-first-C2 mode (erasure or error)

- [c2erronlyl]
  1: Only error correct in CD-last-C2 mode
  0: Error correct in CD-last-C2 mode (erasure or error) CT max erasure generation in CD-last-C2 mode

| CDCONTROL: CD Control Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 1E | - | cdecc | eccmode | c2fgtype [4] | c2fgtype [3] | c2fgtype [2] | c2fgtype [1] | c2fgtype [0] |
| Reset Value | - | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

- [cdecc] Repeat correction in CD mode (change name to existing VCDREP bit)
  1: Repeat correction
  0: Correct once

- [eccmode]
  1: In CD repeat correction mode (cdecc = 1), don't correct errors in the firstsection, but correct the last section.
  0: Correct the errors in both the first and last sections in CD repeat correction Mode.

- c2fgtype[4:0] Flag setting condition select in CD mode
  c2fgtype[4];
  1: If maxmodc2f/maxmodc2l = "1" in CD-C2 mode, C1 flag copy [11]
  0: If maxmodc2f/maxmodc2l = "1" in CD-C2 mode, C2 flag out [01]

- c2fgtype[3];
  1: If an overflow occurs in CD-C2 mode, C1 flag copy [11]
  0: If an overflow occurs in CD-C2 mode, C2 flag out [01]

- c2fgtype[2]; CD repeat correction mode
  1: Max correcting (both error and erasure) in CD-last-C2 mode, C1 flag copt [11] → default
  0: Max correcting (both error and erasure) in CD-last-C2 mode, C2 flag out [01]

- c2fgtype[1]; CD one time correction mode
  1: Max correcting (both error and erasure) in CD-C2 mode, C1 flag copt [11] → default
  0: Max correcting (both error and erasure) in CD-C2 mode, C2 flag out [01]

- c2fgtype[0];
  1: Uncorrectable code in CD-C2 mode, C1 flag copy [11]
  0: Uncorrectable code in CD-C2 mode, C2 flag out [01]

| CDCONTROL: CD Control Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 1F | - | - | - | - | SETFLG[3] | SETFLG[2] | SETFLG[1] | SETFLG[0] |
| Reset Value | - | - | - | - | 1 | 1 | 1 | 1 |

- SETFLG[3:0]
  SETFLG[3];

  - PI flag in DVD mode
    1: Flag setting only when correction is impossible. (error or erasure) → Must be 'default'

  - C1-first flag in CD mode
    1: Flag setting only when correction is impossible (more than 2 errors)
    0: Flag setting even during 2 error correction

- SETFLG[2];

  - PO flag in DVD mode
    1: Flag setting only when correction is impossible (error or erasure) → Must be 'default'

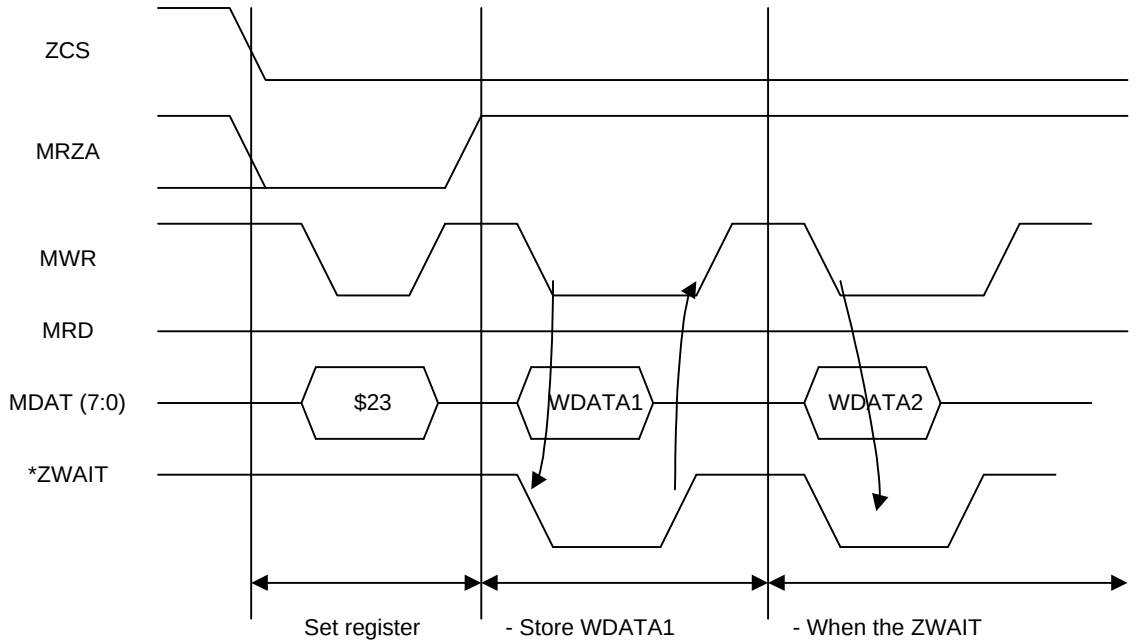
  - C2-first flag in CD mode
    1: Flag setting only when correction is impossible (more than 2 errors) → Must be 'default'

- SETFLG[1]; No DVD mode. C1-last flag in CD mode.
  1: Flag setting only when correction is impossible (more than 2 errors)
  0: Flag setting even during 2 error correction

- SETFLG[0]; No DVD mode. C1-last flag in CD mode.
  1: Flag setting only when correction is impossible (more than 2 errors) → Must be 'default'

| WADRH/M/L: Address Setting on MICOM Direct Access Buffer Mode (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 20 | - | - | - | ADR20 | ADR19 | ADR18 | ADR17 | ADR16 |
| 21 | ADR15 | ADR14 | ADR13 | ADR12 | ADR11 | ADR10 | ADR9 | ADR8 |
| 22 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 |
| WDATA: Data write to buffer (when MDAB = 1) | | | | | | | | |
| 23 | WDT7 | WDT6 | WDT5 | WDT4 | WDT3 | WDT2 | WDT1 | WDT0 |
| Reset Value | 20 - 23 register: all-zero | | | | | | | |

**Buffer Writing**




Set register ADR. $23

- Store WDATA1 (WDT7 ~ WDT0) value to $23 register.
- ZWAIT signal enable (low) until WDATA1 is completely stored in the buffer.

- When the ZWAIT signal is disabled (high), MICOM prepares the next data for transfer (WDATA2).
- $23 register pointer doesn't change. WDATA2 is stored in the register.
- WADR ($20 ~ $22)'s buffer point (ADR20 ~ 0) increases automatically.
- Enable the ZWAIT signal until WDATA2 is completely stored in the buffer pointer. MICOM stores the next value (WDATA3, ..) in the register when ZWAIT is high.

**Figure 5. Buffer Writing**

**Last Writed Address Reading**

Read the buffer pointer value (+ 1) last written in the buffer.

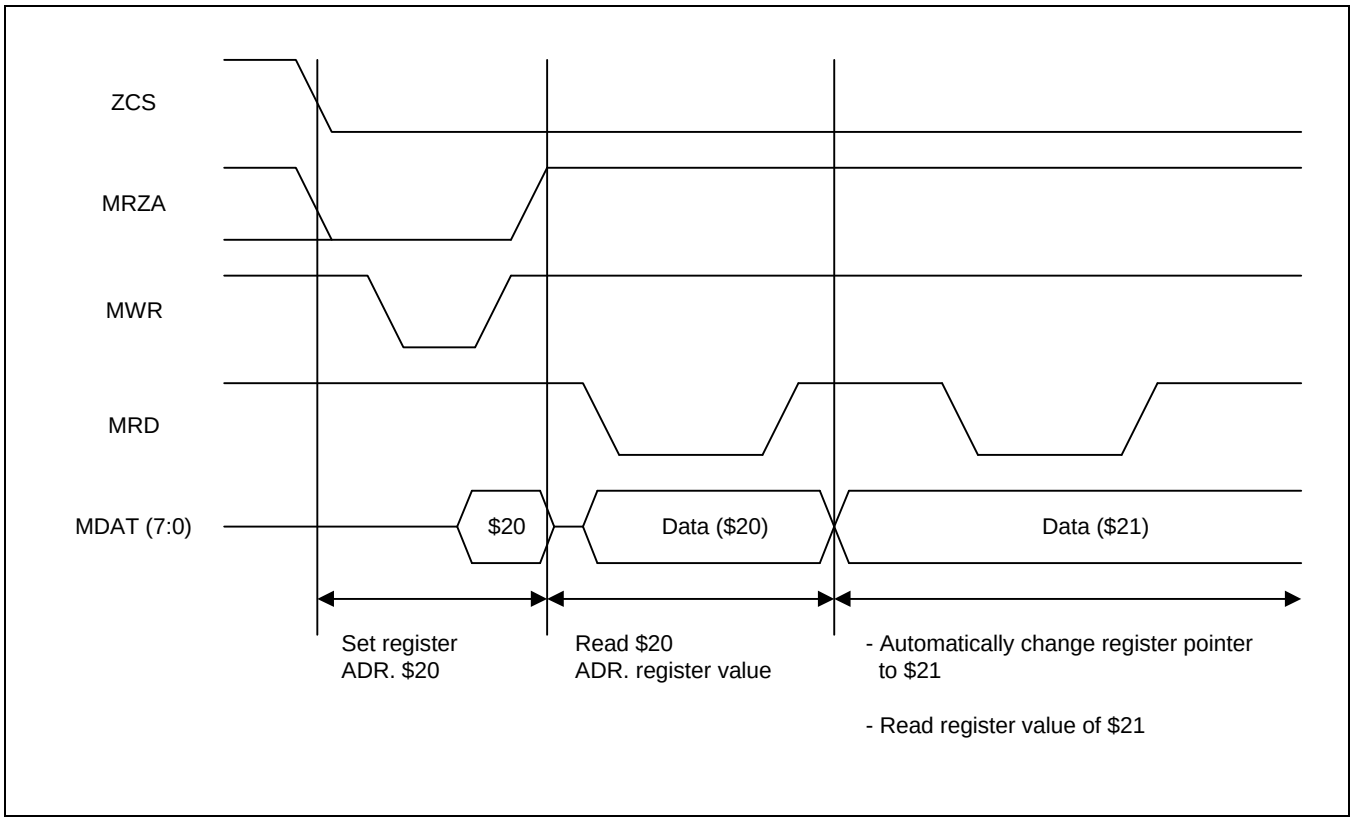



**Figure 6. Last Writed Address Reading**

| Buffering Start Sector Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 30 | B9 - B8 | | | | | | | |
| 31 | B7 - B0 | | | | | | | |
| Reset Value | 3FF | | | | | | | |

Select the start sector unit number for storing EFM data in the buffer. Set W sector unit.

| ECC Start Sector Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 32 | B9 - B8 | | | | | | | |
| 33 | B7 - B0 | | | | | | | |
| Reset Value | 3FF | | | | | | | |

Select the sector unit number for error correction. (Set in units of blocks with B3 - B0 = '0') Set X sector unit.

| Transfer Start Sector Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 34 | B9 - B8 | | | | | | | |
| 35 | B7 - B0 | | | | | | | |
| Reset Value | 1FF | | | | | | | |

Select sector unit number for starting data transfer. Set Z sector unit.

The unit number above is automatically incremented in units of sectors when all applicable start signals are enabled and completed.

Unit Number definition

B9 - 8: Bank 0 - 3

B7 - 4: Block 0 - 12

B3 - 0: Sector 0 - 15

| Over Threshold Size (Sector Unit Number) (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 36 | B9 - B8 | | | | | | | |
| 37 | B7 - B0 | | | | | | | |
| Reset Value | All High | | | | | | | |

Set buffer memory's over threshold size (maximum 16 blocks). In other words, set the maximum allowable value for the absolute value of (unit number W-unit number Z). When the section filled with memory is larger than the selected value, the Z-decoder generates an over interrupt.

| Under Threshold Size (Sector Unit Number) (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 38 | B9 - B8 | | | | | | | |
| 39 | B7 - B0 | | | | | | | |
| Reset Value | All Zero | | | | | | | |

Set buffer memory's under threshold size (maximum 16 blocks). In other words, set the minimum allowable value for the absolute value of (unit number w - unit number Z). When the section filled with memory is less than the selected value, the Z-Decoder generates an under interrupt.

| Transfer Sector Number Select (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 3A | B15 - B8 | | | | | | | |
| 3B | B7 - B0 | | | | | | | |
| Reset Value | All High | | | | | | | |

Sets the number of bytes of the data to be transferred to the A/V decoder or ROM decoder. Maximum number of sectors to be transferred is 64K sectors. After trasferring the predetermined number of sectors, the Z-decoder generates the transfer complete interrupt (TRSCMPLT).

| Buffer Size for MICOM select (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 3C | - | - | - | - | B3 | B2 | B1 | B0 |
| Reset Value | - | - | - | - | 0 | 0 | 0 | 1 |

Select the size of the buffer for MICOM. The size is in units of ECC blocks (16KBytes), and a maximum of 8 blocks is possible in bank units.

(LSB 4 bits: For DVDs '0001'[Block 1] - '1000' [Block 8]
For CDs '0001' - '0111')

The initial value is 1 block.

Bank: composed in units of 4 Mbit. There are 4 banks in a 16M bit, so a buffer for MICOM with a maximum of 32 Block (512K byte $\rightarrow$ 4Mbits) can be guaranteed.

| Decoder Direct Block Copy Source Sector Address Select (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 3D | B9 - B8 | | | | | | | |
| 3E | B7 - B0 | | | | | | | |
| Reset Value | All Zero | | | | | | | |

Source sector address which is used in the mode that automatically moves the data to be used by MICOM within the buffer in units of sectors.

| Decoder Direct Block Copy Target Sector Address Select (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 40 | B9 - B8 | | | | | | | |
| 41 | B7 - B0 | | | | | | | |
| Reset Value | All Zero | | | | | | | |

Target sector address which is used in the mode that automatically moves the data to be used by MICOM within the buffer in units of sectors.

| Descramble Start Sector Unit Number (Read/Write) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 42 | B9 - B8 | | | | | | | |
| 43 | B7 - B0 | | | | | | | |
| Reset Value | 1FF | | | | | | | |

Set descramble starting sector unit number.

The unit number is automatically incremented when all applicable start signals are enabled and completed in units of sector.

Unit number definition

B9 - 8: Bank 0 - 3
B7 - 4: Block 0 - 12
B3 - 0: Sector 0 - 15

| USERREG | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| A8 | - | - | TSTWRD | ectest | - | - | - | - |
| Reset Value | - | - | 0 | 0 | - | - | - | - |

- TSTWRD: For chip testing.
- Ectest: For ECC block simulation (let it be in default state)

| USRREG: ECC Operation Control/Memory Point Reset | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| AA | MONITOR3 | MONITOR2 | MONITOR1 | MONITOR0 | MPRSTZ | TSTENDMUX | TSTPOREND | TSTPIREND |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

- MONITOR 3 - 0: For internal signal monitoring in chip test mode.
- MPRSTZ: BUNP, DUNP, EUNP, and TUNP's initial value select register
  1: TUNP = "1FF"
  0: BUNP, DUNP, EUNP = "3FF"

  Used for stopping a mode by force during ECC's operation (PI read or PO read). When the operation is stopped, the next operation is carried out according to the specified ECC mode. In other words, if you stop the first PI process by force in PI+PO+PI mode, the PO mode is initiated, and if the PO mode is stopped by force, the next PI is initiated. If you stop during the last PI process, the next ECC block's first PI process is initiated.

- Stop operation:
  ① Tstendmux bit set to "1".
  ② Tstpirend if PI. tstporend if PO, set the bit to "1". → Stop the operation at this time.
  ③ Tstpirend or tstporend bit is set to"0".
  ④ Set tstendmux bit to "0"
  - ③ and ④ can be carried out simultaneously.

| USRREG: Data Transfer/Test Mode Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| AE | REQEG | ACKEG | STREG | TOSEG | DTEREG | - | TSTID | TSTIDSY |
| Reset Value | 0 | 0 | 0 | 0 | 0 | - | 0 | 0 |

- REQEG, ACKEG, STREG, TOSEG, DTEREG
  Selects the active mode of the transfer-related signals (DATREQ, DATACK, STROBE, TOS, DTER).

| VALUE | REQEG | ACKEG | STREG | TOSEG | DTEREG |
|---|---|---|---|---|---|
| 1 | Active High | Active High | Falling Edge | Active High | Active High |
| 0 | Active Low | Active Low | Rising Edge | Active Low | Active Low |

- TSTID, TSTIDSY
  For chip testing

| USERREG: PWM Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| C0 | PWM07 | PWM06 | PWM05 | PWM04 | PWM03 | PWM02 | PWM01 | PWM00 |
| C1 | PWM17 | PWM16 | PWM15 | PWM14 | PWM13 | PWM12 | PWM11 | PWM10 |
| C2 | PWM27 | PWM26 | PWM25 | PWM24 | PWM23 | PWM22 | PWM21 | PWM20 |
| C3 | PWM37 | PWM36 | PWM35 | PWM34 | PWM33 | PWM32 | PWM31 | PWM30 |
| C4 | PWM47 | PWM46 | PWM45 | PWM44 | PWM43 | PWM42 | PWM41 | PWM40 |
| C5 | PWM57 | PWM56 | PWM55 | PWM54 | PWM53 | PWM52 | PWM51 | PWM50 |
| C6 | PWM67 | PWM66 | PWM65 | PWM64 | PWM63 | PWM62 | PWM61 | PWM60 |
| C7 | PWM77 | PWM76 | PWM75 | PWM74 | PWM73 | PWM72 | PWM71 | PWM70 |
| Reset Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- PWM output's high pulse width is capable of changing in 0 - 255 steps.
- Resolution: XTI1 1CLK/STEP
- Address: Output pin

| Address | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|---|
| Output PIN | PWMO7 | PWMO6 | PWMO5 | PWMO4 | PWMO3 | PWMO2 | PWMO1 | PWMO0 |

| CAVCONTROL: CAV Control Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| C8 | CKSEL1 | CKSEL0 | - | - | - | CAVVAL10 | CAVVAL9 | CAVVAL8 |
| C9 | CAVVAL7 | CAVVAL6 | CAVVAL5 | CAVVAL4 | CAVVAL3 | CAVVAL2 | CAVVAL1 | CAVVAL0 |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- CKSEL(1:0): Reference clock select for CAV control
- CAVVAL(10:0): Initial value select for CAV control

| CAVCK(1) | CAVCK(0) | Nck | DISC Rotation Number Selection Range | |
|---|---|---|---|---|
| | | | DVD | CD |
| 0 | 0 | 8 | 1372.4 - 2746.5 | 215.2 - 430.7 |
| 0 | 1 | 4 | 686.2 - 1372.4 | 107.6 - 215.2 |
| 1 | 0 | 2 | 343.1 - 686.2 | 53.8 - 107.6 |
| 1 | 1 | 1 | 171.5 - 343.1 | 26.9 - 53.8 |

In CAV mode, the disc rotating speed is set according to the following formula.

DISC RPM = fsys × 10 × Nck / 1024 / CAV_REF

Here, fsys: System clock for DVD (27MHz), for CD (33.8688/8MHz)
Nck: Select clock division ratio using CAVCK[1:0]
In other words, (8 → 1/128, 4 → 1/256, 2 → 1/512, 1 → 1/1024).
CAV_REF26.16: Value defined by (1537- Ncarv).
Has a range of 1408 ≤ CAV_REF ≤ 1537.

$$Formual : CAV\_REF = \frac{XTAL \times 10 \times Nck}{1024 \times RPM}$$

Where XTAL: DVD (XTL1), CD (CK33MI/8)

Example) CAVVAL(10:0) value select for 1440 RPM

$$CAV\_REF = \frac{26.16MHz \times 10 \times 8}{1024 \times 1440} = 1419.27 = 1419$$

$$CAVVAR = 1537 - 1419 = 118 = 76H$$

The CAV_REF value in the formula above can change depending on the fsys.

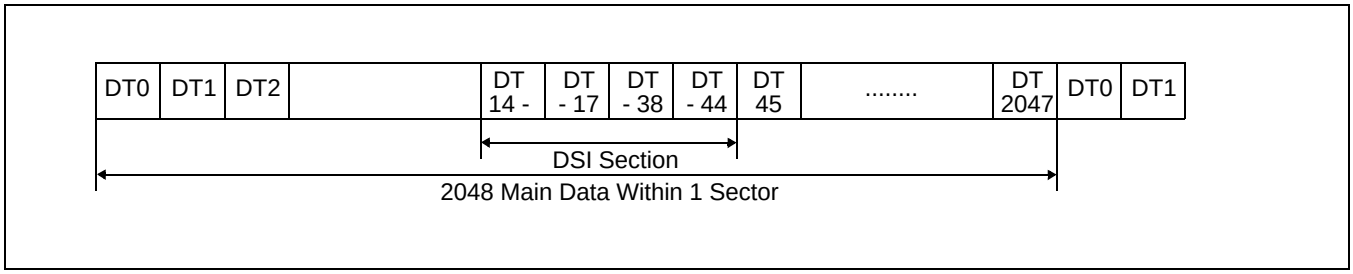
**MICOM READ REGISTER & READ/WRITE REGISTER (R/W UNMARKED; R)**

| INTSTAT1: Interrupt Status Register 1 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 4A | DVDSINT | DSINT | TOSINT | TRSCMPLT | ECCMPLT | EMPTY | OVER | UNDER |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- DVDSINT: DVD Sync interrupt request
  Set to '1' each time a sync (ID sync) is output from the DVD decoder.
  This interrupt is generated when INTCTL3 ($0C)'s CLRINT bit is "1". It is cleared to "0" when MICOM reads the bit of the register

  The first ID sync during abnormal PLAY (such as reset, search or jump) is an inserted ID sync, so you shouldn't use it as an ID interrupt.

- DSINT: DSI interrupt request
  In the DVD decoder, out of the 2048 main data,
  If the system header Start_Code (00, 00, 01, BB) starts at the 15th byte, and
  The Packet_Header (00, 00, 01, BF, **, **) starts at the 39th byte and
  Sub_Stream_id (00),
  the sector is determined to be a DSI pack and sets DSINT to 1. When CLRINT bit is 1, it is cleared to "0" when MICOM reads the bit of the register.




- Don't care in CD mode.

- TOSINT: Top of sector interrupt request
  Request that marks the beginning of the sector during data transfer.
  Cleared to '0' when CLRINT = "1" and MICOM reads the bit of the register.

- TRSCMPLT: Interrupt request sent when transfer is completed for the predetermined number of bytes.

- ECCMPLT: ECC complete interrupt request.
  Interrupt request sent when error correction is completed. Cleared to "0" when CLRINT = "1" and MICOM reads the bit of the register.

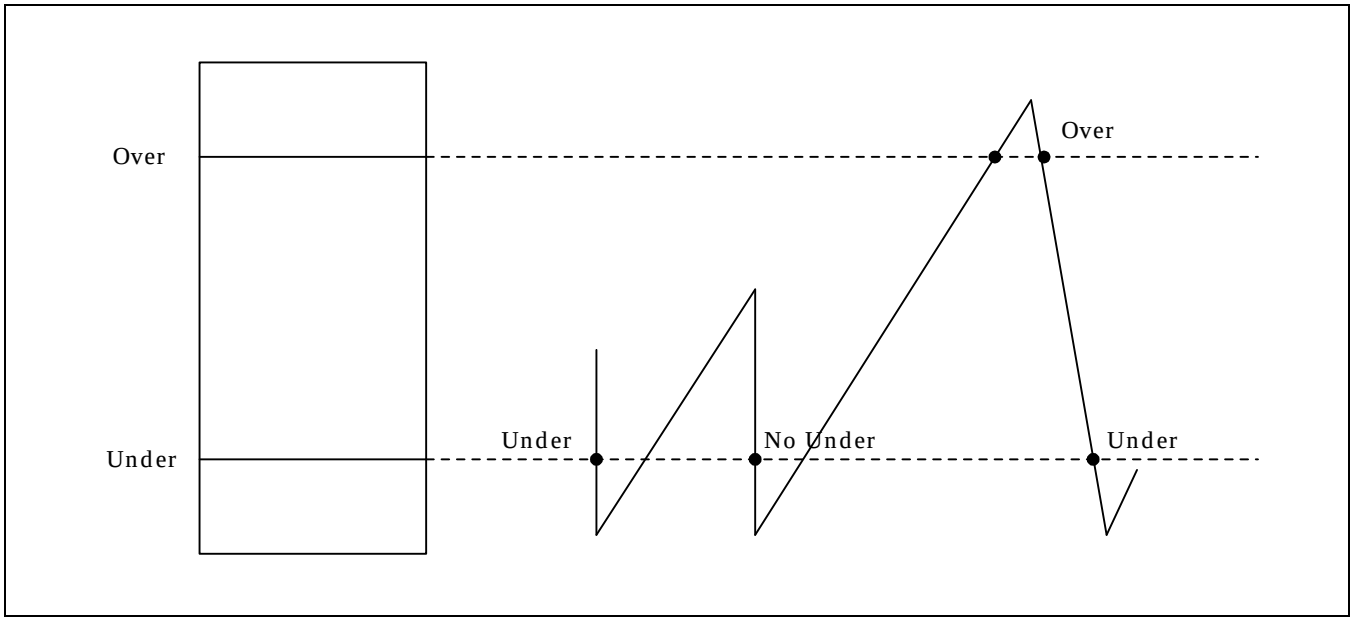
Steps EMPTY, OVER, UNDER are the same as those of DVD Sync

- EMPTY: When there aren't any data (sector) to be transferred to memory.

- OVER: Memory overflow flag. If the section filled with memory when DVD sync is being generated is above the OTS (Over Threshold Size) value, the Z-decoder sends the over interrupt. It is cleared to "0" when CLRINT = "1" and MICOM reads the bit of the register.

- UNDER: Memory underflow flag
  When the section filled with memory is under the UTS (Under Threshold Size) value, the Z-decoder sends the under interrupt.It is cleared to "0" when CLRINT = "1" and MICOM reads the bit of the register.

  - OVER, UNDER interrupt
    The new over interrupt only occurs if there is an over after an over interrupt and under interrupt have already occurred. Likewise, a new under interrupt only occurs if there is an under after an under interrupt has already occurred.



| INTSTAT2: Interrupt Status Register 2 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 4B | SBQINT | MCPINT | - | - | - | - | - | - |
| Reset Value | 0 | 0 | - | - | - | - | - | - |

- SBQINT: Subcode Q sync interrupt
  Detects subcode sync S0, S1 and generates an interrupt.

- MCPINT: MICOM block copy complete interrupt.

| ERRSTAT: ERROR Status Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 4C | EIDERR | DSIERR | IDCONERR | - | ECCERR | EDCFLG | - | SBQERR |
| Reset Value | 0 | 0 | 0 | - | 0 | 0 | - | 0 |

Various error status information can be found using the interrupt status register.

- EIDERR: You can see if there are any errors in the ID address data in the EFM demodulated data sector being input into the current buffer according to the DVDSINT (DVD ID sync interrupt) state.
  1: Errors detected (ID ECC error)
  0: No Errors

- DSIERR: You can see if there are any errors in the currently generated DSINT ($4A) according to the

- DVDSINT (DVD ID sync interrupt) state
  1: Error possible (EDC error)
  0: No errors

- IDCONERR: Continuity error presence in sector ID address of EFM data being writed into the buffer (checks the continuity of two consecutive ID numbers)
  1: Discontinuous
  0: Continuous

- ECCERR: Error presence in current error corrected data, shown by ECCMPLT (ECC complete interrupt) state.
  1: Error present (1 block's ECC results)
  0: No errors

- EDCFLG: Error presence in 2064 bytes of sector data output to the A/V decoder, shown by TOSINT (top of sector interrupt) state.
  1: Error present
  0: No errors

- SBQERR: Error presence in subcode data output to the A/V decoder, shown by SBQINT (subcode Q interrupt) state.
  1: Error present
  0: No errors

| DVDSTATUS: DVD Decoder Status Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 4D | - | - | - | - | SYOK | NOSY | ILSY | - |
| Reset Value | - | - | - | - | 0 | 0 | 0 | - |

The Sync status of the sector with the interrupt can be found by the INTSTAT1 register ($4A)'s DVDSINT interrupt.

- SYOK: "1" is read when ID sync is detected in the same timing as the inserted timing.
- NOSY: "1" is read when ID sync is not detected within window.
- ILSY: "1" is read when ID sync is detected outside window.

| DVDSVSTAT: DVD Decoder Servo Status Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 4E | - | LOCK | GFS | - | - | - | - | - |
| Reset Value | - | 0/X | 0/X | - | - | - | - | - |

- LOCK: "1" when the spindle servo is locked.
- GFS: "1" when the 16-8 frame sync (17.58kHz) from playback is found by accurate timing.

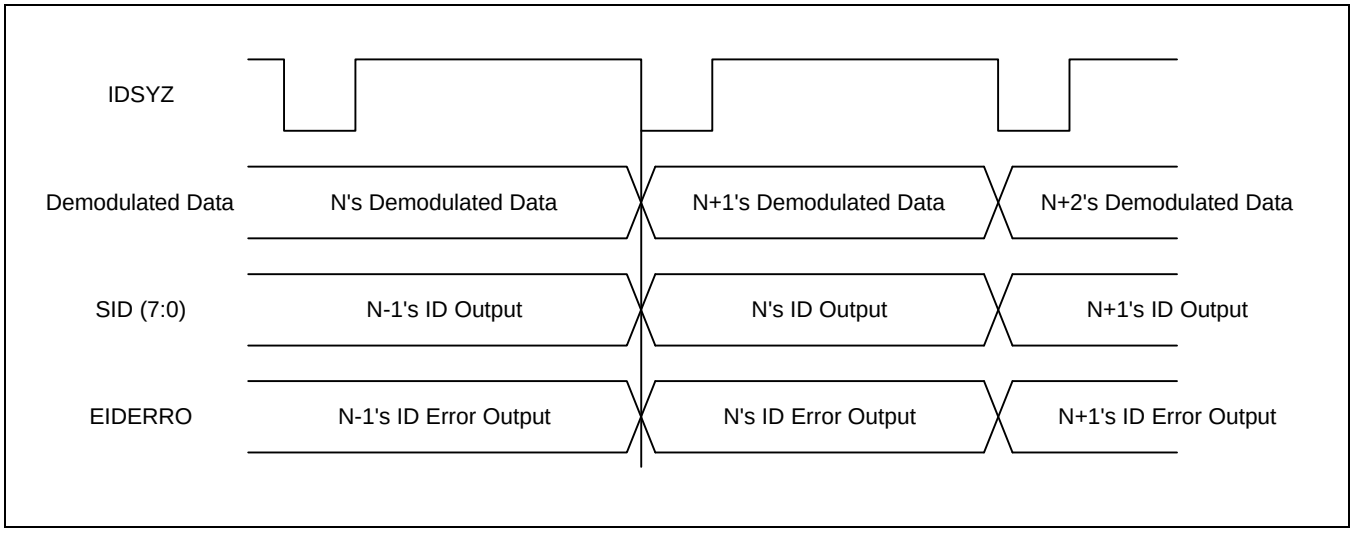
| CDSUBQ: CD-DA Subcode Q Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 50 | SBQ79 - SBQ72 | | | | | | | |
| ↓<br>↓<br>↓ | ↓<br>↓<br>↓ | | | | | | | |
| 59 | SBQ07 - SBQ00 | | | | | | | |
| Reset Value | X | X | X | X | X | X | X | X |

CD-DA Subcode Q data storage.

When S0S1 (serve code block sync) is low, this data is valid.

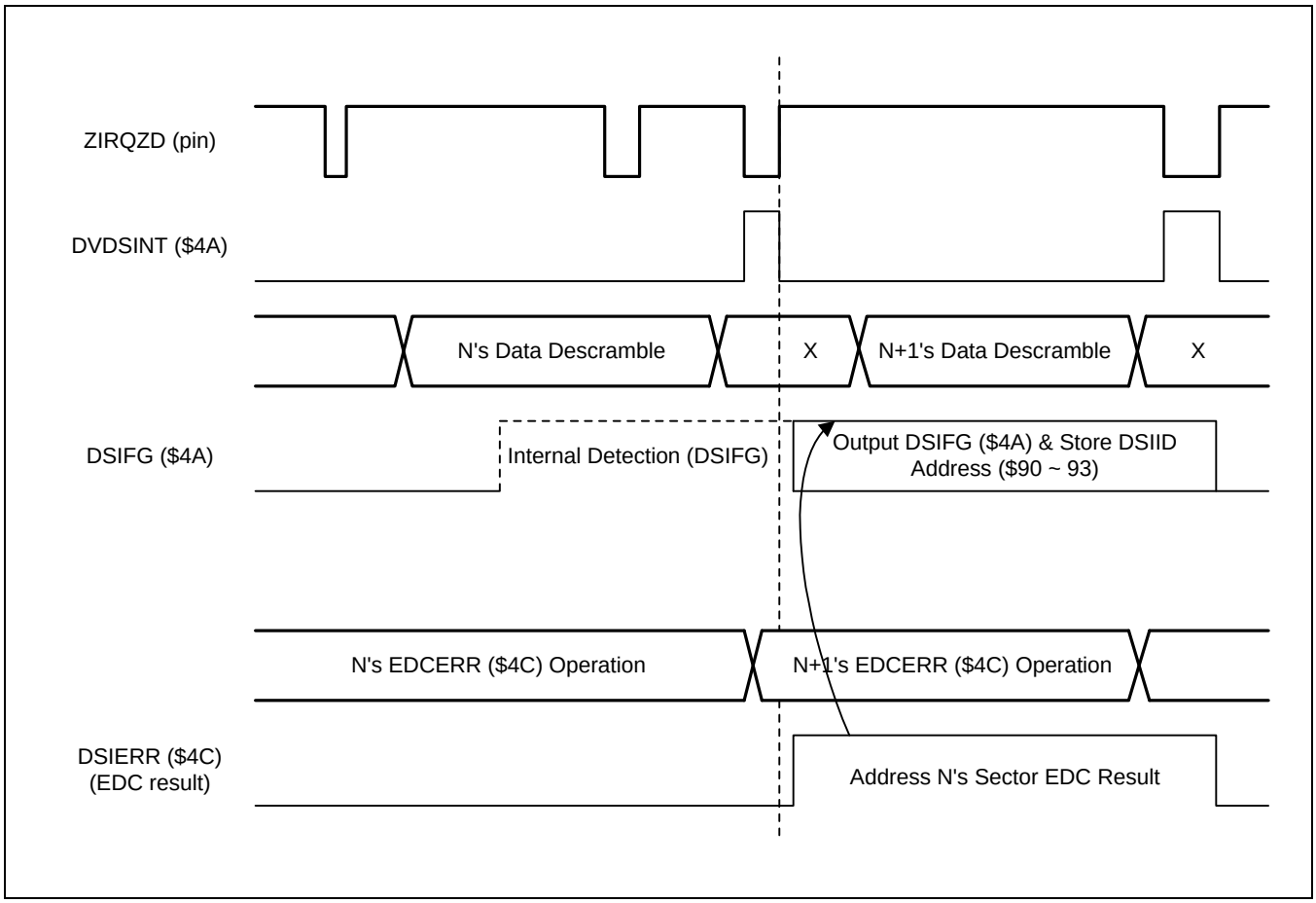
| SEEKIDADR: ID Data During EFM Demodulation | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 60 | SID31 - SID24 | | | | | | | |
| 61 | SID23 - SID16 | | | | | | | |
| 62 | SID15 - SID08 | | | | | | | |
| 63 | SID07 - SID00 | | | | | | | |
| Reset Value | X | X | X | X | X | X | X | X |

This data is used for the ID address of the data being currently EFM demodulated, seamless buffering control, and disc search. it is valid until next DVDSINT interrupt.



| TRANSIDADR: ID Data During Data Transfers to A/V Decoder | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 64 | TID31 - TID24 | | | | | | | |
| 65 | TID23 - TID16 | | | | | | | |
| 66 | TID15 - TID08 | | | | | | | |
| 67 | TID07 - TID00 | | | | | | | |
| Reset Value | X | X | X | X | X | X | X | X |

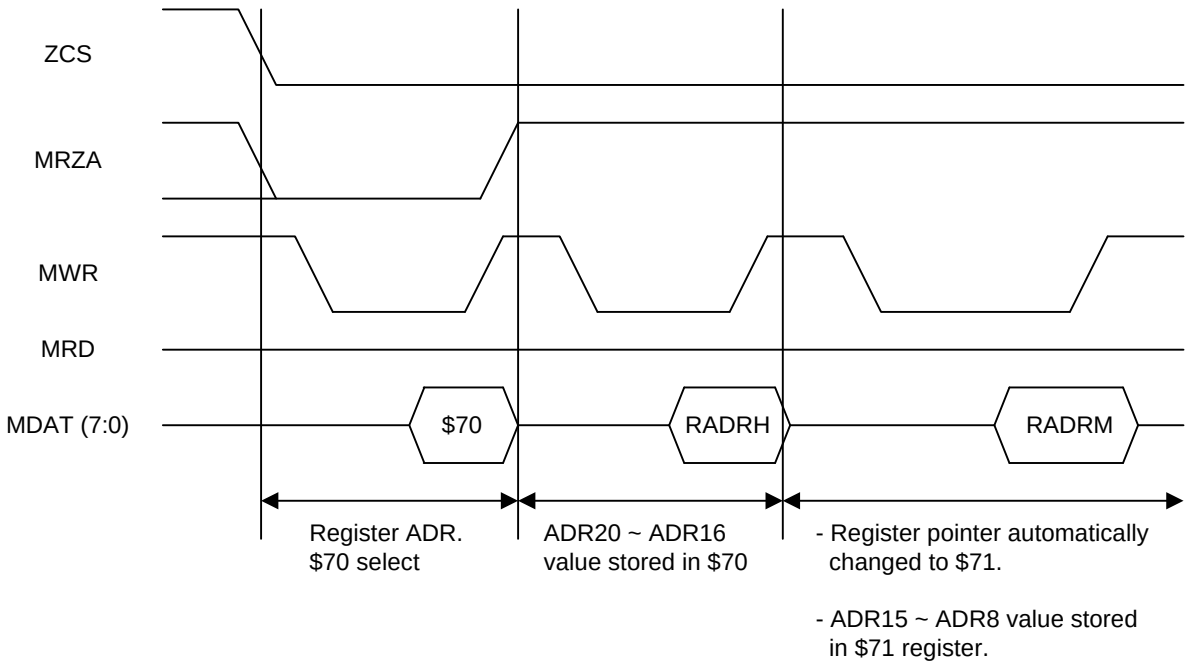
ID address of the data being output to the A/V decoder or ROM decoder after decoding. This data is valid until the next TOSINT interrupt.



| RADR, RDATA: MDAB Register for Direct Access on DRAM (MDAB = 1) (Read/Write Register) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit6** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 70 | - | - | - | ADR20 | ADR19 | ADR18 | ADR17 | ADR16 |
| 71 | ADR15 | ADR14 | ADR13 | ADR12 | ADR11 | ADR10 | ADR9 | ADR8 |
| 72 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 |
| RDATA: Data read from buffer (When MDAB = 1) | | | | | | | | |
| 73 | RDT7 | RDT6 | RDT5 | RDT4 | RDT3 | RDT2 | RDT1 | RDT0 |
| Reset Value | All Zero | | | | | | | |

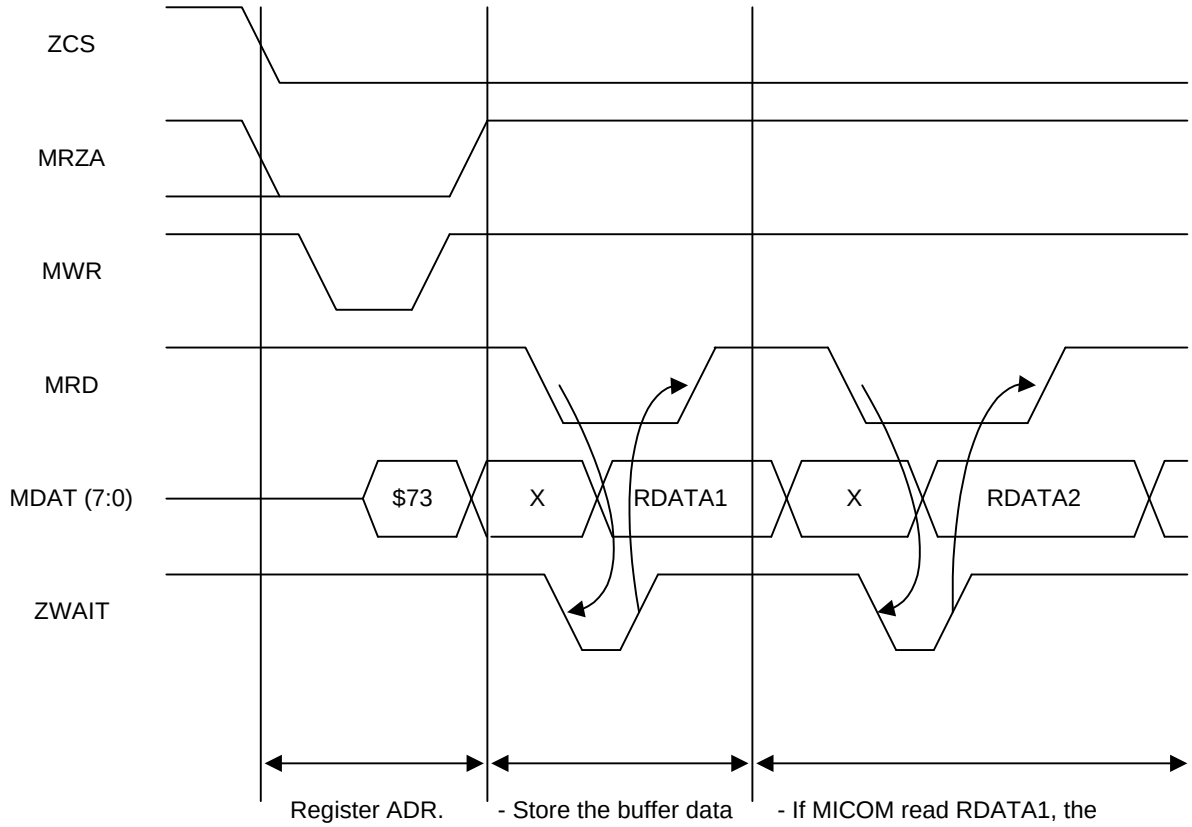
**READ ACCESS**

**Buffer Read Address Setting**




70's register address doesn't automatically increase, so it must always be set by MICOM.

**Buffer Reading**



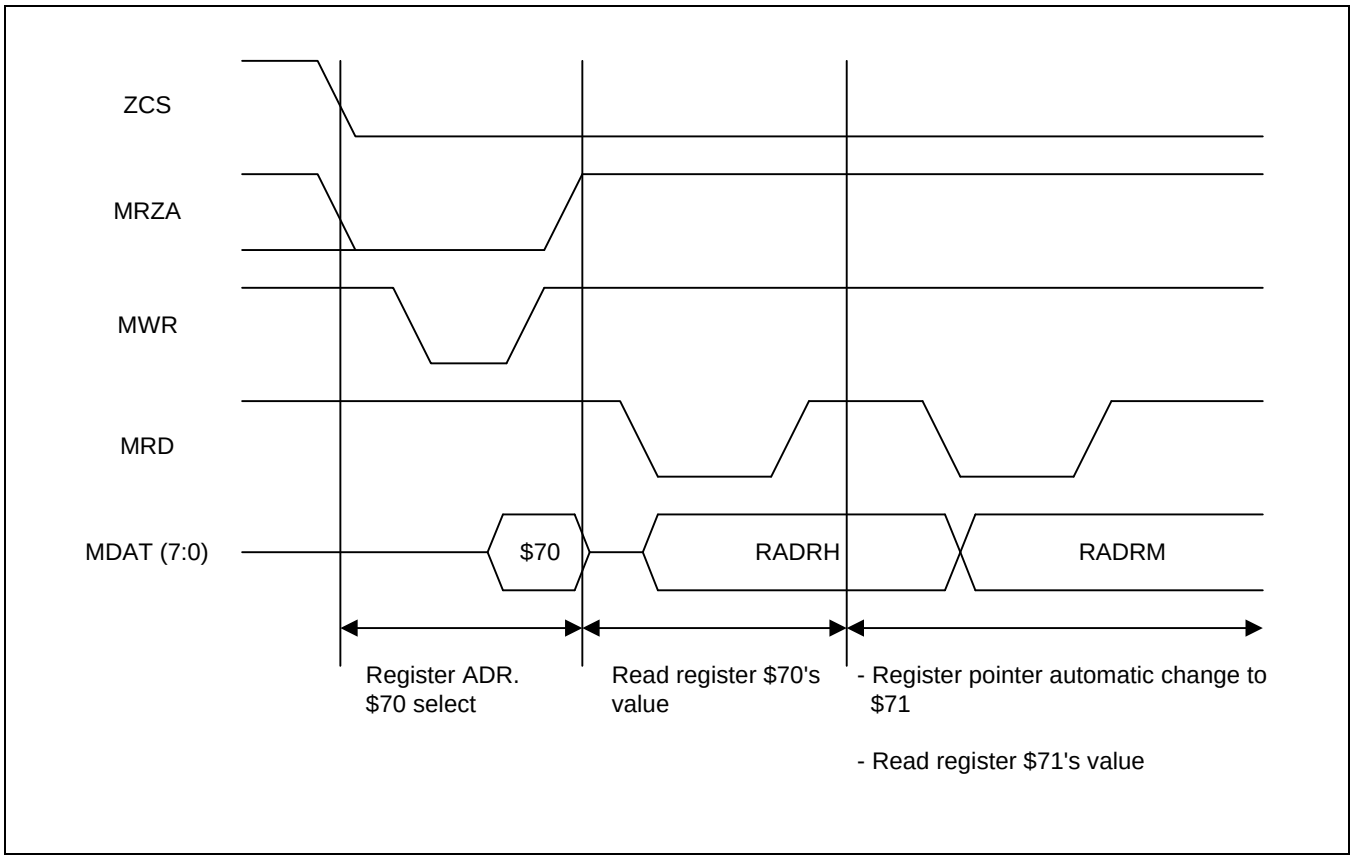

Register ADR. $73 select.

- Store the buffer data selected by RADR ($70~$72)'s buffer pointer into the register $73 (RDATA1: RDT7~RDT0).
- Enable ZWAIT (low) after MRD falling, and when RDATA1 storage in register $73 is completed, disable ZWAIT signal.
- When ZWAIT signal is disabled (high), MICOM read RDATA1 and MRD rising.

- If MICOM read RDATA1, the $73 register pointer stays the same, while the RDAT ($70~72)'s buffer pointer automatically increases to move RDATA2 to register $73.
- Enable ZWAIT (low) after MRD falling, then disable ZWAIT when RDATA2 is completely stored in register $73.
- When ZWAIT signal is disabled (high), read RDARA1 and MRD rising after RDATA2 read.

**Last Read out Address Reading**

Read the value 'Buffer Pointer+1' from the last read out.



| Buffering End Sector Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 80 | B9 - B8 | | | | | | | |
| 81 | B7 - B0 | | | | | | | |
| Reset Value | B (9:0) = 3FF | | | | | | | |

Sector unit Number of the current buffer after EFM data write completion. Valid until the next DVDSINT interrupt. 1 sector carried out while WRST low is stored. When WRST → 'L', the completed sector no.value is output (valid from first DVDSINT after WRST low).

| ECC End Sector Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 82 | B9 - B8 | | | | | | | |
| 83 | B7 - B0 | | | | | | | |
| Reset Value | B (9:0) = 3FF | | | | | | | |

Sector unit number of the current buffer after error correction is completed. Valid until the next ECCMPT interrupt. When ECCST → 'L', immediately stopped. When ECCST → 'L', (ECC completed < or ended > block no.) is read.

| Transfering End Sector Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 84 | B9 - B8 | | | | | | | |
| 85 | B7 - B0 | | | | | | | |
| Reset Value | B (9:0) = 1FF | | | | | | | |

Buffer unit number of the data continuing to be output to the A/V decoder or ROM decoder after the decoding. Valid until the next TOSINT interrupt. When TRST → 'L' outputs the transfer completed unit number.

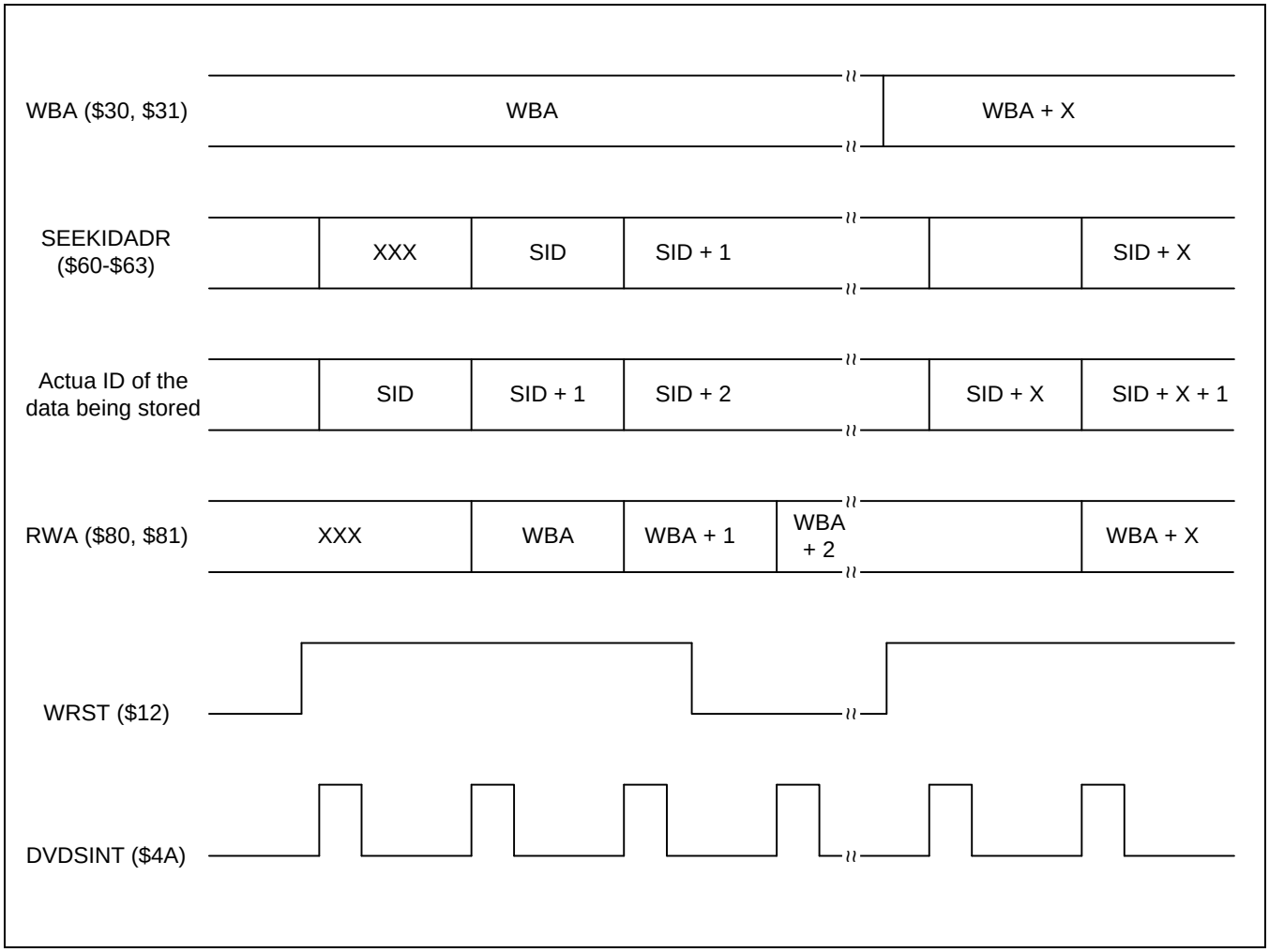
| DSI Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 86 | B9 - B8 | | | | | | | |
| 87 | B7 - B0 | | | | | | | |
| Reset Value | B (9:0) = 000 | | | | | | | |

Unit number of the buffer that stores the DSI sector after DSIFG ($4A) generation. Valid until the next DVDSINT interrupt.

## BUFFER WRITE

### During Re-search or Jump Control

- Set WRST out of write to "0", reassign the memory address to WBA, and write.



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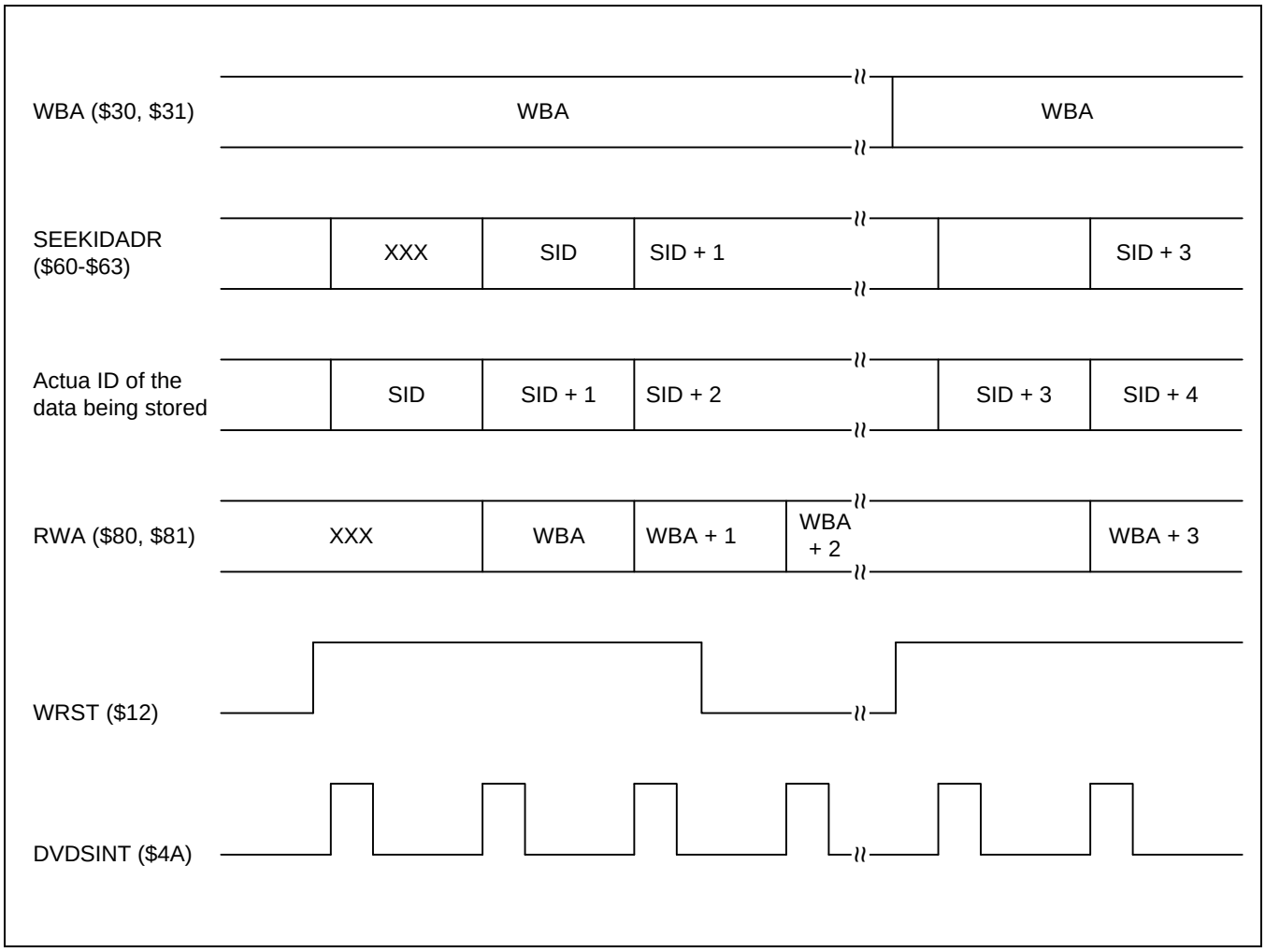
**Write Control According to Over or Under Interrupt**

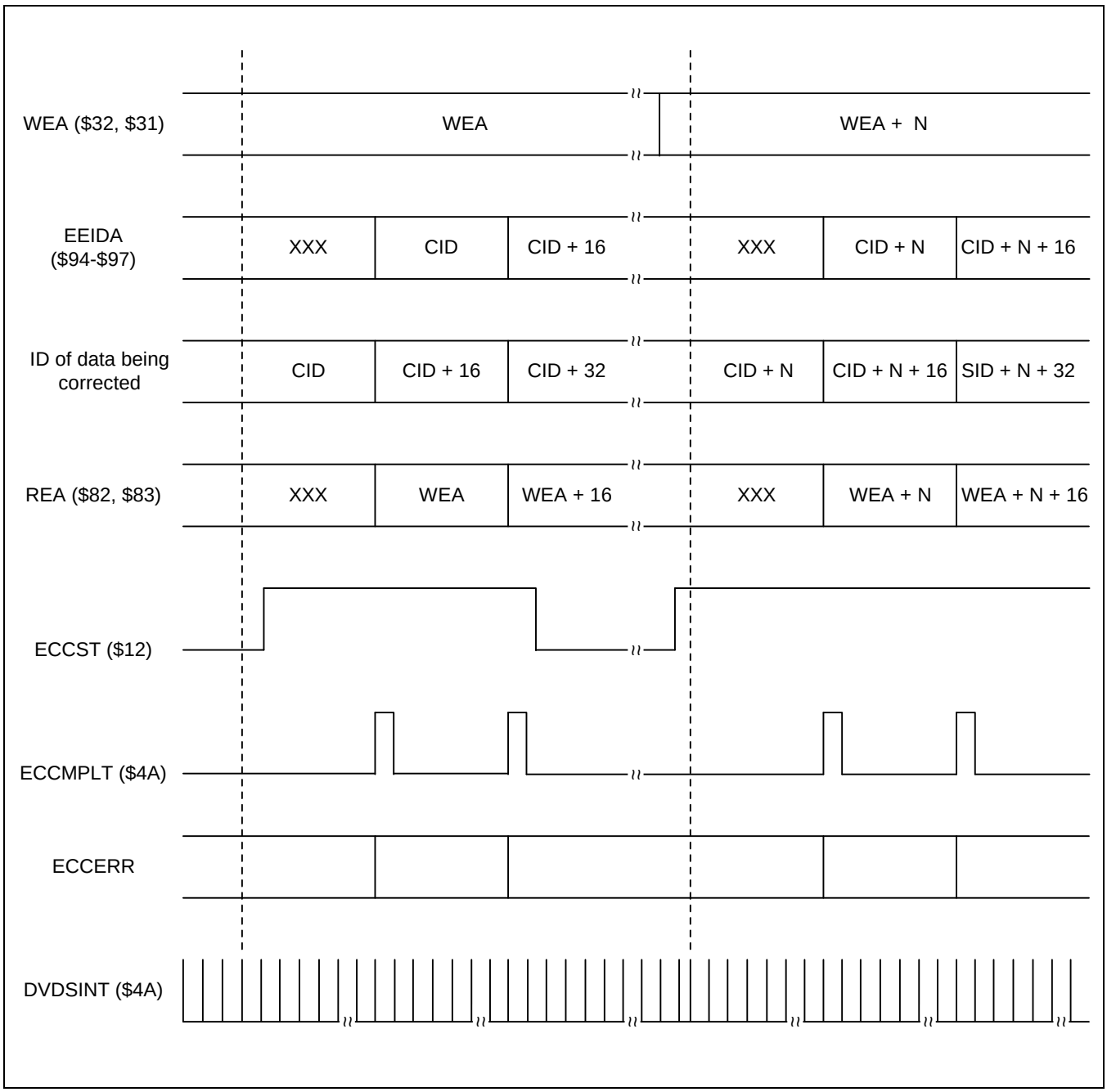
- Stopping and starting write is accomplished by controlling WRST. The write location isn't reloaded.



**ECC CONTROL**

- If ECCST is ‘0’ while must be carrying out ECC, always must be set the next ECC address to WEA.

- If ECCST is ‘0’, stop the current ECC operation in execution.



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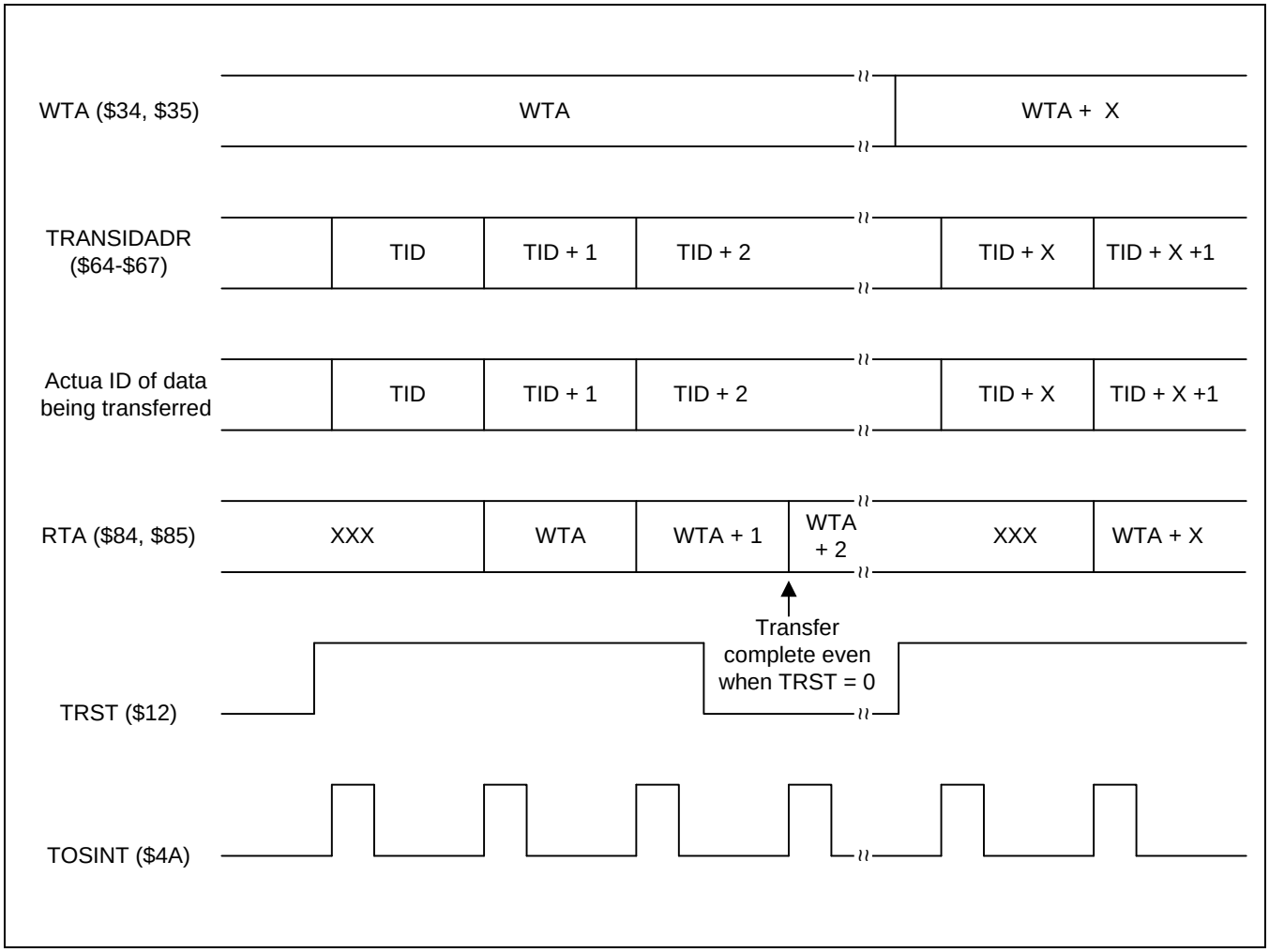
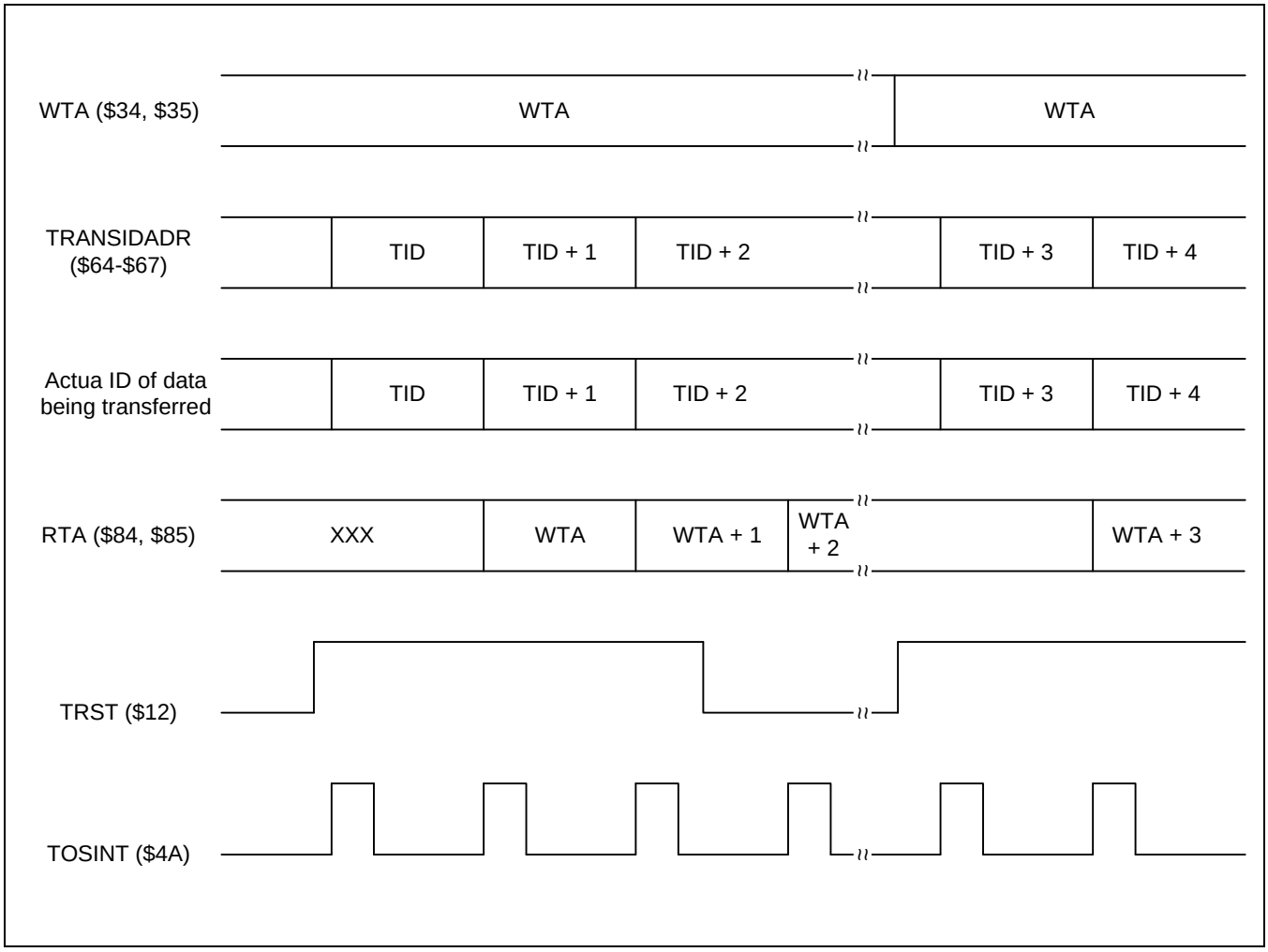
## CONTROL DURING TRANSFER

### Transfer After Reassigning The Memory Address During Transferring:

- Set TRST to ‘0”, reassign a new address to WTA, and start re-transferring by setting TRST to “1”.
  (Even if TRST is ‘0”, reassignment must come after transferring the specified sector amount.)



**Stopping and Starting Transfer by Controlling Only TRST**



| Descramble end Sector Unit Number | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 88 | B9 - B8 | | | | | | | |
| 89 | B7 - B0 | | | | | | | |
| Reset Value | B (9:0) = 3FF | | | | | | | |

Sector unit number of the completely descrambled buffer

| ECC end ID Address | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 94 | B31 - B24 | | | | | | | |
| 95 | B23 - B16 | | | | | | | |
| 96 | B15 - B8 | | | | | | | |
| 97 | B7 - B0 | | | | | | | |
| Reset Value | X | X | X | X | X | X | X | X |

The ID address corresponding to the end sector unit number of the buffer that has just finished error correction. This data is valid until the next ECCMPT interrupt.

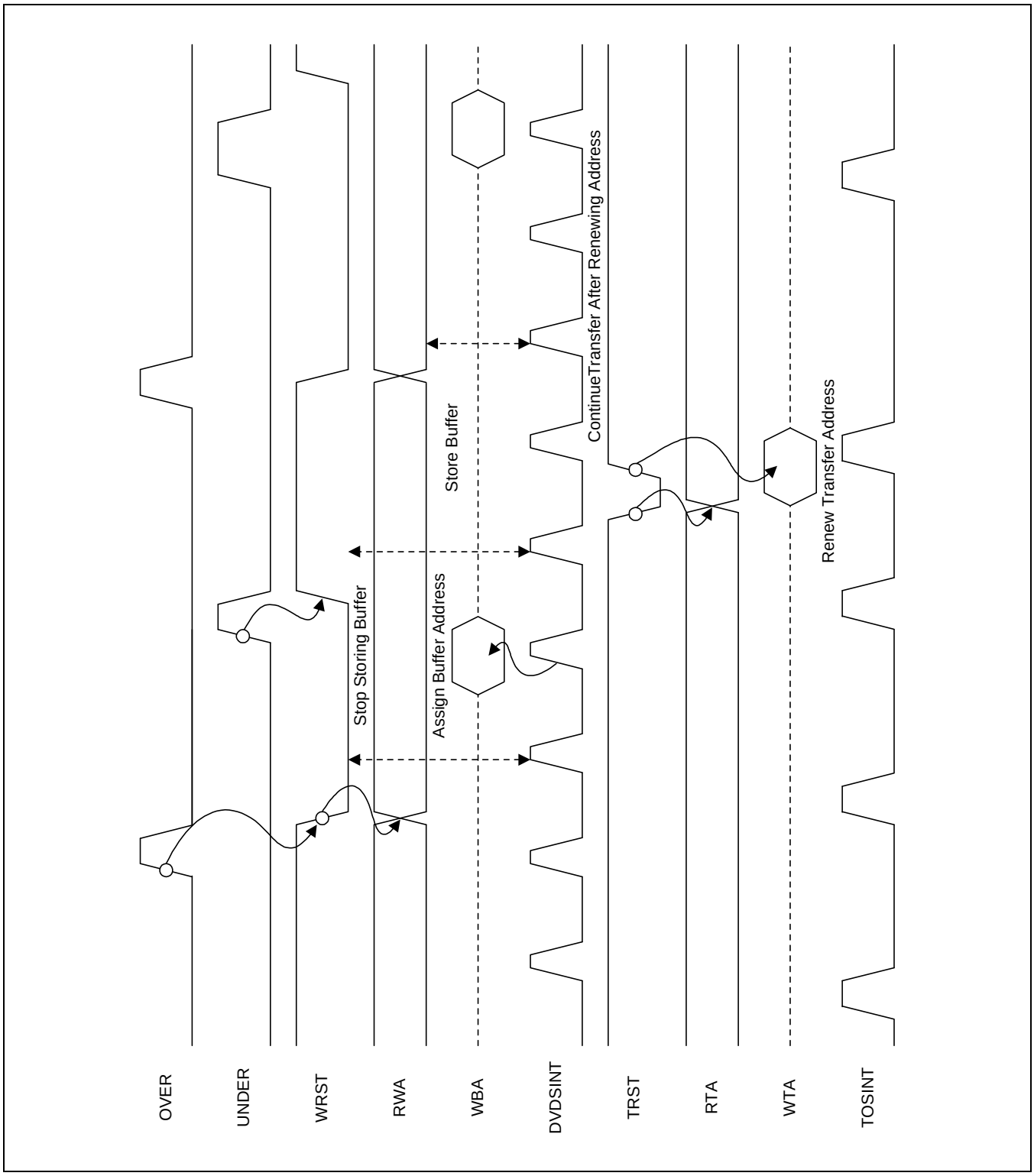
| DSI ID Address | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| 9C | B31 - B24 | | | | | | | |
| 9D | B23 - B16 | | | | | | | |
| 9E | B15 - B8 | | | | | | | |
| 9F | B7 - B0 | | | | | | | |
| Reset Value | X | X | X | X | X | X | X | X |

DSI sector's ID address stored in the buffer after DSIFG ($4A) generation. This data is valid until the next DVDSINT interrupt.

| Remaining Data Size (SECTOR Unit) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address** | **Bit7** | **Bit** | **Bit5** | **Bit4** | **Bit3** | **Bit2** | **Bit1** | **Bit0** |
| F0 | B9 - B8 | | | | | | | |
| F1 | B7 - B0 | | | | | | | |
| Reset Value | X | X | X | X | X | X | X | X |

The difference between the sector unit number of a descrambled buffer and the unit number after transfer to the A/V decoder or ROM decoder. You can find out how much extra data you have to transfer.

## OVER, UNDER INTERRUPT ($4A) APPLICATION

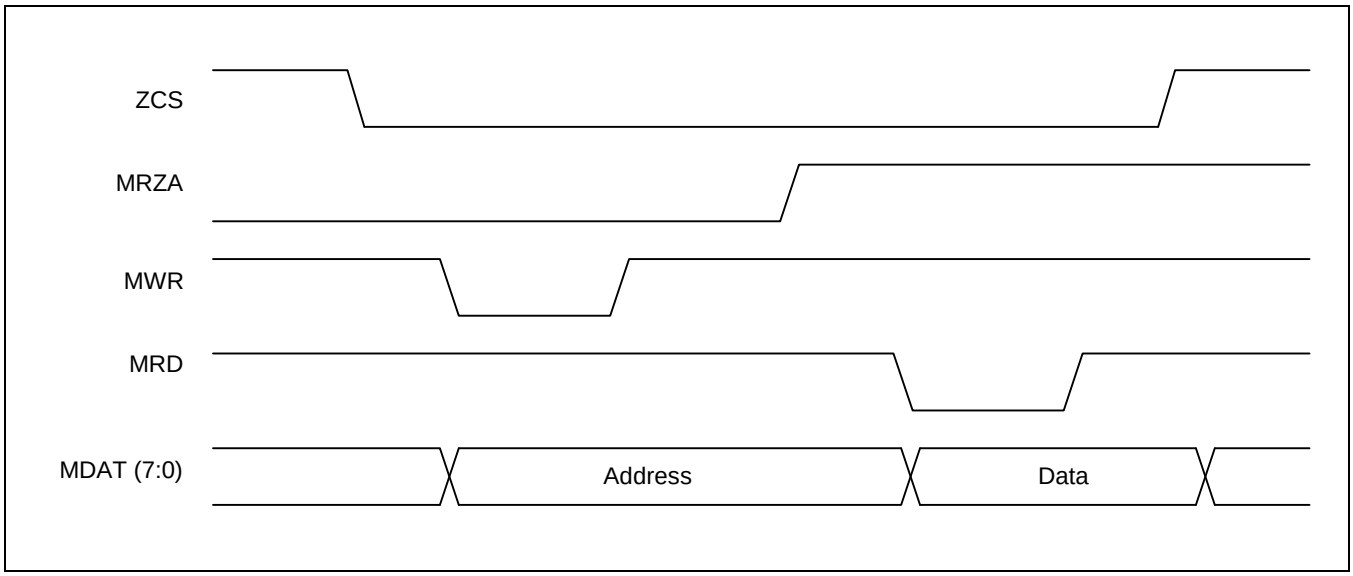


# 5 INTERFACE

## MICOM I/F

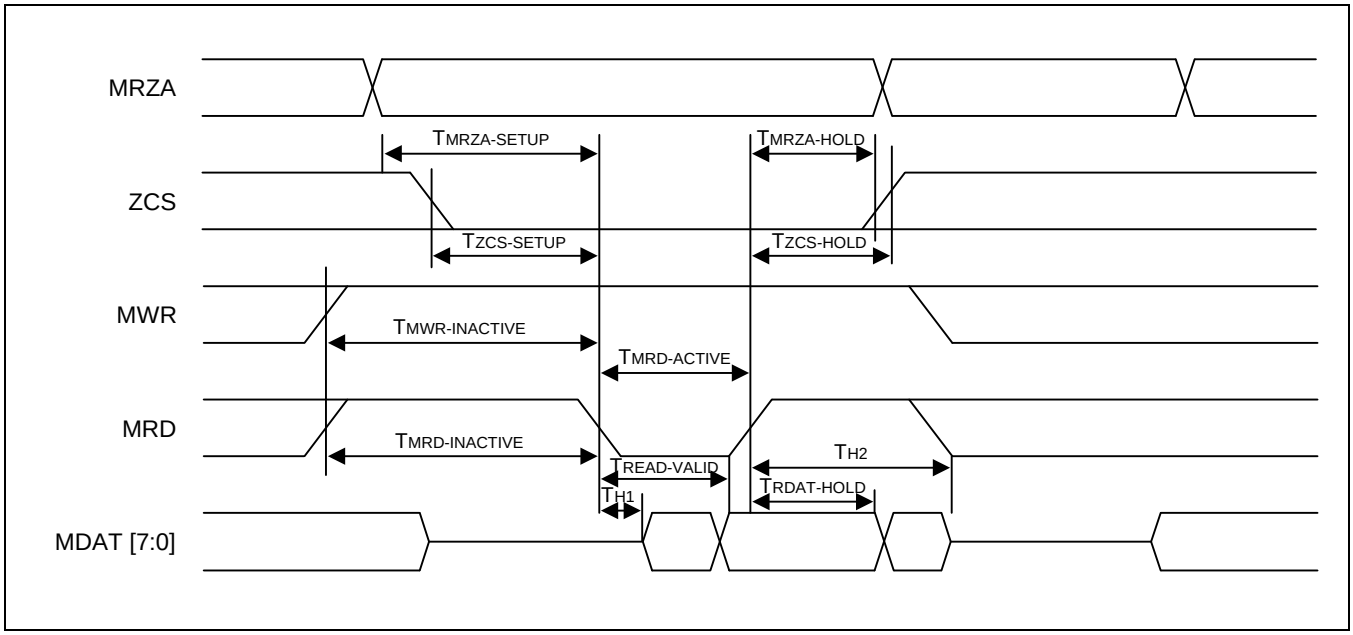
### MICOM I/F TIMING

#### Read Cycle

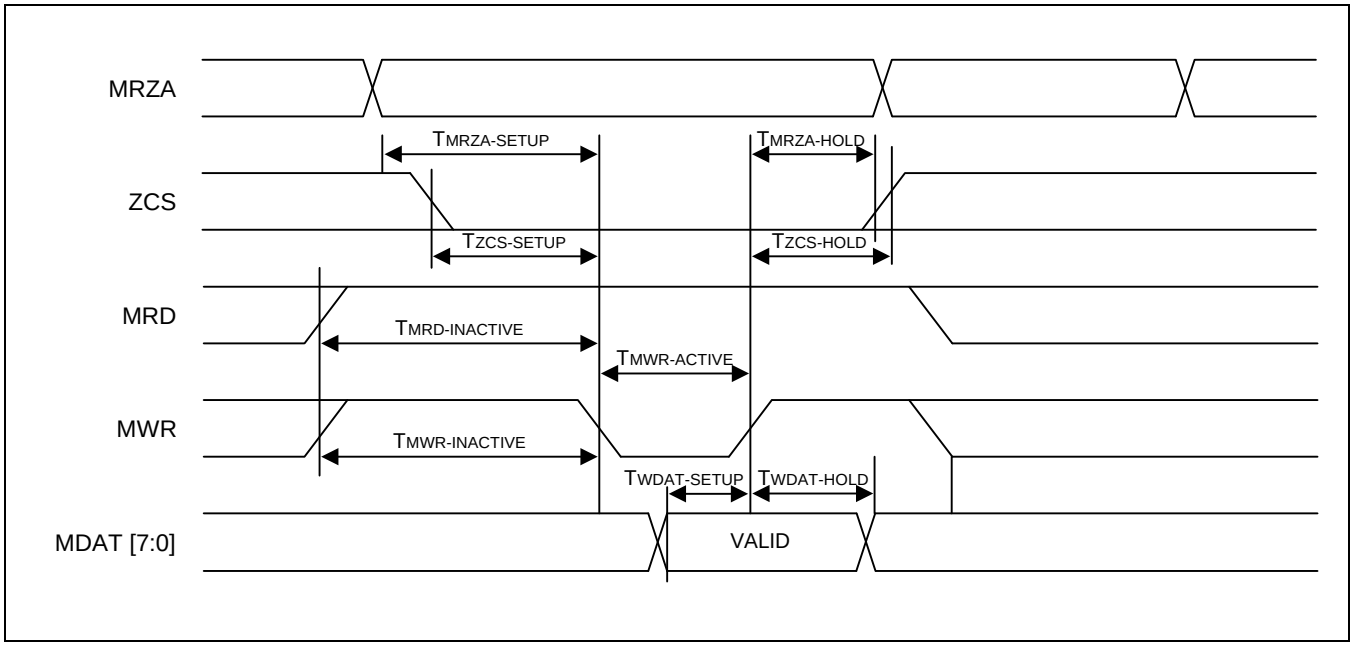



#### Write Cycle

### Read Cycle Timing




### Write Cycle Timing

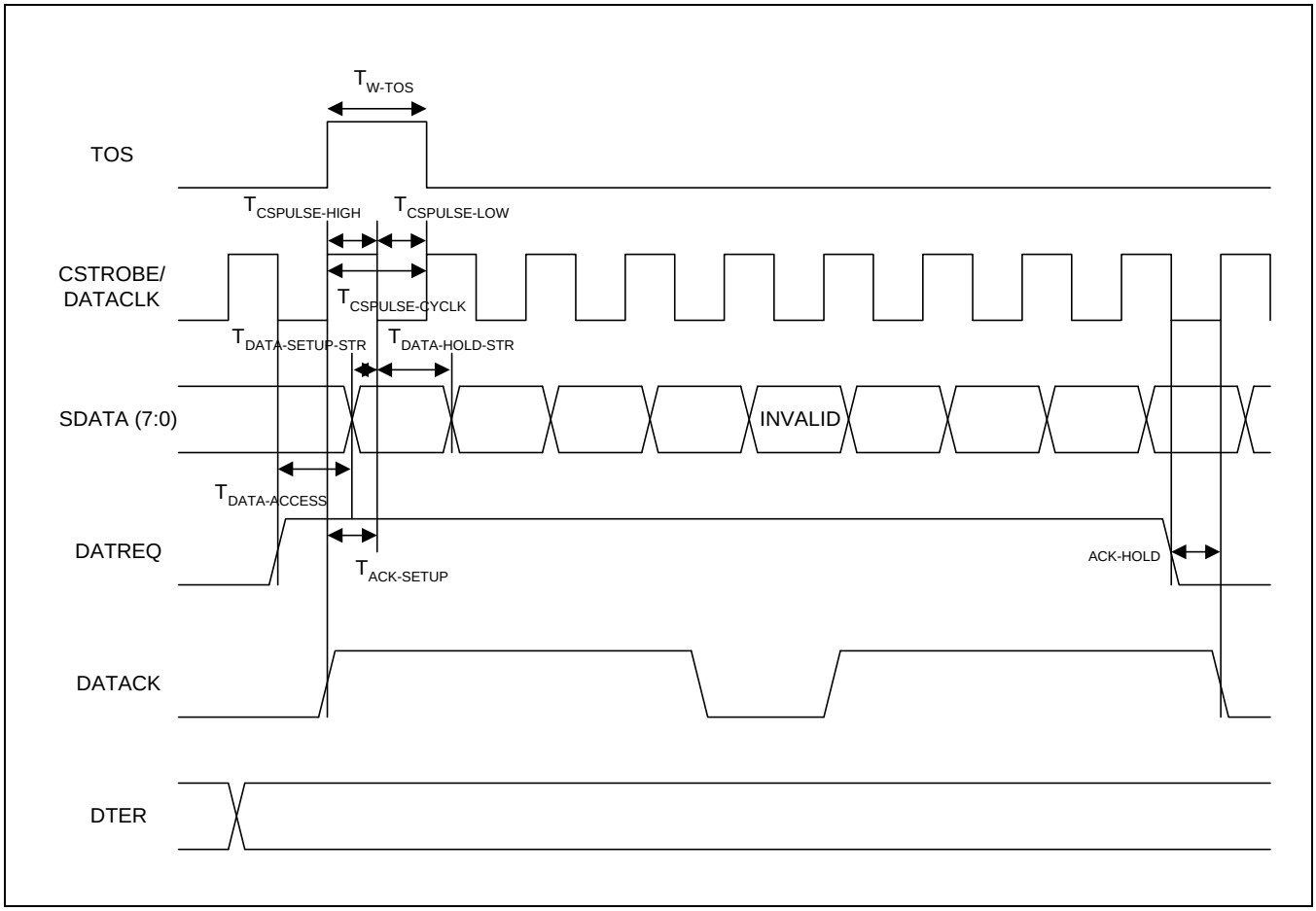


| Time | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{MRZA-SETUP}$ | MRZA setup | 0 | | ns |
| $T_{MRZA-HOLD}$ | MRZA hold | 10 | | ns |
| $T_{ZCS-SETUP}$ | ZCS setup | 10 | | ns |
| $T_{ZCS-HOLD}$ | ZCS hold | 10 | | ns |
| $T_{MWR-INACTIVE}$ | MWR inactive | 30 | | ns |
| $T_{MWR-ACTIVE}$ | MWR active pulse width | 30 | | ns |
| $T_{MRD-INACTIVE}$ | MRD inactive | 30 | | ns |
| $T_{MRD-ACTIVE}$ | MRD active pulse width | 120 | | ns |
| $T_{READ-VALID}$ | MRD active to read data valid | | 60 | ns |
| $T_{H1}$ | MRD active to MDAT(7:0) OW-impedance | - | | ns |
| $T_{H2}$ | MRD inactive to MDAT(7:0) IGH-impedance | - | - | ns |
| $T_{RDAT-HOLD}$ | Read data hold after MRD inactive | 10 | | ns |
| $T_{WDAT-SETUP}$ | Write data setup | 20 | | ns |
| $T_{WDAT-HOLD}$ | Write data hold | 10 | | ns |

There should be no glitches in signals MRZA, ZCS, MWR, and MRD.

## AV DECODER I/F

Equal spacing timing transfer method (DVD-P I/F)




MODE1: 2048 bytes main data only → compared to MODE2, Tdata-access has a delay longer by 16bytes at the beginning of data transfer, but the overall data rate is the same.

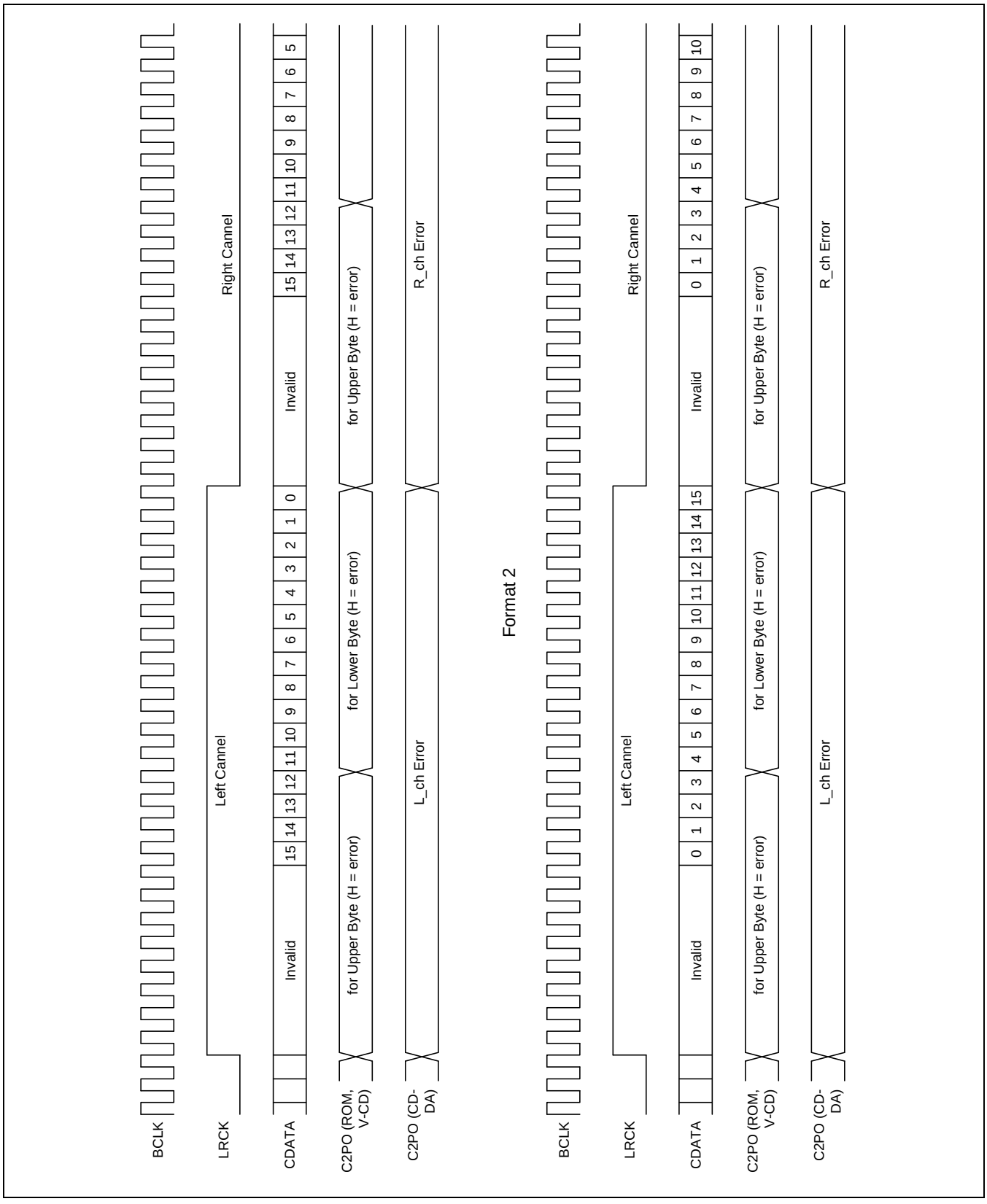
MODE2: 2064 bytes data in a sector
(4bytes ID + 2bytes IEC + 6bytes RSV + 2048bytes main data + 4bytes EDC)

- The DTER signal is output in units of sectors.
- Data is taken at CSTROBE/DATACLK'S falling edge (rising edge in reverse mode).
- CSTROBE/DATACLK'S duty cycle is not regular
- Tcspulse-high/low: 4T
- Tcspulse-cycle: 8T (240 ns)
- CSTROBE, DATREQ, DATACK'S edge is programmable (reversible).

**Timing Spec**

| Time | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{DATA-SETUP-STR}$ | SDATA(7:0) setup to cstrobe asserted (synchronous) | 5 | 4T | ns |
| $T_{DATA-HOLD-STR}$ | SDATA(7:0) hold from cstrobe asserted (synchronous) | 5 | 4T | ns |
| $T_D$ | Delay from datreq asserted to datack (asynchronous) | 0 | | ns |
| $T_{ACK-LOW}$ | Datack low time (asynchronous) | 50 | | ns |
| $T_{CSPULSE-CYCLE}$ | Datack period | 236 | | ns |
| $T_{ACK-HOLD}$ | Datack disabled time | 12 | 4T | ns |
| $T_{SDATA-D}$ | SDATA(7:0) delay from datack falling | | 10 | ns |
| $T_{ACK-SETUP}$ | Datack setup to cstrobe (synchronous) | 5 | | ns |
| $T_{ACK-HOLD}$ | Datack hold from cstrobe (synchronous) | 5 | | ns |

## CD-DA/ CD-ROM/ V-CD DATA OUTPUT TIMING (FORMAT 1, FORMAT 2)



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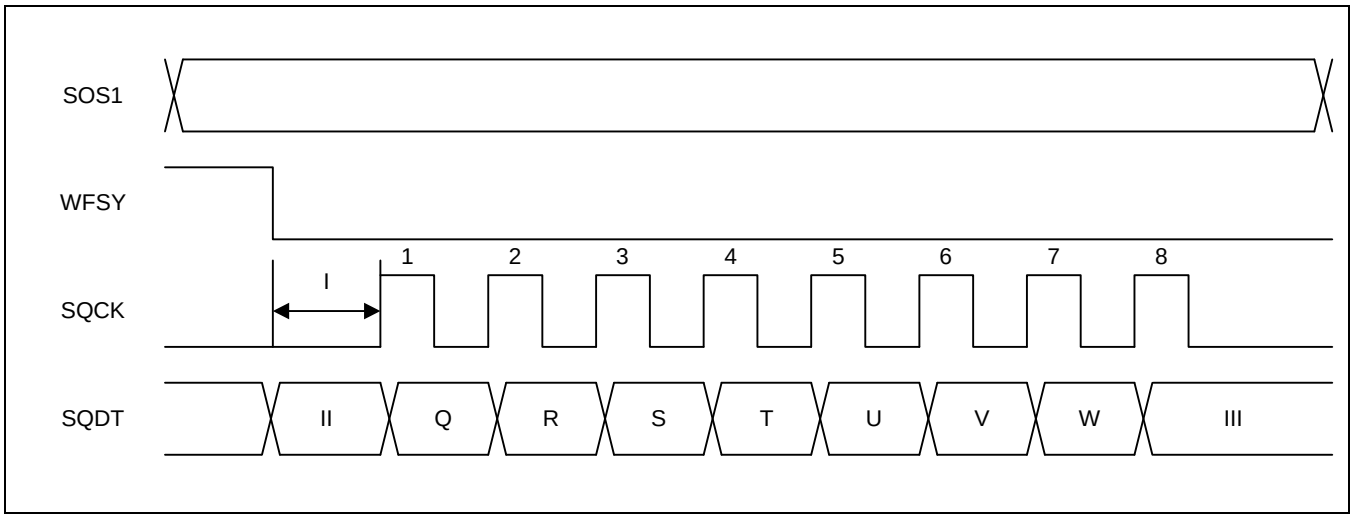
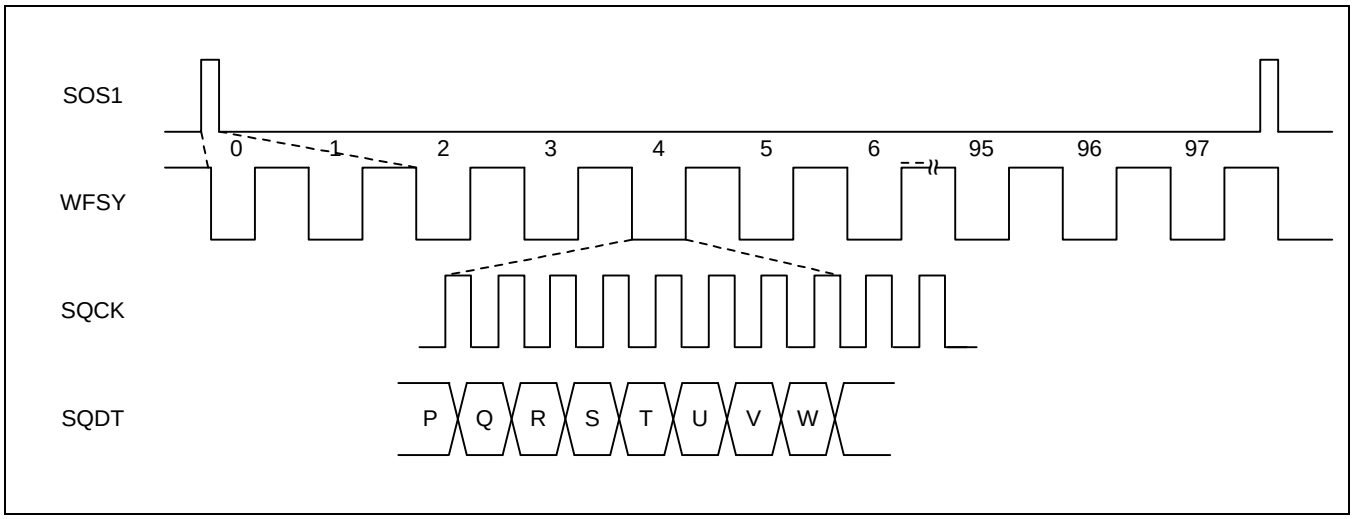
## SUBCODE OUTPUT I/F (FOR CD-G)




I: After WFSY becomes falling edge, SQCK becomes "L" at about 10 μ sec.

II: If S0S1 is "L", subcode P is output, and if "H", subcode sync S0 and S1 are output.

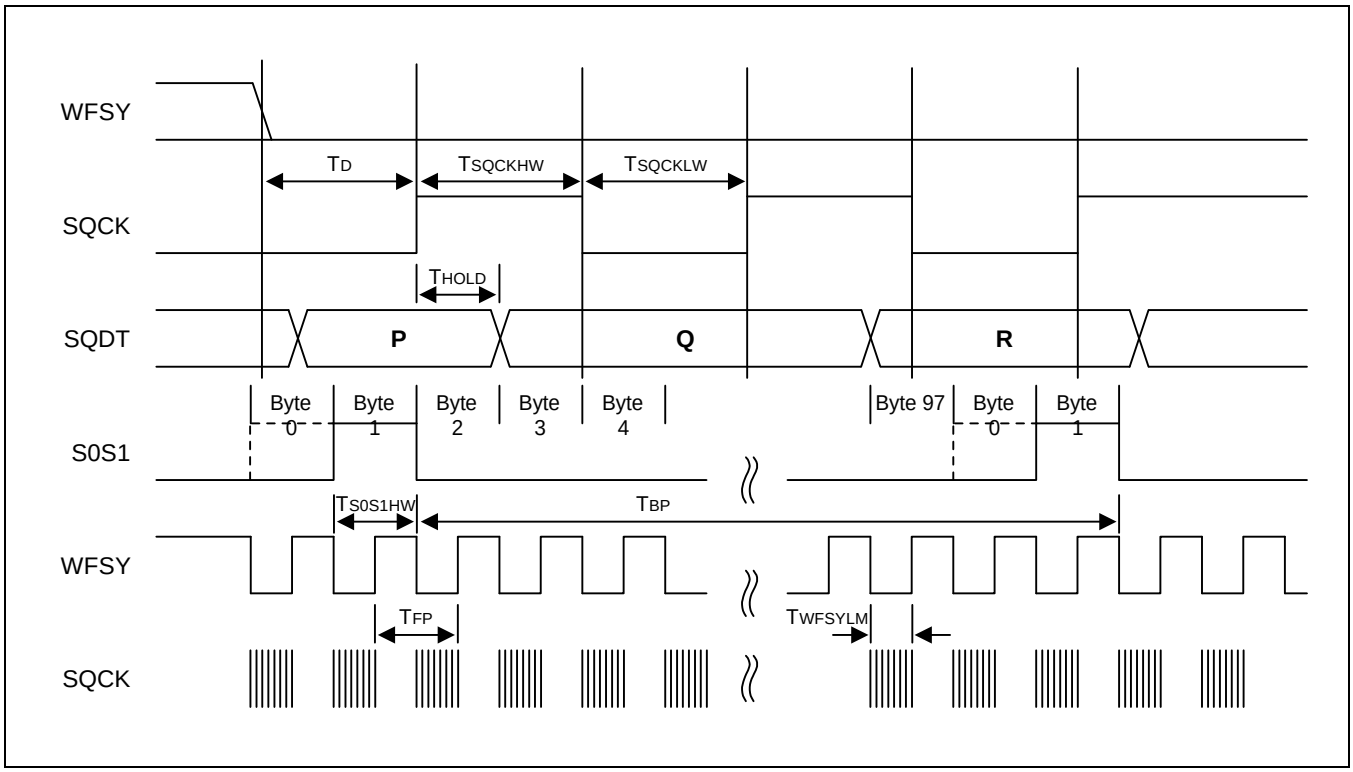
III: If pulses are input to the SQCK terminal over seven, subcode data (P, Q, R, S, T, U, V, W) are repeated.




1 subcode sync = 98 EFM FRAMEs (1 EFM FRAME = 7.35kHz, 1 subcode sync = 75Hz)

98 EFM FRAMEs = 2bytes for subcode sync (S0, S1) + 96bytes for subcode data

96bytes subcode data = 1(P) bit × 96 + 1(Q) bit × 80 + 16bits (CRC for EDC) for CDP + 6(R - W) bits × 96 for CDG




| Time | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_D$ | Delay time from WFSY low to SQCK high edge for "P" subcode bit (SQCK input) | 1 | - | - | us |
| $T_{SQCKHW}$ | SQCK (input) high pulse width | 1 | - | 3 | us |
| $T_{SQCKLW}$ | SQCK (input) low pulse width | 1 | - | 3 | us |
| $T_{HOLD}$ | SQDT hold time from SQCK high | 0 | - | - | ns |
| $T_{S0S1HW}$ | S0S1 high pulse width | - | 136 | - | us |
| $T_{BP}$ | Block period | - | 13 | - | ms |
| $T_{FP}$ | Frame period | - | 136 | - | us |
| $T_{WFSYLW}$ | WFSY low pulse width | - | 68 | - | us |

SQDT read should be completed when WFSY is low ($T_{WFSYLW}$).

# 6 MISCELLANEOUS

## EXTERNAL DRAM MEMORY MAP

ECC 13 block can be stored using 4M DRAM, and can carry out the following: EFM+demodulation 1 block, ECC 1 block, descramble 1 block, and TRANS 1 block.

: Memory mapping (512 x 512 x 16) for DVDP.
1 sector standard: ID(4), IEC(2), RSV(6), DPDATA(2048), EDC(4), PI(120), PO(182)

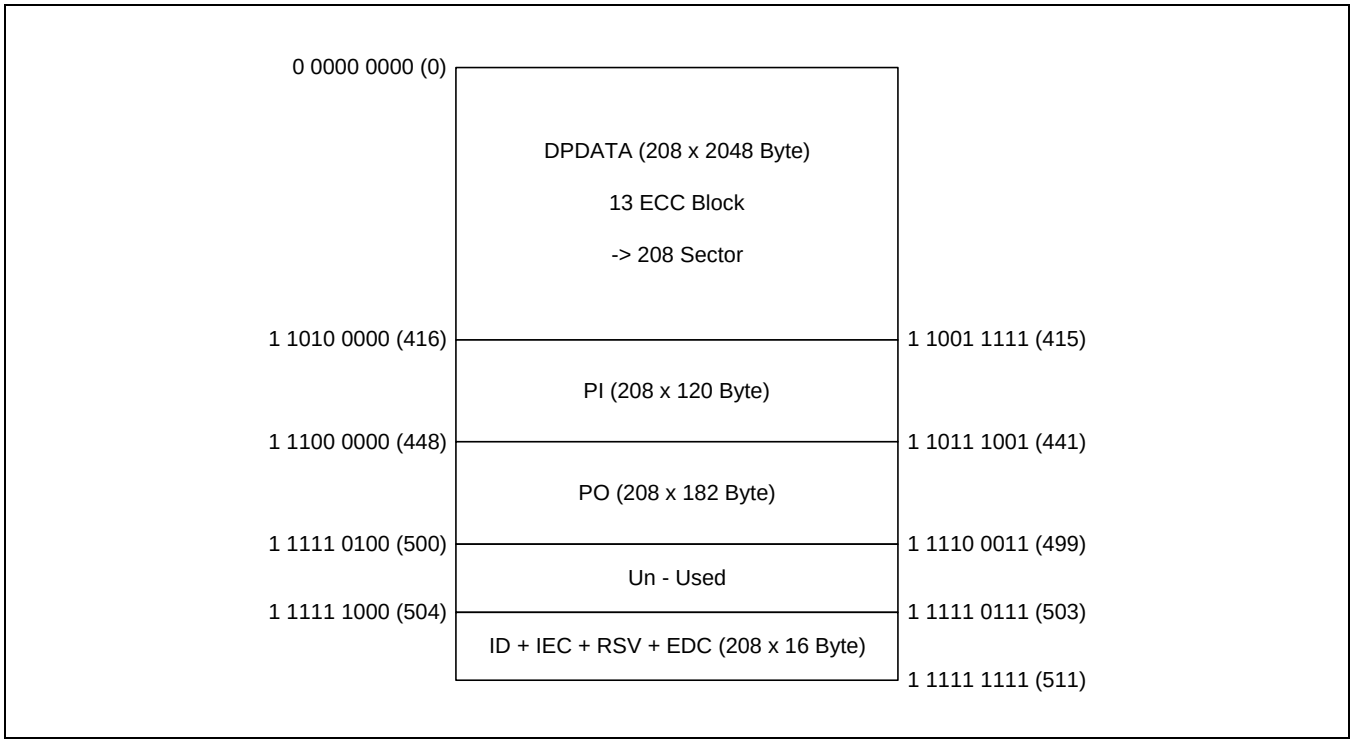



**Figure 7. External DRAM Memory Map**

### MEMORY MAPPING DEFINITION BY SECTOR

PI: 128byte per sector.
- 1 row address increases per 8 sectors.

PO: 256byte per sector.
- 1 row address increases per 4 sectors.

ID, IEC, RSV, EDC: 32bytes per sector.
- 1 row address increases per 32 sectors.

## ADDRESS MAPPING

### Data Mapping

| ECC Block Number | ID Sector Number | Row Address | | | | | | | | | Column Address | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | x |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | x | x |
| 1 | 0 - 15 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 2 | 0 - 15 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| . . . | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| 12 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | x | x |

### PI Mapping

| ECC Block Number | ID Sector Number | Row Address | | | | | | | | | Column Address | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x |
| | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | x | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x | x | x |
| 1 | 0 - 15 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | x |
| 2 | 0 - 15 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x |
| . . . | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| 12 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x | x | x |

**PO Mapping**

| ECC Block Number | ID Sector Number | Row Address | | | | | | | | | Column Address | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x |
| | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x |
| 1 | 0 - 15 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x |
| 2 | 0 - 15 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | x | x |
| . . . | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| 12 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x |

**ID(4) + IEC(2) + RSV(6) + EDC(4)**

| ECC Block Number | ID Sector Number | Row Address | | | | | | | | | Column Address | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x |
| 1 | 0 - 15 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x |
| 2 | 0 - 15 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x |
| . . . | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| 12 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x |
| | . . . | . . . | | | | | | | | | . . . | | | | | | | | |
| | 15 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | x | x | x | x |

Lower 4bits is mapped by sectors

→ ID: “0000” - “0001”, IEC: “0010”, RSV: “0011” - “0110”, EDC: “1000” - “1001”

## CIRCUIT APPLICATION

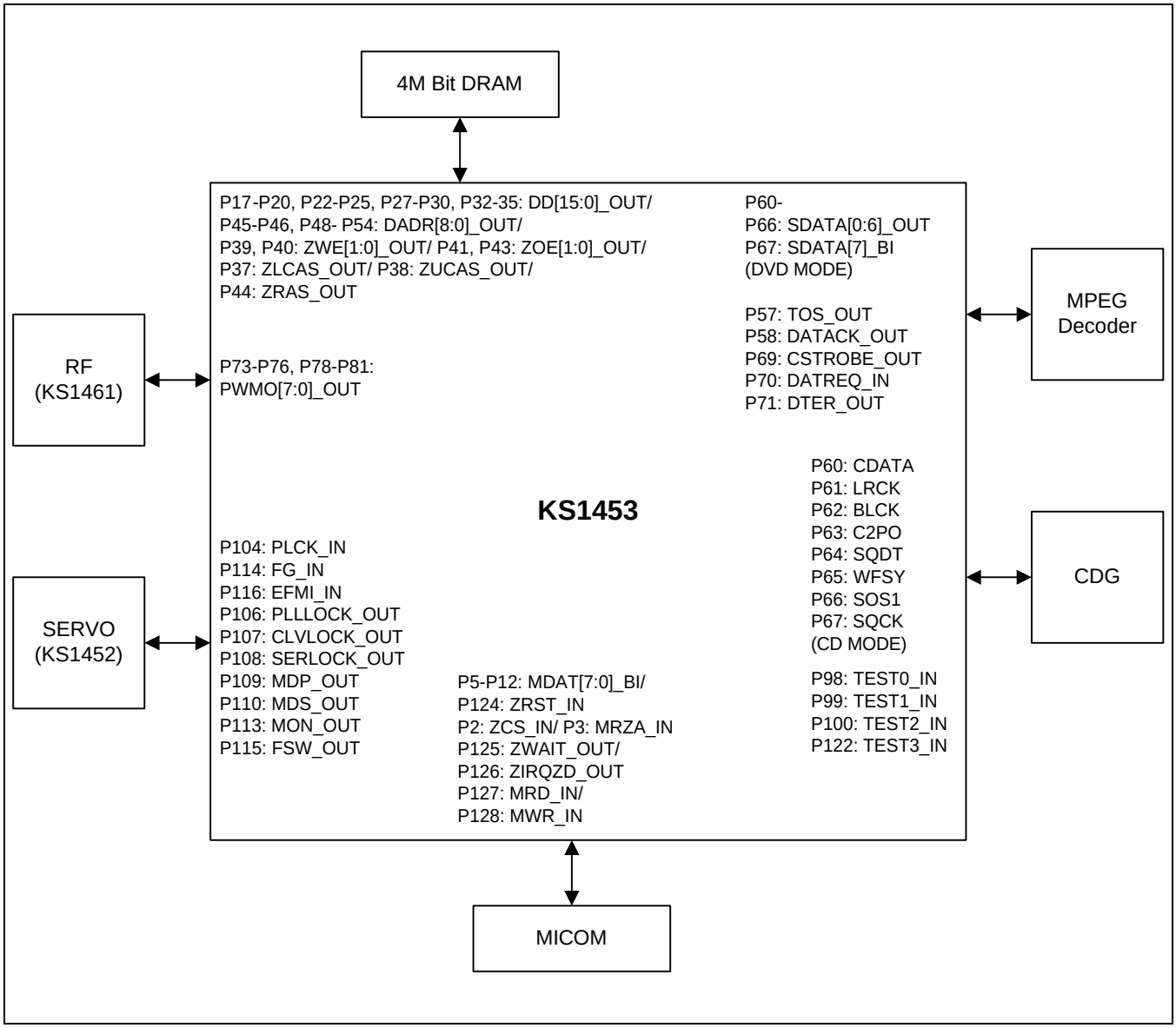



**Figure 8. Circuit Application**

## PACKAGE DIMENSIONS

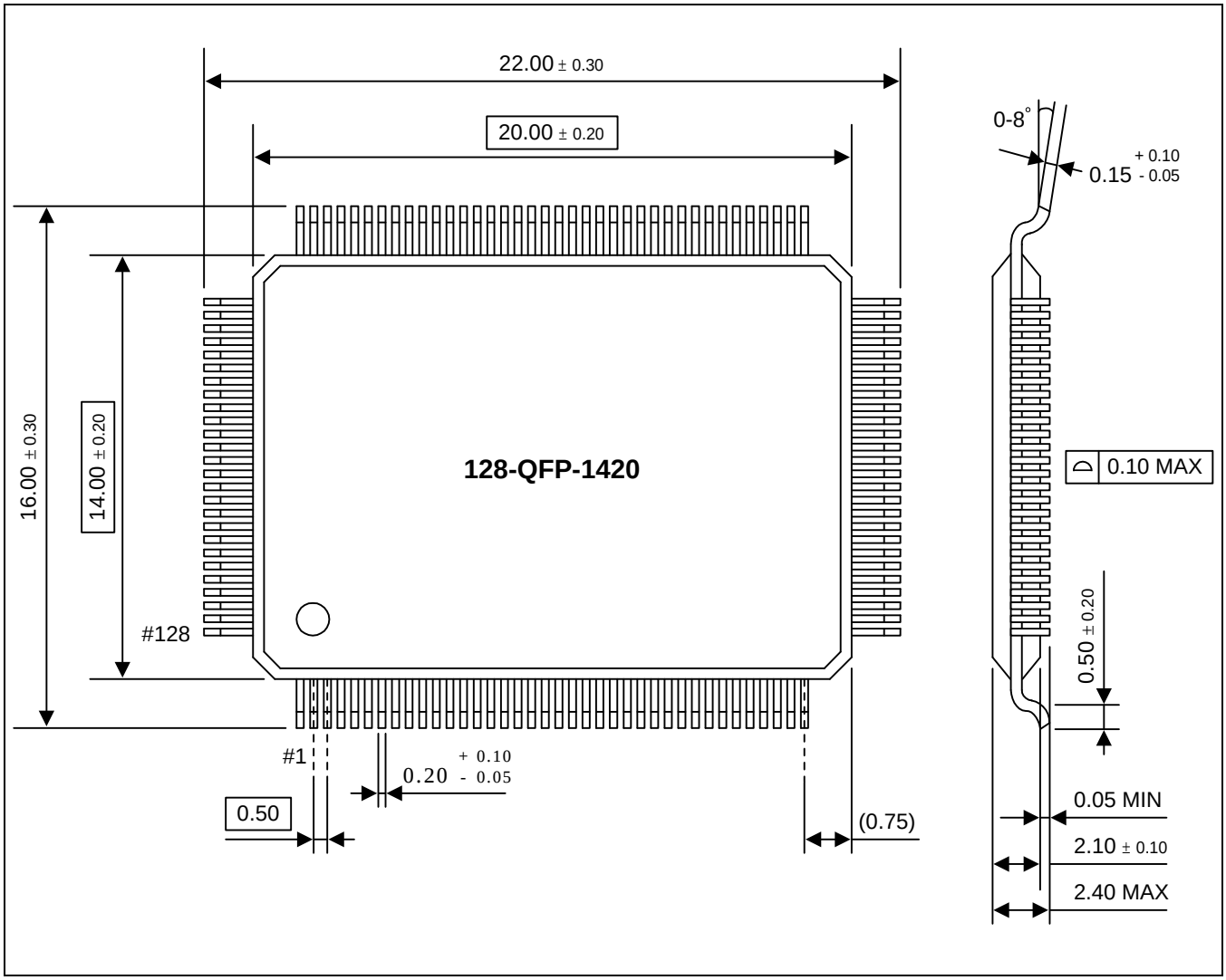



**Figure 9. Package Dimensions**