# IMS1820M CMOS High Performance 64K x 4 Static RAM MIL-STD-883C

### Advance Information

## FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 64K x 4 Bit Organization
- 30, 35 and 45 ns Address Access Times
- 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Outputs
- Three-state Output
- 24 Pin 300-mil DIP and 28 Pin LCC
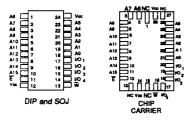- Single +5V ± 10% Operation
- Power Down Function

## DESCRIPTION

The INMOS IMS1820M is a high performance 64Kx4 CMOS Static RAM. The IMS1820M allows speed enhancements to existing 64K x 4 applications with the additional benefit of reduced power consumption .

The IMS1820M features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1820M provides a Chip Enable function (/E) that can be used to place the device into a low power standby mode.
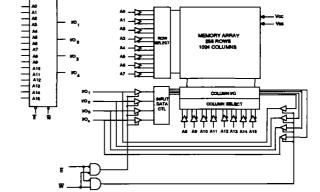
The IMS1820M is a high speed VLSI RAM intended for military applications which require high performance and superior reliability.

## PIN CONFIGURATION    LOGIC SYMBOL    BLOCK DIAGRAM



DIP and SOJ

CHIP CARRIER

## PIN NAMES

| $A_0$ - $A_{15}$ | ADDRESS INPUTS | Vcc | POWER (+5V) |
|---|---|---|---|
| W | WRITE ENABLE | Vss | GROUND |
| I/O-I/O | DATA IN/OUT | | |
| E | CHIP ENABLE | | |