Voltage Detector IC Series

Low Voltage Standard CMOS Voltage Detector IC Series

BU48□□G, BU48□□F, BU48□□FVE, BU49□□G, BU49□□F, BU49□□FVE series

No.09006ECT01

● Description

ROHM standard CMOS reset IC series is a high-accuracy low current consumption reset IC series.
The lineup was established with two output types (Nch open drain and CMOS output) and detection voltage range from 0.9V to 4.8V in increments of 0.1V, so that the series may be selected according to the application at hand.

● Features

1) Detection voltage from 0.9V to 4.8V in 0.1V increments
2) Highly accurate detection voltage: ±1.0%
3) Ultra-low current consumption
4) Nch open drain output (BU48□□G/F/FVE)and CMOS output (BU49□□G/F/FVE)
5) Small surface package SSOP5: BU48□□G, BU49□□G
SOP4: BU48□□F, BU49□□F
VSOF5: BU48□□FVE, BU49□□FVE

● Applications

All electronics devices that use microcontrollers and logic circuits.

● Selection Guide

Part Number : BU4 □□□□

① ② ③

No.	Specifications Description	
①	Output Circuit Format	8:Open Drain Output, 9:CMOS Output
②	Detection Voltage	Example V_{DET}: Represented as 0.1V steps in the range from 0.9V to 4.8V (Displayed as 0.9 in the case of 0.9V)
③	Package	G:SSOP5(SMP5C2)/ F:SOP4/ FVE:VSOF5(EMP5)

● Lineup

Making	Detection voltage	Part Number	Making	Detection voltage	Part Number	Making	Detection voltage	Part Number	Making	Detection voltage	Part Number
JR	4.8V	BU4848	HV	2.8V	BU4828	LH	4.8V	BU4948	KM	2.8V	BU4928
JQ	4.7V	BU4847	HU	2.7V	BU4827	LG	4.7V	BU4947	KL	2.7V	BU4927
JP	4.6V	BU4846	HT	2.6V	BU4826	LF	4.6V	BU4946	KK	2.6V	BU4926
JN	4.5V	BU4845	HS	2.5V	BU4825	LE	4.5V	BU4945	KJ	2.5V	BU4925
JM	4.4V	BU4844	HR	2.4V	BU4824	LD	4.4V	BU4944	KH	2.4V	BU4924
JL	4.3V	BU4843	HQ	2.3V	BU4823	LC	4.3V	BU4943	KG	2.3V	BU4923
JK	4.2V	BU4842	HP	2.2V	BU4822	LB	4.2V	BU4942	KF	2.2V	BU4922
JJ	4.1V	BU4841	HN	2.1V	BU4821	LA	4.1V	BU4941	KE	2.1V	BU4921
JH	4.0V	BU4840	HM	2.0V	BU4820	KZ	4.0V	BU4940	KD	2.0V	BU4920
JG	3.9V	BU4839	HL	1.9V	BU4819	KY	3.9V	BU4939	KC	1.9V	BU4919
JF	3.8V	BU4838	HK	1.8V	BU4818	KX	3.8V	BU4938	KB	1.8V	BU4918
JE	3.7V	BU4837	HJ	1.7V	BU4817	KW	3.7V	BU4937	KA	1.7V	BU4917
JD	3.6V	BU4836	HH	1.6V	BU4816	KV	3.6V	BU4936	JZ	1.6V	BU4916
JO	3.5V	BU4835	HG	1.5V	BU4815	KU	3.5V	BU4935	JY	1.5V	BU4915
JB	3.4V	BU4834	HF	1.4V	BU4814	KT	3.4V	BU4934	JX	1.4V	BU4914
JA	3.3V	BU4833	HE	1.3V	BU4813	KS	3.3V	BU4933	JW	1.3V	BU4913
HZ	3.2V	BU4832	HD	1.2V	BU4812	KR	3.2V	BU4932	JV	1.2V	BU4912
HY	3.1V	BU4831	HC	1.1V	BU4811	KQ	3.1V	BU4931	JU	1.1V	BU4911
HX	3.0V	BU4830	HB	1.0V	BU4810	KP	3.0V	BU4930	JT	1.0V	BU4910
HW	2.9V	BU4829	HA	0.9V	BU4809	KN	2.9V	BU4929	JS	0.9V	BU4909

● **Absolute maximum ratings (Ta=25°C)**

Parameter S		ymbol	Limits	Unit
Power Supply Voltage		VDD-GND	-0.3 ~ +7	V
Output Voltage	Nch Open Drain Output	VOUT	GND-0.3 ~ +7	V
	CMOS Output		GND-0.3 ~ VDD+0.3	
Power Dissipation	SSOP5 *1*4	400 Pd	540	mW
	SOP4 *2*4			
	VSOF5 *3*4	210		
Operating Temperature		Topr	-40 ~ +125	°C
Ambient Storage Temperature		Tstg	-55 ~ +125	°C

*1 When used at temperatures higher than Ta=25°C, the power is reduced by 5.4mW per 1°C above 25°C.
*2 When used at temperatures higher than Ta=25°C, the power is reduced by 4.0mW per 1°C above 25°C.
*3 When used at temperatures higher than Ta=25°C, the power is reduced by 2.1mW per 1°C above 25°C.
*4 When a ROHM standard circuit board (70mm×70mm×1.6mm, glass epoxy board)is mounted.

● **Electrical characteristics**

Parameter S	ymbol	Condition		Limit Min.	Limit Typ.	Limit Max.	Unit
Detection Voltage	VDET	VDD=H→L , Ta=25°C RL=470kΩ	BU4848	4.752	4.800	4.848	V
			BU4847	4.653	4.700	4.747	
			BU4846	4.554	4.600	4.646	
			BU4845	4.455	4.500	4.545	
			BU4844	4.356	4.400	4.444	
			BU4843	4.257	4.300	4.343	
			BU4842	4.158	4.200	4.242	
			BU4841	4.059	4.100	4.141	
			BU4840	3.960	4.000	4.040	
			BU4839	3.861	3.900	3.939	
			BU4838	3.762	3.800	3.838	
			BU4837	3.663	3.700	3.737	
			BU4836	3.564	3.600	3.636	
			BU4835	3.465	3.500	3.535	
			BU4834	3.366	3.400	3.434	
			BU4833	3.267	3.300	3.333	
			BU4832	3.168	3.200	3.232	
			BU4831	3.069	3.100	3.131	
			BU4830	2.970	3.000	3.030	
			BU4829	2.871	2.900	2.929	
			BU4828	2.772	2.800	2.828	
			BU4827	2.673	2.700	2.727	
			BU4826	2.574	2.600	2.626	
			BU4825	2.475	2.500	2.525	
			BU4824	2.376	2.400	2.424	
			BU4823	2.277	2.300	2.323	
			BU4822	2.178	2.200	2.222	
			BU4821	2.079	2.100	2.121	
			BU4820	1.980	2.000	2.020	
			BU4819	1.881	1.900	1.919	
			BU4818	1.782	1.800	1.818	
			BU4817	1.683	1.700	1.717	
			BU4816	1.584	1.600	1.616	
			BU4815	1.485	1.500	1.515	
			BU4814	1.386	1.400	1.414	
			BU4813	1.287	1.300	1.313	
			BU4812	1.188	1.200	1.212	
			BU4811	1.089	1.100	1.111	
			BU4810	0.990	1.000	1.010	
			BU4809	0.891	0.900	0.909	
Detection Voltage Temperature Coefficient	VDET/ΔT Ta	a=-40°C~125°C *1		-	±30	-	ppm/°C
Hysteresis Voltage	ΔVDET	VDD=L→H→L Ta=-40°C~125°C RL=470kΩ	VDET≤1.0V	VDET ×0.03	VDET ×0.05	VDET ×0.08	V
			VDET≥1.1V	VDET ×0.03	VDET ×0.05	VDET ×0.07	

*1 Designed Guarantee.(Outgoing inspection is not done on all products.)
*This product is not designed for protection against radioactive rays.

● **Electrical characteristics (Unless Otherwise Specified Ta=-25 to 125°C)**

Parameter S	ymbol	Condition		Limit			Unit
				Min. T	yp.	Max.	
Circuit Current when ON	IDD1 V	DD=VDET-0.2V	VDET =0.9-1.3V -		0.15	0.88	μA
			VDET =1.4-2.1V -		0.20	1.05	
			VDET =2.2-2.7V -		0.25	1.23	
			VDET =2.8-3.3V	-	0.30	1.40	
			VDET =3.4-4.2V	-	0.35	1.58	
			VDET =4.3-4.8V	-	0.40	1.75	
Circuit Current when OFF	IDD2 V	DD=VDET+2.0V	VDET =0.9-1.3V -		0.30	1.40	μA
			VDET =1.4-2.1V -		0.35	1.58	
			VDET =2.2-2.7V	-	0.40	1.75	
			VDET =2.8-3.3V	-	0.45	1.93	
			VDET =3.4-4.2V	-	0.50	2.10	
			VDET =4.3-4.8V	-	0.55	2.28	
Operating Voltage Range	VOPL	VOL≤0.4V, Ta=25~125°C, RL=470kΩ 0.70			-	-	V
		VOL≤0.4V, Ta=-40~25°C, RL=470kΩ 0.90			-	-	
'Low' Output Current (Nch)	IOL	VDS=0.05V V DD=0.85V 20			100	-	μA
		VDS=0.5V V DD=1.5V V DET=1.7-4.8V 1.0			3.3	-	mA
		VDS=0.5V V DD=2.4V V DET=2.7-4.8V 4.0			7.2	-	
'High' Output Current (Pch) (only BU49□□G/F/FVE)	IOH	VDS=0.5V V DD=4.8V V DET=0.9-3.9V 1.7			3.4	-	mA
		VDS=0.5V V DD=6.0V V DET=4.0-4.8V 2.0			4.0	-	
Output Leak Current when OFF (only BU48□□G/F/FVE)	Ileak	VDD=VDS=7V Ta=-40°C~85°C		- 0		0.1	μA
		VDD=VDS=7V Ta=85°C~125°C		- 0		1	

* This product is not designed for protection against radioactive rays.

● **Block Diagrams**

BU48□□G/F/FVE

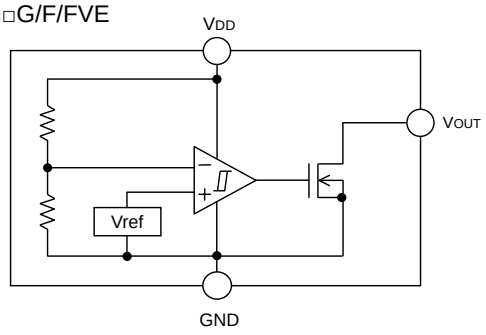


Fig.1

BU49□□G/F/FVE

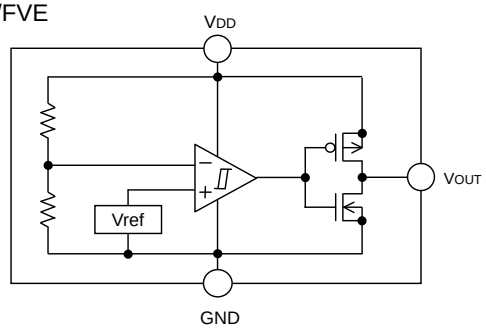
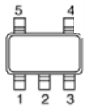


Fig.2

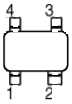
TOP VIEW



SSOP5

PIN No.	Symbol	Function
1 VOUT		Reset output
2	VDD	Power supply voltage
3	GND	GND
4	N.C.	Unconnected terminal
5	N.C.	Unconnected terminal

TOP VIEW



SOP4

PIN No.	Symbol	Function
1 VOUT		Reset output
2	VDD	Power supply voltage
3	N.C.	Unconnected terminal 3
4	GND	GND

TOP VIEW

VSOF5

PIN No.	Symbol	Function
1	VOUT	Reset output
2	SUB	Substrate*
	N.C.	Unconnected terminal
4	VDD	Power supply voltage
5 GND		GND

*Connect the substrate to VDD

● **Reference Data (Unless specified otherwise, Ta=25°C)**

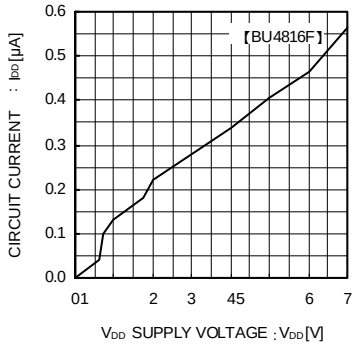


Fig.3 Circuit Current

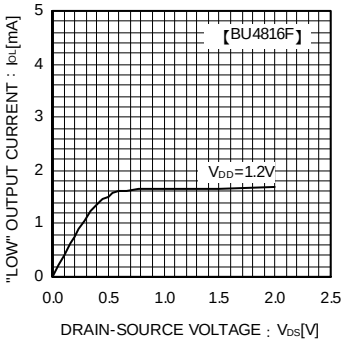


Fig.4 “LOW” Output Current

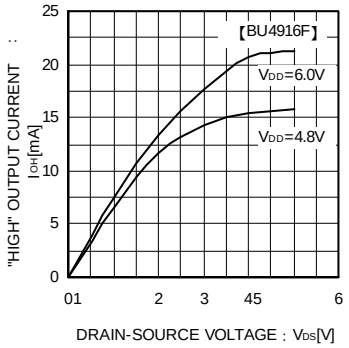


Fig.5 “High” Output Current

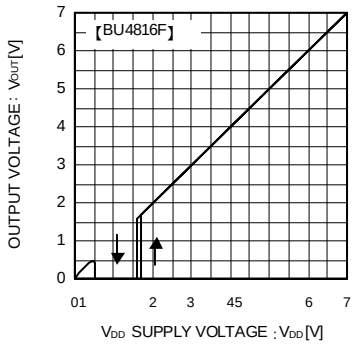


Fig.6 I/O Characteristics

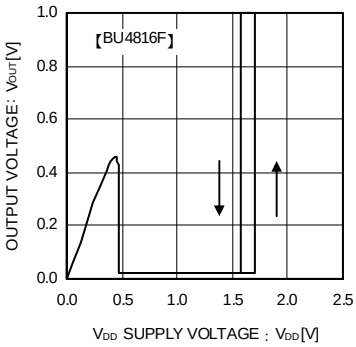


Fig.7 Operating Limit Voltage

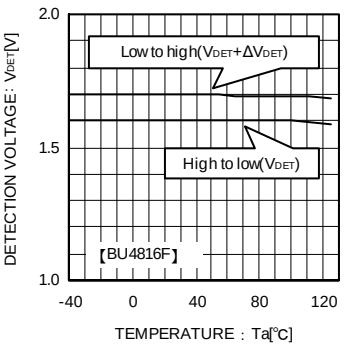


Fig.8 Detecting Voltage
Release Voltage

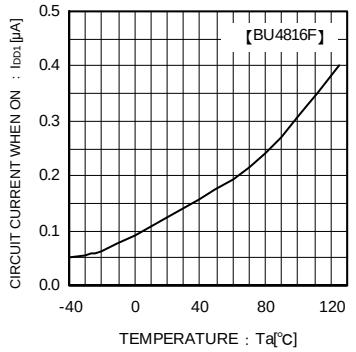


Fig.9 Circuit Current when ON

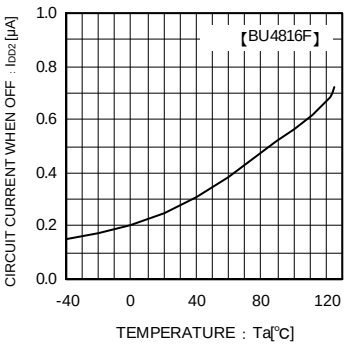


Fig.10 Circuit Current when OFF

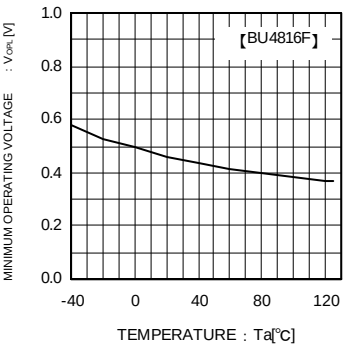


Fig.11 Operating Limit Voltage

● **Reference Data**

Examples of Output rising value(T_{PLH})and Output falling value(T_{PHL})

Part Number	T_{PLH}[µs] T	$_{PHL}$[µs]
BU4845G/F/FVE	23.3	275.9
BU4945G/F/FVE	3.5	354.3
	V_{DD}=4.3V→5.1V	V_{DD}=5.1V→4.3V

* This data is for reference only.

This figure will vary with the application, so please confirm actual operation conditions before use.

● **Explanation of Operation**

For both the open drain type(Fig.12)and the CMOS output type(Fig.13), the detection and release voltages are used as threshold voltages. When the voltage applied to the V_{DD} pins reaches the applicable threshold voltage, the Vout terminal voltage switches from either “High” to “Low” or from “Low” to “High”. Because the BU48□□G/F/FVE series uses an open drain output type, it is possible to connect a pull-up resistor to V_{DD} or another power supply [The output “High” voltage (V_{OUT}) in this case becomes V_{DD} or the voltage of the other power supply].

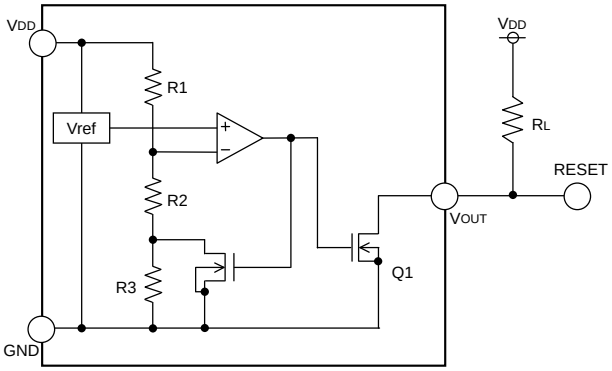


Fig.12 (BU48□□ type internal block diagram)

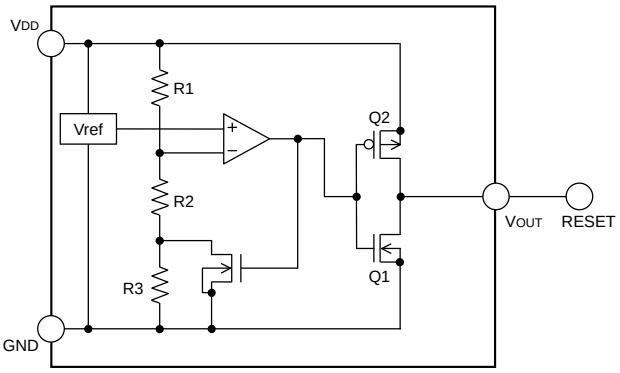


Fig.13 (BU49□□ type internal block diagram)

● **Timing Waveforms**

Example:The following shows the relationship between the input voltage V_{DD}, the CT Terminal Voltage V_{CT} and the output voltage V_{OUT} when the input power supply voltage V_{DD} is made to sweep up and sweep down (The circuits are those in Fig.12 and 13).

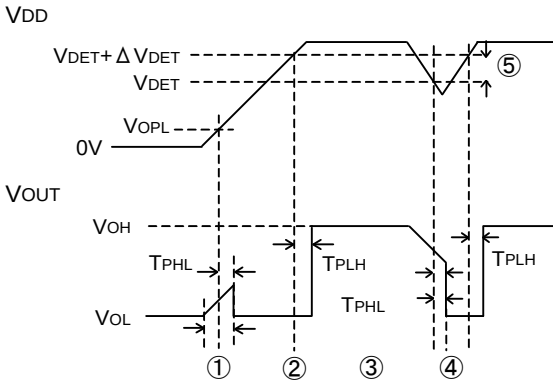


Fig.14

①When the power supply is turned on, the output is unsettled from after overing the operating limit voltage (V_{OPL}) until T_{PHL}. Therefore it is possible that the reset signal is not output when the rise time of VDD is faster than T_{PHL}.

②When V_{DD} is greater than V_{OPL} but less than the reset release voltage (V_{DET} + V_{DET}), output (V_{OUT}) voltages will switch to L.

③If V_{DD} exceeds the reset release voltage (V_{DET} + V_{DET}), then V_{OUT} switches from L to H (with a delay of T_{PLH}).

④If V_{DD} drops below the detection voltage (V_{DET}) when the power supply is powered down or when there is a power supply fluctuation, V_{OUT} switches to L (with a delay of T_{PHL}).

⑤The potential deference between the detection voltage and the release voltage is known as the hysteresis width (V_{DET}). The system is designed such that the output does not flip-flop with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

● **Circuit Applications**

1) Examples of a common power supply detection reset circuit

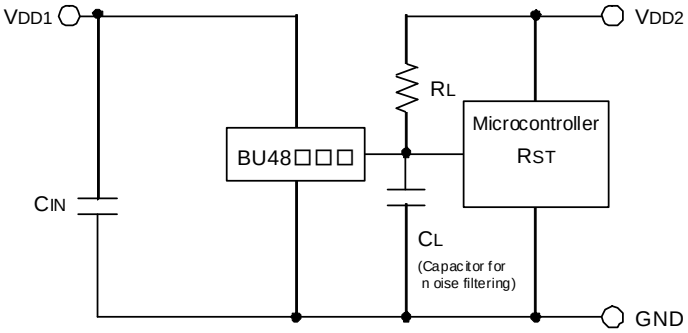


Fig.15 Open collector Output type

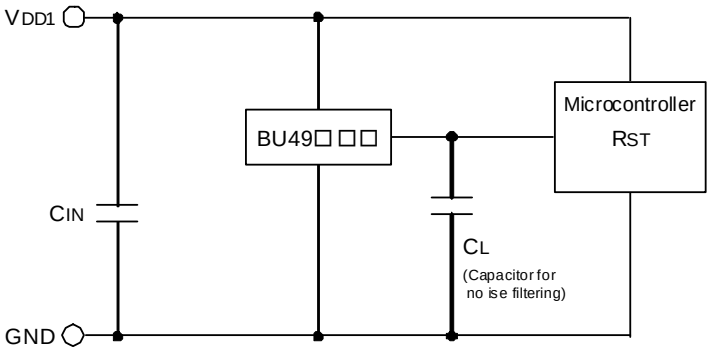


Fig.16 CMOS Output type

Application examples of BU48□□G/F/FVE series (Open Drain output type) and BU49□□G/F/FVE series (CMOS output type) are shown below.

CASE1:The power supply of the microcontroller ($V_{DD}2$) differs from the power supply of the reset detection ($V_{DD}1$). Use the Open Drain Output Type (BU48□□G/FVE) attached a load resistance (RL) between the output and $V_{DD}2$. (As shown Fig.15)

CASE2:The power supply of the microcontroller ($V_{DD}1$) is same as the power supply of the reset detection ($V_{DD}1$). Use CMOS output type (BU43□□G/FVE) or Open Drain Output Type (BU48□□G/FVE) attached a load resistance (RL) between the output and $V_{DD}1$. (As shown Fig.16)

When a capacitance CL for noise filtering or setting the output delay time is connected to the Vout pin (the reset signal input terminal of the microcontroller), please take into account the waveform of the rise and fall of the output voltage (Vout).

2) Examples of the power supply with resistor dividers

In applications where the power supply input terminal (VDD) of an IC with resistor dividers, it is possible that a through-current will momentarily flow into the circuit when the output logic switches, resulting in malfunctions (such as output oscillatory state).

(Through-current is a current that momentarily flows from the power supply (VDD) to ground (GND) when the output level switches from “High” to “Low” or vice versa.)

Consider the use of BD48□□ when the power supply input it with resistor dividers.

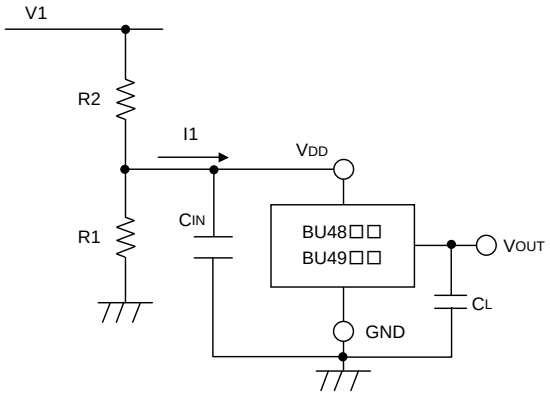


Fig.17

● **Operation Notes**

1. Absolute maximum range
   Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2. GND potential
   GND terminal should be a lowest voltage potential every state.
   Please make sure all pins that are over ground even if include transient feature.

3. Electrical Characteristics
   Be sure to check the electrical characteristics, that are one the tentative specification will be changed by temperature, supply voltage, and external circuit.

4. Bypass Capacitor for Noise Rejection
   Please put into the to reject noise between V_{DD} pin and GND with 1uF over and between V_{OUT} pin and GND with 1000pF. If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point.

5. Short Circuit between Terminal and Soldering
   Don't short-circuit between Output pin and V_{DD} pin, Output pin and GND pin, or V_{DD} pin and GND pin. When soldering the IC on circuit board please is unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

6. Electromagnetic Field
   Mal-function may happen when the device is used in the strong electromagnetic field.

7. The V_{DD} line inpedance might cause oscillation because of the detection current.

8. A V_{DD} -GND capacitor (as close connection as possible) should be used in high V_{DD} line impedance condition.

9. Lower than the mininum input voltage makes the V_{OUT} high impedance, and it must be V_{DD} in pull up (V_{DD}) condition.

10. Recommended value of RL Resistar is over 10kΩ (VDET=1.5V~4.8V),
    over 100kΩ (VDET=0.9~1.4V).

11. This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If 10MΩ leakage is assumed between the CT terminal and the GND terminal, 1MΩ connection between the CT terminal and the V_{DD} terminal would be recommended. Also, if the leakage is assumed between the V_{OUT} terminal and the GND terminal, the pull up resistor should be less than 1/10 of the assumed leak resistance.

12. External parameters
    For R_L, the recommended range is 10kΩ~1MΩ. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

13. Power on reset operation
    Please note that the power on reset output varies with the Vcc rise up time. Please verify the actual operation.

14. Precautions for board inspection
    Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the test operation.
    To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handing, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

15. When the power supply, is turned on because of incertain cases, momentary Rash-current flow into the IC at the logic unsettled, the couple capacitance, GND pattern of width and leading line must be considered.

● **Part Number Selection**

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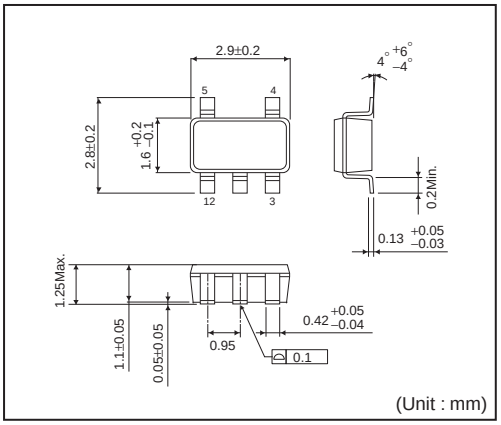
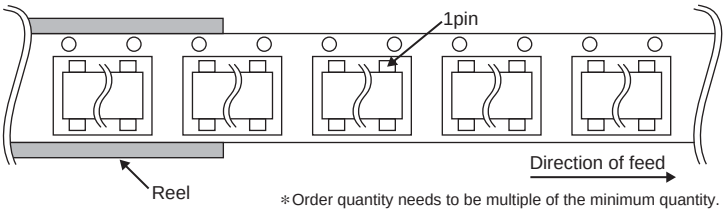
- BU48: Standard CMOS reset IC Open drain type
- BU49: Standard CMOS reset IC CMOS Output type
- Detection voltage: 09: 0.9V (0.1V step); 48: 4.8V
- Package: G: SSOP5; F: SOP4; FVE: VSOF5
- Taping Specifications: Embossed Taping

SSOP5



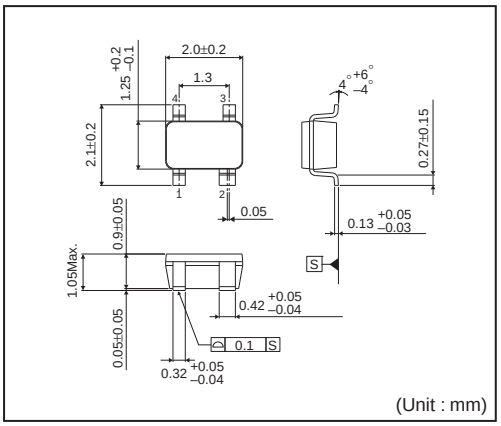
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



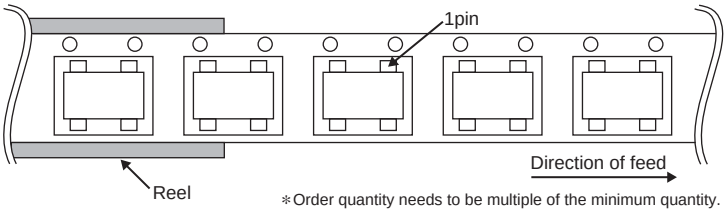
∗Order quantity needs to be multiple of the minimum quantity.

SOP4



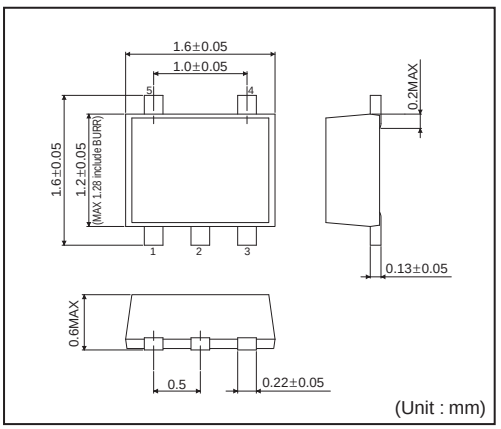
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



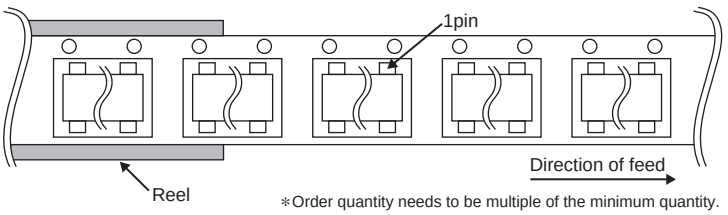
∗Order quantity needs to be multiple of the minimum quantity.

VSOF5



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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