NEC

MOS INTEGRATED CIRCUIT

μPD431000A

1M-BIT CMOS STATIC RAM
128K-WORD BY 8-BIT

Description

The μPD431000A is a high speed, low power, and 1,048,576 bits (131,072 words × 8 bits) CMOS static RAM.

The μPD431000A has two chip enable pins ($\overline{CE1}$, CE2) to extend the capacity. And battery backup is available. In addition to this, A and B versions are wide voltage versions.

The μPD431000A is packed in 32-pin plastic DIP, 32-pin plastic SOP, and 32-pin plastic TSOP(I).

Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150, 250 ns (MAX.)
★ • Wide voltage range (A version: V_{CC} = 3.0 V to 5.5 V, B version: V_{CC} = 2.7 V to 5.5 V)
- 2 V (MIN.) data retention
- Output Enable input for easy application
- Two Chip Enable inputs: $\overline{CE1}$, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Standby supply current μA (MAX.)	Data retention supply current[Note 1] μA (MAX.)
μPD431000A-L	70, 85	4.5 to 5.5	0 to 70	100	15
μPD431000A-LL				20	3
μPD431000A-A	70[Note 2], 100, 120	3.0 to 5.5		13[Note 3]	
μPD431000A-B	70[Note 2], 100, 120, 150	2.7 to 5.5		11[Note 4]	

Notes 1. $T_A \leq 40$ °C

2. V_{CC} = 4.5 to 5.5 V

3. 20 μA (V_{CC} > 3.6 V)

4. 20 μA (V_{CC} > 3.3 V)

The information in this document is subject to change without notice.

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Printed in Japan

The mark ★ shows major revised points.

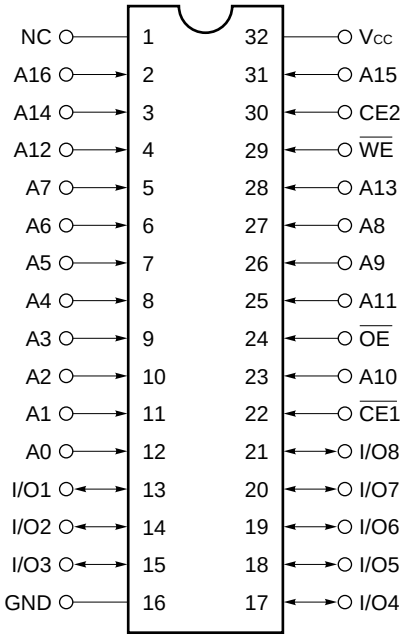
★ Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD431000ACZ-70L	32-pin Plastic DIP (600 mil)	70	4.5 to 5.5	0 to 70	L Version
μPD431000ACZ-85L		85			
μPD431000ACZ-70LL		70			LL Version
μPD431000ACZ-85LL		85			
μPD431000AGW-70L	32-pin Plastic SOP (525 mil)	70			L Version
μPD431000AGW-85L		85			
μPD431000AGW-70LL		70			LL Version
μPD431000AGW-85LL		85			
μPD431000AGW-A10		100	3.0 to 5.5		A Version
μPD431000AGW-A12		120			
μPD431000AGW-B10		100	2.7 to 5.5		B Version
μPD431000AGW-B12		120			
μPD431000AGW-B15		150			
μPD431000AGZ-70LL-KJH	32-pin Plastic TSOP (I) (8 × 20 mm) (Normal bent)	70	4.5 to 5.5		LL Version
μPD431000AGZ-A10-KJH		100	3.0 to 5.5		A Version
μPD431000AGZ-A12-KJH		120			
μPD431000AGZ-B10-KJH		100	2.7 to 5.5		B Version
μPD431000AGZ-B12-KJH		120			
μPD431000AGZ-B15-KJH		150			
μPD431000AGZ-70LL-KKH	32-pin Plastic TSOP (I) (8 × 20 mm) (Reverse bent)	70	4.5 to 5.5		LL Version
μPD431000AGZ-A10-KKH		100	3.0 to 5.5		A Version
μPD431000AGZ-A12-KKH		120			
μPD431000AGZ-B10-KKH		100	2.7 to 5.5		B Version
μPD431000AGZ-B12-KKH		120			
μPD431000AGZ-B15-KKH		150			
μPD431000AGU-70LL-9JH	32-pin Plastic TSOP (I) (8 × 13.4 mm) (Normal bent)	70	4.5 to 5.5		LL Version
μPD431000AGU-A10-9JH		100	3.0 to 5.5		A Version
μPD431000AGU-A12-9JH		120			
μPD431000AGU-B10-9JH		100	2.7 to 5.5		B Version
μPD431000AGU-B12-9JH		120			
μPD431000AGU-B15-9JH		150			
μPD431000AGU-70LL-9KH	32-pin Plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)	70	4.5 to 5.5		LL Version
μPD431000AGU-A10-9KH		100	3.0 to 5.5		A Version
μPD431000AGU-A12-9KH		120			
μPD431000AGU-B10-9KH		100	2.7 to 5.5		B Version
μPD431000AGU-B12-9KH		120			
μPD431000AGU-B15-9KH		150			

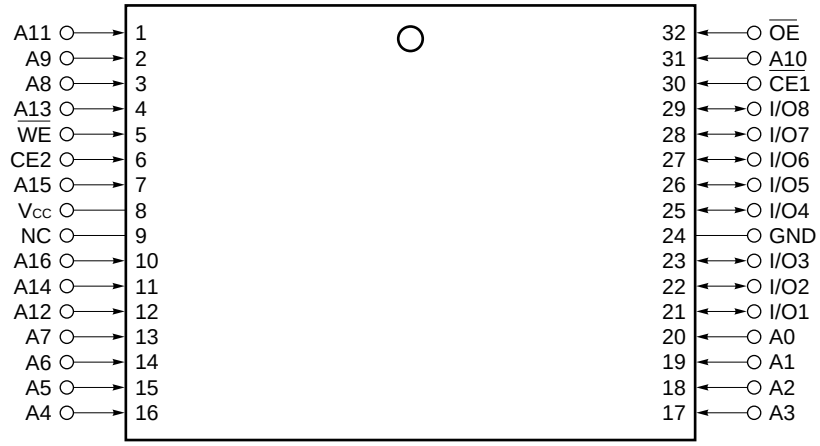
Pin Configuration (Marking side)

32-pin Plastic DIP (600 mil)
[μPD431000ACZ]

32-pin Plastic SOP (525 mil)
[μPD431000AGW]



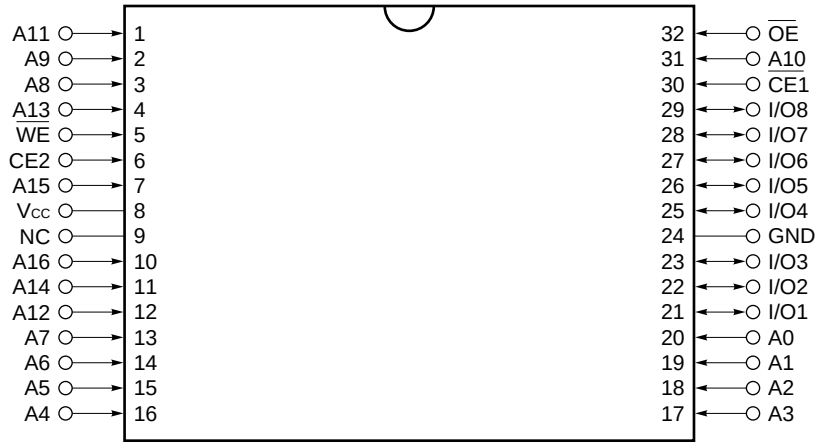
32-pin Plastic TSOP (I) (8 × 20mm)
(Normal bent)
[μPD431000AGZ-KJH]



32-pin Plastic TSOP (I) (8 × 20mm)
(Reverse bent)
[μPD431000AGZ-KKH]

A0 to A16	: Address inputs
I/O1 to I/O8	: Data inputs/outputs
$\overline{CE1}$, CE2	: Chip Enable 1, 2
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
V_{CC}	: Power supply
GND	: Ground
NC	: No connection

32-pin Plastic TSOP (I) (8 × 13.4mm)
(Normal bent)
[μPD431000AGU-9JH]



32-pin Plastic TSOP (I) (8 × 13.4mm)
(Reverse bent)
[μPD431000AGU-9KH]

A0 to A16	: Address inputs
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$\overline{CE1}$, CE2	: Chip Enable 1, 2
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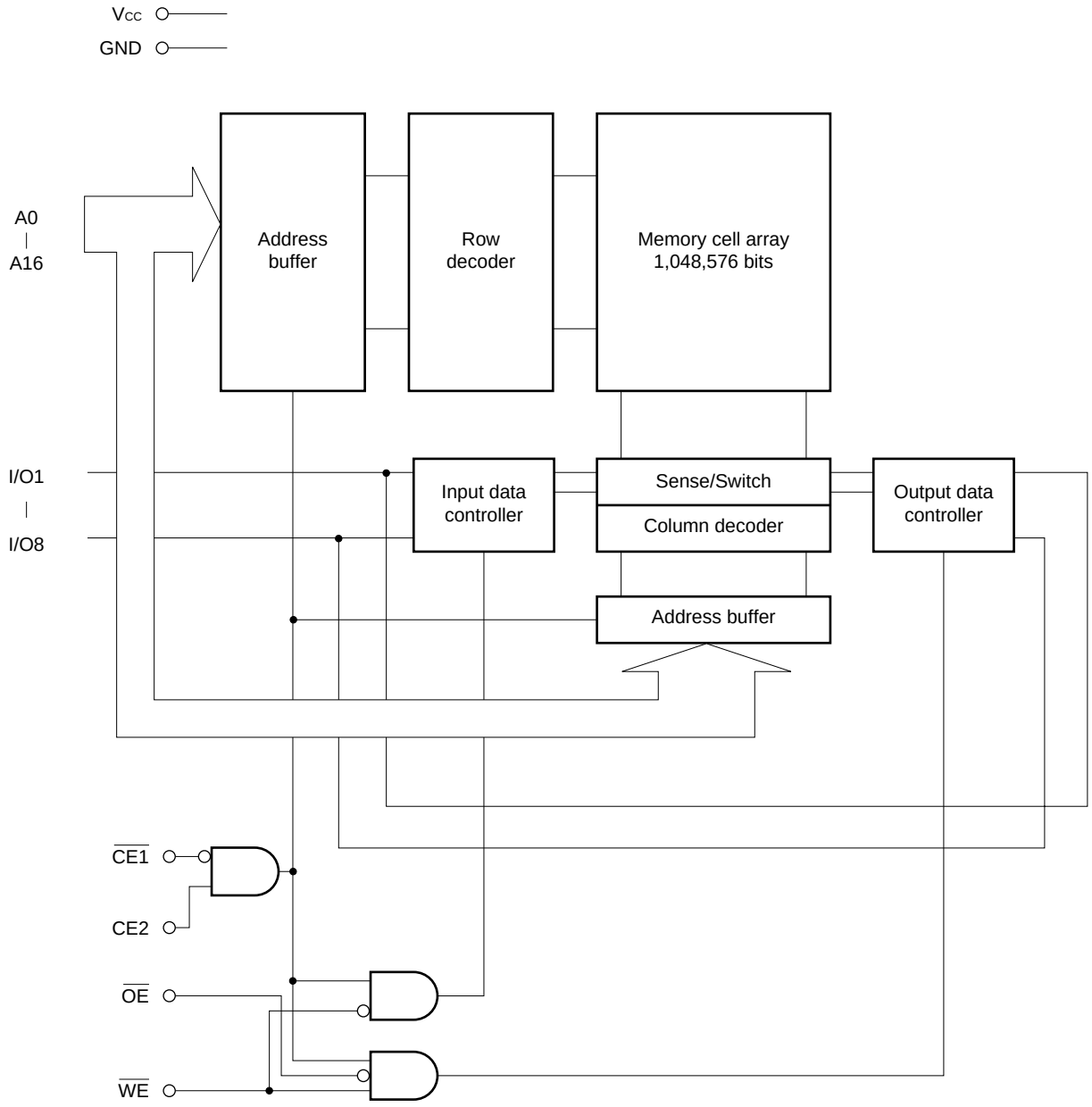
Block Diagram



Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Supply current
H	×	×	×	Not selected	High impedance	I_{SB}
×	L	×	×			I_{CCA}
L	H	H	H	Output disable		
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5[Note] to +7.0	V
Input/Output voltage	V_T	–0.5[Note] to V_{CC} + 0.5	V
Operating ambient temperature	T_A	0 to 70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width 30 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (1/2)

Parameter	Symbol	μPD431000A-L μPD431000A-LL		μPD431000A-A		Unit
		MIN.	MAX.	MIN.	MAX	
Supply voltage	V_{CC}	4.5	5.5	3.0	5.5	V
High level input voltage	V_{IH}	2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
Low level input voltage	V_{IL}	–0.3[Note]	+0.8	–0.3[Note]	+0.5	V
Operating ambient temperature	T_A	0	70	0	70	°C

Note –3.0 V (MIN.) (Pulse width 30 ns)

★ Recommended Operating Conditions (2/2)

Parameter	Symbol	μPD431000A-B		Unit
		MIN.	MAX.	
Supply voltage	V_{CC}	2.7	5.5	V
High level input voltage	V_{IH}	2.2	V_{CC} + 0.5	V
Low level input voltage	V_{IL}	–0.3[Note]	+0.5	V
Operating ambient temperature	T_A	0	70	°C

Note –3.0 V (MIN.) (Pulse width 30 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted) (1/2)

Parameter	Symbol	Test Conditions	μPD431000A-L			μPD431000A-LL			μPD431000A-A			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}	–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} Minimum cycle time $I_{I/O}$ = 0 mA		40	70		40	70		40	70	mA
		V_{CC} ≤ 3.6 V			—			—			35	
	I_{CCA2}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA			15			15			15	
		V_{CC} ≤ 3.6 V			—			—			8	
	I_{CCA3}	$\overline{CE1}$ ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V			10			10			10	
		V_{CC} ≤ 3.6 V			—			—			8	
Standby supply current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			3			3			3	mA
		V_{CC} ≤ 3.6 V			—			—			2	
	I_{SB1}	$\overline{CE1}$ ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V		2	100		1	20		1	20	μA
		V_{CC} ≤ 3.6 V			—			—		0.5	13	
	I_{SB2}	CE2 ≤ 0.2 V		2	100		1	20		1	20	
		V_{CC} ≤ 3.6 V		—	—		—	—		0.5	13	
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA, V_{CC} ≥ 4.5 V	2.4			2.4			2.4			V
		I_{OH} = –0.5 mA	—			—			2.4			
	V_{OH2}	I_{OH} = –0.02 mA	—			—			V_{CC} –0.1			
Low level output voltage	V_{OL1}	I_{OL} = 2.1 mA, V_{CC} ≥ 4.5 V			0.4			0.4			0.4	V
		I_{OL} = 1.0 mA			—			—			0.4	
	V_{OL2}	I_{OL} = 0.02 mA			—			—			0.1	

Remark These DC characteristics are in common regardless of package types and access time.

★ **DC Characteristics (Recommended operating conditions unless otherwise noted) (2/2)**

Parameter	Symbol	Test Conditions	μPD431000A-B			Unit
			MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} Minimum cycle time $I_{I/O}$ = 0 mA		40	70	mA
		V_{CC} ≤ 3.3 V		—	30	
	I_{CCA2}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA			15	
		V_{CC} ≤ 3.3 V			7	
	I_{CCA3}	$\overline{CE1}$ ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V			10	
		V_{CC} ≤ 3.3 V			7	
Standby supply current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			3	mA
		V_{CC} ≤ 3.3 V			2	
	I_{SB1}	$\overline{CE1}$ ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V		1	20	μA
		V_{CC} ≤ 3.3 V		0.5	11	
	I_{SB2}	CE2 ≤ 0.2 V		1	20	
		V_{CC} ≤ 3.3 V		0.5	11	
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA, V_{CC} ≥ 4.5 V	2.4			V
		I_{OH} = –0.5 mA	2.4			
	V_{OH2}	I_{OH} = –0.02 mA	V_{CC} – 0.1			
Low level output voltage	V_{OL1}	I_{OL} = 2.1 mA, V_{CC} ≥ 4.5 V			0.4	V
		I_{OL} = 1.0 mA			0.4	
	V_{OL2}	I_{OL} = 0.02 mA			0.1	

Remark These DC characteristics are in common regardless of package types and access time.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

AC Characteristics (Recommended operating conditions unless otherwise noted)

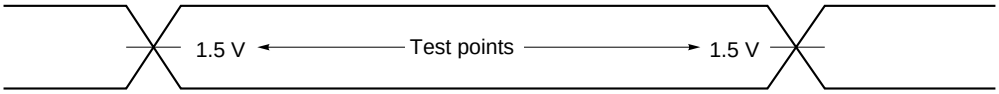
AC Test Conditions

Input waveform (Rise/fall time ≤ 5 ns)

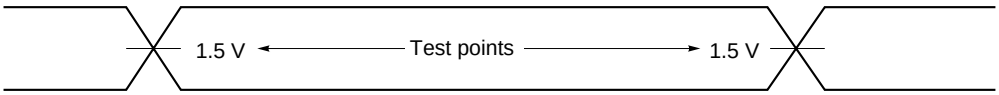
Input pulse levels

0.8 V to 2.2 V : μPD431000A-L, 431000A-LL

0.5 V to 2.2 V : μPD431000A-A, 431000A-B



Output waveform



★ **Output load**

AC characteristics should be measured with the following output load conditions.

Part number	Output load conditions	
	t_{AA}, t_{CO1}, t_{CO2}, t_{OE}, t_{OH}	t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{WHZ}, t_{OW}
μPD431000A-A10, 431000A-A12 μPD431000A-B10, 431000A-B12	1TTL + 50 pF	1TTL + 5 pF
μPD431000A-B15	1TTL + 100 pF	1TTL + 5 pF
μPD431000A-L, 431000A-LL	See **Figure 1**	See **Figure 2**

Figure 1

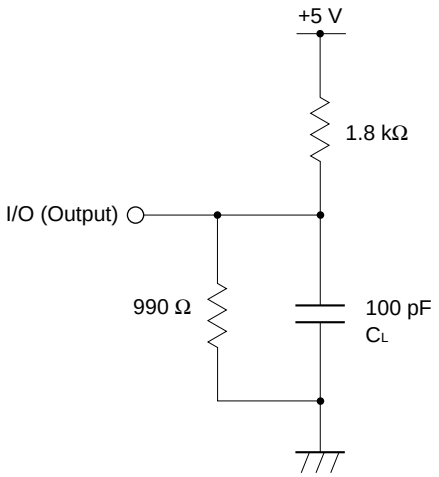
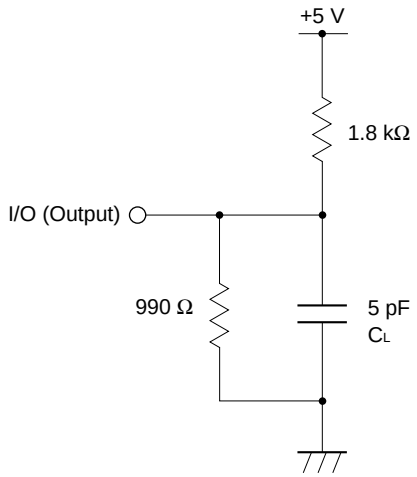


Figure 2



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle (1/2)

Parameter	Symbol	$V_{CC} \geq 4.5$ V				$V_{CC} \geq 3.0$ V				Unit	Condition
		μPD431000A-70 μPD431000A-A μPD431000A-B		μPD431000A-85		μPD431000A-A10		μPD431000A-A12			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		120		ns	
Address access time	t_{AA}		70		85		100		120	ns	**Note**
$\overline{CE1}$ access time	t_{CO1}		70		85		100		120	ns	
CE2 access time	t_{CO2}		70		85		100		120	ns	
$\overline{OE}$ to output valid	t_{OE}		35		45		50		60	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
$\overline{CE1}$ to output in low impedance	t_{LZ1}	10		10		10		10		ns	
CE2 to output in low impedance	t_{LZ2}	10		10		10		10		ns	
$\overline{OE}$ to output in low impedance	t_{OLZ}	5		5		5		5		ns	
$\overline{CE1}$ to output in high impedance	t_{HZ1}		25		30		35		40	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35		40	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		25		30		35		40	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

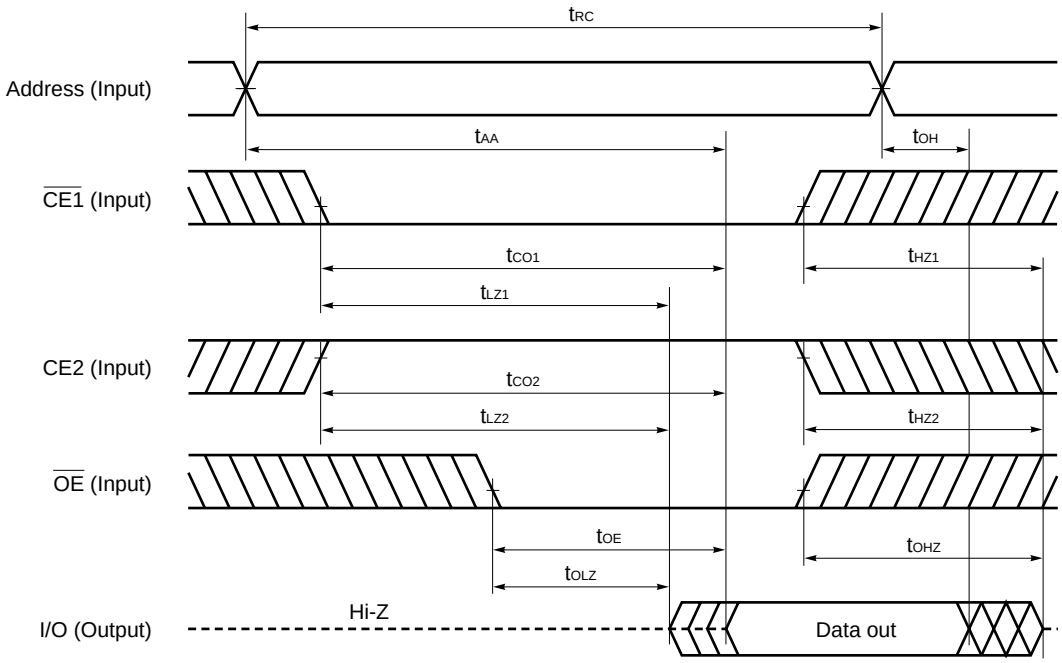
★ Read Cycle (2/2)

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD431000A-B10		μPD431000A-B12		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		150		ns	
Address access time	t_{AA}		100		120		150	ns	**Note**
$\overline{CE1}$ access time	t_{CO1}		100		120		150	ns	
CE2 access time	t_{CO2}		100		120		150	ns	
$\overline{OE}$ to output valid	t_{OE}		50		60		70	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
$\overline{CE1}$ to output in low impedance	t_{LZ1}	10		10		10		ns	
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
$\overline{OE}$ to output in low impedance	t_{OLZ}	5		5		5		ns	
$\overline{CE1}$ to output in high impedance	t_{HZ1}		35		40		50	ns	
CE2 to output in high impedance	t_{HZ2}		35		40		50	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		35		40		50	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Read Cycle Timing Chart



Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle (1/2)

Parameter	Symbol	$V_{CC} \geq 4.5$ V				$V_{CC} \geq 3.0$ V				Unit	Condition
		μPD431000A-70 μPD431000A-A μPD431000A-B		μPD431000A-85		μPD431000A-A10		μPD431000A-A12			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		120		ns	
$\overline{CE1}$ to end of write	t_{CW1}	55		70		80		100		ns	
CE2 to end of write	t_{CW2}	55		70		80		100		ns	
Address valid to end of write	t_{AW}	55		70		80		100		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	50		60		60		85		ns	
Write recovery time	t_{WR}	5		5		0		0		ns	
Data valid to end of write	t_{DW}	35		35		60		60		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		25		30		35		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

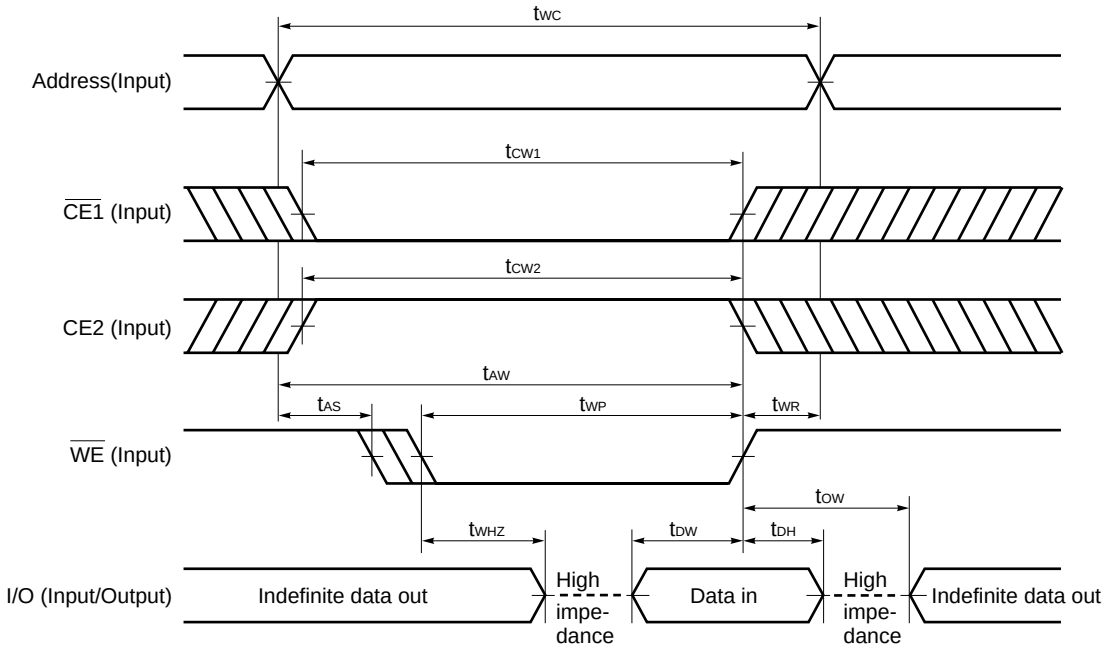
★ Write Cycle (2/2)

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD431000A-B10		μPD431000A-B12		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		150		ns	
$\overline{CE1}$ to end of write	t_{CW1}	80		100		120		ns	
CE2 to end of write	t_{CW2}	80		100		120		ns	
Address valid to end of write	t_{AW}	80		100		120		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	60		85		100		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	60		60		80		ns	
Data hold time	t_{DH}	0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		35		40		50	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



Cautions 1. During address transition, at least one of pins $\overline{CE1}$, CE2, $\overline{WE}$ should be inactivated.

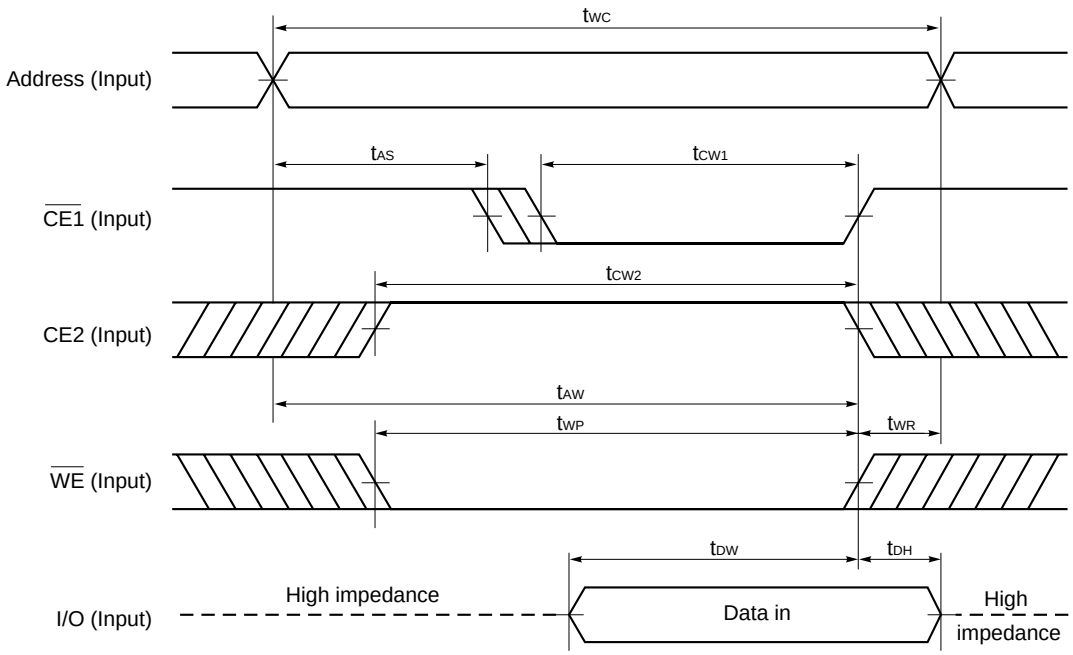
2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level CE2.

2. If $\overline{CE1}$ changes to low level at the same time or after the change of $\overline{WE}$ to low level, or if CE2 changes to high level at the same time or after the change of $\overline{WE}$ to low level, the I/O pins will remain high impedance state.

3. When $\overline{WE}$ is at low level, the I/O pins are always high impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 ($\overline{CE1}$ Controlled)

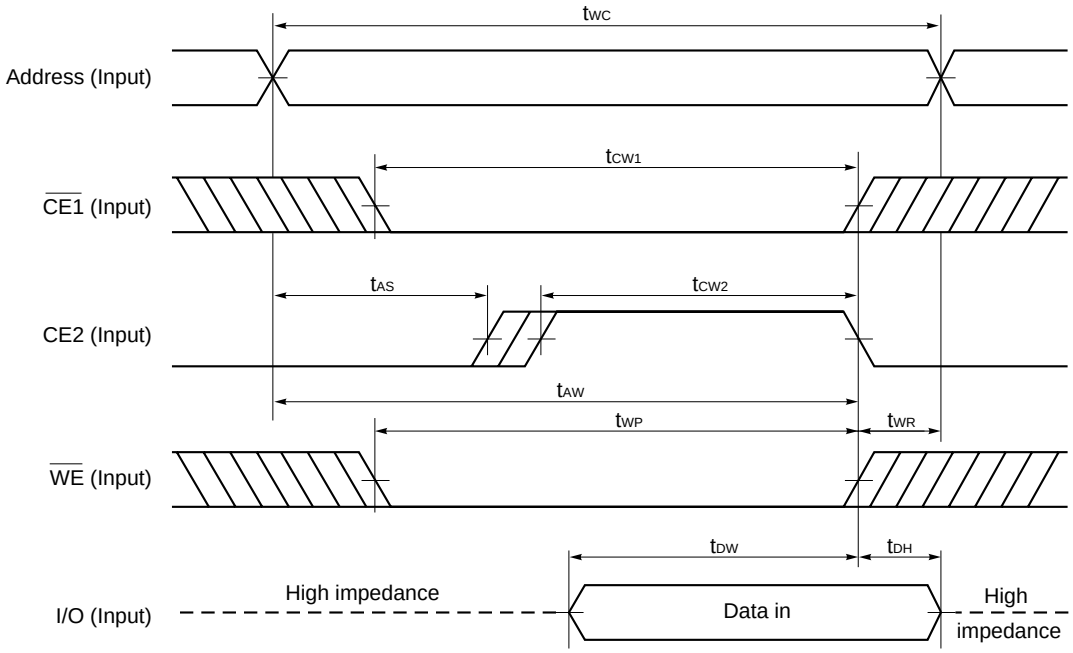


Cautions 1. During address transition, at least one of pins $\overline{CE1}$, CE2, $\overline{WE}$ should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins $\overline{CE1}$, CE2, $\overline{WE}$ should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level CE2.

★ Low V_{CC} Data Retention Characteristics

L Version (μPD431000A-L: T_A = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	$\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} – 0.2 V	2.0		5.5	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2.0		5.5	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, $\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		1	50 Note	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		1	50 Note	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 15 μA (T_A ≤ 40 °C)

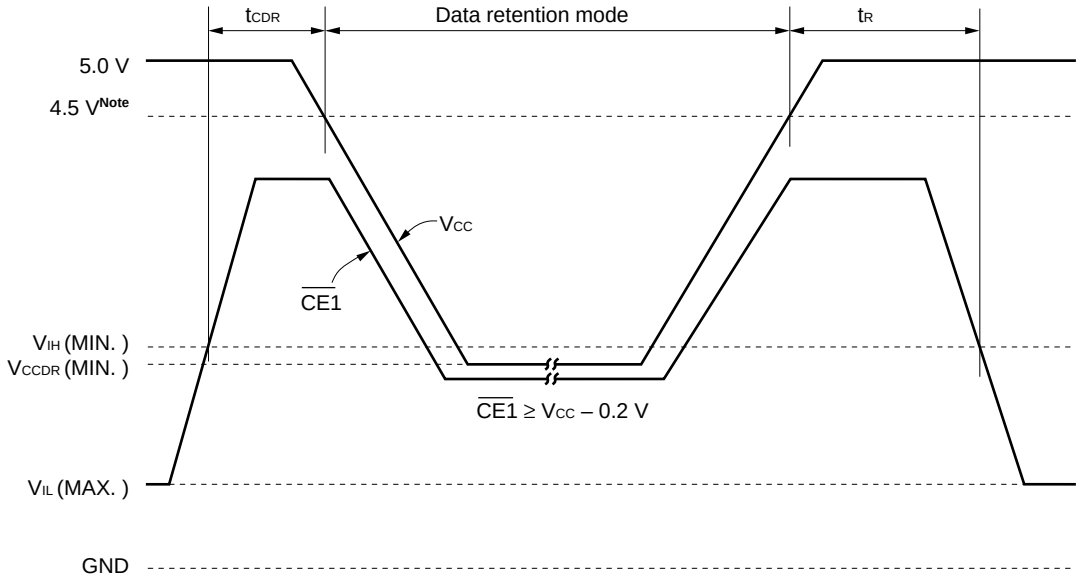
LL Version, A Version, and B Version (μPD431000A-LL, 431000A-A, 431000A-B: T_A = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	$\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} – 0.2 V	2.0		5.5	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2.0		5.5	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, $\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		0.5	10 Note	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.5	10 Note	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 3 μA (T_A ≤ 40 °C)

★ **Data Retention Timing Chart**

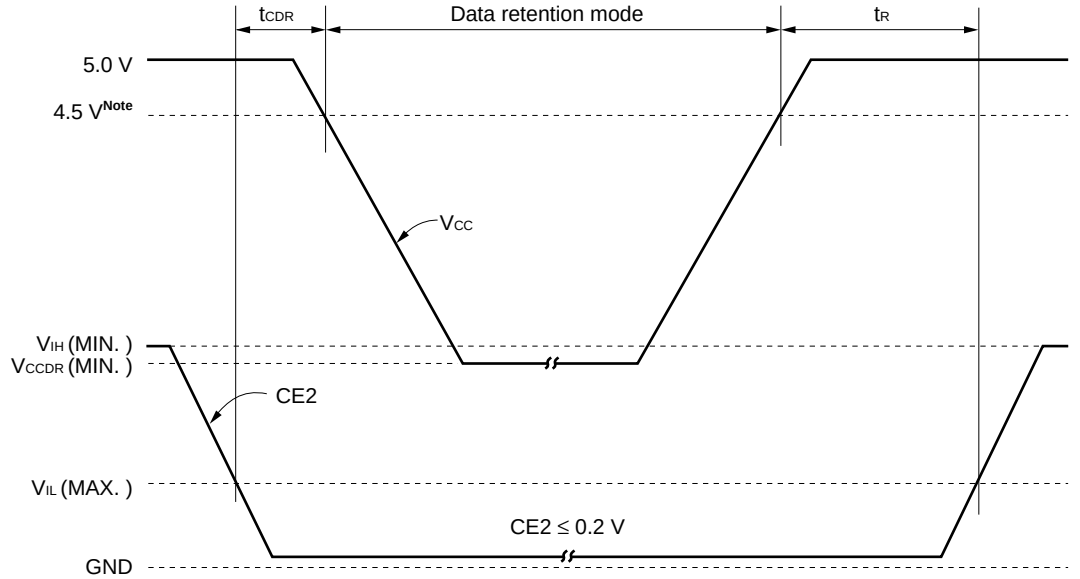
(1) $\overline{CE1}$ Controlled



Note A version: 3.0 V, B version: 2.7 V

Remark On the data retention mode by controlling $\overline{CE1}$, the input level of CE2 must be CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V. The other pins (Address, I/O, $\overline{WE}$, $\overline{OE}$) can be in high impedance state.

(2) CE2 Controlled

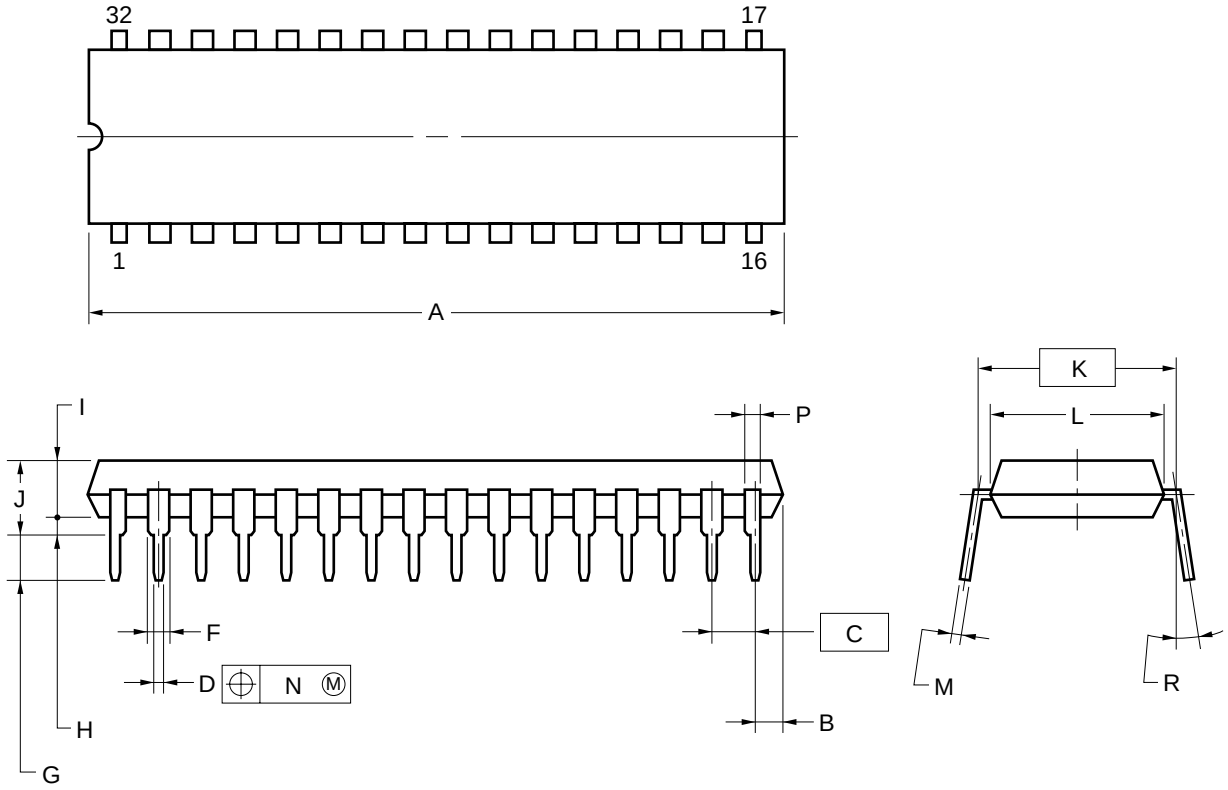


Note A version: 3.0 V, B version: 2.7 V

Remark The other pins ($\overline{CE1}$, Address, I/O, $\overline{WE}$, $\overline{OE}$) can be in high impedance state.

Package Drawings

32PIN PLASTIC DIP (600 mil)



NOTES

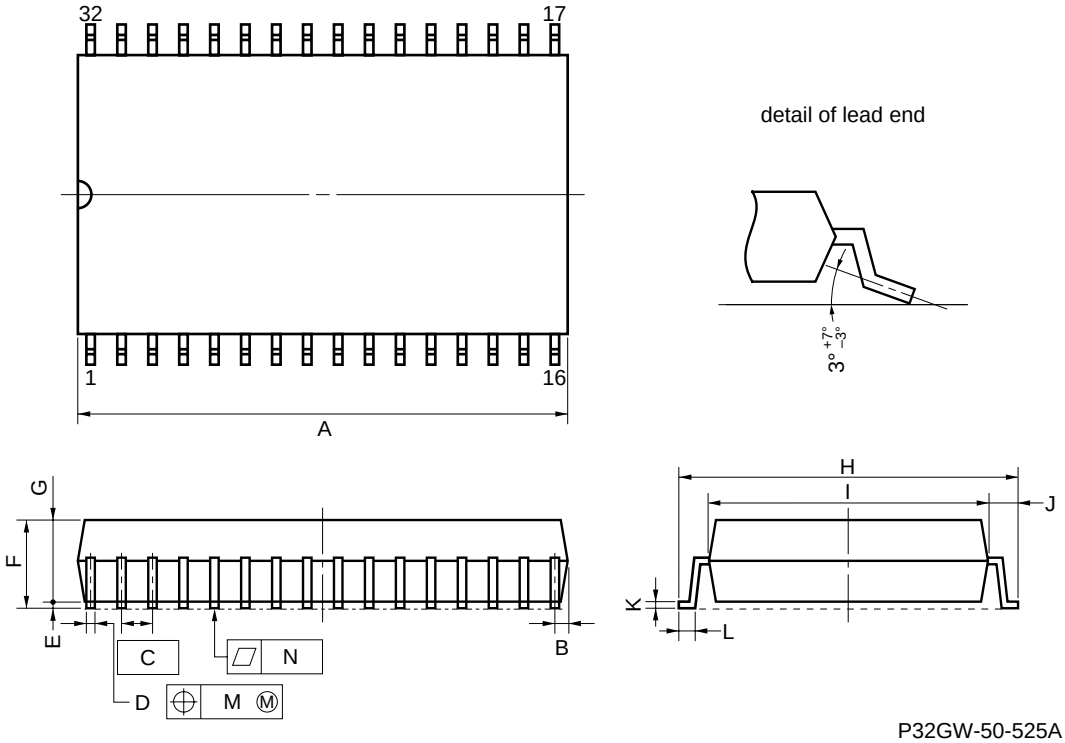
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	40.64 MAX.	1.600 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P32C-100-600A-1

32 PIN PLASTIC SOP (525 mil)



P32GW-50-525A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

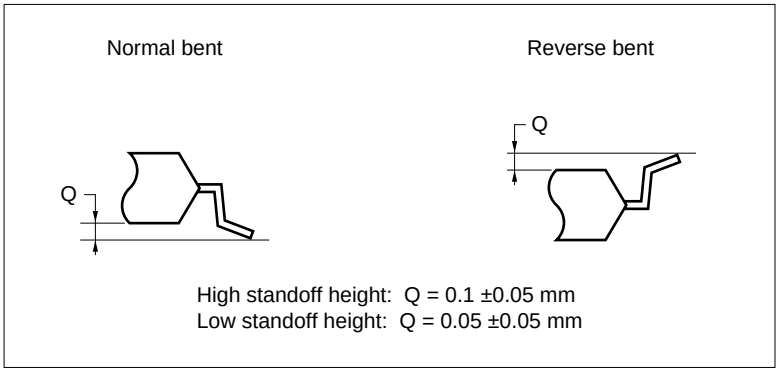
ITEM	MILLIMETERS	INCHES
A	20.61 MAX.	0.812 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.15±0.05	0.006
F	2.95 MAX.	0.117 MAX.
G	2.7	0.106
H	14.1±0.3	0.555±0.012
I	11.3	0.445
J	1.4±0.2	0.055±0.008
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

★ **Notice of change in 32-pin plastic TSOP (I) (8 × 20 mm) standoff height**

We are changing the 32-pin plastic TSOP (I) (8 × 20 mm) standoff height 0.05 ±0.05 mm (low standoff height) to 0.1 ±0.05 mm (high standoff height). Each lot version is identified by the fifth character of the lot number.

Difference between high standoff height and low standoff height

Detail of lead end

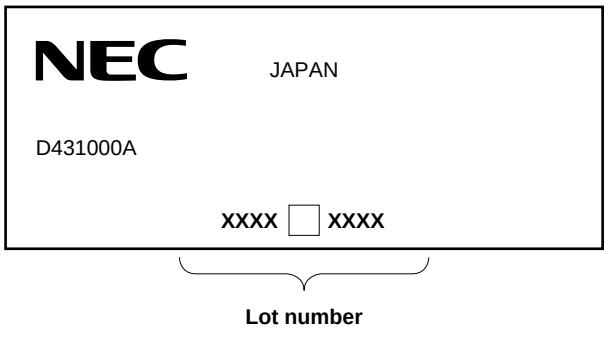


Identification of each lot version

Each lot version is identified by the fifth character of the lot number.

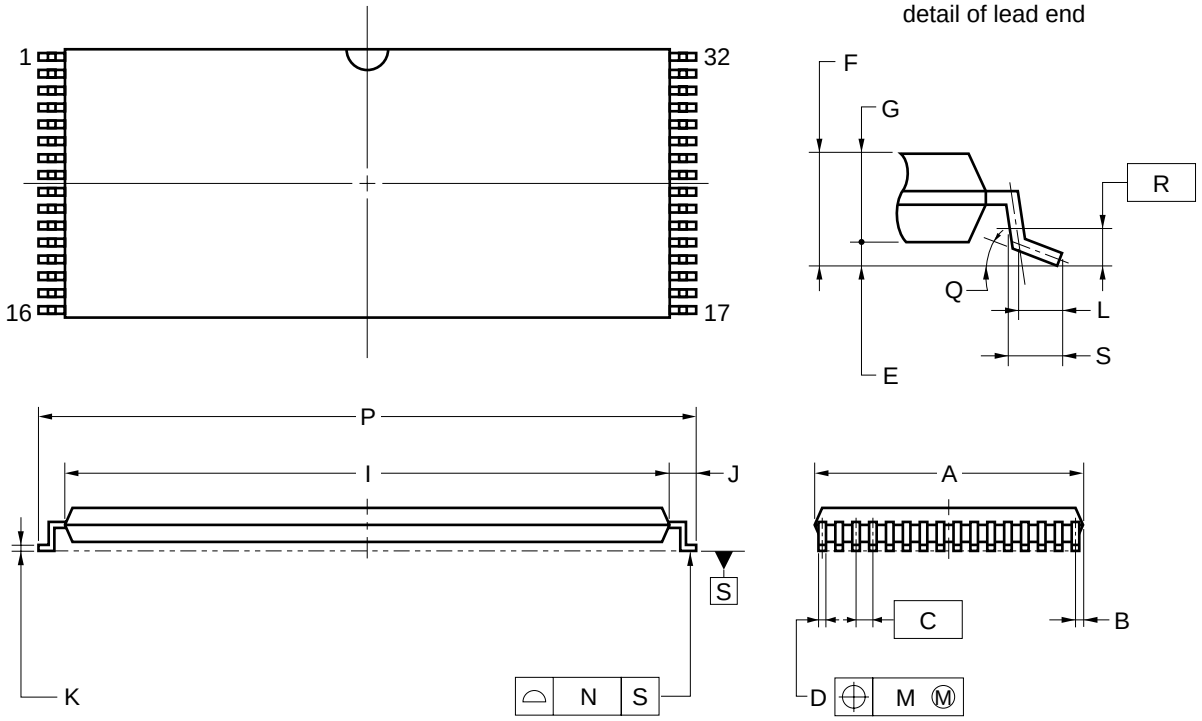
Fifth character of the lot number	Lot version	Standoff height
R	R version	0.1 ±0.05 mm (High standoff height)
H	H version	0.05 ±0.05 mm (Low standoff height)

Marking Example



★ **High standoff height**

32 PIN PLASTIC TSOP (I) (8×20)



NOTES

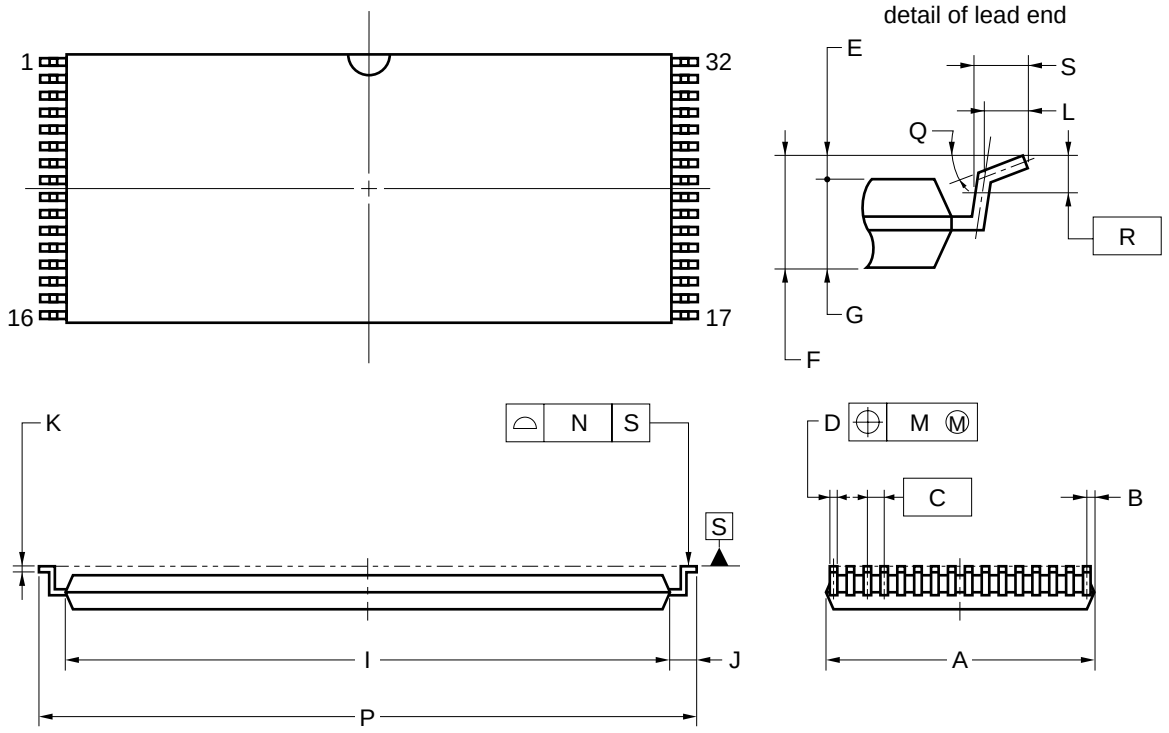
1. Controlling dimension — Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97±0.08	$0.038^{+0.004}_{-0.003}$
I	18.4±0.1	$0.724^{+0.005}_{-0.004}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S32GZ-50-KJH1

★ **High standoff height**

32 PIN PLASTIC TSOP (I) (8×20)



NOTES

1. Controlling dimension —— Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>).

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
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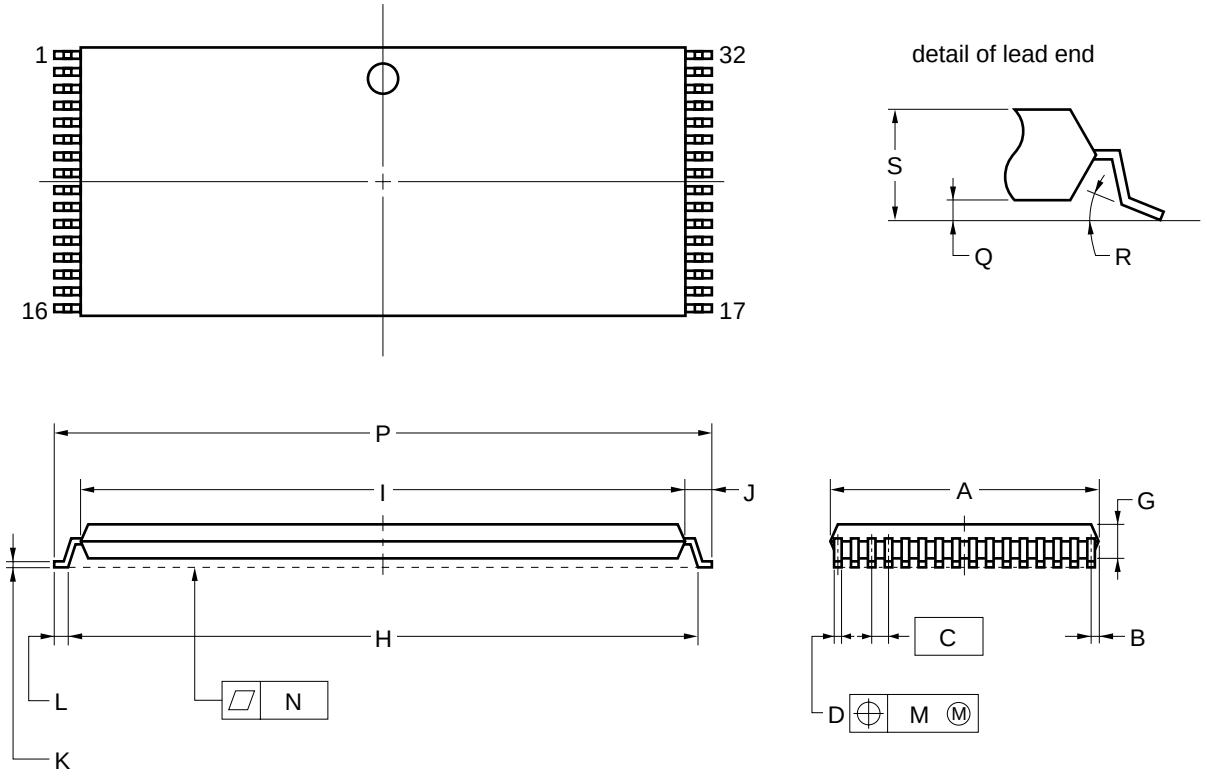
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22 ± 0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97 ± 0.08	$0.038^{+0.004}_{-0.003}$
I	18.4 ± 0.1	$0.724^{+0.005}_{-0.004}$
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	0.145 ± 0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0 ± 0.2	$0.787^{+0.009}_{-0.008}$
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25	0.010
S	0.60 ± 0.15	$0.024^{+0.006}_{-0.007}$

S32GZ-50-KKH1

Low standoff height

32 PIN PLASTIC TSOP (I) (8×20)



NOTES

(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

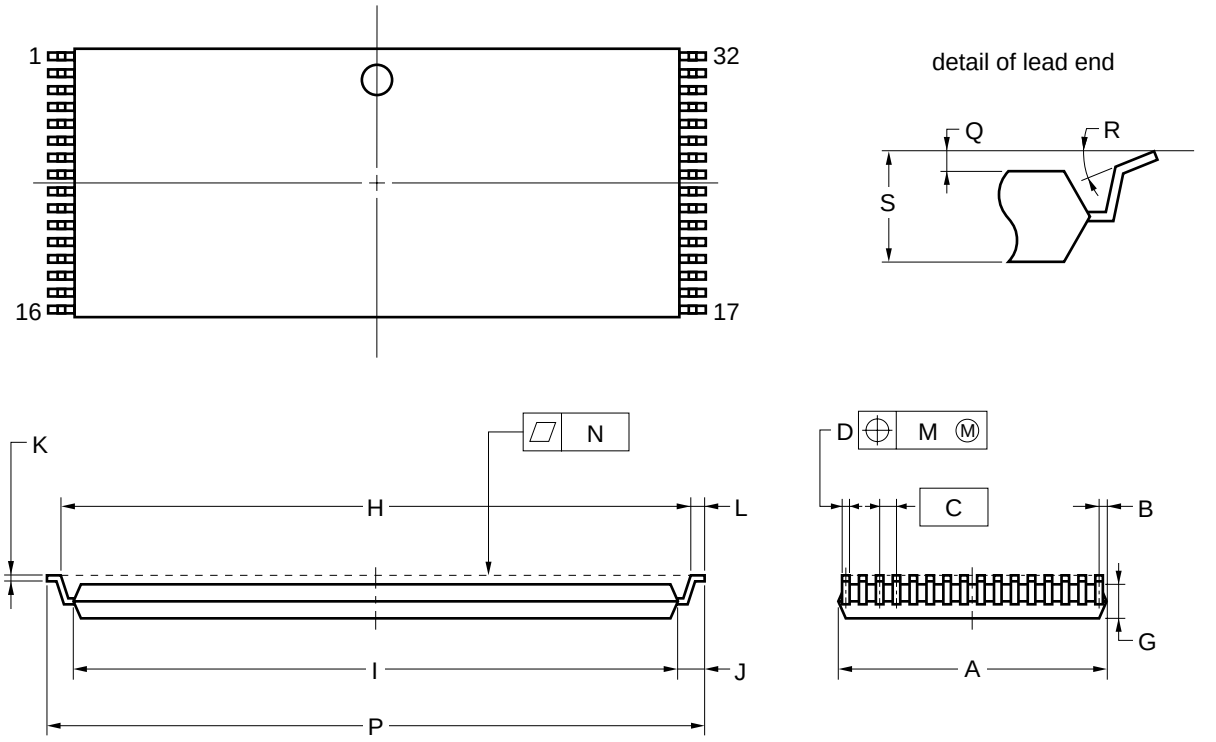
(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	19.0±0.2	0.748±0.008
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.1 MAX.	0.044 MAX.

S32GZ-50-KJH-3

Low standoff height

32 PIN PLASTIC TSOP (I) (8×20)



NOTES

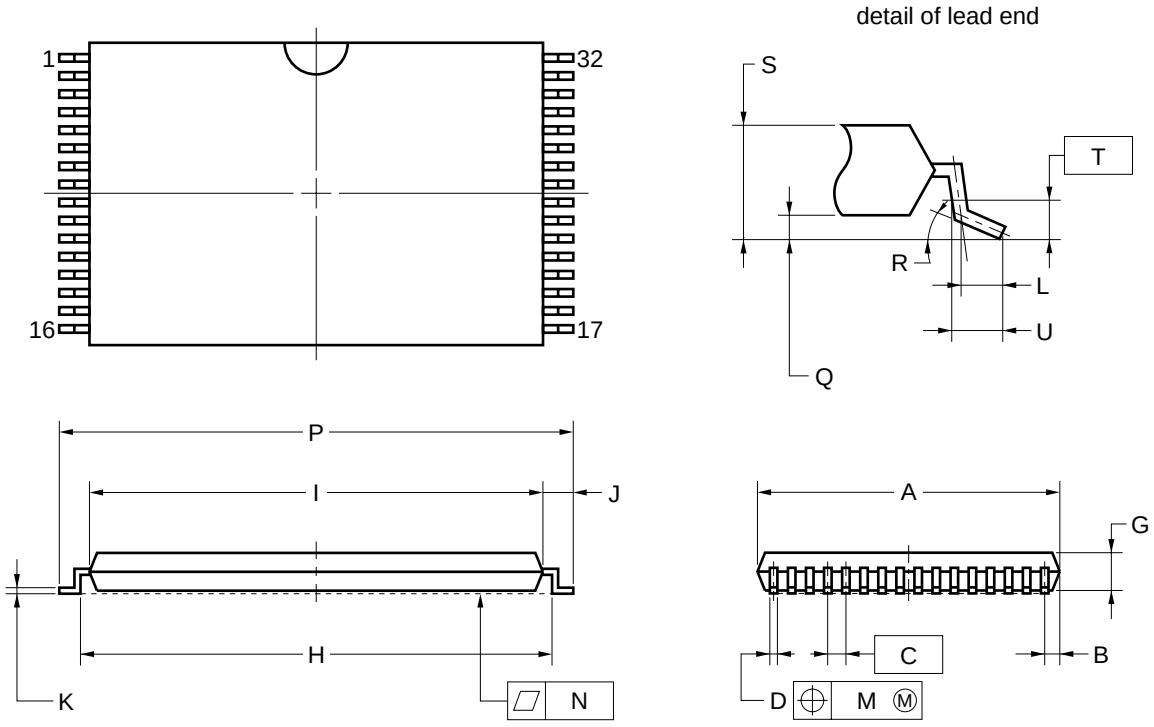
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	19.0±0.2	0.748±0.008
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.1 MAX.	0.044 MAX.

S32GZ-50-KKH-3

32PIN PLASTIC TSOP (I) (8x13.4)



NOTE

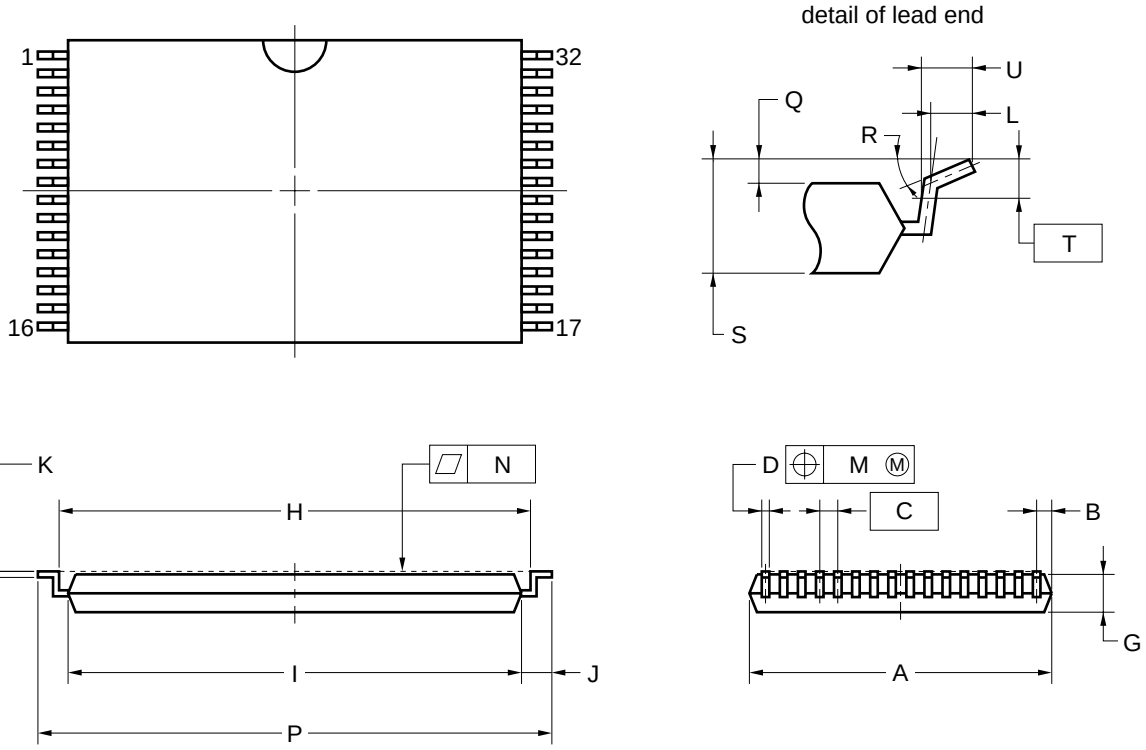
(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.331 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.02 (T.P.)
D	0.22 ± 0.05	$0.009^{+0.002}_{-0.003}$
G	1.0 ± 0.05	$0.039^{+0.003}_{-0.009}$
H	12.4±0.2	0.488±0.008
I	11.8 ± 0.1	$0.465^{+0.004}_{-0.005}$
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
M	0.08	0.003
N	0.08	0.003
P	13.4 ± 0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1 ± 0.05	0.004±0.002
R	$3^\circ{}^{+5^\circ}_{-3^\circ}$	$3^\circ{}^{+5^\circ}_{-3^\circ}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.01
U	0.16 ± 0.15	$0.006^{+0.007}_{-0.006}$

P32GU-50-9JH

32PIN PLASTIC TSOP (I) (8x13.4)



NOTE

(1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

(2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. <0.331 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.02 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
G	1.0±0.05	$0.039^{+0.003}_{-0.009}$
H	12.4±0.2	0.488±0.008
I	11.8±0.1	$0.465^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5	0.020
M	0.08	0.003
N	0.08	0.003
P	13.4±0.2	$0.528^{+0.008}_{-0.009}$
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.	0.048 MAX.
T	0.25	0.01
U	0.16±0.15	$0.006^{+0.007}_{-0.006}$

P32GU-50-9KH

Recommended Soldering Conditions

The following conditions must be met when soldering conditions of the μPD431000A.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD431000AGW : 32-pin Plastic SOP (525 mil)
μPD431000AGZ-KJH : 32-pin Plastic TSOP(I) (8 × 20 mm) (Normal bent)
μPD431000AGZ-KKH : 32-pin Plastic TSOP(I) (8 × 20 mm) (Reverse bent)
μPD431000AGU-9JH : 32-pin Plastic TSOP(I) (8 × 13.4 mm) (Normal bent)
μPD431000AGU-9KH : 32-pin Plastic TSOP(I) (8 × 13.4 mm) (Reverse bent)

Please consult with our sales offices

Type of Through Hole Mount Device

μPD431000ACZ: 32-pin Plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature: 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

M4 96.5