Low-power frequency synthesizer for mobile radio communications

UMA1014

FEATURES

- Single chip synthesizer; compatible with Philips cellular radio chipset
- Fully programmable RF divider
- I²C interface for two-line serial bus
- On-chip crystal oscillator/TCXO buffer from 3 to 16 MHz
- 16 reference division ratios allowing 5 to 100 kHz channel spacing
- 1/8 crystal frequency output
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm output
- Status register including out-of-lock indication and power failure
- Power-down mode.

APPLICATIONS

- Cellular mobile radio (NMT, AMPS, TACS)
- Private mobile radio (PMR)
- Cordless telephones.

GENERAL DESCRIPTION

The UMA1014 is a low-power universal synthesizer which has been designed for use in channelized radio communication. The IC is manufactured in bipolar technology and is designed to operate at 5 to 100 kHz channel spacing with an RF input from 50 to 1100 MHz. The channel is programmed via a standard I²C-bus. A low-power sensitive RF divider is incorporated together with a dead-zone eliminated, 3-state phase comparator. The low-noise charge pump delivers 1 mA or 1/2 mA output current to enable a better compromise between fast switching and loop bandwidth. A power-down circuit enables the synthesizer to be set to idle mode.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{CP}	supply voltage range	4.5	5.0	5.5	V
$I_{CC} + I_{CP}$	supply current	–	13	–	mA
I_{CCpd}	I_{CC} in power-down	–	2.5	–	mA
f_{ref}	phase comparator reference frequency	5	–	100	kHz
f_{RF}	RF input frequency	50	–	1100	MHz
T_{amb}	operating ambient temperature range	−40	–	85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1014T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

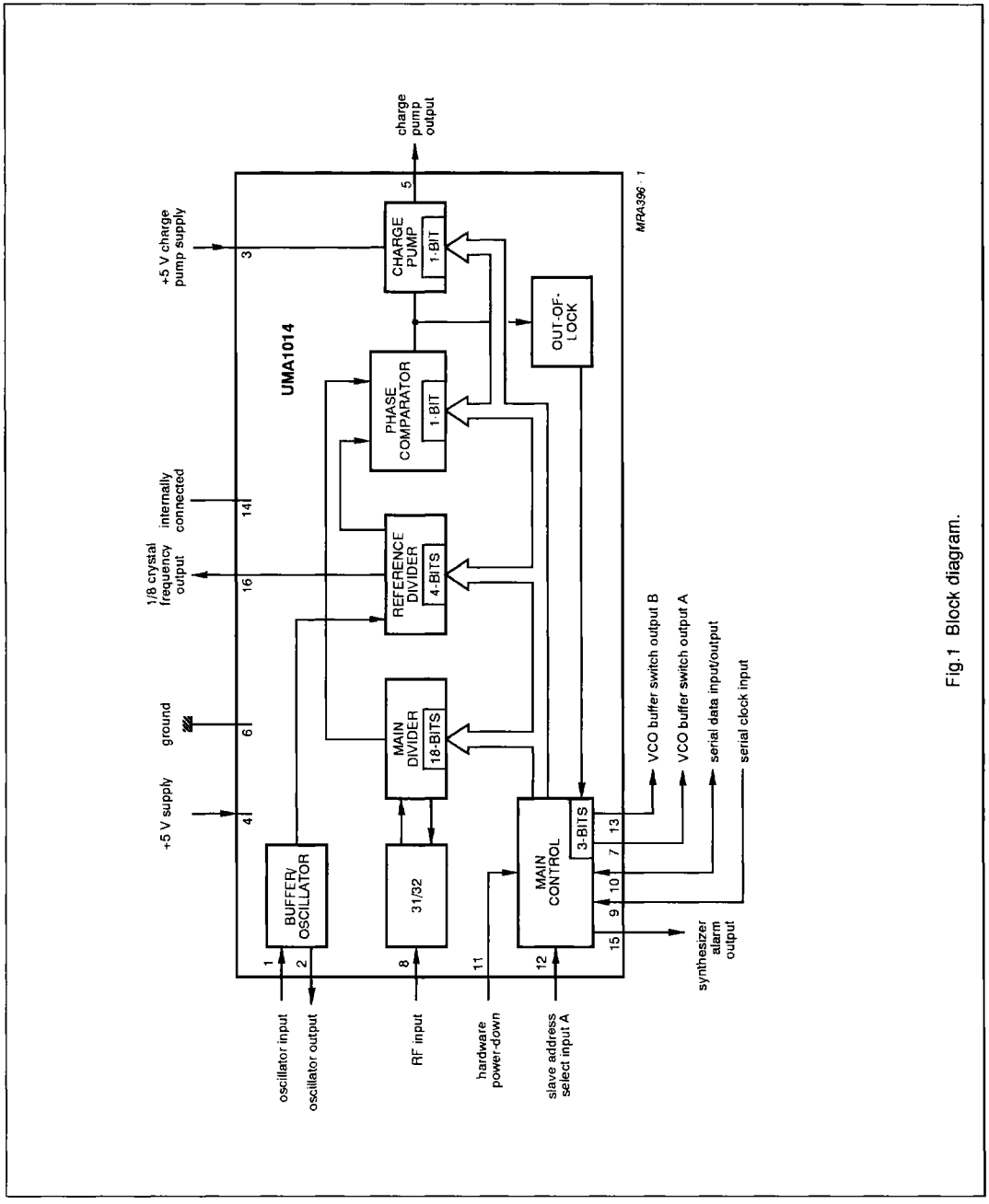


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCIN	1	oscillator or TCXO input
OSCOUT	2	oscillator output
V_{CP}	3	5 V charge pump supply
V_{CC}	4	5 V supply
PCD	5	charge pump output
GND	6	ground
VCOA	7	VCO buffer switch output A (including out-of-lock)
RF	8	RF input
SCL	9	serial clock input
SDA	10	serial data input/output
$\overline{HPD}$	11	hardware power-down (active LOW)
SAA	12	slave address select input A
VCOB	13	VCO buffer switch output B
i.c.	14	internally connected
SYA	15	synthesizer alarm output
FX8	16	1/8 crystal frequency output

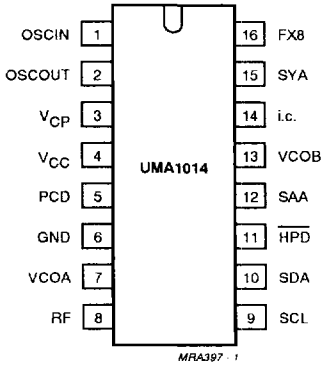


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UMA1014 is a low-power frequency synthesizer for radio communication which operates in the 50 to 1100 MHz range. The device includes an oscillator/buffer circuit, a reference divider, an RF divider, a 3-state phase comparator, a charge pump and a main control circuit to transfer the serial data into the four internal 8-bit registers. The V_{CC} supply feeds the logic part, the V_{CP} supply feeds the charge-pump only. Both supplies are +5 V (±10%). The power-down facility puts the synthesizer in the idle mode (all current supplies are switched off except in the control part). This allows any I²C transfer and all information in the registers is retained thus enabling fast power-up.

Main divider

The main divider is a pulse swallow type counter which is fully programmable. After a sensitive input amplifier (50 mV, −13 dBm), the RF signal is applied to a 31/32 duo-modulus counter. The output is then used as the clock for the 5-bit swallow counter R = (MD4 to MD0) and the 13-bit main counter N = (MD17 to MD5). The ratio is transferred via the I²C-bus to the registers B, C and D, and then buffered in an 18-bit latch. The ratio in the divider chain is updated with the new information when the least significant bit is received (i.e. D0). This update is synchronized to the output of the divider in order to limit the phase error during small jumps of the synthesized frequency.

The main divider can be programmed to any value between 2048 and 262143 (i.e. $2^{18}-1$). If ratio X, below 2048, is sent to the divider, the ratio (X + 2048) will be programmed. When it is required to switch between adjacent channels it is possible to program register D only, thus allowing shorter I²C programming time.

Oscillator

The oscillator is a common collector Colpitts type with external capacitive feedback. The oscillator has very small temperature drift and high voltage supply rejection. A TCXO or other type of clock can be used to drive the oscillator by connecting the source (preferably AC-coupled) to pin 1 and leaving pin 2 open-circuit. The oscillator acts as a buffer in this mode and requires no additional external components. The signal from the clock source should have a minimum space width of 31 ns.

Reference divider

The reference divider is semi-programmable with 16 division ratios which can be selected via the I²C-bus. The programming uses four bits of the register A (A3 to A0) as listed in Table 2. These ratios allow the use of a large number of crystal frequencies from 3 MHz up to 16 MHz. All main channel spacings can be obtained with a single crystal/TXCO frequency of 9.6 MHz.

Phase comparator

A diagram of the phase comparator and charge pump is illustrated in Fig.3.

The phase comparator is both a phase and frequency detector. The detector comprises dual flip-flops together with logic circuitry to eliminate the dead-zone. When a phase error is detected the UP or DOWN signal goes HIGH. This switches on the corresponding current generator which produces a source or sink current for the loop filter. When no phase error is detected PCD goes high impedance. The final tuning voltage for the VCO is provided by the loop filter. The charge pump current is programmable via the I²C-bus. When IPCD (bit 5) is set to logic 1 the charge pump delivers 1 mA; when IPCD is set to logic 0 the charge pump delivers 0.5 mA.

The phase comparator has a phase inverter logic input (PHI). This allows the use of inverted or non-inverted loop filter configurations. It is thus possible to use a passive loop filter which offers higher performances without an operational amplifier. The function of the phase comparator is given in Table 3 and a typical transfer curve is illustrated in Fig.4.

Out-of-lock detector

An out-of-lock detector using the UP and DOWN signals from the phase comparator is included on-chip. The pin VCOA is an open collector output which is forced LOW during an out-of-lock condition. The same information is also available via the I²C-bus in the status register (bit OOL). When the phase error (measured at the phase comparator) is greater than approximately 200 ns, an out-of-lock condition is immediately flagged. The flag is only released after 6 reference cycles when the phase error is less than 200 ns.

Table 1 Division ratio in the main divider

MAIN COUNTER: N								SWALLOW COUNTER: R		
MD17	MD16	MD15	...	MD8	MD7	...	MD5	MD4	...	MD0
B1	B0	C7	...	C0	D7	...	D5	D4	...	D0
MSB										LSB

Table 2 Reference divider programming

A3(RD3)	A2(RD2)	A1(RD1)	A0(RD0)	REFERENCE DIVISION RATIO	CHANNEL SPACING FOR 9.6 MHz AT OSCIN
0	0	0	0	128	75 kHz
0	0	0	1	160	60 kHz
0	0	1	0	192	50 kHz
0	0	1	1	240	40 kHz
0	1	0	0	256	37.5 kHz
0	1	0	1	320	30 kHz
0	1	1	0	384	25 kHz
0	1	1	1	480	20 kHz
1	0	0	0	512	18.75 kHz
1	0	0	1	640	15 kHz
1	0	1	0	768	12.5 kHz
1	0	1	1	960	10 kHz
1	1	0	0	1024	9.375 kHz
1	1	0	1	1280	7.5 kHz
1	1	1	0	1536	6.25 kHz
1	1	1	1	1920	5 kHz

Table 3 Operation of the phase comparator

	PHI = 0 (PASSIVE LOOP FILTER)			PHI = 1 (ACTIVE LOOP FILTER)		
	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$
UP	0	1	0	1	0	0
DOWN	1	0	0	0	1	0
I_{pcd}	−1 mA	1 mA	< ±5 nA	1 mA	−1 mA	< ±5 nA

MAIN CONTROL

The control part consists mainly of the I²C-bus control interface and a set of four registers A, B, C and D. The serial input data (SDA) is converted into 8-bit parallel words and stored in the appropriate registers. The data transmission to the synthesizer is executed in the burst mode with the following format:

//slave addr./subaddr./data1/data2/.../datan//; n up to 4

Data byte 1 is written in the register indicated by the subaddress. An auto-increment circuit, if enabled (AVI = 1), then provides the correct addressing for the ensuing data bytes. Since the length of the data burst is not fixed, it is possible to program only one register or the whole set. The registers are structured in such a way so that the burst, for normal operation, is kept as short as possible. The bits that are only programmed during the set-up (reference division ratio, power-down, phase inversion and current on PCD) are stored in registers A and B.

In the slave address six bits are fixed, the remaining two bits depend on the application.

Table 4 Slave address

1	1	0	0	0	1	$\overline{SAA}$	R/$\overline{W}$

SAA is the slave address. When SAA goes HIGH then $\overline{SAA}$ = 0, when SAA goes LOW then $\overline{SAA}$ = 1. This allows the use of two UMA1014s on the same bus but using a different address. R/$\overline{W}$ should be set to logic 0 when writing to the synthesizer or set to logic 1 when reading the status register.

The subaddress includes the register pointer, and sets the two flags related to the auto-increment (AVI) and the alarm disable (DI).

Table 5 Subaddress

X	X	X	DI	AVI	X	SB1	SB0

Where:

X = not used

DI (Disable Interrupt):
DI = 1 disables the alarm on SYA
DI = 0 enables the alarm.

AVI (Auto Value Increment):
AVI = 1 enables the automatic increment
AVI = 0 disables the auto-increment.

SB1/SB0 are the pointers of the register where DATA1 will be written (see Table 6).

When the auto-increment is disabled (AVI = 0), the subaddress pointer will maintain the same value during the I²C-bus transfer. All the data bytes will then be written consecutively in the register pointed by the subaddress.

Table 6 Pointer of the registers

SB1	SB0	REGISTER POINTED
0	0	A
0	1	B
1	0	C
1	1	D

Status register and synthesizer alarm

When an out-of-lock condition or a power dip occurs, SYA, which is an open collector output, is forced LOW and latched. The pin SYA will be released after the status register is read via the I²C-bus.

The status register contains the following information:

Table 7 Status register

0	0	0	OOL	0	LOOL	LPD	DI

Where:

OOL = momentary out-of-lock
LOOL = latched out-of-lock
LPD = latched power dip
DI = disable interrupt (of the last write cycle).

The I²C-bus protocol to read this internal register is a single byte without subaddressing:

//slave address (R/$\overline{W}$ = 1)/status register (read)//

Table 8 Bit allocation

REGISTER	POINTER	BIT ALLOCATION								PRESET
		7	6	5	4	3	2	1	0	
A	00	PD	X	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10100101
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Where X = not used

Table 9 Register allocation

REGISTER NAME	BIT NAME	FUNCTION		PRESET VALUE
A	PD	power down	PD = 0 normal operation	0
	IPCD	programmable charge pump current	IPCD = 1 = 1 mA; IPCD = 0 = 0.5 mA	0
	RD3...RD0	reference ratio	see Table 2	1110; r = 1536
B	PHI	phase inverter	PHI = 0 passive loop filter	0
	VCOA	VCO switch A	set pin 7	1
	VCOB	VCO switch B	set pin 13	0
	MD17, MD16	bits 17 and 16	MSB of main divider ratio	01
C	MD15 to MD8	bits 15 to 8	main divider ratio	00111000
D	MD7 to MD0	bits 7 to 0	main divider ratio	10000000; r = 80000

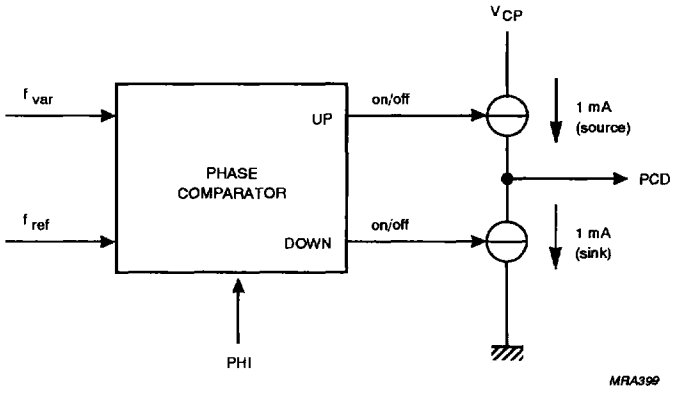


Fig.3 Phase comparator block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage range	−0.3	7.0	V
V_i	voltage range to ground (all pins)	0	V_{CC}	V
T_{stg}	IC storage temperature range	−55	+125	°C
T_{amb}	operating ambient temperature range	−40	+85	°C

HANDLING

Every pin referenced to ground withstands ESD (HMB) tests in accordance with MIL-STD-883C method 3015 class 2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling Integrated Circuits.

CHARACTERISTICS

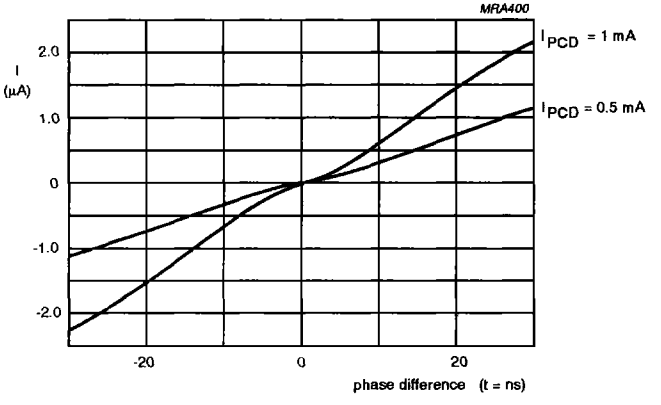
T_{amb} = 25 °C; V_{CC} = 4.5 to 5.5 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and V_{CP})						
V_{CC}	supply voltage range		4.5	–	5.5	V
I_{CC}	supply current		–	11.5	13.5	mA
I_{CCpd}	supply current	power-down	–	2.5	3.3	mA
V_{CP}	charge pump supply voltage		4.5	–	5.5	V
I_{CP}	charge pump supply current	IPCD = 0.5 mA	–	1.4	1.8	mA
I_{CPpd}	charge pump supply current	power-down	–	0.01	–	mA
RF dividers (pin RF)						
f_{RF}	frequency range		50	–	1100	MHz
$V_{RF(rms)}$	input voltage level (RMS value)	50 to 100 MHz	150	–	200	mV
		100 to 1100 MHz	50	–	150	mV
R_I	input resistance	at 1 GHz	–	200	–	Ω
		at 100 MHz	–	600	–	Ω
C_I	input capacitance	note 1	–	2.0	–	pF
R_{RF}	division ratios		2048	–	262143	–
Oscillator and reference divider (pins OSCIN and OSCOUT)						
f_{OSC}	oscillator frequency range		3	–	16	MHz
$V_{OSC(RMS)}$	input level sine wave (RMS value)		0.15	–	V_{CC}/2.8	V
$V_{OSC(p-p)}$	input level square wave (peak-to-peak value)		0.45	–	V_{CC}	V
t_{OSC_mk}	input mark width	see Fig.8	10	–	–	ns
t_{OSC_sp}	input space width		31	–	–	ns
Z_{OSC}	output impedance at pin OSCOUT		–	–	2	kΩ
R_{ref}	reference division ratio	see Table 1	128	–	1920	
1/8 crystal frequency (open collector output) (pin FX8)						
I_{OL}	LOW level output current	$V_{OL} \geq 0.6$ V	1.0	–	–	mA
Phase comparator (pin PCD)						
f_{PCD}	frequency range		5	–	100	kHz
I_{PCD}	output current	V_{PCD} = 2.5 V				
		bit IPCD = 1	0.9	1.2	1.4	mA
		bit IPCD = 0	0.45	0.6	0.75	mA
I_{PCDL}	output leakage current		–5	±1	+5	nA
V_{PCD}	output voltage		0.4	–	V_{CP}–0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock and serial data input (pins SCL and SDA)						
f_{CLK}	clock frequency		0	–	100	kHz
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	1.5	V
I_{IH}	HIGH level input current		–	3	10	μA
I_{IL}	LOW level input current		−10	−5	–	μA
C_I	input capacitance		–	–	10	pF
I_{sink}	SDA sink current	V_{OL} = 0.4 V	3	–	–	mA
Slave address select input (pin SAA) and Hardware power-down input (pin HPDN)						
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	0.4	V
I_{IH}	HIGH level input current		–	–	0.1	μA
I_{IL}	LOW level input current		−10	–	–	μA
VCO output switches (pins VCOA and VCOB) and synthesizer alarm (pin SYA); note2						
I_{OL}	LOW level sink current	$V_{OL} \geq 0.4$ V	400	–	–	μA

Notes

1. C_I is in parallel with R_I.
2. Pin VCOA is forced to logic 0 during out-of-lock condition.



The current I_{PCD} is averaged over a reference period of 24 μs.

Fig.4 Gain of phase detector and charge pump.

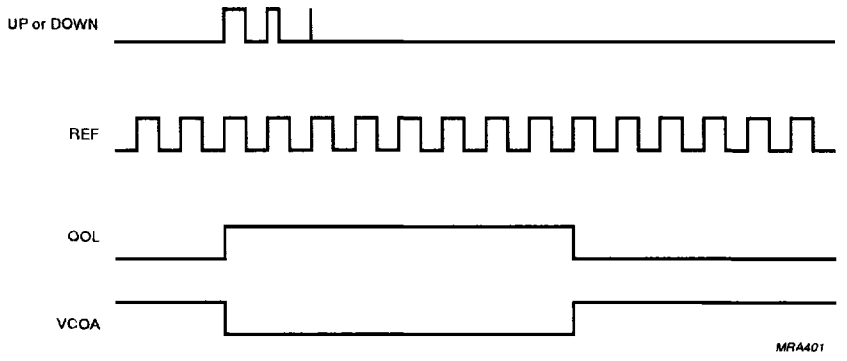


Fig.5 Out-of-lock function.

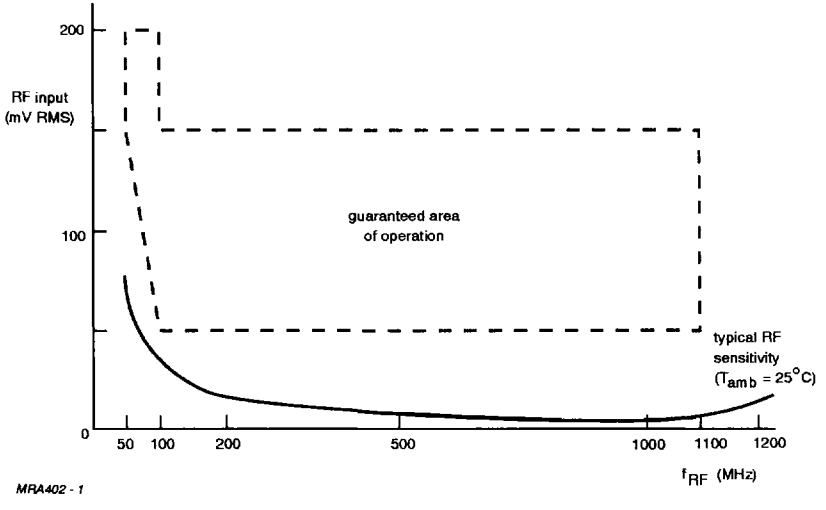


Fig.6 RF input high frequency sensitivity.

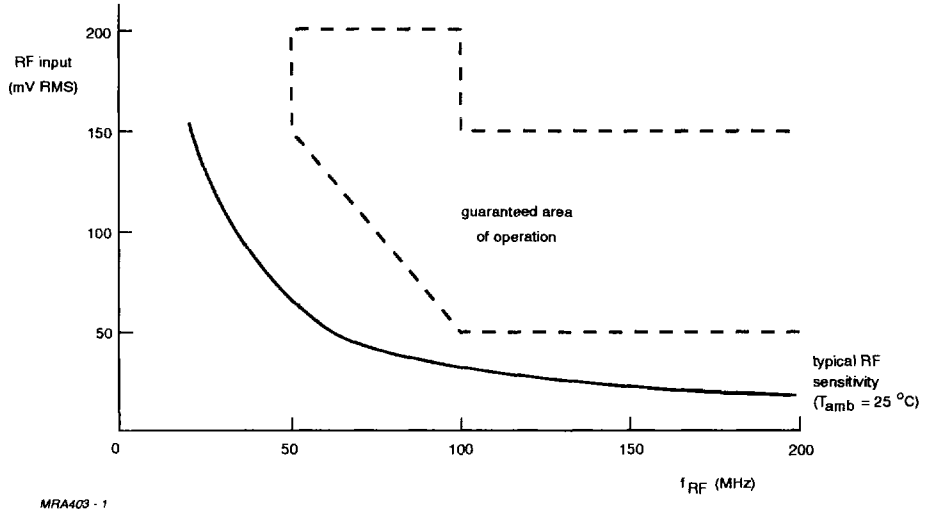


Fig.7 RF input low frequency sensitivity.

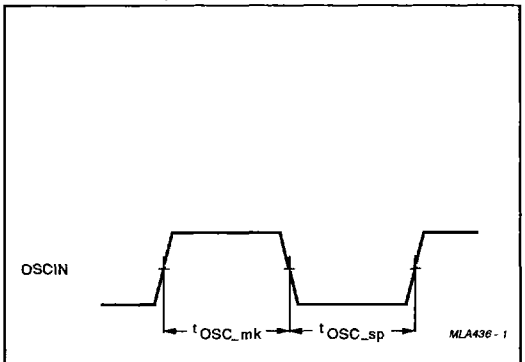
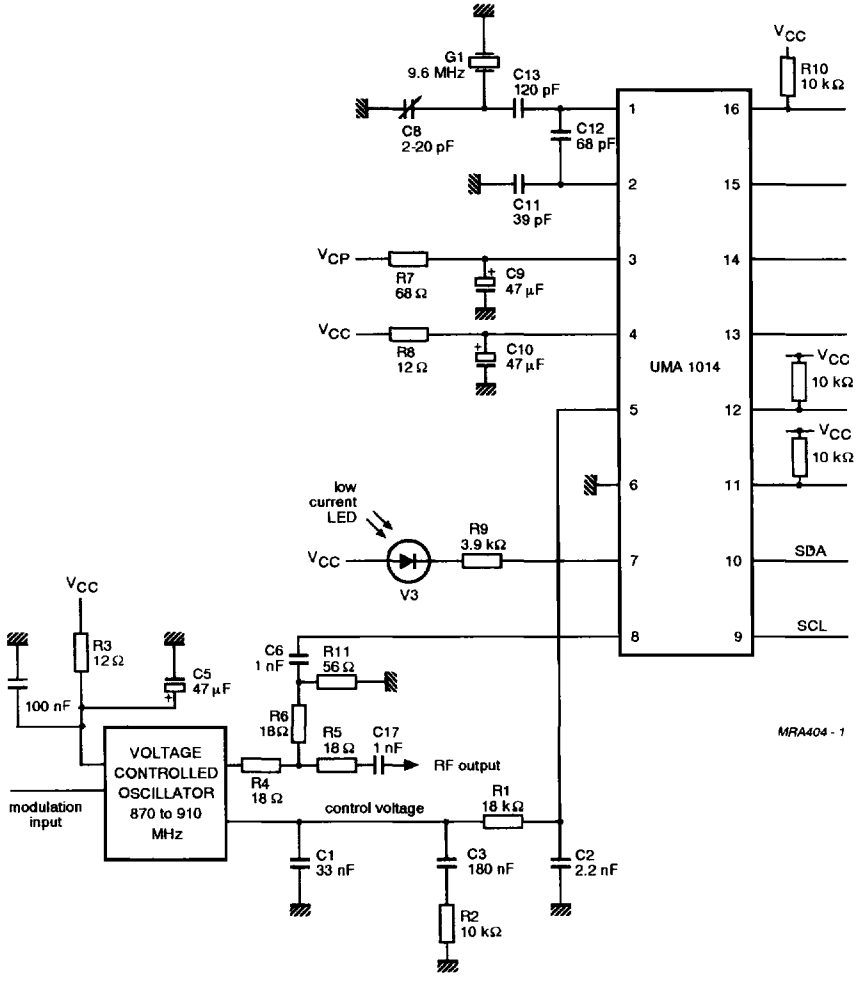


Fig.8 Oscillator input timing.

APPLICATION INFORMATION



ETACS application for:
V_{CO} sensitivity = 11 MHz/V.
Channel spacing = 12.5 kHz.

Fig.9 Typical cellular mobile radio application.