SCG4521
Synchronous Clock Generators

PLL

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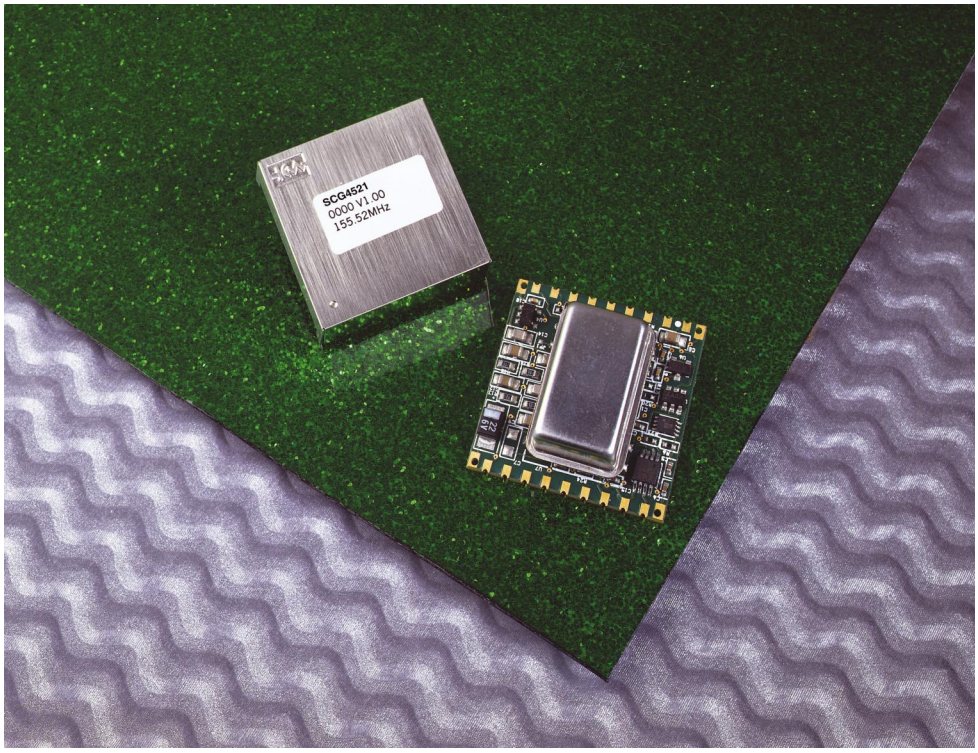


Features

- Dual 19.44 MHz Input References
- Primary 155.52 MHz LVPECL Outputs with Disable Function
- Secondary 51.84 MHz CMOS Output
- Phase Locked Output Frequency Control
- Intrinsically Low Jitter Crystal Oscillator
- LOR & LOL Alarm
- Force Free Run Function
- Automatic Free Run operation on loss of both References A & B
- Input Duty Cycle Tolerant
- 3.3V dc Power Supply
- Small Size: 1 Square Inch

Bulletin	**SG036**
Page	**1 of 16**
Revision	**A02**
Date	**25 Oct 01**
Issued By	**MBatts**

General Description

The SCG4521 is a mixed-signal phase locked loop generating LVPECL outputs from an intrinsically low jitter, voltage controlled, crystal oscillator. The LVPECL outputs may be disabled.

The SCG4521 can lock to one of two external references, which is selectable using the SEL_{AB} input select pin. The unit has a fast acquisition time of about 1.5 seconds and it is tolerant of different reference duty cycles.

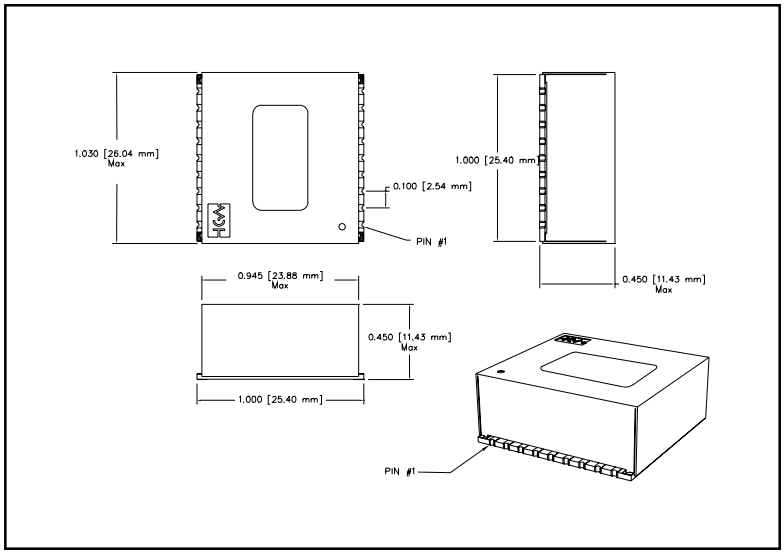
The SCG4521 provides two types of output logic. The primary output is a differential LVPECL output at 155.52 MHz. The secondary output is a CMOS output at 51.84 MHz that is derived from the LVPECL output. Both outputs are phase aligned to the selected input reference.

The SCG4521 includes an alarm output that indicates deviations from normal operation. If a Loss-of-Reference (LOR) or Loss-of-Lock (LOL) is detected the alarm with indicate the need for a reference rearrangement. If both references A and B are absent the module will enter Free Run operation. The FR_{status} pin will indicate that the module is in Free Run operation. Frequency stability during Free Run operation is guaranteed to ±20 ppm. Additionally the Free Run mode may be entered manually.

The package dimensions are 1" x 1" x .45" on a 6 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand 63/37 alloys, 180°C surface mount reflow processes.

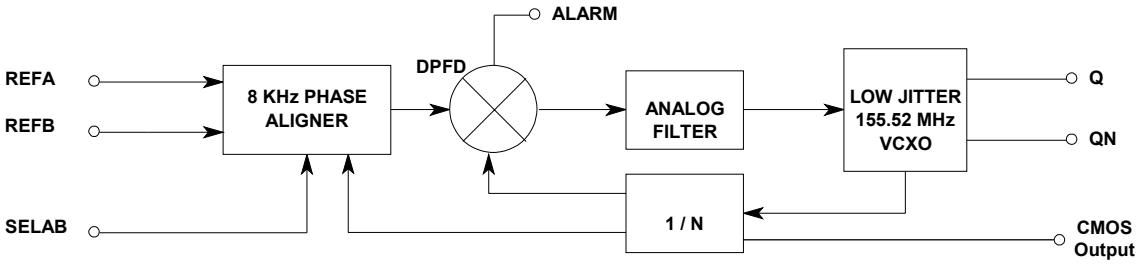
Package Outline

Figure 1



Block Diagram

Figure 2



Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V_i	Input Voltage	-0.5	-	+5.5	Volts	1.0
T_s	Storage Temperature	-65.0	-	+100	°C	1.0

Operating Specifications

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	3.135	3.3	3.465	Volts	2.0
I_{cc}	Power Supply Current	170	250	320	mA	5.0
T_o	Temperature Range	0	-	70	°C	
F_{REF}	External Reference Frequency		19.44		MHz	
F_{fr}	Free Run Frequency	-20	-	20	ppm	
F_{LV}	LVPECL Differential Output Frequency		155.52		MHz	
F_{CM}	CMOS Output Frequency		51.84		MHz	
F_{cap}	Capture/pull-in range	-25	-	25	ppm	
F_{bw}	Jitter Filter Bandwidth	-	-	10	Hz	3.0
T_{jtol}	Input Jitter Tolerance	-	-	6.25	µs	
T_{aq}	Acquisition Time	-	1	-	s	4.0
T_{rf}	Output Rise and Fall Time (20% 80%)	100	225	350	ps	5.0
LV_{DC}	LVPECL Output Duty Cycle	40		60	%	
CM_{DC}	CMOS Output Duty Cycle	40		60	%	
LV_S	LVPECL Output Jitter (OC-48)			<1	psRMS	6.0
CM_S	CMOS Output Jitter	3		5	psRMS	6.0
$MTIE_{sr}$	MTIE at Synchronization Rearrangement		GR-253-CORE.1999 R5-136			7.0, 7.1

NOTES:

1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2.0 Requires external regulation and supply decoupling. (22 uF, 330 pF)

3.0 3db loop response.

4.0 From a 20 PPM step in reference frequency at 25°C @ 3.3V

5.0 50-ohm load biased to 1.3 volts.

6.0 Jitter based on SONET OC-48 bandwidth. (12KHz to 20 MHz)

7.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing.

7.1 If the selected reference is removed system response to the ALARM must be less than 10µs.

Input And Output Characteristics

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
CMOS Input and Output Characteristics						
V_{ih}	High Level Input Voltage	2.0	-	5.5	V	
V_{il}	Low Level Input Voltage	0.0	-	0.8	V	
T_{io}	I/O to Output Valid	-	-	10	ns	
C_l	Output Capacitance	-	-	10	pF	
V_{oh}	High Level Output Voltage	2.4	-	-	V	
V_{ol}	Low Level Output Voltage	-	-	0.4	V	
T_{ir}	Input Reference Pulse Width	12.5	-	-	ns	
PECL Output Characteristics						
V_{oh}	High Level PECL Voltage	2.27	2.34	2.52	V	
V_{ol}	Low Level PECL Voltage	1.49	1.51	1.68	V	
C_l	Output Capacitance	-	-	10	pF	
T_{skew}	Differential Output Skew	-	50	-	ps	

Input Selection / Output Response

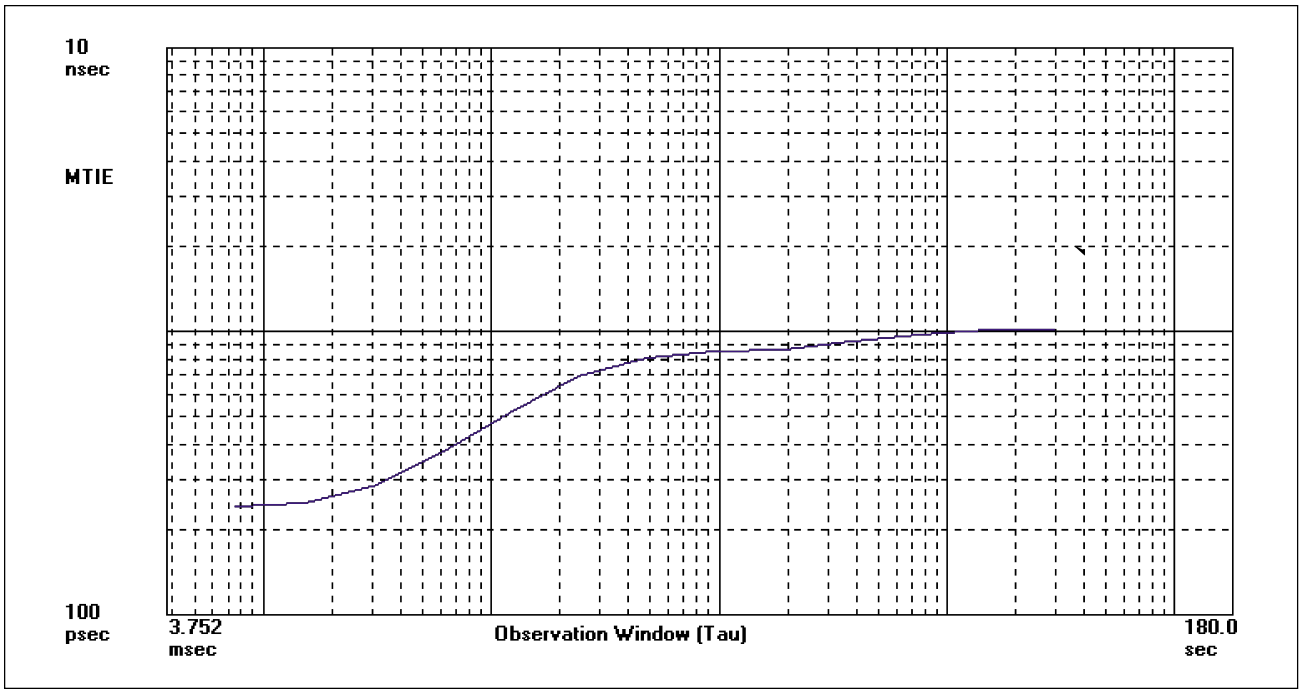
Table 4

INPUTS						OUTPUTS				NOTE
RESET	**ENABLE**	**SEL_{AB}**	**REF_A**	**REF_B**	**FR**	**FR_{status}**	**ALARM**	**Q**	**QN**	
1	0	X	X	X	X	1	X	X	X	FR
X	1	X	X	X	X	X	X	0	1	
0	0	X	X	X	1	1	X	X	X	FR
0	0	0	A	A	0	0	0	X	X	RA
0	0	1	A	A	0	0	0	X	X	RB
0	0	0	NA	A	0	0	1	X	X	U
0	0	1	NA	A	0	0	0	X	X	RB
0	0	1	A	NA	0	0	1	X	X	U
0	0	0	A	NA	0	0	0	X	X	RA
0	0	X	NA	NA	0	1	1	X	X	FR

NOTES:
A Active
FR Free Run Mode
NA Not Active
RA Locked to Reference A
RB Locked to Reference B
U Unstable (due to conditions shown, switch to active reference or Free Run)
X Don't care

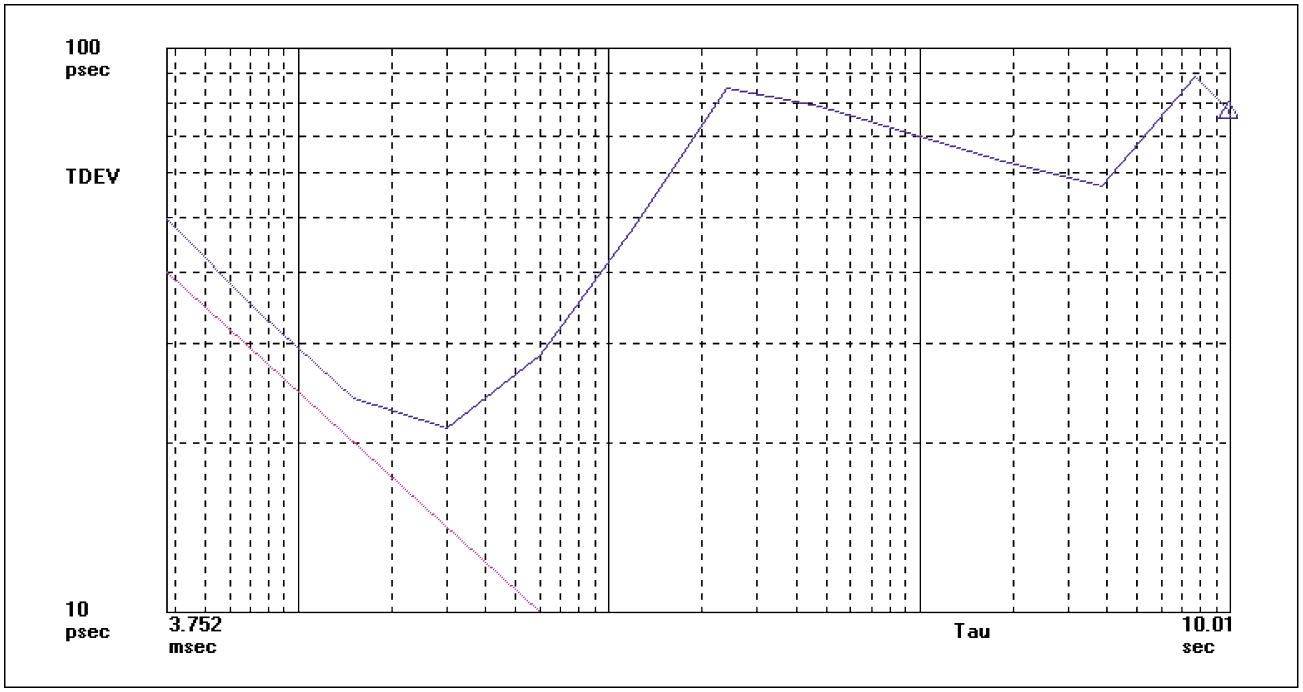
Typical MTIE Measurement

Figure 3



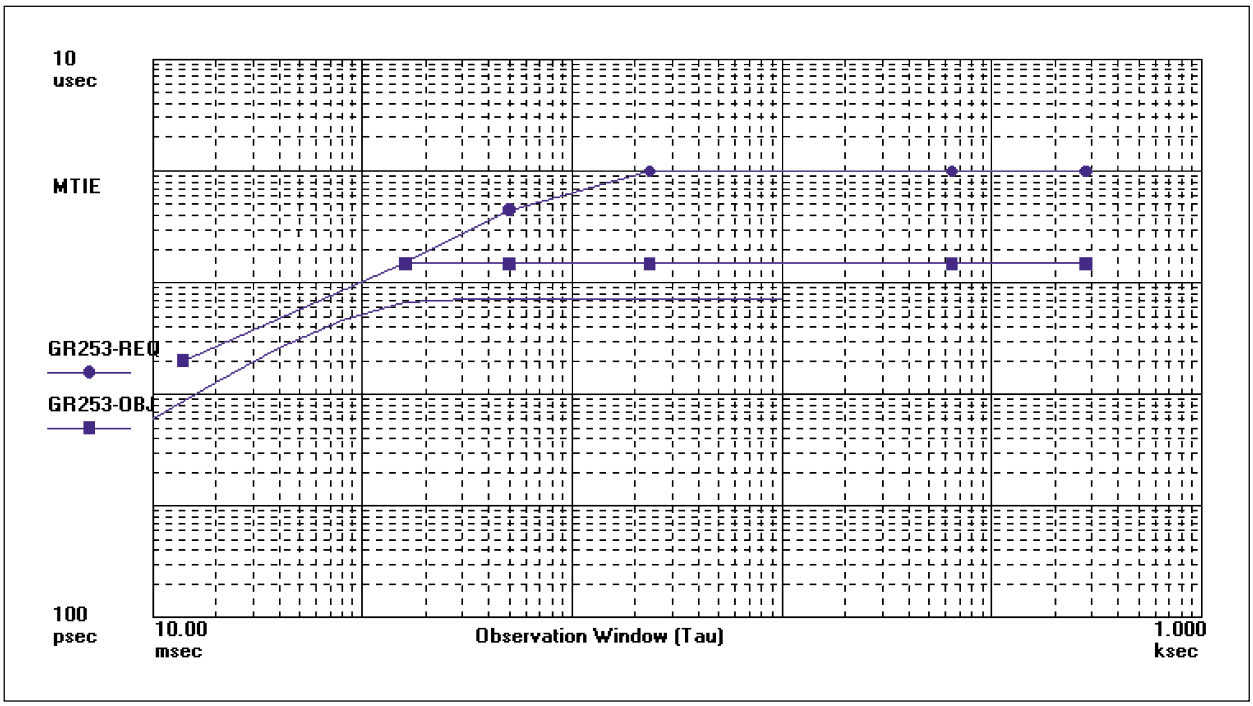
Typical TDEV Measurement

Figure 4



Typical MTIE at Synchronization Rearrangement. Reference B Equal to Inverse of Reference A, No Modulation.

Figure 5



Pin Description

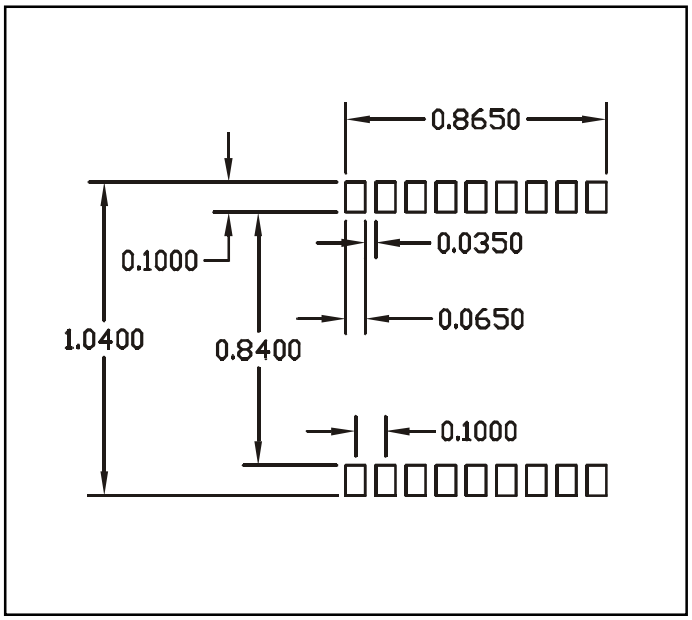
Table 5

Pin #	Pin Name	Pin Information	Note
1	ENABLE	VCXO Enable. (Enable = 0, Disable = 1)	9.0
2	TCK	No Connection, Internal Factory Programming Input.	8.0
3	TDO	No Connection, Internal Factory Programming Input.	8.0
4	REF_A	CMOS Reference Frequency Input. (19.44 MHz)	
5	SEL_{AB}	Input Reference Select Pin. (REFA = 0, REFB = 1)	9.0
6	RESET	RESET. (RESET = 1)	9.0
7	REF_B	CMOS Reference Frequency Input. (19.44 MHz)	
8	V_{ee}	Ground.	
9	FR_{status}	Free Run Status. (FR = 1)	
10	V_{cc}	Supply Voltage relative to ground.	
11	CMOS Output	CMOS Output (51.84 MHz)	
12	ALARM	Loss of Reference / Lock alarm. (Alarm = 1)	
13	FR	Force Free Run. (Phase Lock = 0, Free Run = 1)	9.0
14	TDI	No Connection, Internal Factory Programming Input.	8.0
15	TMS	No Connection, Internal Factory Programming Input.	8.0
16	QN	LVPECL Complementary Output.	
17	V_{ee}	Ground.	
18	Q	LVPECL Output.	

NOTES
8.0 Do not connect pin
9.0 Input pulled to ground

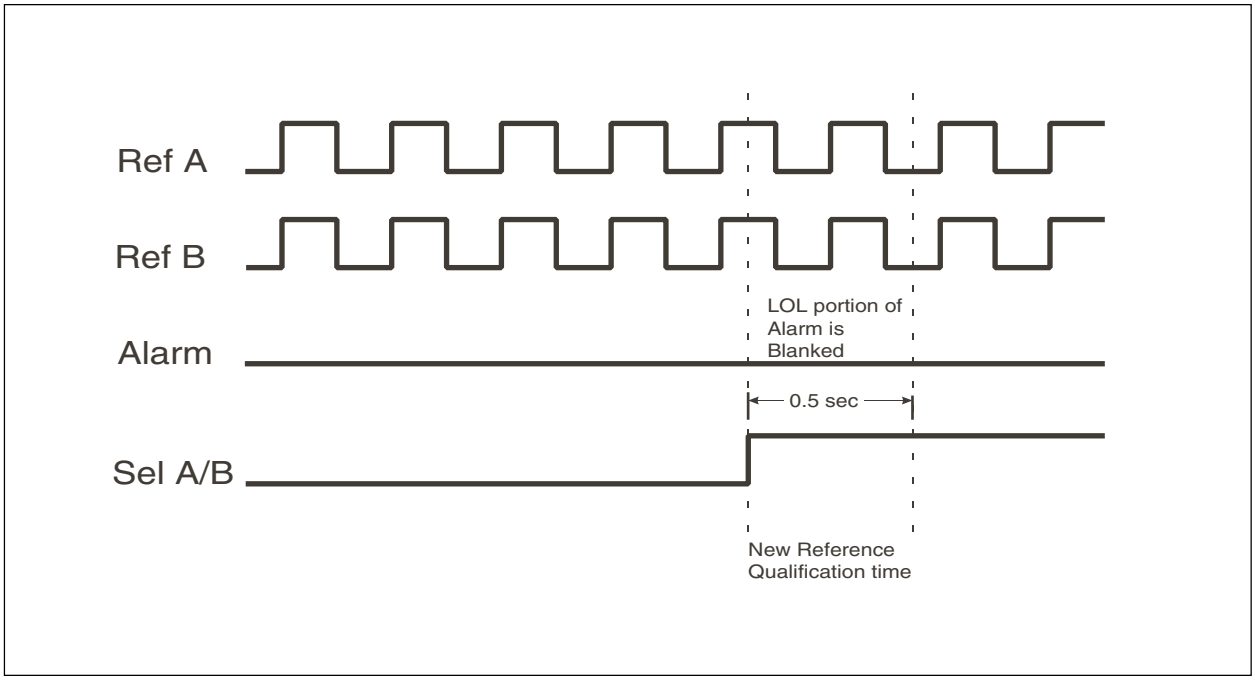
Circuit Board Footprint Recommendations

Figure 6



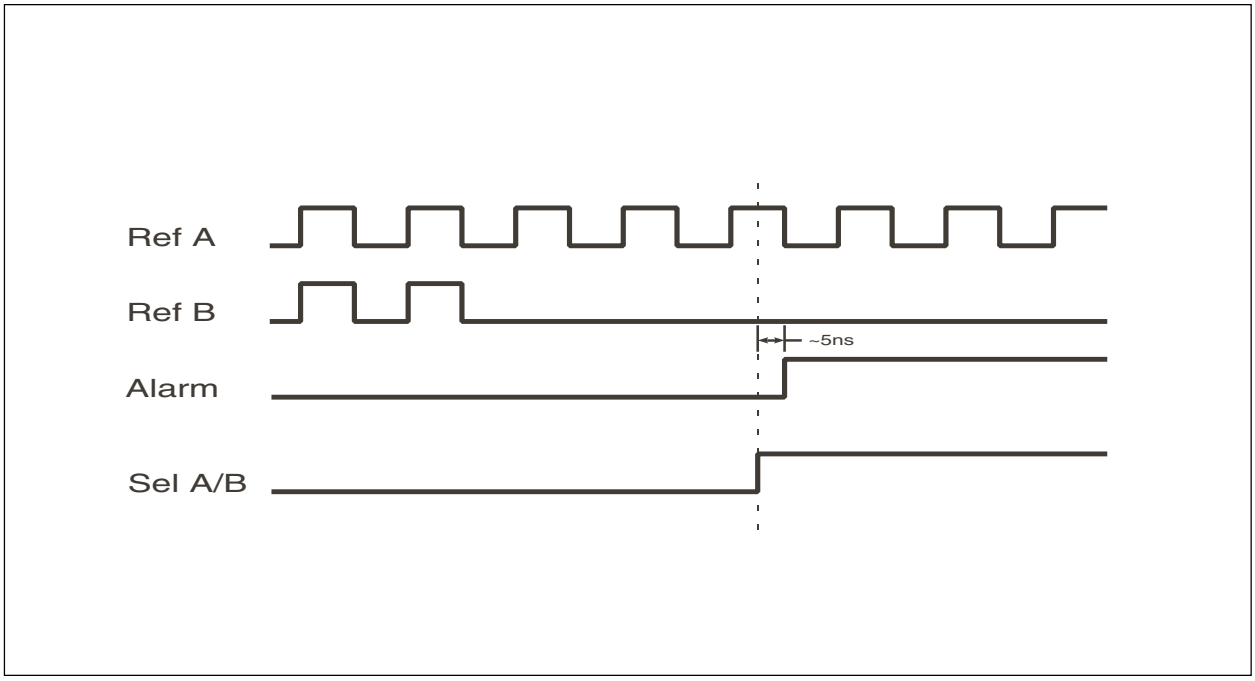
Switch from A to B when both are good signals

Figure 7



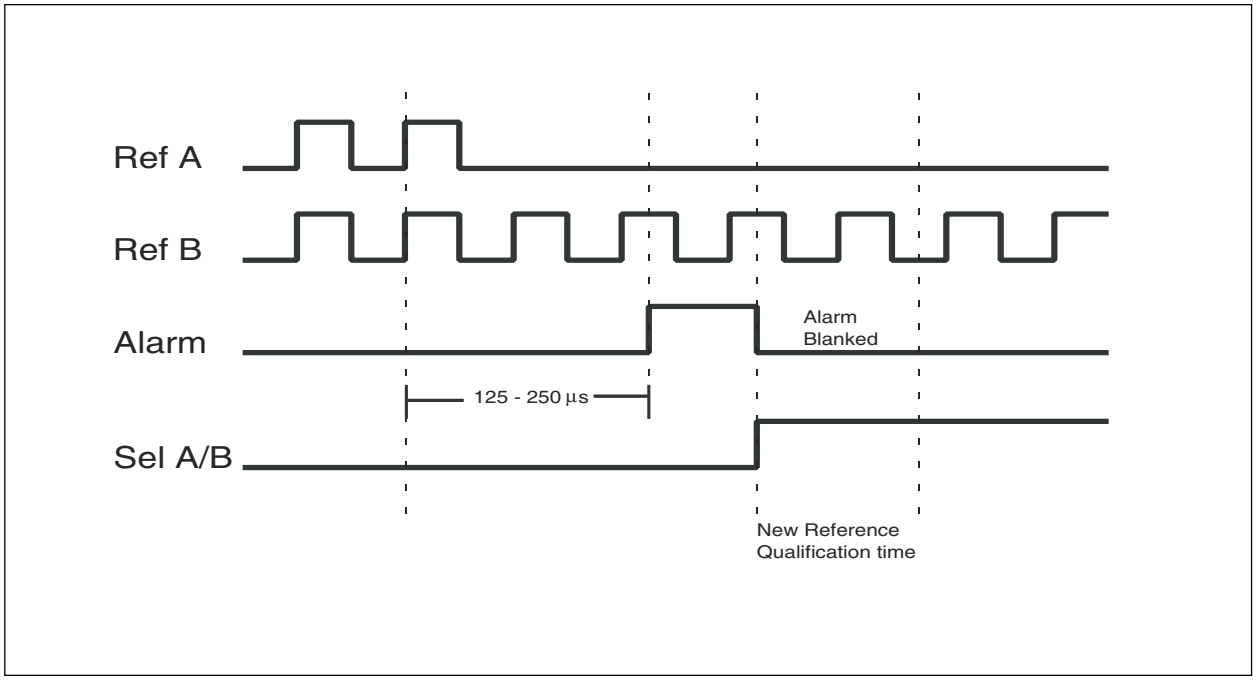
Switch from A to B when Reference B is lost

Figure 8



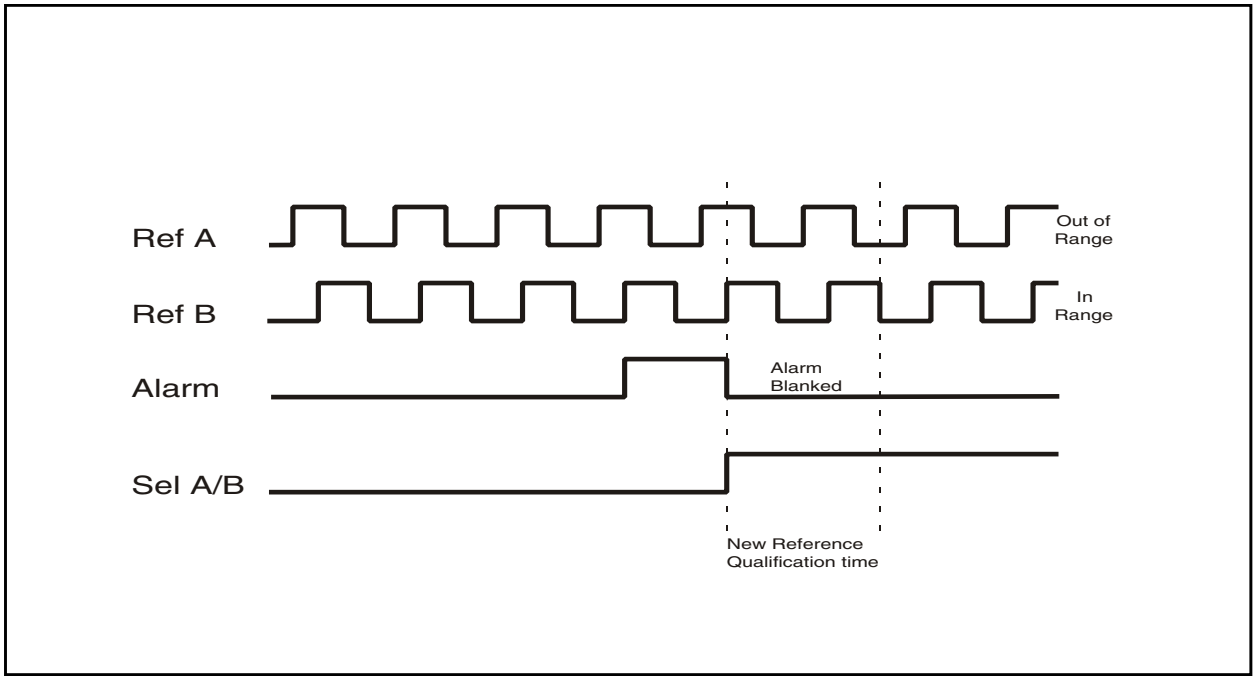
Switch from A to B after Reference A is lost

Figure 9



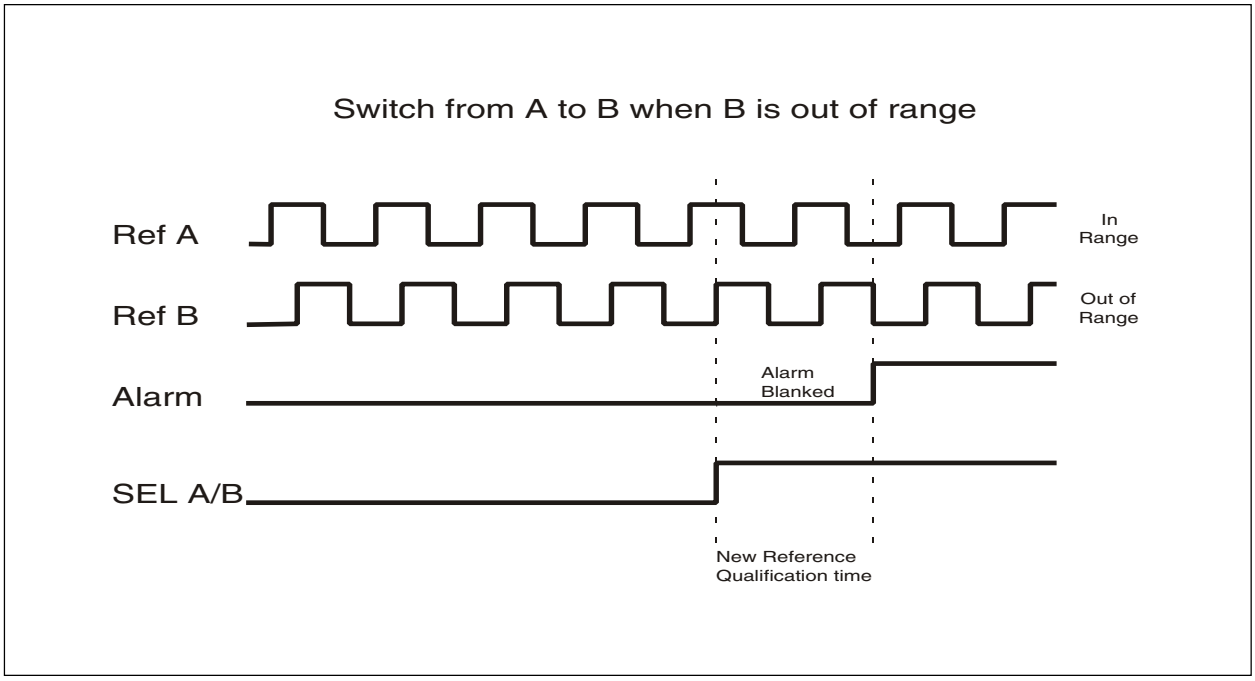
Switch from A to B when A is out of range

Figure 10



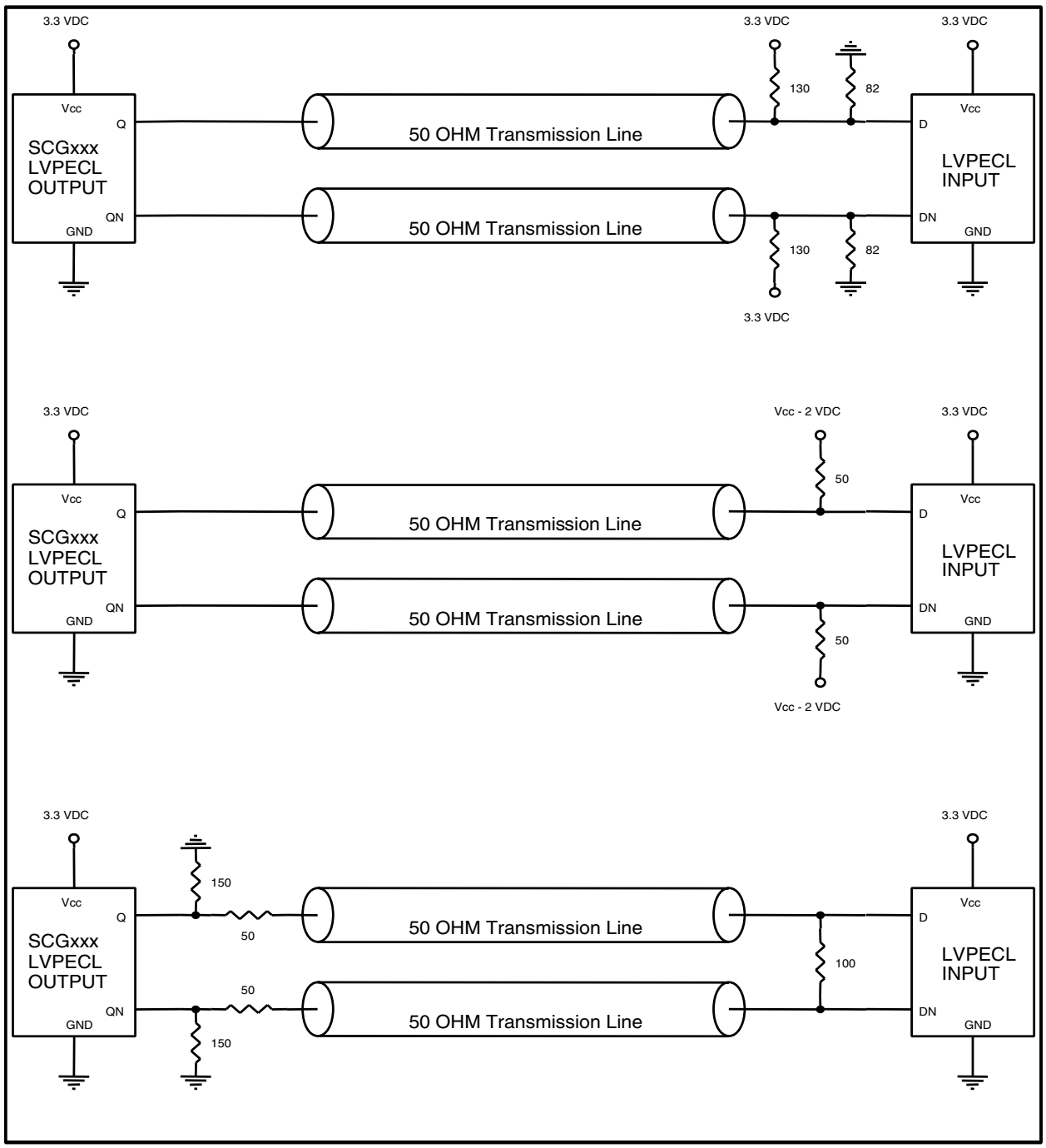
Switch from A to B when B is out of range

Figure 11



Recommended PECL Termination

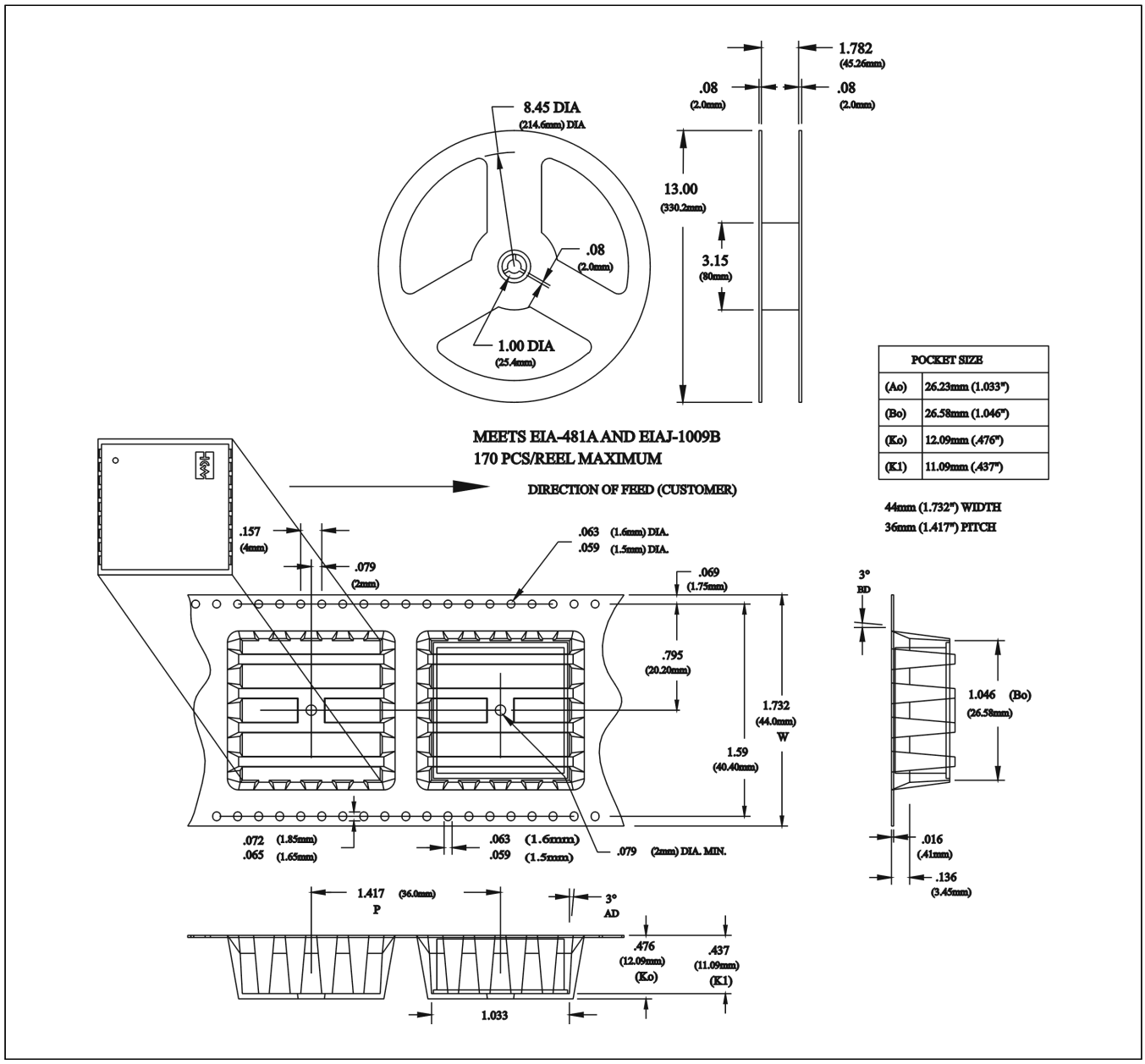
Figure 12



If PECL outputs do not drive a long line (< 0.5"),
a single 150Ω termination resistor to ground may be used for each pin.

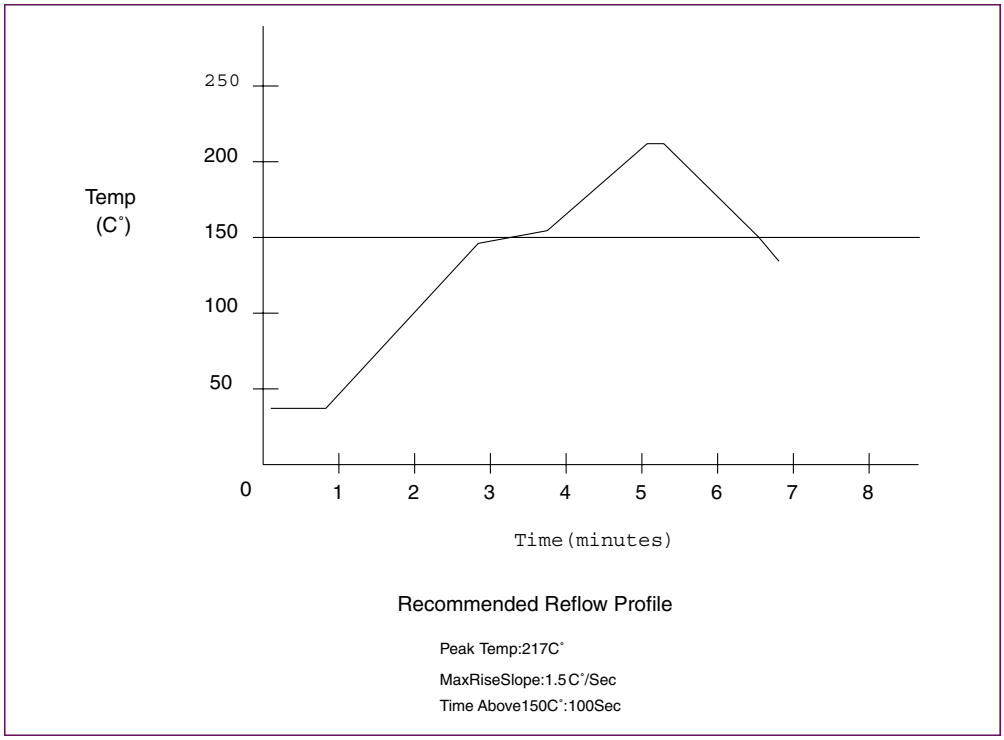
Tape and Reel Packaging

Figure 13



Solder Profile

Figure 14



Recommended Reflow Profile

Peak Temp:217C˚

MaxRiseSlope:1.5C˚/Sec

Time Above150C˚:100Sec

Revision	Revision Date	Note
A00	9/4/01	Advance Information Release
A01	10/9/01	Changed PECL phase noise spec and max current spec.
A02	10/25/01	Added input reference frequency to table 2