3A, 21V 500kHz Synchronous Step-Down Converter

General Description

The RT7263A is a synchronous step-down regulator with an internal power MOSFET. It achieves 3A of continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. An adjustable soft-start reduces the stress on the input source at startup.

The RT7263A requires a minimal number of readily available external components, providing a compact solution.

Ordering Information

RT7263A □ □

- Package Type
  - QW : WDFN-14L 4x3 (W-Type)
  - SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  - Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

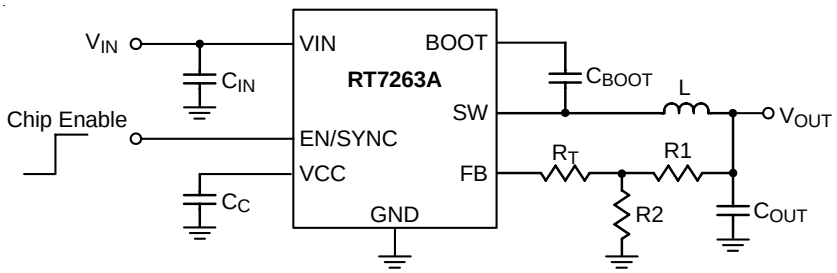
Features

- **Wide Input Range : 4.5V to 21V**
- **Adjustable Output from 0.808V to 15V**
- **3A Output Current**
- **120mΩ/40mΩ Internal Power MOSFET Switch**
- **Internal Compensation Minimizes External Parts**
- **500kHz Fixed Switching Frequency**
- **Synchronized External Clock from 300kHz to 2MHz**
- **Adjustable Soft-Start**
- **Cycle-by-Cycle Over Current Limit**
- **Thermal Shutdown Protection**
- **Available in SOP-8 (Exposed Pad) and WDFN-14L 4x3 Packages**
- **RoHS Compliant and Halogen Free**

Applications

- Distributive Power Systems
- Battery Charger
- DSL Modems
- Pre-Regulator for Linear Regulators

Simplified Application Circuit



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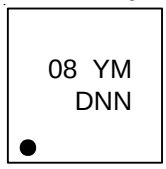
Marking Information

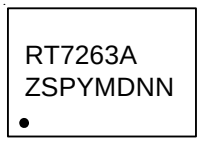
RT7263AZQW



08 : Product Code

YMDNN : Date Code

RT7263AZSP

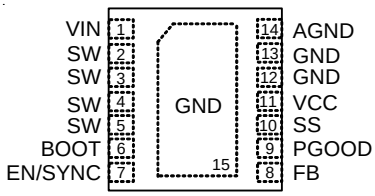


RT7263AZSP : Product Number

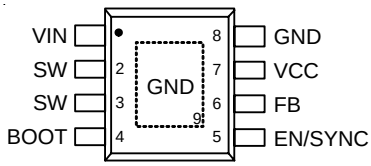
YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WDFN-14L 4x3



SOP-8 (Exposed Pad)

Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN-14L 4x3	SOP-8 (Exposed Pad)		
1	1	VIN	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.5V to 21V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
2, 3, 4, 5	2, 3	SW	Switch Node. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BOOT to power the high side switch.
6	4	BOOT	Bootstrap for High Side Gate Driver. Connect a 100nF or greater capacitor from SW to BOOT to power the high side switch driver.
7	5	EN/SYNC	Enable or External Frequency Synchronization Input. For automatic start-up, connect the EN/SYNC pin to VIN with a 100kΩ resistor. The switching frequency can be changed by an external clock applying to the SYNC pin.
8	6	FB	Feedback Input. FB senses the output voltage via an external resistive voltage divider. The feedback reference voltage is 0.808V typically.
9	--	PGOOD	Power Good Indicator is an Open Drain Output. The power good rising/falling threshold is 90%/70% of regulation output voltage.
10	--	SS	Soft-Start Control Input. Connect a capacitor from SS to GND to set the soft-start period.
11	7	VCC	Bias Supply. Decouple with 0.1μF to 0.22μF capacitor between this pin and GND.
12, 13, 15 (Exposed Pad)	8, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
14	--	AGND	Analog Ground. Connect this pin to the system ground in PCB layout.

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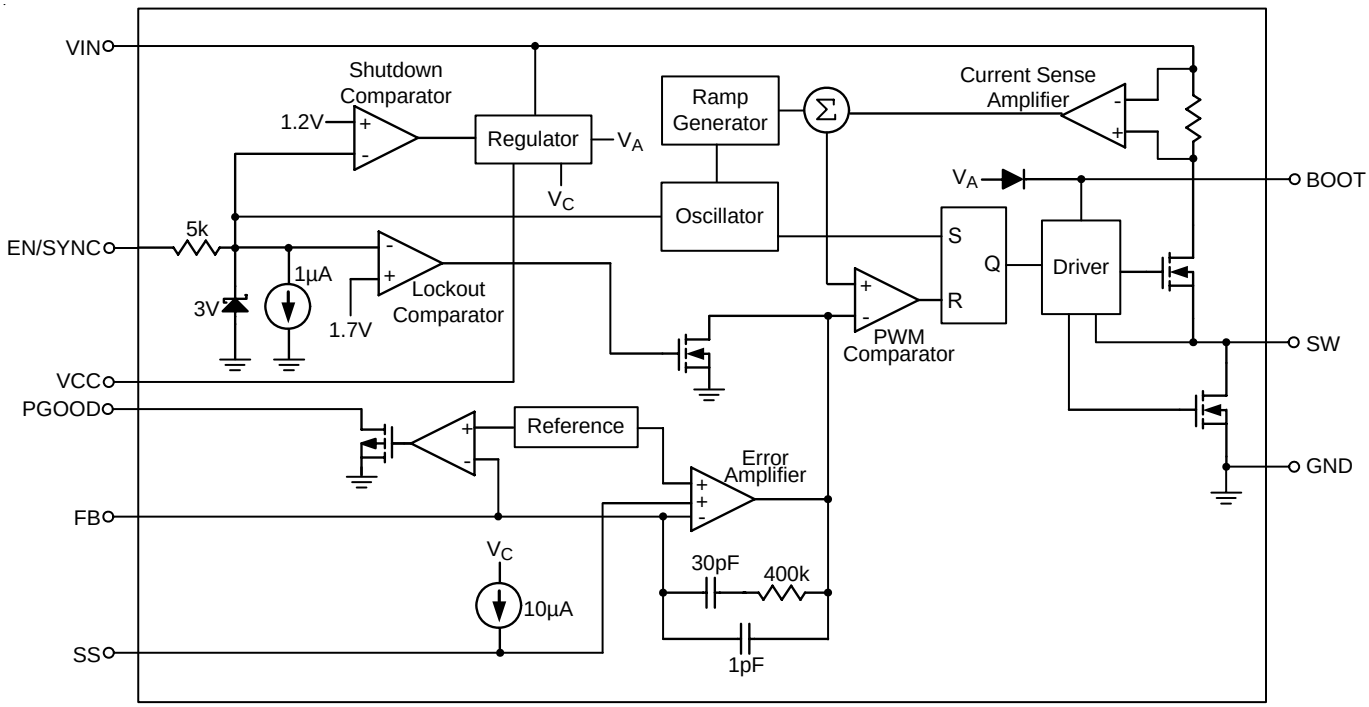
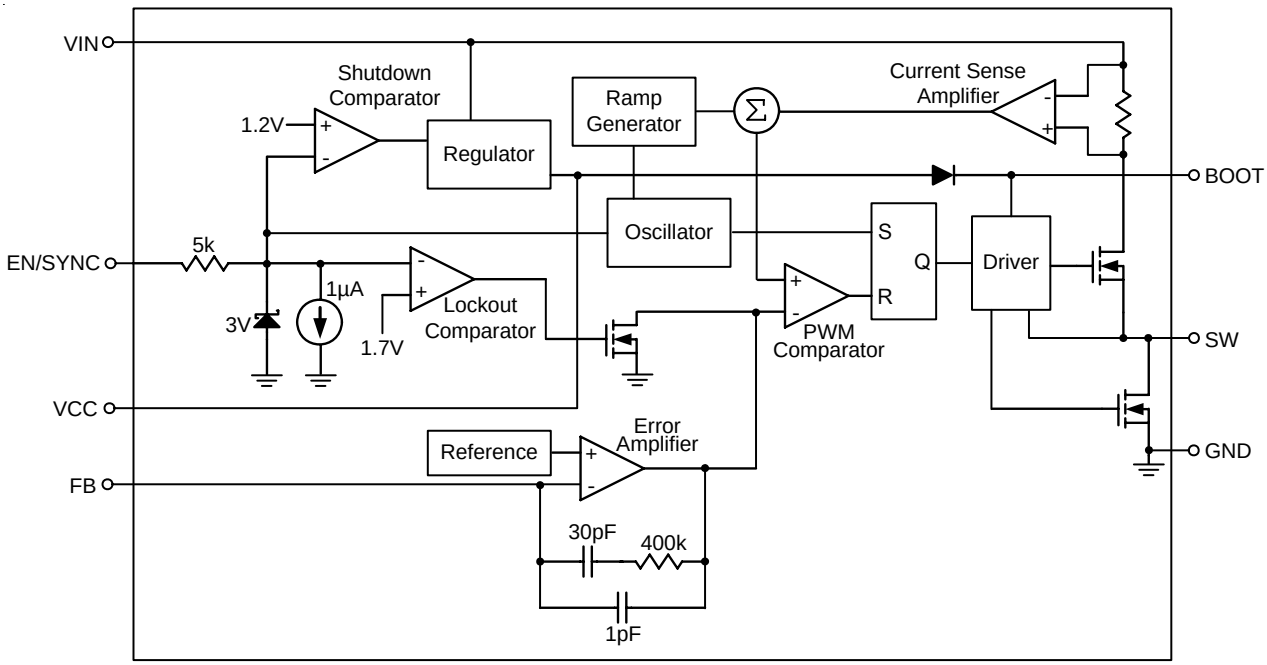
Function Block Diagram

For WDFN-14L 4x3 Package



For SOP-8 (Exposed Pad) Package



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Operation

The RT7263A is a constant frequency, current mode synchronous step-down converter. In normal operation, the high side N-MOSFET is turned on when the S-R latch is set by the oscillator and is turned off when the current comparator resets the S-R latch. While the high side N-MOSFET is turned off, the low side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

Error Amplifier

The error amplifier adjusts its output voltage by comparing the feedback signal (V_{FB}) with the internal reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the error amplifier's output voltage then rises to allow higher inductor current to match the load current.

Oscillator

The internal oscillator runs at fixed frequency 500kHz. In short circuit condition, the frequency is reduced to 150kHz for low power consumption.

Internal Regulator

The regulator provides low voltage power to supply the internal control circuits and the bootstrap power for high side gate driver.

Enable

The converter is turned on when the EN pin is higher than 2V. When the EN pin is lower than 0.4V, the converter will enter shutdown mode and reduce the supply current to be less than 1μA.

Soft-Start (SS)

An internal current source charges an internal capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 4ms.

UV Comparator

If the feedback voltage (V_{FB}) is lower than 0.4V, the UV Comparator will go high to turn off the high side MOSFET. The output under voltage protection is designed to operate in Hiccup mode. When the UV condition is removed, the converter will resume switching.

Thermal Shutdown

The over temperature protection function will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 30°C, the converter will automatically resume switching.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 26V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
- Boot Voltage, BOOT ---------- (SW – 0.3V) to (SW + 6V)
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-14L 4x3 ---------- 1.667W
  - SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  - WDFN-14L 4x3, θ_{JA} ---------- 60°C/W
  - WDFN-14L 4x3, θ_{JC} ---------- 7°C/W
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 21V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current		I_{SHDN}	V_{EN} = 0	--	0	1	μA
Quiescent Current		I_Q	V_{EN} = 2V, V_{FB} = 1V	--	0.7	--	mA
Upper Switch On Resistance		$R_{DS(ON)1}$		--	120	--	mΩ
Lower Switch On Resistance		$R_{DS(ON)2}$		--	40	--	mΩ
Switch Leakage		I_{LEAK}	V_{EN} = 0V, V_{SW} = 0V or 12V	--	0	10	μA
Current Limit		I_{LIMIT}	$V_{BOOT} - V_{SW}$ = 4.8V	5.4	6.5	--	A
Oscillator Frequency		f_{SW}	V_{FB} = 0.75V	425	500	575	kHz
Short Circuit Frequency			V_{FB} = 0V	--	150	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 0.8V	--	90	--	%
Minimum On Time		t_{ON}		--	100	--	ns
Feedback Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 21V	0.796	0.808	0.82	V
Feedback Current		I_{FB}		--	10	50	nA
EN Voltage	Logic-High	V_{IH}		2	--	5.5	V
	Logic-Low	V_{IL}		--	--	0.4	

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Current			V_{EN} = 2V	--	1	--	μA
			V_{EN} = 0V	--	0	--	
SYNC Threshold Voltage	Logic-High	V_{SYNCH}		1.8	--	--	V
	Logic-Low	V_{SYNCL}		--	--	0.4	
SYNC Frequency Range		f_{SYNC}		0.3	--	2	MHz
SYNC Input Current		I_{SYNC}	V_{SYNC} = 6V	--	1.5	2.5	μA
Power Good Rising Threshold				--	90	--	%
Power Good Falling Threshold				--	70	--	%
Power Good Sink Current Capability			Sink 4mA	--	--	0.4	V
Power Good Leakage Current				--	10	--	nA
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	3.8	4	4.2	V
Under Voltage Lockout Threshold Hysteresis		ΔV_{UVLO}		--	400	--	mV
VCC Regulator				--	5	--	V
VCC Load Regulation			I_{CC} = 5mA	--	5	--	%
Soft-Start Period		t_{SS}	C_{SS} = 47nF	--	4.7	--	ms
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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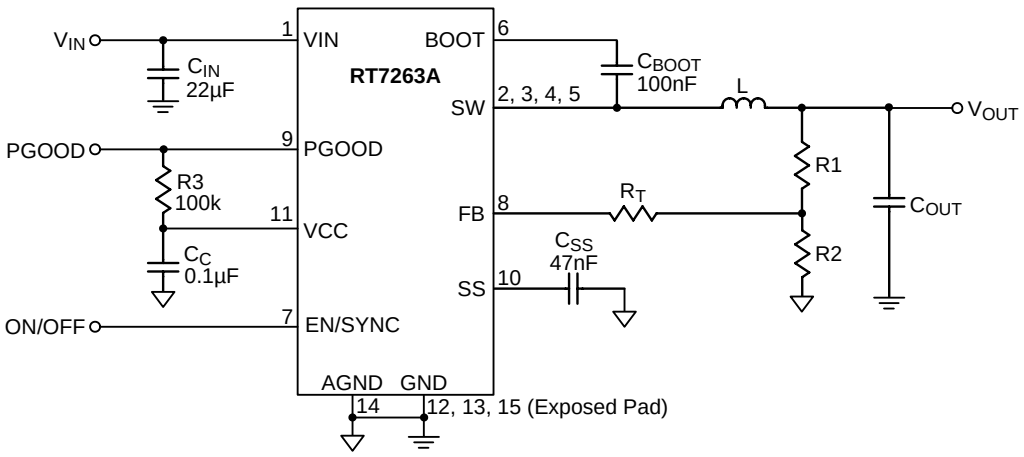
Typical Application Circuit

For WDFN-14L 4x3 Package



For SOP-8 (Exposed Pad) Package

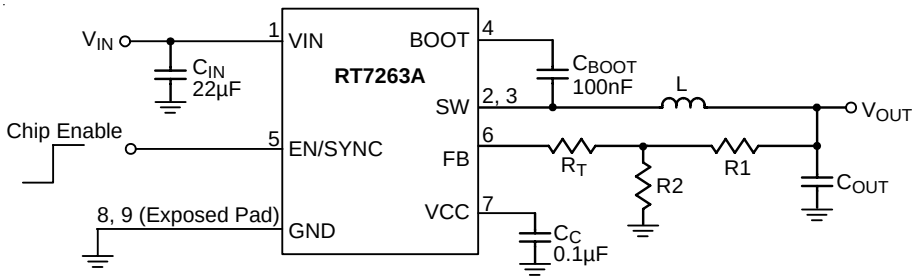


Table 1. Recommended Components Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (µH)	C_{OUT} (µF)
5	75	14.46	0	4.7	22 x 2
3.3	75	24.32	0	3.6	22 x 2
2.5	75	35.82	0	3.6	22 x 2
1.8	5	4.07	30	2	22 x 2
1.5	5	5.84	39	2	22 x 2
1.2	5	10.31	47	2	22 x 2
1.05	5	16.69	47	1.5	22 x 2

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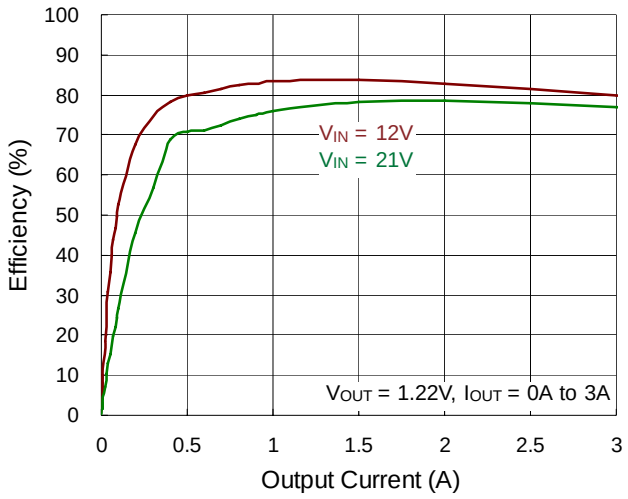
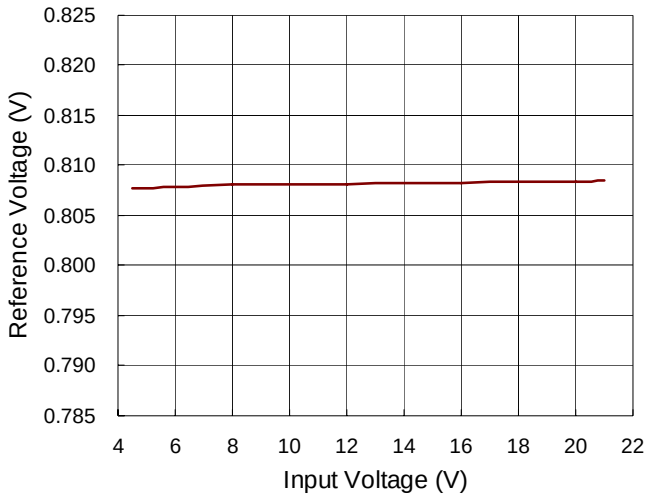
Typical Operating Characteristics

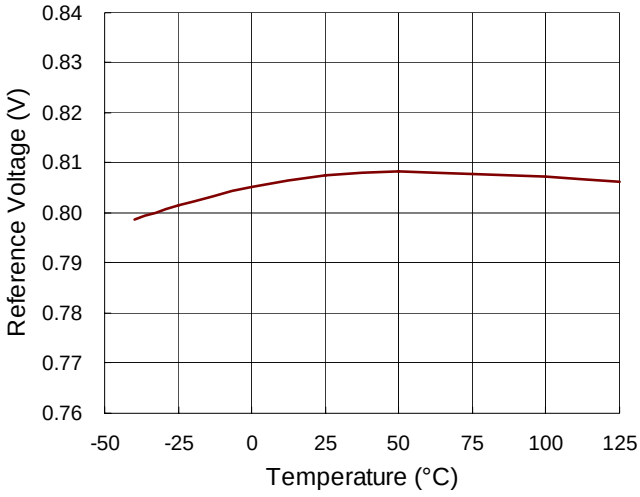
Efficiency vs. Output Current



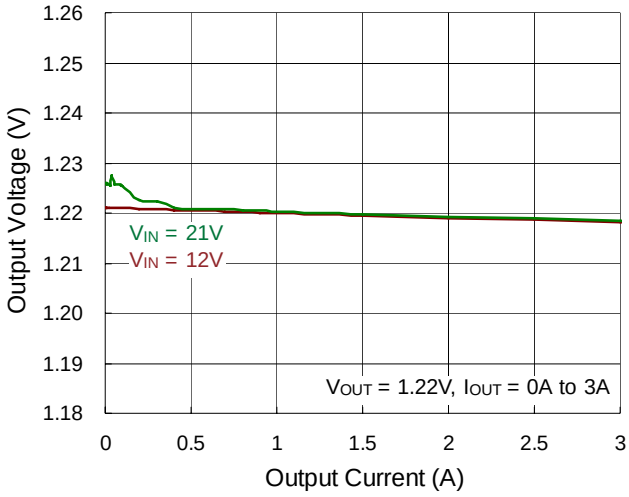
Reference Voltage vs. Input Voltage



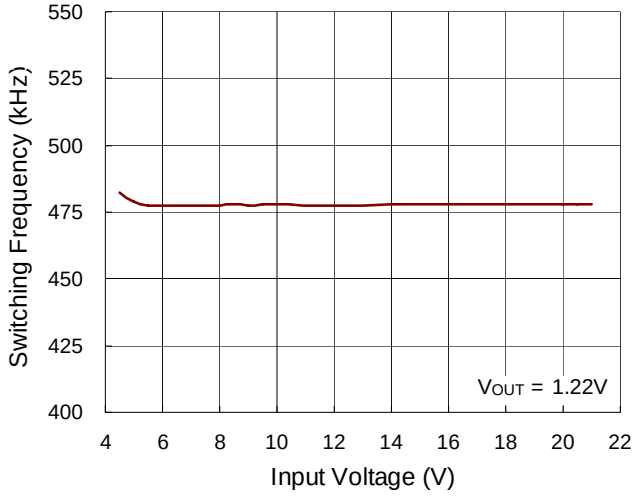
Reference Voltage vs. Temperature



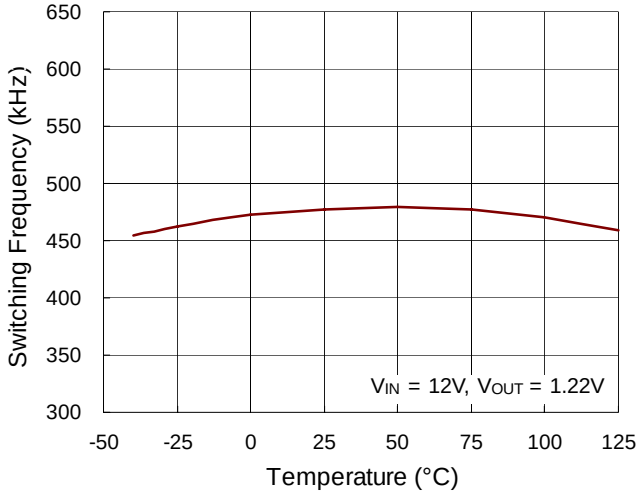
Output Voltage vs. Output Current



Switching Frequency vs. Input Voltage



Switching Frequency vs. Temperature



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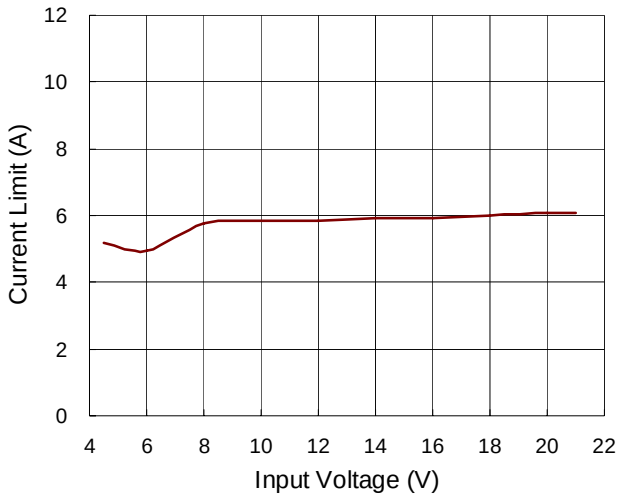
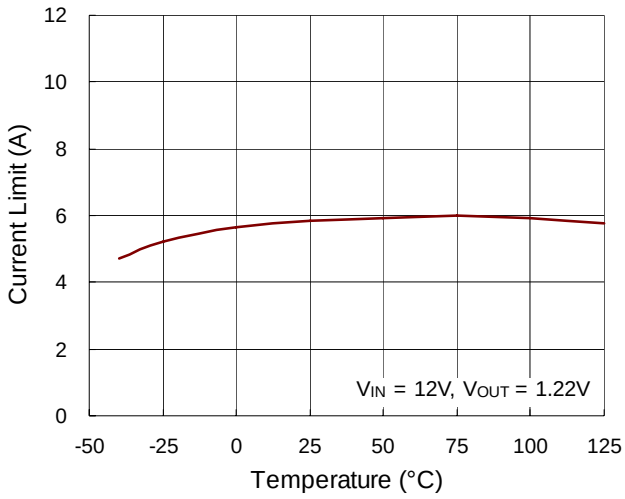
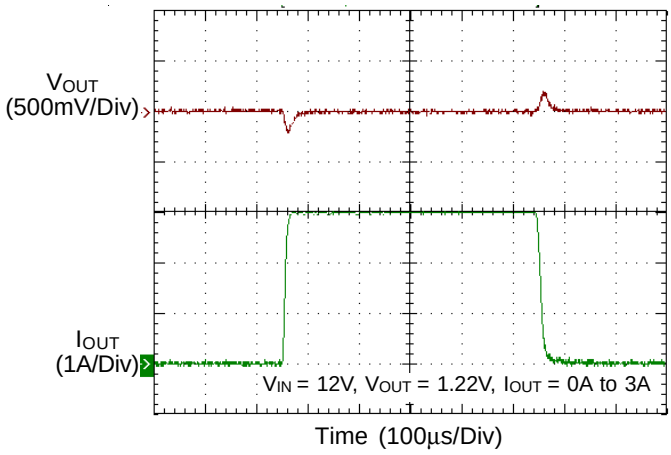
Current Limit vs. Input Voltage



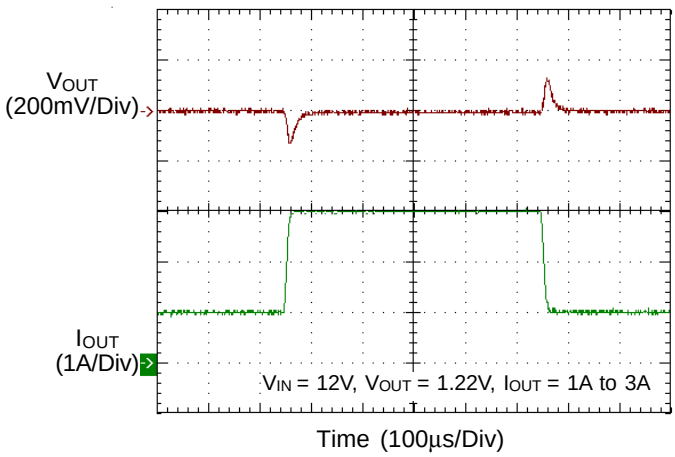
Current Limit vs. Temperature



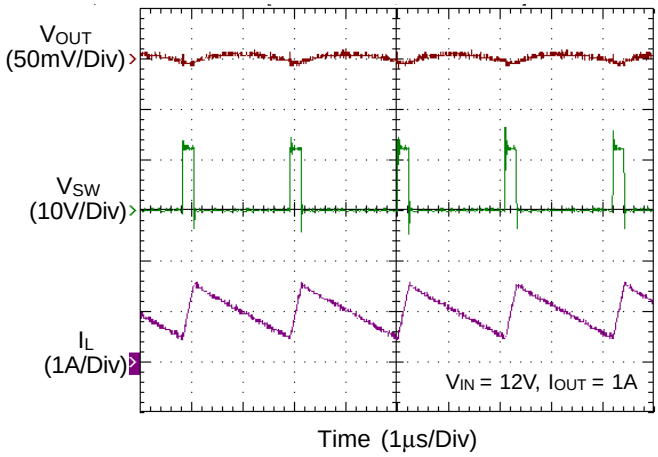
Load Transient Response



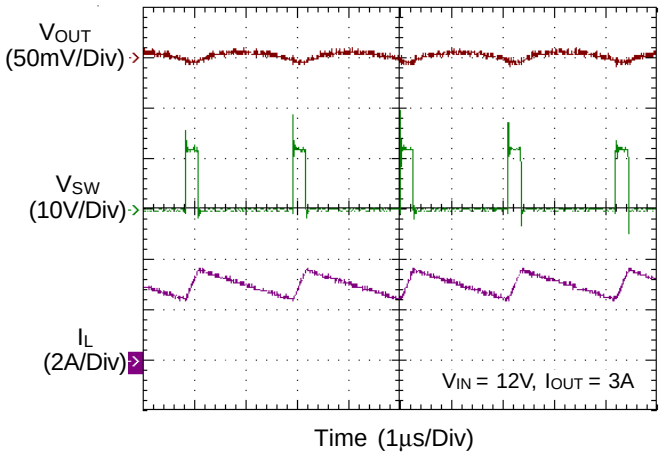
Load Transient Response



Output Ripple Voltage



Output Ripple Voltage



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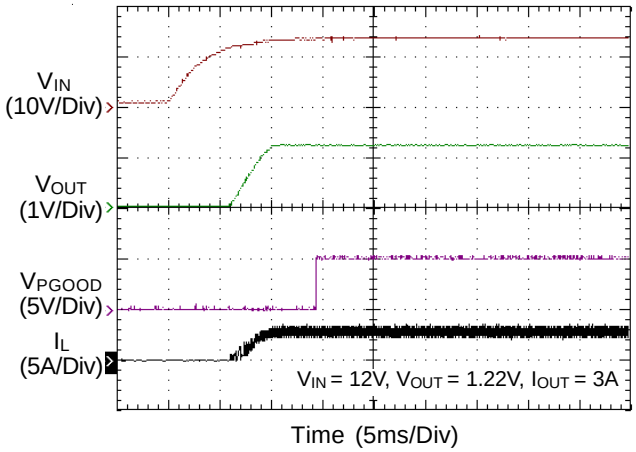
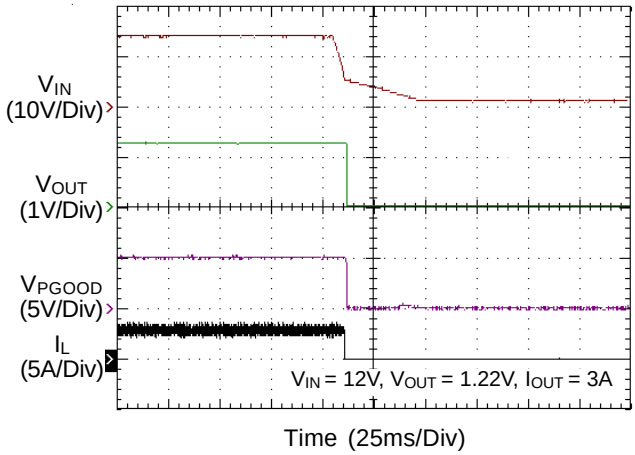
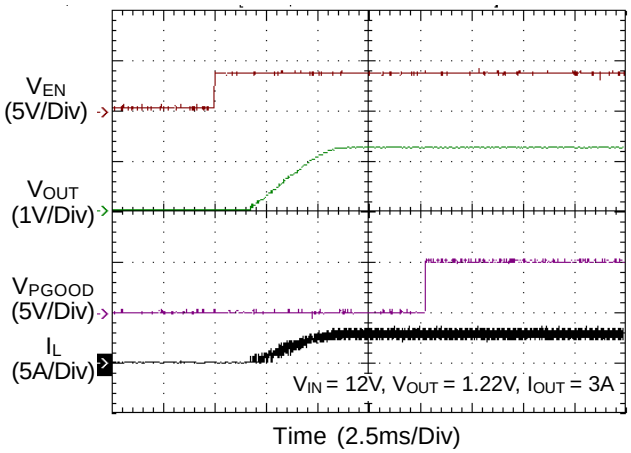
Power On from VIN



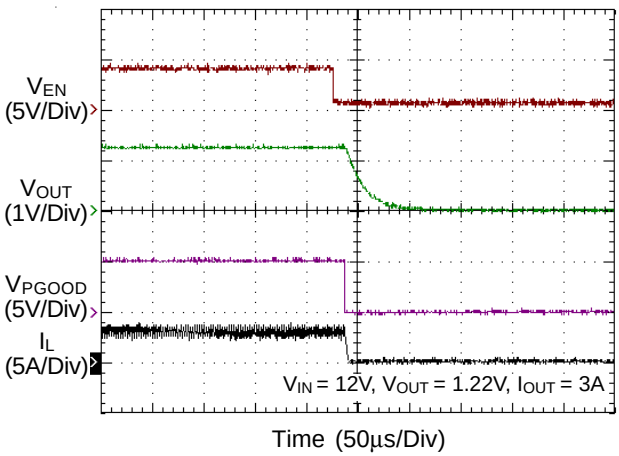
Power Off from VIN



Power On from EN



Power Off from EN



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Application Information

The IC is a synchronous high voltage step-down converter that can support the input voltage range from 4.5V to 21V and the output current can be up to 3A.

Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage 0.808V (typ.).

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

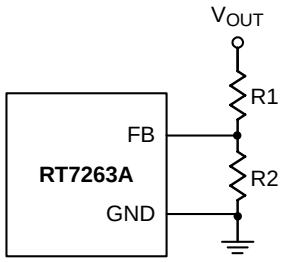

Figure 1. Output Voltage Setting

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT pin and SW pin as shown in Figure 2. This capacitor provides the gate driver voltage for the high side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the IC. Note that the external boot voltage must be lower than 5.5V.

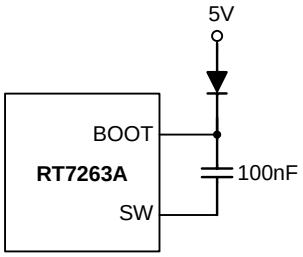

Figure 2. External Bootstrap Diode

Soft-Start for WDFN-14L Package

The RT7263AZQW (WDFN-14L package) contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing is programmed by the external capacitor between SS pin and GND. The chip provides an internal 10μA charge current for the external capacitor. If 47nF capacitor is used to set the soft-start, the period will be 4.7ms (typ.).

Soft-Start for SOP-8 (Exposed Pad) Package

The RT7263AZSP (SOP-8 (Exposed Pad) package) contains an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. Soft-start automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the internal reference, causing the duty pulse width to increase slowly and in turn reduce the output surge current. The typical soft-start time for this IC is set at 2ms.

Under Voltage Lockout Threshold

The IC includes an input Under Voltage Lockout Protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (4.2V), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage (3.8V) during normal operation, the device stops switching. The UVLO rising and falling threshold voltage includes a hysteresis to prevent noise caused reset.

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT7263A quiescent current drops to lower than 1μA. Driving the EN pin high (2V < EN < 5.5V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and C_{EN} capacitor from the VIN pin (see Figure 3).

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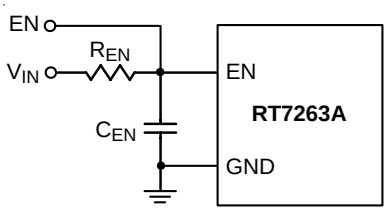

Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin, as shown in Figure 4. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} pin and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

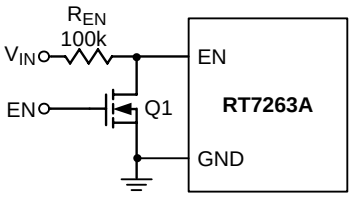

Figure 4. Digital Enable Control Circuit

The chip starts to operate when V_{IN} rises to 4.2V (UVLO threshold). During the V_{IN} rising period, if an 8V output voltage is set, V_{IN} is lower than the V_{OUT} target value and it may cause the chip to shut down. To prevent this situation, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust enable threshold, as shown in Figure 5. For example, the setting V_{OUT} is 8V and V_{IN} is from 0V to 12V, when V_{IN} is higher than 10V, the chip is triggered to enable the converter. Assume R_{EN1} = 50kΩ. Then,

$$R_{EN2} = \frac{(R_{EN1} \times V_{IH(MIN)})}{(V_{IN_S} - V_{IH(MIN)})}$$

where $V_{IH(MIN)}$ is the minimum threshold of enable rising (2V) and V_{IN_S} is the target turn on input voltage (10V in this example). According to the equation, the suggested resistor R_{EN2} is 12.5kΩ.

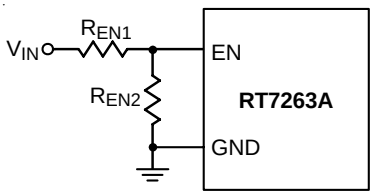

Figure 5. Resistor Divider for Lockout Threshold Setting

Operating Frequency and Synchronization

The internal oscillator runs at 500kHz (typ.) when the EN/SYNC pin is at logic-high level (>2V). If the EN pin is pulled to low-level for 10μs above, the IC will shut down. The RT7263A can be synchronized with an external clock ranging from 300kHz to 2MHz applied to the EN/SYNC pin. The external clock duty cycle must be from 30% to 90%.

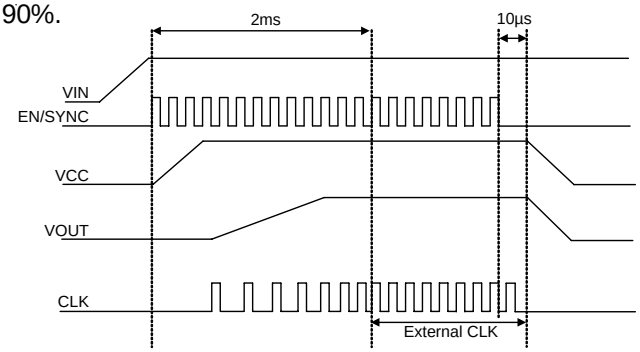

Figure 6. Startup Sequence Using External Sync Clock

Figure 6 shows the synchronization operation in startup period. When the EN/SYNC is triggered by an external clock, the RT7263A enters soft-start phase and the output voltage starts to rise. During the soft-start phase region, the oscillation frequency will be proportional to the feedback voltage until it is higher than 0.7V. With higher V_{FB}, the switching frequency is relatively higher. After startup period about 2ms, the IC operates with the same frequency as the external clock.

Power Good Output

The power good output is an open-drain output and requires a pull up resistor. When the output voltage is lower than 70% of its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within the allowed tolerances once more. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over and the output voltage has reached 90% of its set voltage.

Output Under Voltage Protection (Hiccup Mode)

For the IC, Hiccup Mode of Under Voltage Protection (UVP) is provided. When the FB voltage drops below half of the feedback reference voltage, V_{FB}, the UVP function will be triggered and the IC will shut down for a period of time and then recover automatically. The Hiccup Mode of UVP can reduce input current in short-circuit conditions.

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Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. Highest efficiency operation is achieved by reducing ripple current at low frequency, but it requires a large inductor to attain this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference and it is highly recommended to keep inductor value as close as possible to the recommended inductor values for each V_{OUT} as shown in Table 1.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

Input and Output Capacitors Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, one 22µF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to table 3 for more detail.

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (µF)	Case Size
C_{IN}	**MURATA**	GRM32ER71C226M	22	1210
C_{IN}	**TDK**	C3225X5R1C226M	22	1210
C_{OUT}	**MURATA**	GRM31CR60J476M	47	1206
C_{OUT}	**TDK**	C3225X5R0J476M	47	1210
C_{OUT}	**MURATA**	GRM32ER71C226M	22	1210
C_{OUT}	**TDK**	C3225X5R1C226M	22	1210

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal

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for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at excessively high temperatures. When the junction temperature is higher than 150°C, the chip is shut down the switching operation. The chip is automatically re-enabled when the junction temperature cools down by approximately 30°C.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-14L 4x3 package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for WDFN-14L 4x3 package

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 7 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

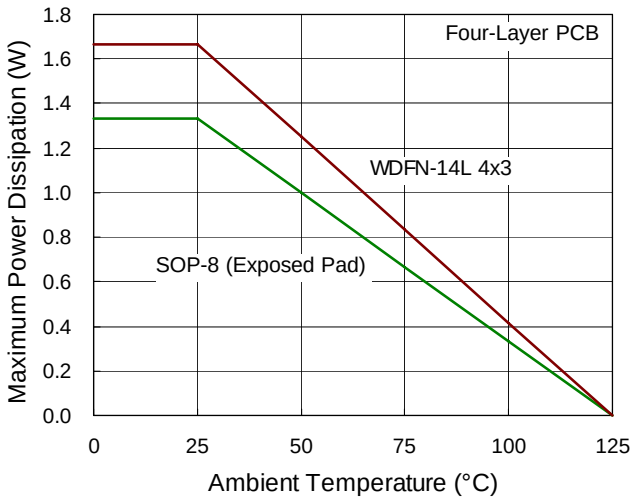

Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the IC.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the IC.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 8 for reference.

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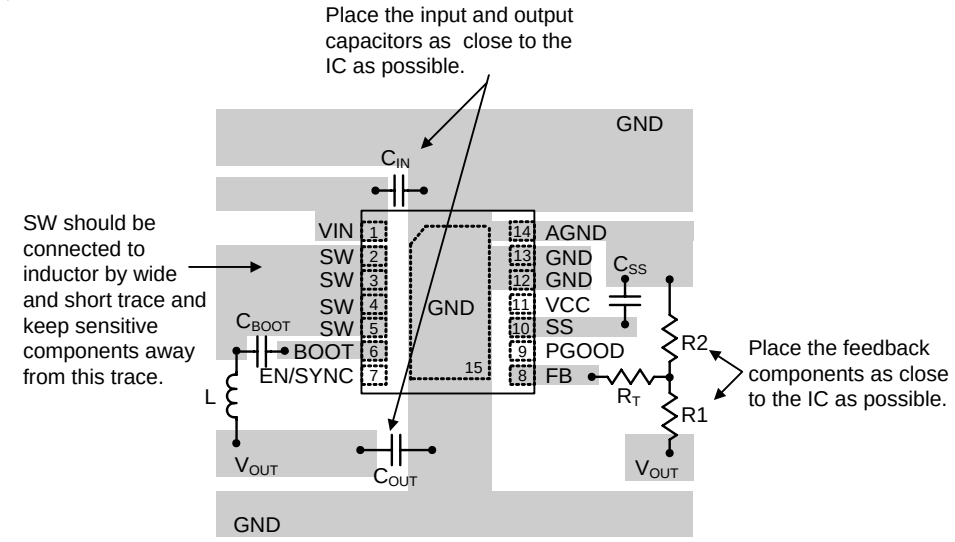

Figure 8 (a). PCB Layout Guide for WDFN-14L 4x3

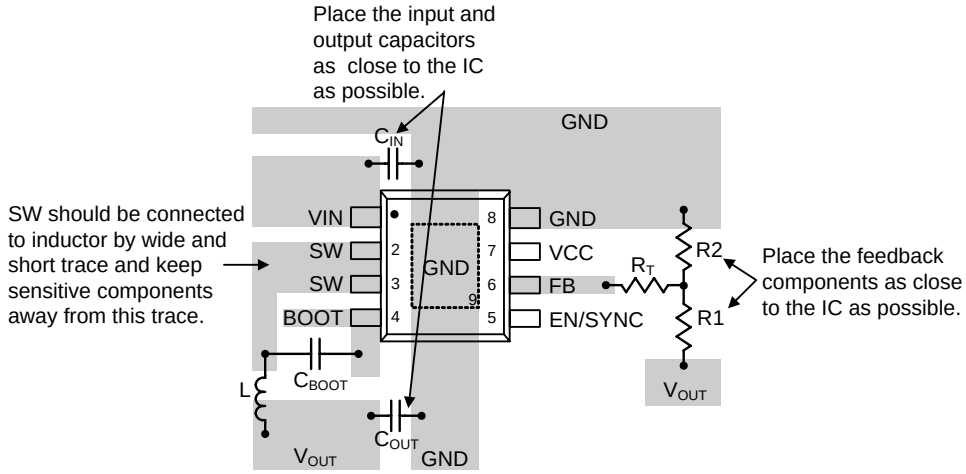

Figure 8 (b). PCB Layout Guide for SOP-8 (Exposed Pad)

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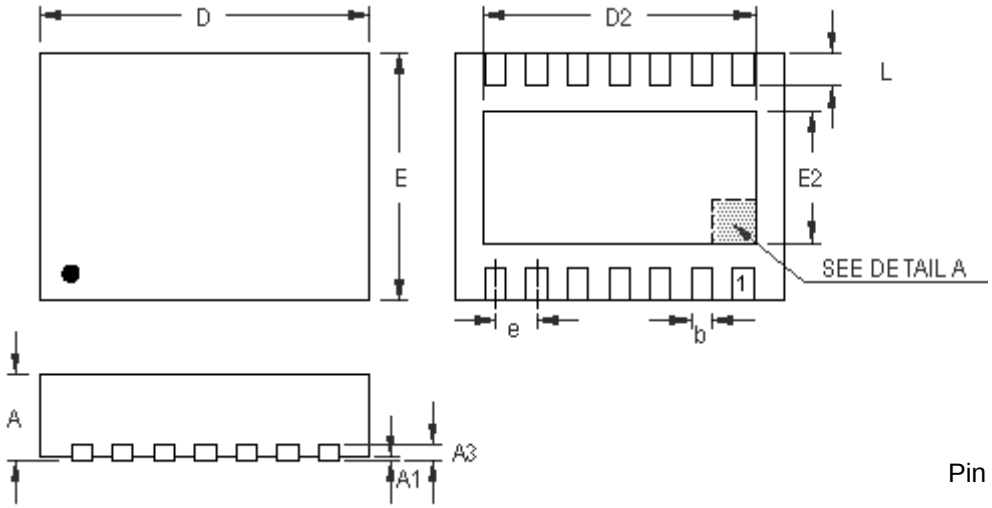
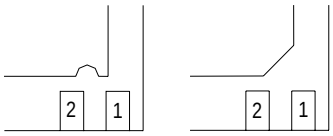
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.900	4.100	0.154	0.161
D2	3.250	3.350	0.128	0.132
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 14L DFN 4x3 Package

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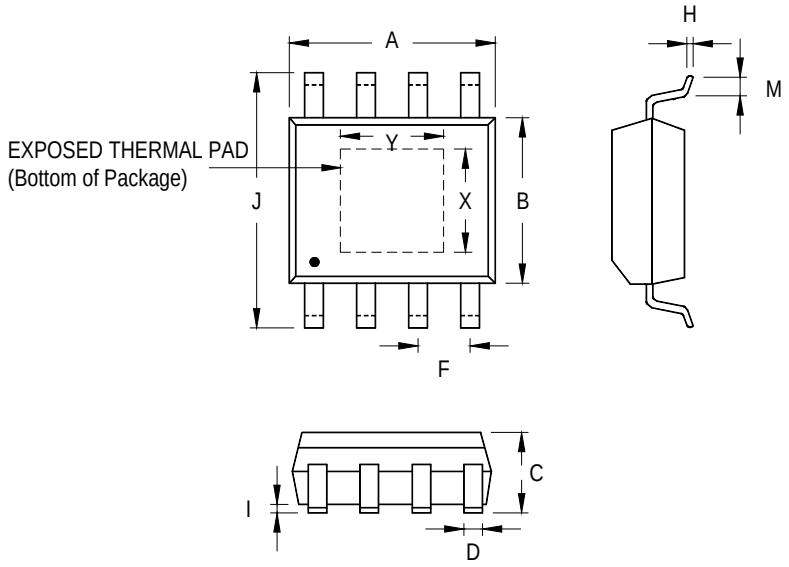

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Richtek Technology Corporation

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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