LC876796B/80B/72B

8-Bit Single Chip Microcontroller

LC876796B

8 bit Single Chip Microcontroller incorporating 96KB ROM and 2048 byte RAM on chip

LC876780B

8 bit Single Chip Microcontroller incorporating 80KB ROM and 2048 byte RAM on chip

LC876772B

8 bit Single Chip Microcontroller incorporating 72KB ROM and 2048 byte RAM on chip

Overview

The LC876796B/ LC876780B/ LC876772B are 8 bit single chip microcomputers with the following on-chip functional blocks:

- CPU: operable at a minimum bus cycle time of 100ns
- On-chip ROM Maximum Capacity : LC876796B 96K bytes
  LC876780B 80K bytes
  LC876772B 72K bytes
- On-chip RAM: 2048 bytes
- VFD automatic display controller / driver
- 16 bit timer / counter (can be divided into two 8 bit timers)
- 16 bit timer / counter (can be divided into two 8 bit timers / two 8 bit PWM)
- four 8 bit timer with prescaler
- timer for use as date / time clock
- High speed clock counter
- System clock divider function
- synchronous serial I/O port (with automatic block transmit / receive function)
- asynchronous / synchronous serial I/O port
- 14-channel × 8-bit AD converter
- Weak signal detector
- 21-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

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Features

(1) Read-Only Memory (ROM): LC876796B 98304 × 8 bits
: LC876780B 81920 × 8 bits
: LC876772B 73728 × 8 bits

(2) Random Access Memory (RAM): LC876796B/80B/72B 2048 × 9 bits

(3) Minimum Bus Cycle Time: 100ns (10MHz)
Note: The bus cycle time indicates ROM read time.

(4) Minimum Instruction Cycle Time (tCYC) : 300ns (10MHz)

(5) Ports
- Input/output ports
  Data direction programmable for each bit individually : 20 (P1n, P70 to P73, P8n)
- 15V withstand input/output ports
  Data direction programmable in nibble units : 8 (P0n)
  (When N-channel open drain output is selected, data can be input in bit units.)
  Data direction programmable for each bit individually : 8 (P3n)
- Input ports : 2 (XT1,XT2)
- VFD output ports
  Large current outputs for digits : 9 (S0 / T0 to S8 / T8)
  Large current outputs for digits / segments : 7 (S9 / T9 to S15 / T15)
  digit / segment outputs : 8 (S16 to S23)
  segment outputs : 28 (S24 to S51)
  Other functions
  Input/output ports : 12 (PFn, PG0 to PG3)
  Input ports : 24 (PCn, PDn, PEn)
- Oscillator pins : 2 (CF1,CF2)
- Reset pin : 1 (RES#)
- Power supply : 6 (VSS1 to 2, VDD1 to 4)

(6) VFD automatic display controller
- Programmable segment/digit output pattern
  Output can be switched between digit/segment waveform output (pins 9 to 24 can be used for output of digit waveforms).
  parallel-drive available for large current VFD.
- 16-step dimmer function available

(7) Weak signal detection (MIC signals etc)
- Counts pulses with width greater than a preset value
- 2 bit counter

(8) Timers
- Timer 0: 16 bit timer / counter with capture register
  Mode 0: 2 channel 8-bit timer with programmable 8 bit prescaler and 8 bit capture register
  Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register + 8 bit Counter with 8-bit capture register
  Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
  Mode 3: 16 bit counter with 16 bit capture register

- Timer 1: PWM / 16 bit timer / counter with toggle output
  Mode 0: 8 bit timer (with toggle output) + 8 bit timer / counter (with toggle output)
  Mode 1: 2 channel 8 bit PWM
  Mode 2: 16 bit timer / counter (with toggle output) Toggle output also possible using the lower order 8 bits.
  Mode 3: 16 bit timer (with toggle output) The lower order 8 bits can be used as PWM output.

- Timer 4: 8 bit timer with 6 bit prescaler
- Timer 5: 8 bit timer with 6 bit prescaler
- Timer 6: 8 bit timer with 6 bit prescaler
- Timer 7: 8 bit timer with 6 bit prescaler

- Base Timer
  1) The clock signal can be selected from any of the following.
     Sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output from timer 0
  2) Interrupts can be selected to occur at one of five different times.

(9) High speed clock counter
1) Capable of counting maximum: 20MHz clock (Using main clock 10MHz)
2) Real time output

(10) Serial-interface
- SIO 0: 8 bit synchronous serial Interface
  1) LSB first / MSB first function available
  2) Internal 8 bit baud-rate generator (maximum transmit clock period 4/3 Tcyc)
  3) Consecutive automatic data communication (1-256 bits)
- SIO 1: 8 bit asynchronous / synchronous serial interface
  Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2–512 Tcyc)
  Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8–2048Tcyc)
  Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2–512 Tcyc)
  Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

(11) AD converter
-8 bits × 14 channels

(12) Remote control receiver circuit (connected to P73/INT3/T0IN terminal)
-Noise rejection function (noise rejection filter time constant can selected from 1 / 32 / 128 Tcyc)

(13) Watchdog timer
- The watching timer period is set using an external RC.
- Watchdog timer can produce interrupt, system reset.

(14) Interrupts: 21-source, 10-vectored interrupts

1) Three priority (low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is refused.

2) If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/Base timer/INT5
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/MIC/T6/T7
10	0004BH	H or L	VFD automatic display controller/Port0/T4/T5

- Priority Level: X>H>L
- For equal priority levels, vector with lowest address takes precedence.

(15) Subroutine stack levels: 1024 levels max. Stack is located in RAM.

(16) Multiplication and division

- 16 bit × 8 bit (executed in 5 cycles)
- 24 bit × 16 bit (12 cycles)
- 16 bit ÷ 8 bit (8 cycles)
- 24 bit ÷ 16 bit (12 cycles)

(17) Oscillation circuits

- On-chip RC oscillation circuit for system clock use.
- On-chip CF oscillation circuit for system clock use. (R_f built in)
- On-chip Crystal oscillation circuit low speed system clock use. (Rd, R_f external)
- On-chip frequency -variable RC oscillation circuit for system clock use

(18) System clock divider function

- Able to reduce current consumption

Available minimum instruction cycle time: 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs. (Using 10MHz main clock)

(19) Standby function

- HALT mode

HALT mode is used to reduce power consumption. Program execution is stopped. Peripheral circuits still operate but VFD display and some serial transfer operations stop.

1) Oscillation circuits are not stopped automatically.

2) Release occurs on system reset or by interrupt.

-HOLD mode

HOLD mode is used to reduce power consumption. Both program execution and peripheral circuits are stopped.

1) CF, RC and crystal oscillation circuits stop automatically.
2) Release occurs on any of the following conditions.
   (1) input to the reset pin goes low
   (2) a specified level is input at least one of INT0, INT1, INT2, INT4, INT5
   (3) an interrupt condition arises at port 0

-X'tal HOLD made

X'tal HOLD mode is used to reduce power consumption. Program execution is stopped. All peripheral circuits except the base timer are stopped.

1) CF and RC oscillation circuits stop automatically.
2) Crystal oscillator is maintained in its state at HOLD mode inception.
3) Release occurs on any an any of the following conditions
   (1) input to the reset pin goes low
   (2) a specified level is input to at least one of INT0, INT1, INT2, INT4, INT5
   (3) an interrupt condition arises at port 0
   (4) an interrupt condition arises at the base-timer

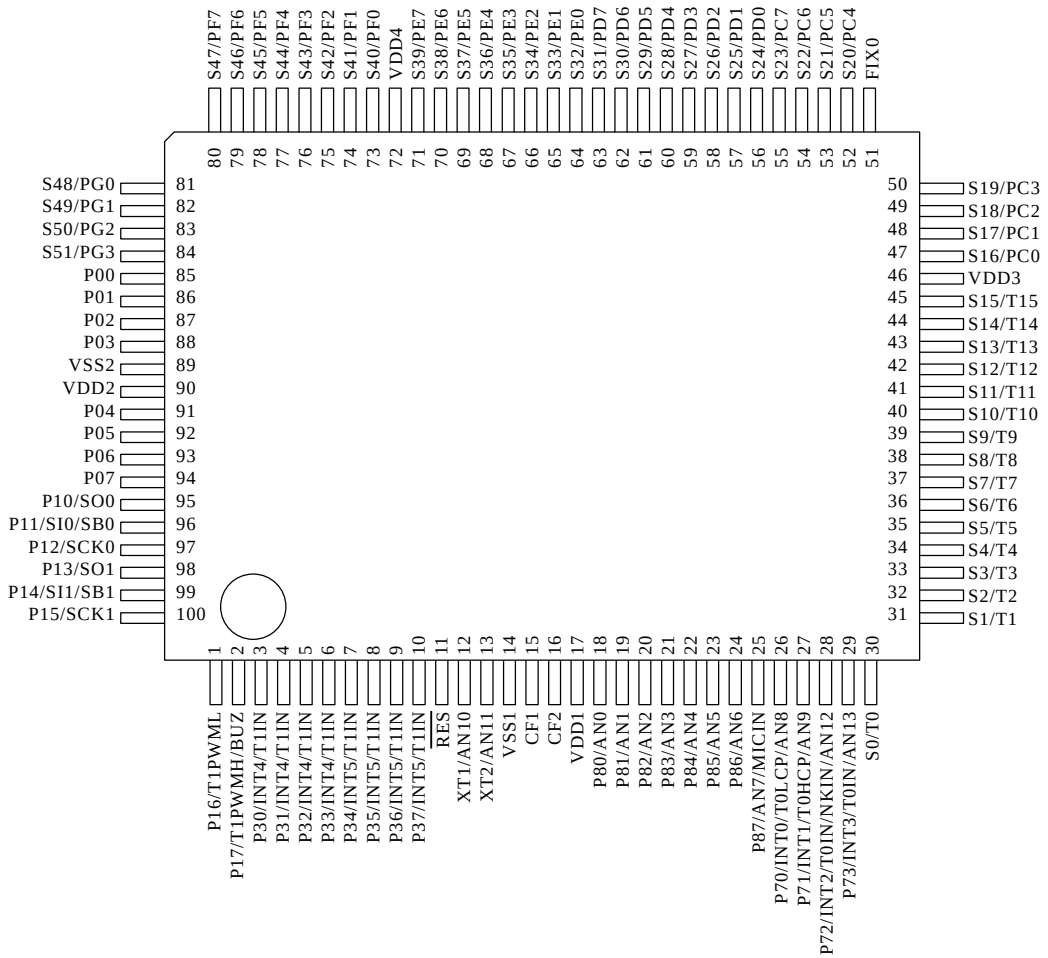
(20) Factory shipment

-delivery form QIP100E (LEAD FREE PRODUCT)

(21) Development tools

- Evaluation chip : LC876093
- Emulator : EVA62S + ECB876600 (Evaluation chip board) + SUB876700 + POD100QFP
  : ICE-B877300 + SUB876700 + POD100QFP
- Flash ROM version: LC87F67C8A

Pin Assignment



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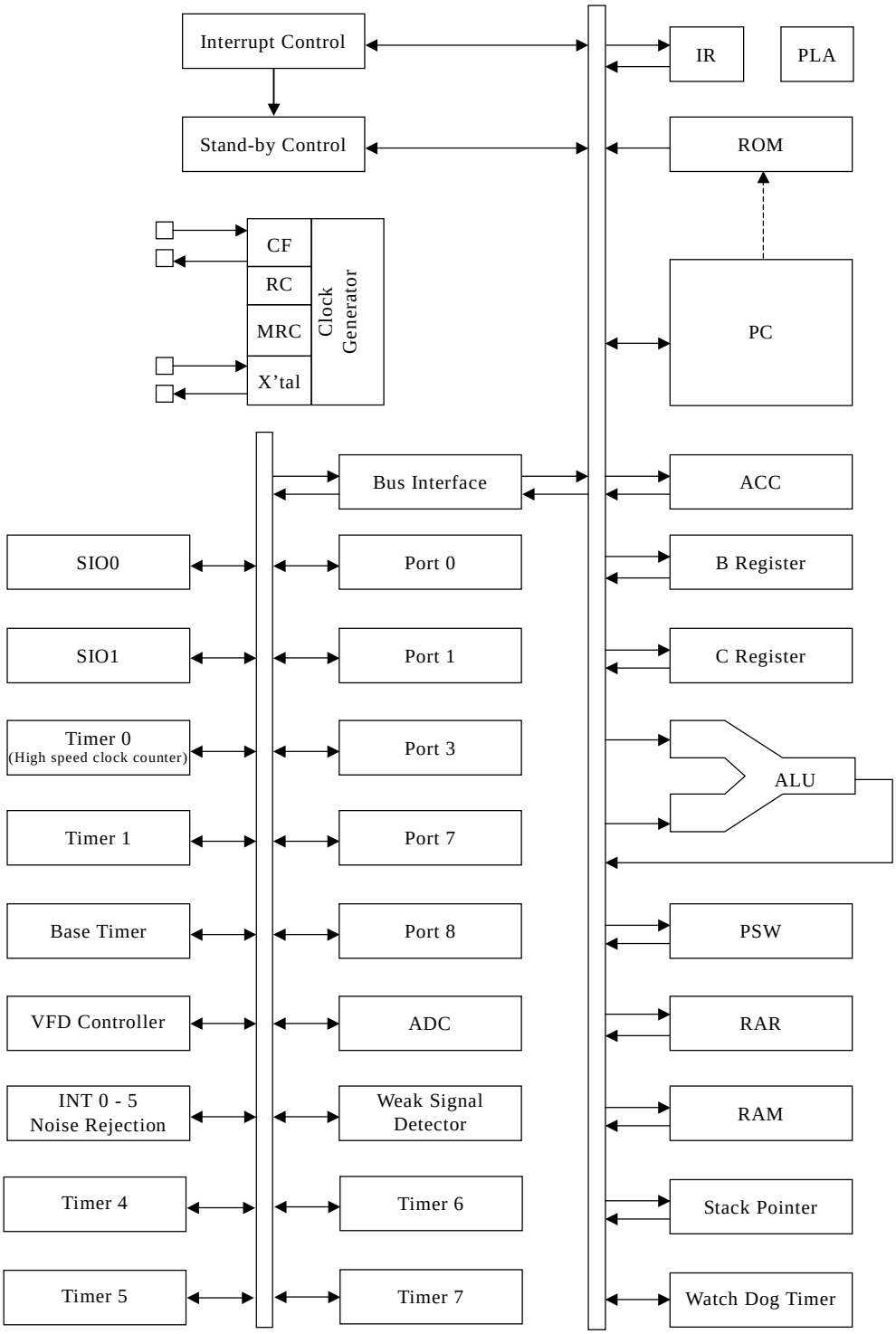
System Block Diagram



Pin Assignment

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>VSS1
VSS2</td><td>-</td><td>• Power supply (-)</td><td>No</td></tr>
<tr><td>VDD1
VDD2
VDD3
VDD4</td><td>-</td><td>• Power supply (+)</td><td>No</td></tr>
<tr><td>FIX0</td><td>-</td><td>• Test pin
Set as VSS with the user’s option. (see Note 1)</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8bit input/output port
• Data direction programmable in nibble units
• Use of pull-up resistor can be specified in nibble units
• Input for HOLD release
• Input for port 0 interrupt
• 15V withstand at N-channel open drain output</td><td>Yes</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8bit input/output port
• Data direction programmable for each bit
• Use of pull-up resistor can be specified for each bit
• Other pin functions
P10: SIO0 data output
P11: SIO0 data input / bus input / output
P12: SIO0 clock input / output
P13: SIO1 data output
P14: SIO1 data input / bus input / output
P15: SIO1 clock input / output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output / Buzzer output</td><td>Yes</td></tr>
<tr><td>PORT3
P30 to P37</td><td>I/O</td><td>• 8bit input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• 15V withstand at N-channel open drain output
• Other functions:
P30 to P33: INT4 input / HOLD release input / Timer 1 event input / Timer 0L capture input / Timer 0H capture input
P34 to P37: INT5 input / HOLD release input / Timer 1 event input / Timer 0L capture input / Timer 0H capture input
The following types of interrupt detection are possible:
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT5</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>Yes</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>PORT7
P70 to P73</td><td>I/O</td><td>• 4bit input/output port
• Data direction can be specified for each bit
• Use of pull-up resistor can be specified for each bit
• Other functions
P70: INT0 input / HOLD release input / Timer0L capture input / Output for watchdog timer
P71: INT1 input / HOLD release input / Timer0H capture input
P72: INT2 input / HOLD release input / Timer 0 event input / Timer0L capture input / High speed clock counter input
P73: INT3 input(noise rejection filter attached input) / Timer 0 event input / Timer 0H capture input
AD input port: AN8(P70), AN9(P71), AN12(P72), AN13(P73)
The following types of interrupt detection are possible:
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>No</td></tr>
<tr><td>PORT8

P80 to P87</td><td>I/O</td><td>• 8bit input/output port
• Input/output can be specified in a bit unit
• Other functions:
AD input port: AN0 to AN7
Weak signal detector input port: MICIN(P87)</td><td>No</td></tr>
<tr><td>S0/T0 to S8/T8</td><td>O</td><td>• Large current output for VFD display controller digit (can be used for segment)</td><td>No</td></tr>
<tr><td>S9/T9 to S15/T15</td><td>O</td><td>• Large current output for VFD display controller segment/digit</td><td>No</td></tr>
<tr><td>S16 to S23</td><td>I/O</td><td>• Output for VFD display controller segment/digit
• Other functions:
High voltage input port: PC0 to PC7</td><td>No</td></tr>
<tr><td>S24 to S31</td><td>I/O</td><td>• Output for VFD display controller segment
• Other functions:
High voltage input port: PD0 to PD7</td><td>No</td></tr>
<tr><td>S32 to S39</td><td>I/O</td><td>• Output for VFD display controller segment
• Other functions
High voltage input port: PE0 to PE7</td><td>No</td></tr>
<tr><td>S40 to S47</td><td>I/O</td><td>• Output for VFD display controller segment
• Other functions:
High voltage input/output port: PF0 to PF7</td><td>No</td></tr>
<tr><td>S48 to S51</td><td>I/O</td><td>• Output for VFD display controller segment
• Other functions:
High voltage input/output port: PG0 to PG3</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>Reset terminal</td><td>No</td></tr>
<tr><td>XT1</td><td>I</td><td>• Input for 32.768kHz crystal oscillation
• Other functions:
General purpose input port
When not in use, connect to VDD1.
AD input port: AN10</td><td>No</td></tr>
</table>

Pin name	I/O	Function	Option
XT2	I/O	• Output for 32.768kHz crystal oscillation • Other functions: General purpose input port When not in use, set to oscillation mode and leave open circuit. AD input port: AN11	No
CF1	I	Input terminal for ceramic oscillator	No
CF2	O	Output terminal for ceramic oscillator	No

Note 1: The LC876700 series can be mounted onto the circuit board intended for the LC876500 and LC876600 series. In this case, the minus voltage of the VFD power supply is supplied to the FIX0 pin. Using a negative voltage does not alter the FIX0 pin's operation.

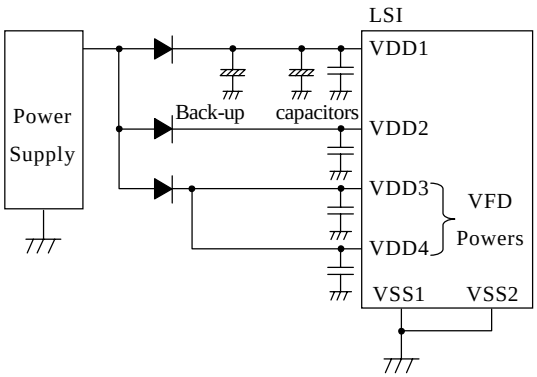
Port Output Configuration

Output configuration and pull-up/pull-down resistor options are shown in the following table.
Input/output is possible even when port is set to output mode.

Terminal	Option applies to:	Options	Output Format	Pull-up resistor	Pull-down resistor
P00 to P07	1 bit units	1	CMOS	Programmable (Note 1)	-
		2	15V Nch-open drain	None	-
P10 to P17	each bit	1	CMOS	Programmable	-
		2	Nch-open drain	Programmable	-
P30 to P37	each bit	1	CMOS	Programmable	-
		2	15V Nch-open drain	None	-
P70	-	None	Nch-open drain	Programmable	-
P71 to P73	-	None	CMOS	Programmable	-
P80 to P87	-	None	Nch-open drain	None	-
S0/T0 to S15/T15 S16 to S51	-	None	High voltage Pch-open drain	-	None
XT1	-	None	Input only	None	-
XT2	-	None	Output for 32.768kHz crystal oscillation	None	-

Note 1: Programmable pull-up resisters of Port 0 can be attached in nibble units (P00-03, P04-07).

* Note 1: Connect as follows to reduce noise on VDD and increase the back-up time.
VSS1, and VSS2 must be connected together and grounded.
* Note 2: The power supply for the internal memory is VDD1 but it uses the VDD2 as the power supply for ports. When the VDD2 is not backed up, the port level does not become “H” even if the port latch is in the “H” level. Therefore, when the VDD2 is not backed up and the port latch is “H” level, the port level is unstable in the HOLD mode, and the back up time becomes shorter because the through current runs from VDD to GND in the input buffer.
If VDD2 is not backed up, output “L” by the program or pull the port to “L” by the external circuit in the HOLD mode so that the port level becomes “L” level and unnecessary current consumption is prevented.



1. Absolute maximum ratings / Ta=25°C and VSS1=VSS2=0V

Parameter		Symbol	Pins	Conditions		Limits			
					VDD[V]	min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1,VDD2, VDD3,VDD4	VDD1=VDD2= VDD3=VDD4		-0.3		+7.0	V
Input voltage		VI(1)	XT1,XT2,CF1, $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	FIX0			VDD-45		VDD+0.3	
Output voltage		VO(1)	S0/T0 to S15/T15			VDD-45		VDD+0.3	
Input/Output voltage		VIO(1)	•Port 0: CMOS output option •Port 1 •Port 3: CMOS output option •Port 7 •Port 8			-0.3		VDD+0.3	
		VIO(2)	•Port 0 open drain •Port 3 open drain			-0.3		15	
		VIO(3)	S16 to S51			VDD-45		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Port 0, 1, 3	•CMOS output selected •Current at each pin		-10			mA
		IOPH(2)	Port 71,72,73	Current at each pin		-3			
		IOPH(3)	S0/T0 to S15/T15	Current at each pin		-30			
		IOPH(4)	S16 to S51	Current at each pin		-15			
	Total output current	ΣIOAH(1)	Port 0	Total of all pins		-30			
		ΣIOAH(2)	Port 1,3	Total of all pins		-30			
		ΣIOAH(3)	Port 7	Total of all pins		-5			
		ΣIOAH(4)	S0/T0 to S15/T15	Total of all pins		-65			
		ΣIOAH(5)	S16 to S27	Total of all pins		-60			
		ΣIOAH(6)	S28 to S39	Total of all pins		-60			
		ΣIOAH(7)	S40 to S51	Total of all pins		-60			
Low level output current	Peak output current	IOPL(1)	Port 0,1,3	For each pin				20	
		IOPL(2)	Port 7,8	For each pin				5	
	Total output current	ΣIOAL(1)	Port 00,01,02,03	Total of all pins				50	
		ΣIOAL(2)	•Port 04,05,06,07 •Port 1,3	Total of all pins				50	
		ΣIOAL(3)	Ports 7,8	Total of all pins				20	
Maximum power dissipation		Pdmax	QIP100E	Ta = -30 to+70°C				502	mW
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-55		125	

2. Recommended operating range / Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2=VDD3 =VDD4	0.294µs ≦ Tcyc ≦ 200µs		4.5		6.0	V
Hold voltage	VHD	VDD1	RAM and the register data are kept in HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	•Port 0,3: CMOS output option •Port 8	Output disable	4.5–6.0	0.3VDD +0.7		VDD	
	VIH(2)	Port 0,3: N-ch open drain output	Output disable	4.5–6.0	0.3VDD +0.7		13.5	
	VIH(3)	•Port 1 •Port 71,72,73 •P70 port input/ interrupt	Output disable	4.5–6.0	0.3VDD +0.7		VDD	
	VIH(4)	S16 to S51	Output P-channel Tr. OFF	4.5–6.0	0.33VDD +1.0		VDD	
	VIH(5)	Port 87 Weak signal input	Output disable	4.5–6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output disable	4.5–6.0	0.9VDD		VDD	
	VIH(7)	XT1, XT2, CF1, $\overline{RES}$		4.5–6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	•Port 0,3: CMOS output option •Port 8	Output disable	4.5–6.0	VSS		0.15VDD +0.4	
	VIL(2)	Port 0,3: N-ch open drain output	Output disable	4.5–6.0	VSS		0.15VDD +0.4	
	VIL(3)	•Port 1 •Port 71,72,73 •P70 port input / interrupt	Output disable	4.5–6.0	VSS		0.1VDD +0.4	
	VIL(4)	S16 to S51	Output P-channel Tr. OFF	4.5–6.0	-35		0.2VDD	
	VIL(5)	Port 87 weak signal input	Output disable	4.5–6.0	VSS		0.25VDD	
	VIL(6)	Port 70 Watchdog timer	Output disable	4.5–6.0	VSS		0.8VDD -1.0	
	VIL(7)	XT1,XT2,CF1, $\overline{RES}$		4.5–6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5–6.0	0.294		200	µs
External system clock frequency	fEXCF(1)	CF1	•CF2 open circuit •system clock divider set to 1/1 •external clock DUTY = 50±5%	4.5–6.0	0.1		10	MHz
			•CF2 open circuit •system clock divider set to 1/2	4.5–6.0	0.2		20	

Continued

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Oscillation stabilizing time period (Note 1)	FmCF(1)	CF1, CF2	10MHz ceramic resonator oscillation Refer to figure 1	4.5–6.0		10		MHz
	FmCF(2)	CF1, CF2	4MHz ceramic resonator oscillation Refer to figure 1	4.5–6.0		4		
	FmRC		RC oscillation	4.5–6.0	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation	4.5-6.0		50		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	4.5–6.0		32.768		kHz

(Note 1) The oscillation constant is shown in table 1 and table 2.

3. Electrical characteristics / Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Input high current	IIH(1)	Ports 0,3: N-ch open drain output	•Output disable •VIN=13.5V (including OFF state leak current of the output Tr.)	4.5–6.0			5	µA
	IIH(2)	Port 0,1,3,7,8	•Output disable •Pull-up resister OFF. •VIN=VDD (including OFF state leak current of the output Tr.)	4.5–6.0			1	
	IIH(3)	S16 to S51 (Port C,D,E,F,G)	When configured as an input port VIN=VDD	4.5–6.0			60	
	IIH(4)	$\overline{RES}$	VIN=VDD	4.5–6.0			1	
	IIH(5)	XT1,XT2	When configured as an input port VIN=VDD	4.5–6.0			1	
	IIH(6)	CF1	VIN=VDD	4.5–6.0			15	
	IIH(7)	P87/AN7/MICIN weak signal input	VIN=VBIS+0.5V (VBIS : Bias voltage)	4.5–6.0	4.2	8.5	15	
Input low current	IIL(1)	Port 0,1,3,7,8	•Output disable •Pull-up resister OFF. •VIN=VSS (including OFF state leak current of the output Tr.)	4.5–6.0	-1			
	IIL(2)	$\overline{RES}$	VIN=VSS	4.5–6.0	-1			
	IIL(3)	XT1,XT2	When configured as an input port VIN=VSS	4.5–6.0	-1			
	IIL(4)	CF1	VIN=VSS	4.5–6.0	-15			
	IIL(5)	P87/AN7/MICIN weak signal input	VIN=VBIS-0.5V (VBIS : Bias voltage)	4.5–6.0	-15	-8.5	-4.2	
Output high voltage	VOH(1)	Port 0,1,3: CMOS output option	IOH=-1.0mA	4.5–6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5–6.0	VDD-0.5			
	VOH(3)	Port 7	IOH=-0.4mA	4.5–6.0	VDD-1			
	VOH(4)	S0/T0 to S15/T15	IOH=-20.0mA	4.5–6.0	VDD-1.8			
	VOH(5)		IOH=-1.0mA IOH at any single pin is not over 1mA.	4.5–6.0	VDD-1			
	VOH(6)	S16 to S51	IOH=-5.0mA	4.5–6.0	VDD-1.8			
	VOH(7)		IOH=-1.0mA IOH at any single pin is not over 1mA.	4.5–6.0	VDD-1			
Output low voltage	VOL(1)	Port 0,1,3	IOL=10mA	4.5–6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5–6.0			0.4	
	VOL(3)	Port 7,8	IOL=1mA	4.5–6.0			0.4	
Pull-up resistor	Rpu	Port 0,1,3,7	VOH=0.9VDD	4.5–6.0	15	40	70	kΩ

Continued

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	Max.	unit
Output off-leak current	IOFF(1)	S0/T0 to S15/T15, S16 to S51	•Output P-ch Tr. OFF •VOUT=VSS	4.5–6.0	-1			µA
	IOFF(2)		•Output P-ch Tr. OFF •VOUT=VDD-40V	4.5–6.0	-30			
Resistance of the low level hold Tr.	Rinpd	S16 to S51	•Output P-ch Tr. OFF	4.5–6.0		200		kΩ
Hysteresis voltage	VHIS(1)	•Port 1,7 • $\overline{\text{RES}}$		4.5–6.0		0.1VDD		V
	VHIS(2)	Port 87 weak signal input		4.5–6.0		0.1VDD		
Pin capacitance	CP	All pins	•All other terminals connected to VSS. •f=1MHz •T_a=25°C	4.5–6.0		10		pF
Input sensitivity	Vsen	Port 87 weak signal input		4.5–6.0	0.12VDD			Vpp

4. Serial input/output characteristics / Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter			Symbol	Pins	Conditions		Limits			
						VDD[V]	min.	typ.	max.	unit
Serial clock	Input clock	Cycle Time	tSCK(1)	SCK0(P12)	Refer to figure 6	4.5–6.0	4/3			tCYC
		Low Level pulse width	tSCKL(1)				2/3			
			tSCKLA(1)				2/3			
		High Level pulse width	tSCKH(1)				2/3			
			tSCKHA(1)				5			
		Cycle Time	tSCK(2)	SCK1(P15)	Refer to figure 6	4.5–6.0	2			
		Low Level pulse width	tSCKL(2)				1			
		High Level pulse width	tSCKH(2)				1			
	Output clock	Cycle Time	tSCK(3)	SCK0(P12)	•CMOS output option •Refer to figure 6	4.5–6.0	4/3			
		Low Level pulse width	tSCKL(3)					1/2		tSCK
			tSCKLA(2)					3/4		
		High Level pulse width	tSCKH(3)					1/2		
			tSCKHA(2)					2		
		Cycle Time	tSCK(4)	SCK1(P15)	•CMOS output option •Refer to figure 6	4.5–6.0	2			tCYC
		Low Level pulse width	tSCKL(4)					1/2		tSCK
		High Level pulse width	tSCKH(4)					1/2		
Serial input	Data set-up time		tsDI	SI0(P11), SI1(P14), SB0(P11), SB1(P14)	•Measured with respect to SI0CLK leading edge. •Refer to figure 6	4.5–6.0	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdDO	SO0(P10), SO1(P13), SB0(011), SB1(P14)	•Measured with respect to SI0CLK trailing edge. •When port is open drain: Time delay from SI0CLK trailing edge to the SO data change. •Refer to figure 6	4.5–6.0			1/3 tCYC +0.05	

5. Pulse input conditions / Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P30 to P33) INT5(P34 to P37)	•Interrupt acceptable •Events to timer 0,1 can be input.	4.5–6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (Noise rejection ratio set to 1/1.)	•Interrupt acceptable •Events to timer 0 can be input.	4.5–6.0	2			
	tPIH(3) tPIL(3)	INT3(P73) (Noise rejection ratio set to 1/32.)	•Interrupt acceptable •Events to timer 0 can be input.	4.5–6.0	64			
	tPIH(4) tPIL(4)	INT3(P73) (Noise rejection ratio set to 1/128.)	•Interrupt acceptable •Events to timer 0 can be input.	4.5–6.0	256			
	tPIH(5) tPIL(5)	MICIN(P87)	•Weak signal detection counter enabled	4.5–6.0	1			
	tPIH(6) tPIL(6)	NKIN(P72)	•High speed clock counter countable	4.5–6.0	1/12			
	tPIL(7)	$\overline{\text{RES}}$	•Reset possible	4.5–6.0	200			µs

6. AD converter characteristics / Ta=-30°C to + 70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Resolution	N	AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2), AN12(P72), AN13(P73)		4.5–6.0		8		bit
Absolute precision	ET		(Note2)	4.5–6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 32 × tCYC (ADCR2=0) (Note 3)	4.5–6.0	15.62 (tCYC= 0.488µs)		97.92 (tCYC= 3.06µs)	µs
			AD conversion time = 64 × tCYC (ADCR2=1) (Note 3)		18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			4.5–6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5–6.0			1	µA
	IAINL		VAIN=VSS	4.5–6.0	-1			

(Note 2) Absolute precision not including quantizing error (±1/2 LSB).

(Note 3) Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

7. Current dissipation characteristics / Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD1 = VDD2 = VDD3 = VDD4	•FmCF=10MHz for Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider set to 1/1	4.5–6.0		9.5	30	mA
	IDDOP(2)		•CF1=20MHz for external clock •FsX'tal=32.768kHz for crystal oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider set to 1/2	4.5–6.0		10.5	31	
	IDDOP(3)		•FmCF=4MHz Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock: CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider set to 1/1	4.5–6.0		4.2	17	
	IDDOP(4)		•FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz for crystal oscillation •Frequency variable RC oscillation stopped. •System clock: RC oscillation •Divider set to 1/2	4.5–6.0		1	10	
	IDDOP(5)		•FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz for crystal oscillation •Internal RC oscillation stopped. •System clock: 1MHz with frequency variable RC oscillation •Divider set to 1/2	4.5–6.0		2	12	
	IDDOP(6)		•FmCF=0Hz (No oscillation) •FsX'tal=32.768kHz for crystal oscillation •System clock: 32.768KHz •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider set to 1/2	4.5–6.0		40	140	μA

Continued

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Current dissipation HALT mode (Note 4)	IDDHALT(1)	VDD1= VDD2= VDD3= VDD4	HALT mode •FmCF=10MHz for Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider: 1/1	4.5–6.0		4	12	mA
	IDDHALT(2)		HALT mode •CF1=20MHz for external clock •FsX'tal=32.768kHz for crystal oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider 1/2	4.5–6.0		4.8	13	
	IDDHALT(3)		HALT mode •FmCF=4MHz for Ceramic resonator oscillation •FsX'tal=32.768kHz for crystal oscillation •System clock : CF oscillation •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider: 1/1	4.5–6.0		1.8	6	
	IDDHALT(4)		HALT mode •FmCF=0Hz (When oscillation stops.) •FsX'tal=32.768kHz for crystal oscillation •Frequency variable RC oscillation stopped. •System clock : RC oscillation •Divider: 1/2	4.5–6.0		500	1600	µA
	IDDHALT(5)		HALT mode •FmCF=0Hz (When oscillation stops.) •FsX'tal=32.768kHz for crystal oscillation •Internal RC oscillation stopped. •System clock: 1MHz with frequency variable RC oscillation •Divider: 1/2	4.5–6.0		1500	3600	

Continued

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Current dissipation HALT mode (Note 4)	IDDHALT(6)	VDD1= VDD2= VDD3= VDD4	HALT mode •FmCF=0Hz (When oscillation stops.) •FsX'tal=32.768kHz for crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stopped. •Frequency variable RC oscillation stopped. •Divider: 1/2	4.5–6.0		25	100	µA
Current dissipation HOLD mode	IDDHOLD(1)	VDD1	HOLD mode •CF1=VDD or open circuit (when using external clock)	4.5–6.0		0.05	25	
Current dissipation Date/time clock HOLD mode	IDDHOLD(2)	VDD1	Date/time clock HOLD mode •CF1=VDD or open circuit (when using external clock) •FsX'tal=32.768kHz for crystal oscillation	4.5–6.0		20	90	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Main system clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer.

Table 1. Main system clock oscillation circuit characteristics using ceramic resonator

Frequency	Manufacturer	Oscillator	Circuit parameters			Operating supply voltage range [V]	Oscillation stabilizing time		Notes
			C1 [pF]	C2 [pF]	Rd1 [Ω]		Typ [mS]	Max [mS]	
10MHz	MURATA	CSTLS10M0G53-B0	(15)	(15)	150	4.5~6.0	0.04	0.25	Built in C1,C2
		CSTCE10M0G52-R0	(10)	(10)	150	4.5~6.0	0.04	0.25	Built in C1,C2
4MHz	MURATA	CSTLS4M00G56-B0	(47)	(47)	220	4.5~6.0	0.15	0.5	Built in C1,C2
		CSTCR4M00G55-R0	(39)	(39)	0	4.5~6.0	0.05	0.3	Built in C1,C2

The oscillation stabilizing time is a period until the oscillation becomes stable after VDD becomes higher than minimum operating voltage. (Refer to Figure4)

Subsystem clock oscillation circuit characteristics

The characteristics in the table bellow is based on the following conditions:

1. Use the standard evaluation board SANYO has provided.
2. Use the peripheral parts with indicated value externally.
3. The peripheral parts value is a recommended value of oscillator manufacturer

Table 2. Subsystem clock oscillation circuit characteristics using crystal oscillator

Frequency	Manufacturer	Oscillator	Circuit parameters				Operating supply voltage range [V]	Oscillation stabilizing time		Notes
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		Typ [S]	Max [S]	
32.768kHz	SEIKO EPSON									

The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode. (Refer to Figure4)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

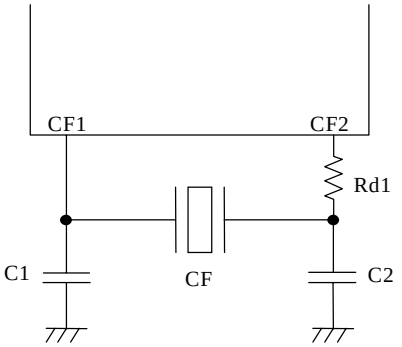


Figure 1 Ceramic oscillation circuit

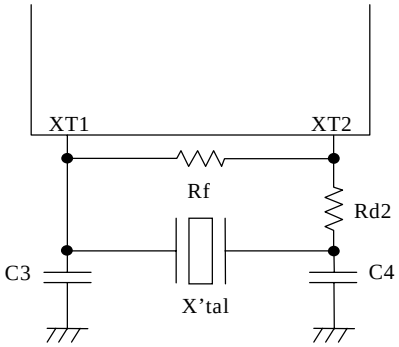


Figure 2 Crystal oscillation circuit

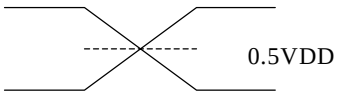
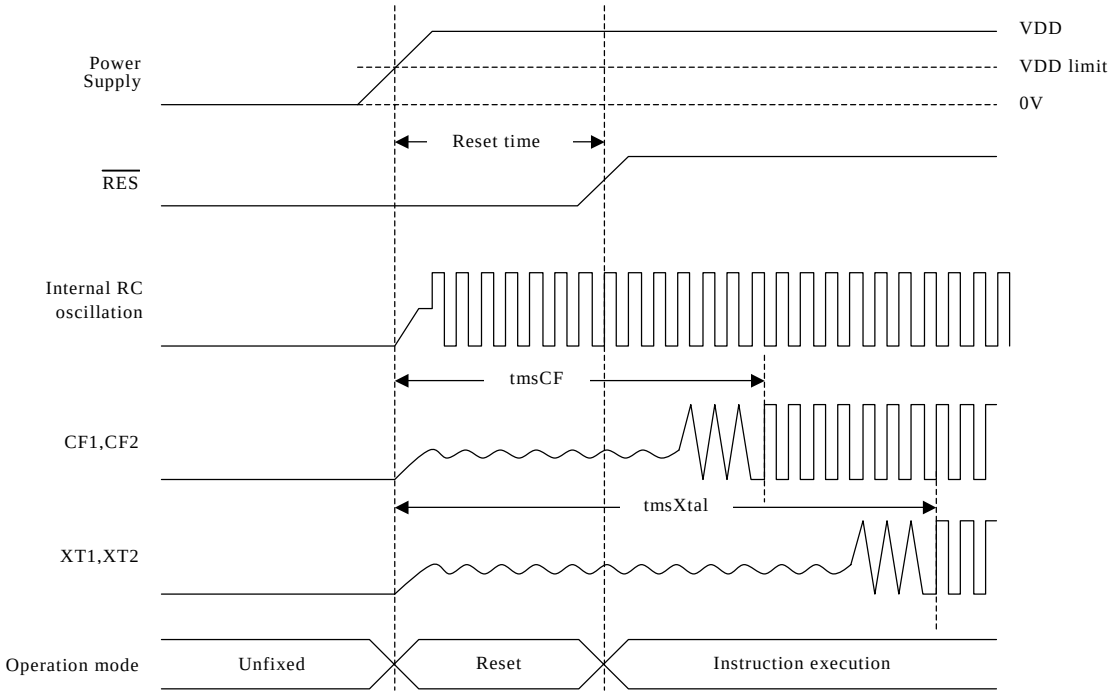
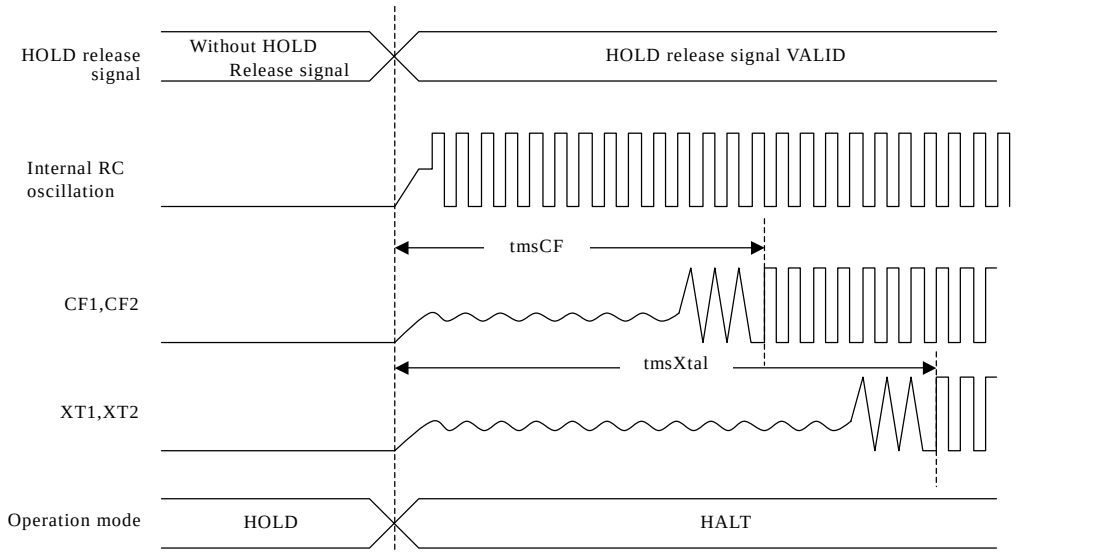


Figure 3 AC timing measurement point

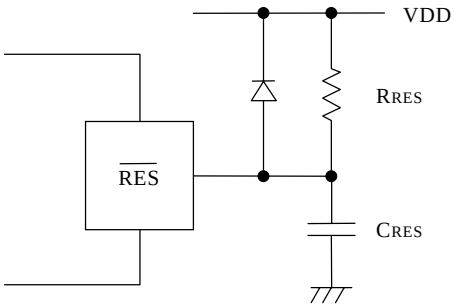


Reset time and oscillation stable time



HOLD release signal and oscillation stable time

Figure 4 Oscillation stablization time



(Note) Set CRES, RRES values such that reset time exceeds 200µs.

Figure 5 Reset circuit

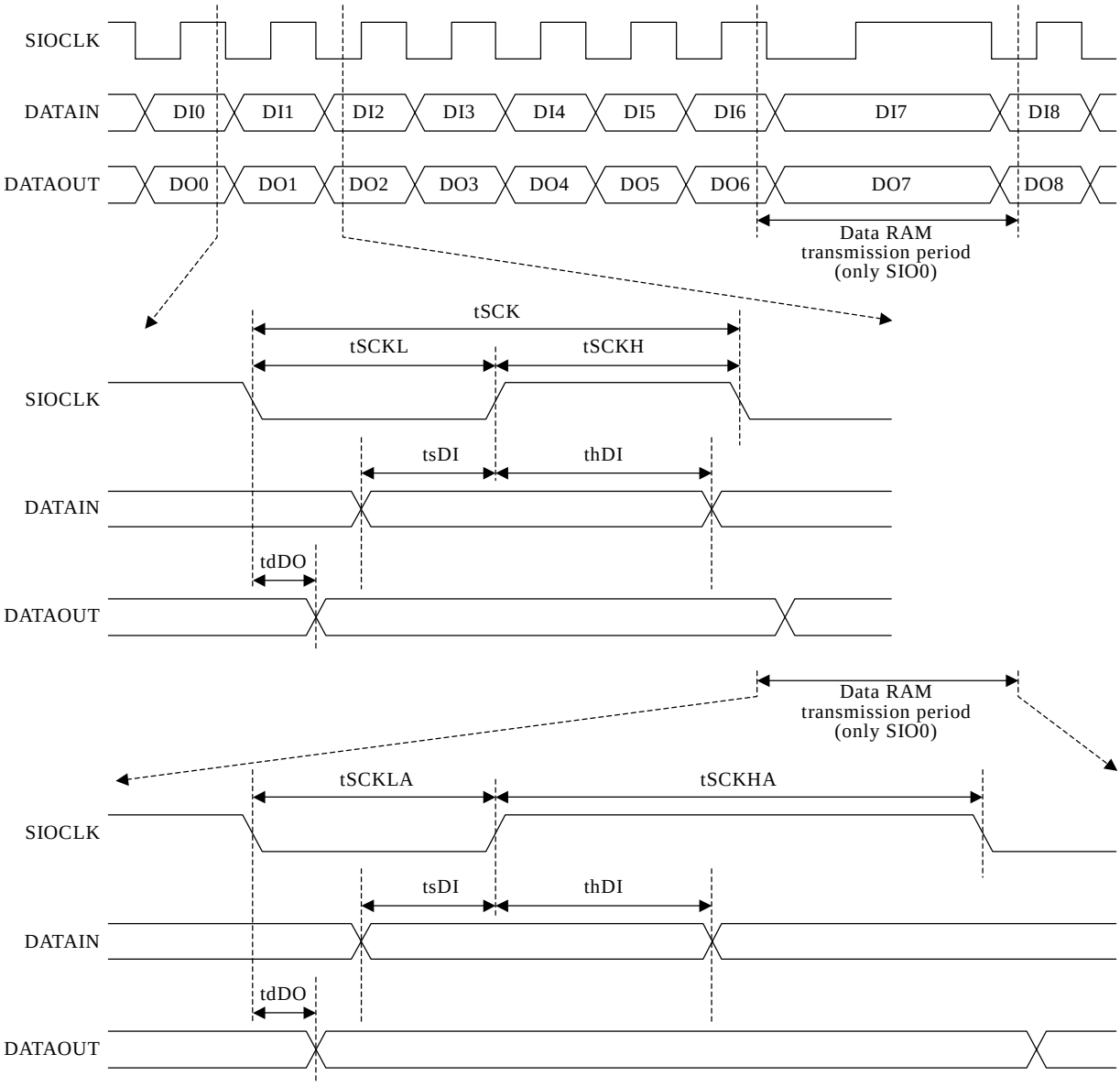


Figure 6 Serial input / output test condition

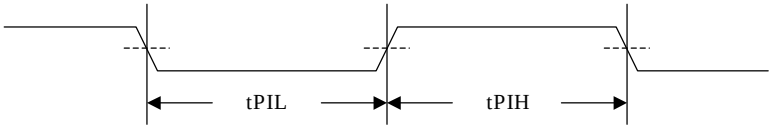


Figure 7 Pulse input timing condition