Document Title

**256Kx8 SUper Low Power and Low Voltage
Full CMOS SRAM Data Sheets for 48-CSP**

Revision History

RevNo.	History	DraftData	Remark
Rev. 0.0	–1'st edition –Package Dimension Finalized	Feb. 6'th, 1997	Preliminary

Rev. 0.1	–2'nd edition
	–Change speed marking method
	  Marking was indicate speed at high power,
	  that change to speed at low power
		Apr. 18'th, 1997	Preliminary

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256Kx8 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Scale Package)

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization : 256Kx8
- Power Supply Voltage
  KM68FS2000Z Family : 2.3V(Min) ~ 3.3V(Max)
  KM68FR2000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68FS2000Z and KM68FR2000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family support various operating temperature ranges and has very small size with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

| Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Power Dissipation		PKG Type
				Standby (I_{SB1})	Operating (I_{CC2})	
KM68FS2000Z	Commercial (0~70°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	10μA (Max)	55mA(Max) 30mA(Max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM68FR2000Z		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	
KM68FS2000ZI	Industrial (-40~85°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	10μA (Max)	55mA(Max) 30mA(Max)	
KM68FR2000ZI		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	

* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	A0	A1	CS2	A3	A6	A8
B	I/O5	A2	$\overline{WE}$	A4	A7	I/O1
C	I/O6		NC	A5		I/O2
D	Vss					Vcc
E	Vcc					Vss
F	I/O7		NC	A17		I/O3
G	I/O8	$\overline{OE}$	$\overline{CS1}$	A16	A15	I/O4
H	A9	A10	A11	A12	A13	A14

* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM
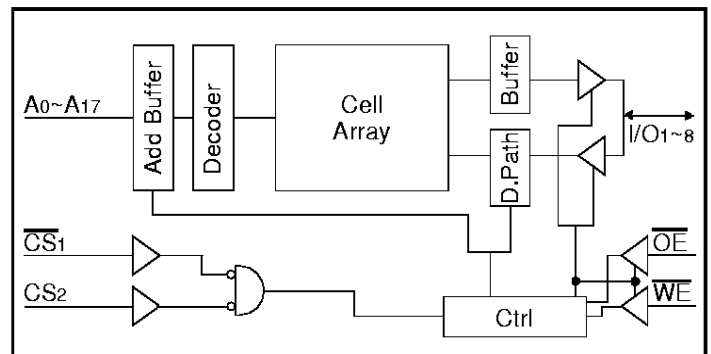
Name	Function	Name	Function
A0~A17	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{CS1}$,CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	N.C.	No Connection

SAMSUNG ELECTRONICS CO., LTD reserves the right to change products and specifications without notice.

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70°C)		Industrial Temp Product (-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM68FS2000Z-15	48-CSP, 2.5V/3.0V, 150/100ns	KM68FS2000Z-15	48-CSP, 2.5V/3.0V, 150/100ns
KM68FR2000Z-30	48-CSP, 1.8V/2.5V, 300ns	KM68FR2000Z-30	48-CSP, 1.8V/2.5V, 300ns

* The meaning of 2.5V/3.0V, 150/100ns is that the operating V_{CC} is ranged from 2.3V(Min) to 3.3V(Max) with speed 150ns @2.5V±0.2 and 100ns @3.0V±0.3. This type of meaning is applied to other notations like the example.

** But in case of KM68FR1000Z-30, there is only one speed bin, 300ns though it supports wide range operating V_{CC}.

ORDERING INFORMATION

KM6 8 X X 2000 X X X – X X

— Blank : Low Low Power
— Access Time : 7=70ns, 8=85ns, 10=100ns, 12=120ns,
        15=150ns, 30=300ns
— Operating Temperature : Blank=Commercial, E=Extended, I=Industrial
— Package Type : G=SOP, T=TSOP Forward R=TSOP Reverse
        Z=48-CSP with 0.75mm pitch
— Die Version : Blank=1'st generation
— Density : 2000=2Mbit
— S=2.3~3.3V, R=1.8~2.7V
— Process Technology : F–Full CMOS(6-Tr Cell)
— Organization : 8= x8
— SEC Standard SRAM

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to 3.6V	V	–
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V	V	–
Power Dissipation	P_D	1.0	W	–
Storage temperature	T_{STG}	-55 to 150	°C	–
Operating Temperature	T_A	0 to 70	°C	KM68FS2000Z KM68FR2000Z
		-40 to 85	°C	KM68FS2000ZI KM68FR2000ZI
Soldering temperature and time	T_{SOLDER}	260°C, 5sec(Lead Only)	–	–

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional opera tion should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect r eliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product		Min	Typ**	Max	Unit
Supply voltage	V_{CC}	KM68FS2000Z Family		2.3	2.5/3.0	3.3	V
		KM68FR2000Z Family		1.8	2.0/2.5	2.7	V
Ground	V_{SS}	All Family		0	0	0	V
Input high voltage	V_{IH}	KM68FS2000Z Family	Vcc=3.0±0.2V	2.2	–	Vcc+0.2	V
			Vcc=2.5±0.2V	2.0	–	Vcc+0.2	V
		KM68FR2000Z Family	Vcc=2.5±0.2V	2.0	–	Vcc+0.2	V
			Vcc=2.0±0.2V	1.6	–	Vcc+0.2	V
Input low voltage	V_{IL}	All Family		-0.2***	–	0.4	V

* 1) Commercial Product : T_A=0 to 70°C, unless otherwise specified
   2) Industrial Product : T_A=-40 to 85°C, unless otherwise specified
** T_A=25°C
*** V_{IL}(Min)=-1.5V for≤30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	–	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	–	10	pF

* Capacitance is sampled not, 100% tested

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DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions[1]			Min	Typ**	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc			–1	–	1	μA
Output leakage current	I_{LO}	$\overline{CS1}$=VIH or CS2=VIL or $\overline{WE}$=VIL, VIO=Vss to Vcc			–1	–	1	μA
Operating power supply current	I_{CC}	$\overline{CS1}$=VIL, CS2=VIH VIN=VIH or VIL, IIO=0mA		Read	–	–	10[5]	mA
				Write	–	–	15[5]	
Average operating current	I_{CC1}	Cycle time=1μs 100% duty, $\overline{CS1}$≤0.2V, CS2≥VIN≥Vcc-0.2V		Read	–	–	10[5]	mA
				Write	–	–	15[5]	
	I_{CC2}	Min cycle, 100% duty, IIO=0mA, $\overline{CS1}$=VIL, or CS2=VIH	Vcc=3.3V@100		–	–	55[4]	mA
			Vcc=2.7V@150		–	–	30	
			Vcc=2.2V@300		–	–	15	
Output low voltage	V_{OL}	I_{OL}	Vcc=3.0V	2.1mA	–	–	0.4	V
			Vcc=2.5V	0.5mA	–	–	0.4	
			Vcc=2.0V	0.33m	–	–	0.4	
Output high voltage	V_{OH}	I_{OH}	Vcc=3.0V	–1.0mA	2.4	–	–	V
			Vcc=2.5V	–0.5mA	2.0	–	–	
			Vcc=2.0V	–	1.6	–	–	
Standby Current(TTL)	I_{SB}	$\overline{CS1}$=VIH, or CS2=VIL			–	–	0.3	mA
Standby Current (CMOS)	KM68FS2000Z KM68FR2000Z	I_{SB1}	$\overline{CS1}$≥Vcc-0.2V CS2≥Vcc-0.2V or CS2≤0.2V, Other input =0~Vcc	Low Low Power	–	0.05	10[2]	μA
	KM68FS2000ZI KM68FR2000ZI			Low Low Power	–	0.05	10[2]	μA

1) –Commercial Product
   TA=0 to 70°C, Vcc=2.3V(Min) ~ 3.3V(Max) for 68FS2000Z Family, Vcc=1.8V(Min) ~ 2.7V(Max)V for 68FR2000Z Family
   –Industrial Product
   TA=–40 to 85°C, Vcc=2.3V(Min) ~ 3.3V(Max) for 68FS2000ZI Family, Vcc=1.8V(Min)~2.7V(Max) for 68FR2000ZI Family.
2) The value has difference by± 1μA.
   Measured at Vcc=3.3V(Max)
3) The value is not 100% tested but obtained statistically at Temp=25°C
4) –The value is measured at Vcc=3.0V±0.3V
   –Icc2=30mA with 120ns cycle at Vcc=2.5V±0.2V, but this value is not 100% tested but obtained statistically.
   –Icc2=15mA with 300ns cycle at Vcc=2.0V±0.2V, but this value is not 100% tested but obtained statistically.
5) The value is measured at Vcc=3.0V±0.3V

A.C OPERATING CONDITIONS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.0V, 2.5V
	0.4 to 1.8V	Vcc=2.0V
Input rising and falling time	5ns	–
Input and output reference voltage	1.5V	Vcc=3.0V
	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V
Output load (See right)	CL=100pF	See Test Condition #2
	CL=30pF	

* See test condition of DC Operating characteristics
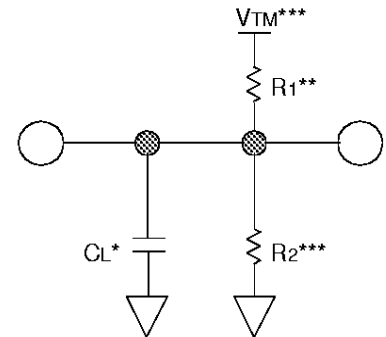
* Including scope and jig capacitance
**R1=3070Ω, R2=3150Ω
***V$_{TM}$=2.8V for Vcc = 3.0V/3.3V
2.3V for Vcc = 2.5V
1.8V for Vcc = 2.0V

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM68FR2000Z	0~70°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Commercial
KM68FS2000Z	0~70°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	
KM68FR2000ZI	–40~85°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Industrial
KM68FS2000ZI	–40~85°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	

* The parameters is measured with 30pF test load

AC CHARACTERISTICS

| Parameter List		Symbol	Speed Bins						Units
			100ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	100	–	150	–	300	–	ns
	Address access time	tAA	–	100	–	150	–	300	ns
	Chip select to output	tCO1	–	100	–	150	–	300	ns
	Output enable to valid output	tOE	–	50	–	75	–	150	ns
	Chip select to low-Z output	tLZ1,tLZ2	10	–	20	–	50	–	ns
	Output enable to low-Z output	tOLZ	5	–	10	–	30	–	ns
	Chip disable to high-Z output	tHZ1,tHZ2	0	30	0	40	0	60	ns
	Output enable to high-Z output	tOHZ	0	30	0	40	0	60	ns
	Output hold from address change	tOH	15	–	15	–	30	–	ns
Write	Write cycle time	tWC	100	–	150	–	300	–	ns
	Chip select to end of write	tCW	80	–	120	–	300	–	ns
	Address set-up time	tAS	0	–	0	–	0	–	ns
	Address valid to end of write	tAW	80	–	120	–	300	–	ns
	Write pulse width	tWP	70	–	100	–	200	–	ns
	Write recovery	tWR	0	–	0	–	0	–	ns
	Write to output high-Z	tWHZ	0	30	0	40	0	60	ns
	Data to write time overlap	tDW	40	–	60	–	120	–	ns
	Data hold from write time	tDH	0	–	0	–	0	–	ns
	End write to output low-Z	tOW	5	–	5	–	20	–	ns

DATA RETENTION CHARACTERISTICS

| Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	VDR	$\overline{CS}1$***$\geq$Vcc-0.2V		1.5	–	3.6	V
Data retention current	IDR	Vcc=3.0V, $\overline{CS}1\geq$Vcc-0.2V	Low Low Power	–	0.05	10	μA
Data retention set-up time	tSDR	See data retention waveform		0	–	–	ns
Recovery time	tRDR			tRC	–	–	

* 1) Commercial Product : TA=0 to 70°C, unless otherwise specified
  2) Industrial Product : TA=-40 to 85°C, unless otherwise specified
** TA=25°C, the value is too small to detect by test machine, 0.01μA statistically
*** $\overline{CS}1 \geq$Vcc-2.0V, CS2$\geq$Vcc-2.0V($\overline{CS}1$ controlled) or CS2$\leq$2.0V(CS2 controlled)

DATA RETENTION WAVE FORM

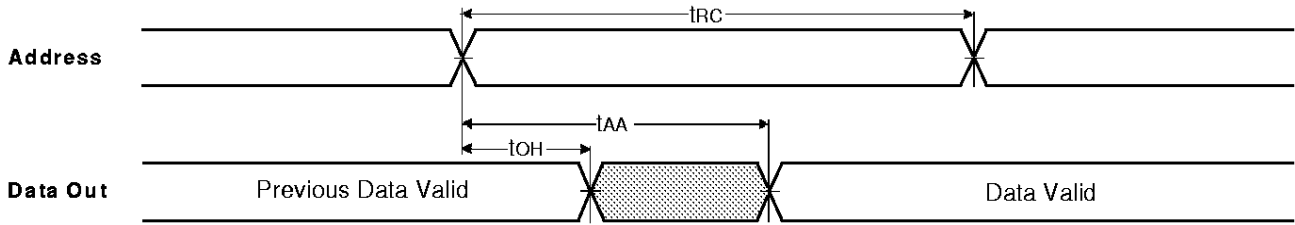### 1) $\overline{CS}1$ controlled
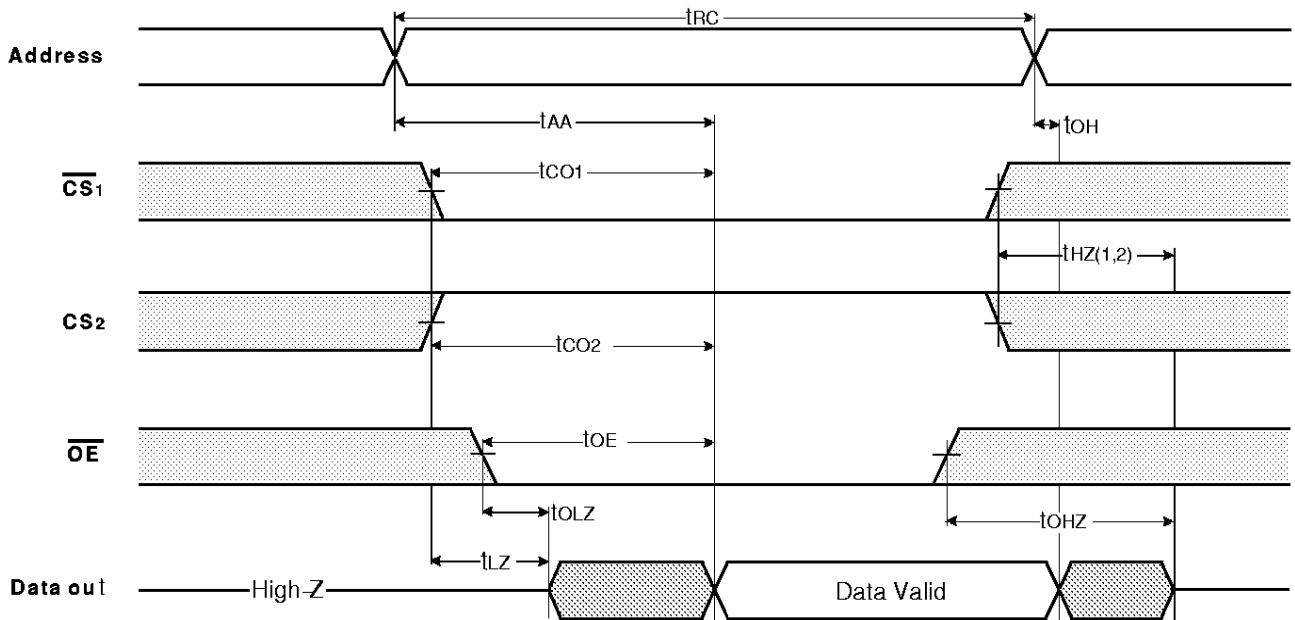

2) CS2 controlled

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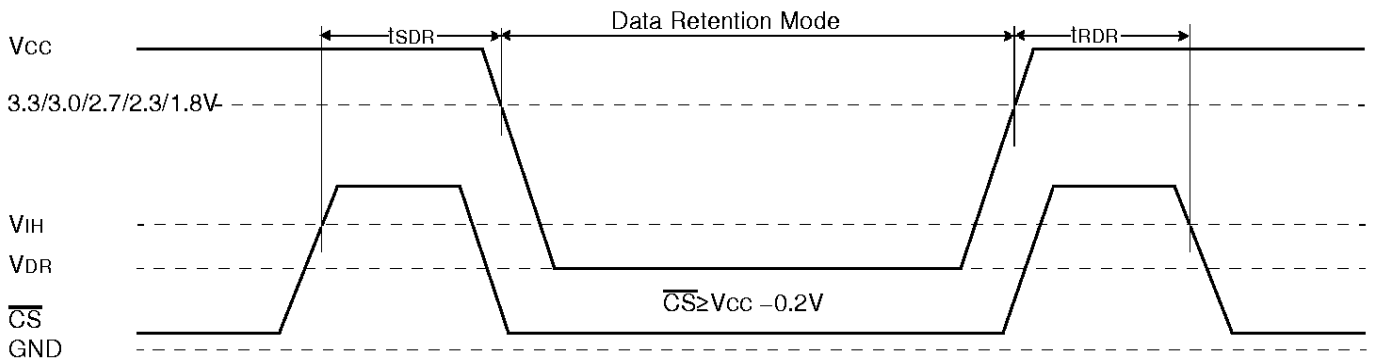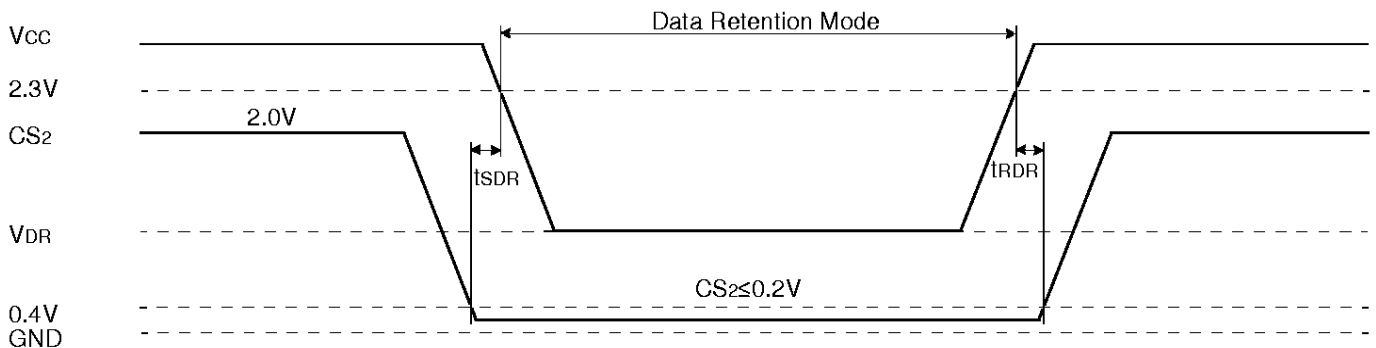
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}_1=\overline{OE}=V_{IL}$, $CS_2=V_{IH}$, $\overline{WE}=V_{IL}$)


### TIMING WAVEFORM OF READ CYCLE(2)($\overline{WE}=V_{IH}$)

NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
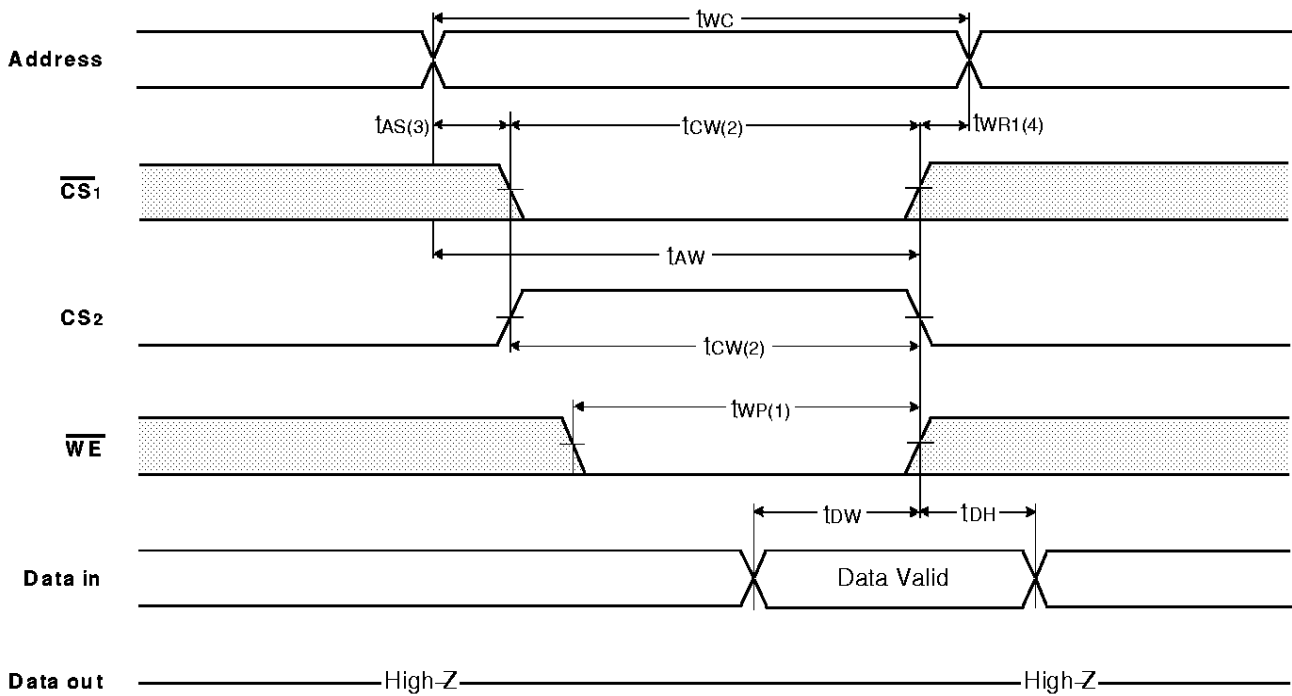
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled)
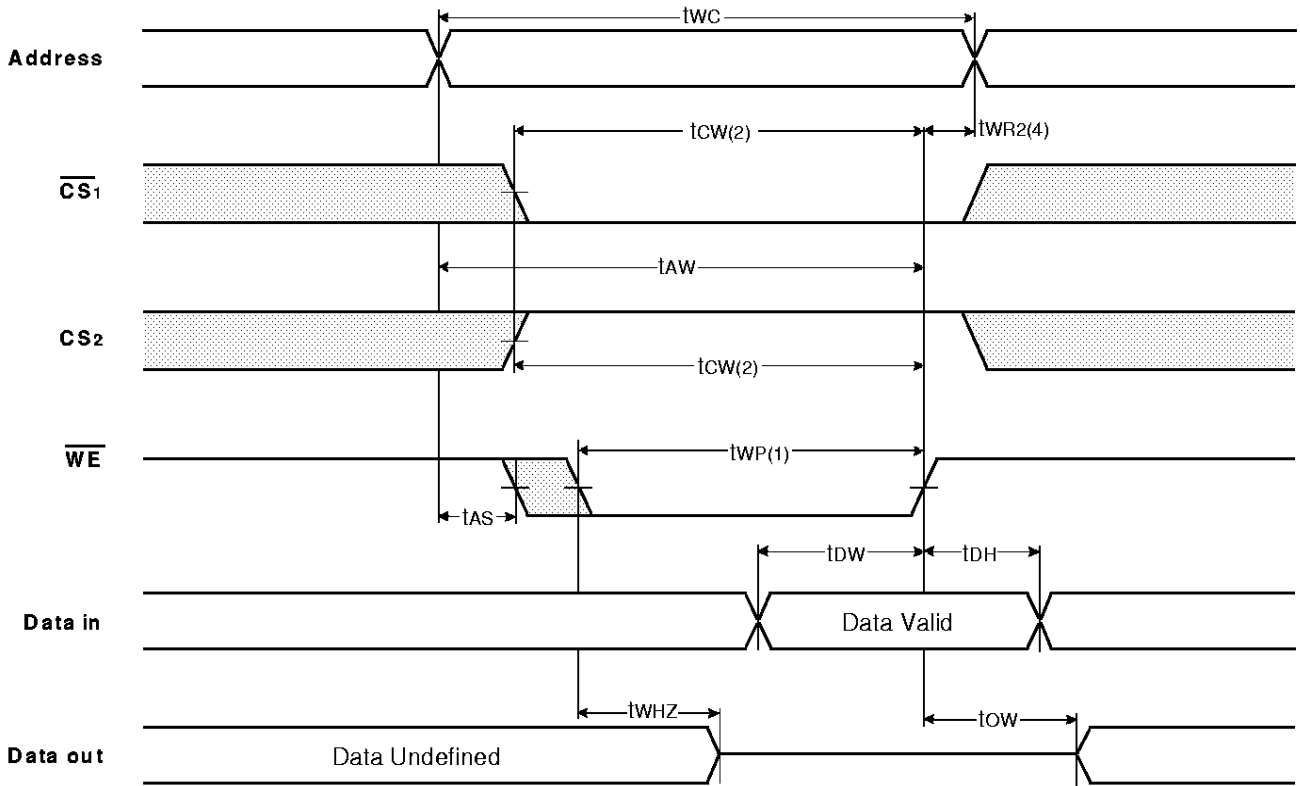
TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}_1$ Controlled)

LECTRONICS
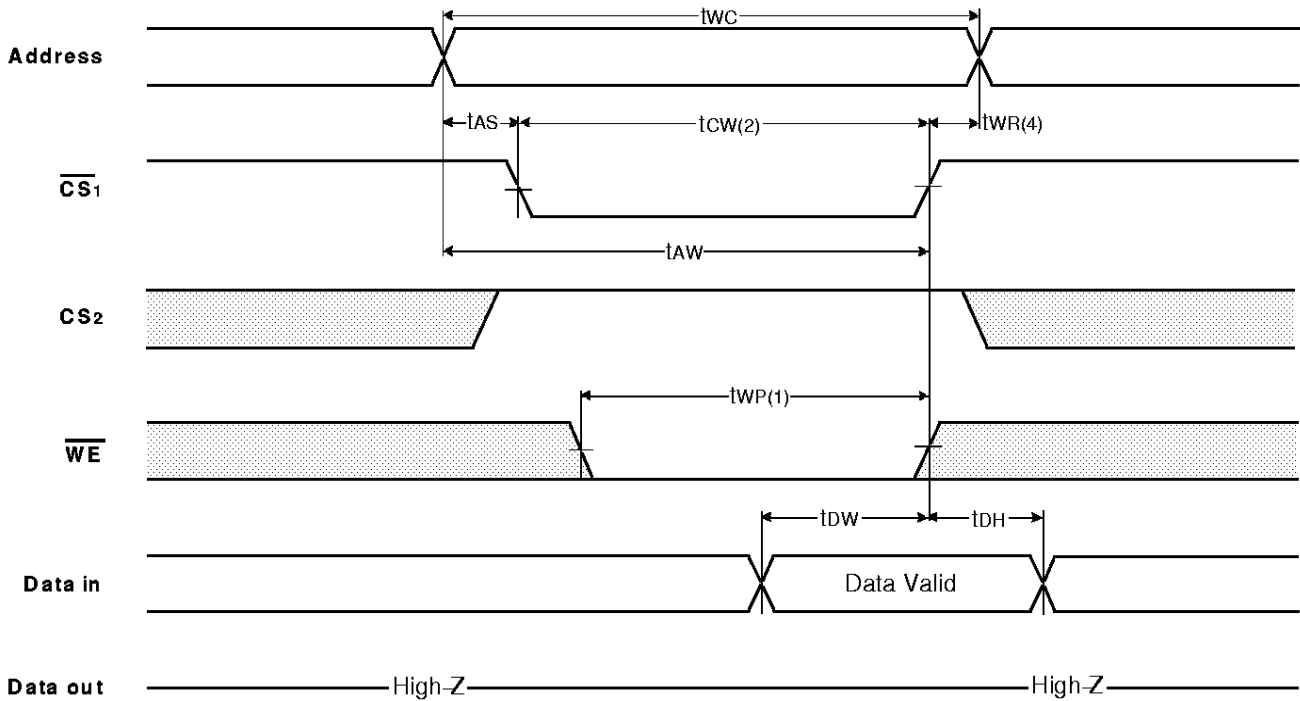
TIMING WAVEFORM OF WRITE CYCLE(3)(CS2 Controlled)

NOTES (WRITE CYCLE)

1. A write occurs during the overlap of low $\overline{CS_1}$ and high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS_1}$ going high ,CS2 going low and $\overline{WE}$ going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of $\overline{CS_1}$ going low or CS2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end or write to the address change. tWR1 applied in case a write ends at $\overline{CS_1}$ or $\overline{WE}$ going high, tWR2 applied in case a write ends at CS2 going to low.
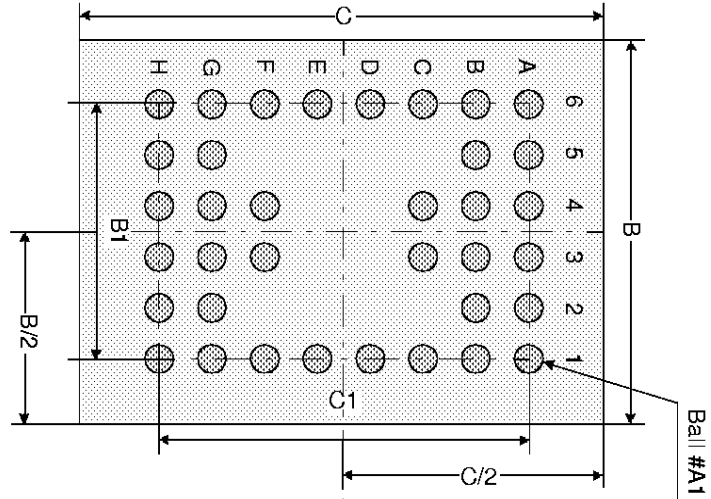
FUNCTIONAL DESCRIPTION

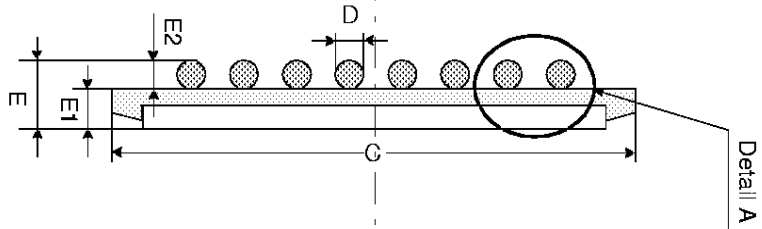| $\overline{CS_1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O$_{1\sim8}$	Current Mode
H	X*	X	X	Power Down	High-Z	I$_{SB}$
X	L	X	X	Power Down	High-Z	I$_{SB}$,I$_{SB1}$
L	H	H	H	Output Disable	High-Z	I$_{CC}$
L	H	H	L	Read	Dout	I$_{CC}$
L	H	L	X	Write	Din	I$_{CC}$

* X means do not care (high or low)

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PACKAGE DIMENSIONS (Units : mm)
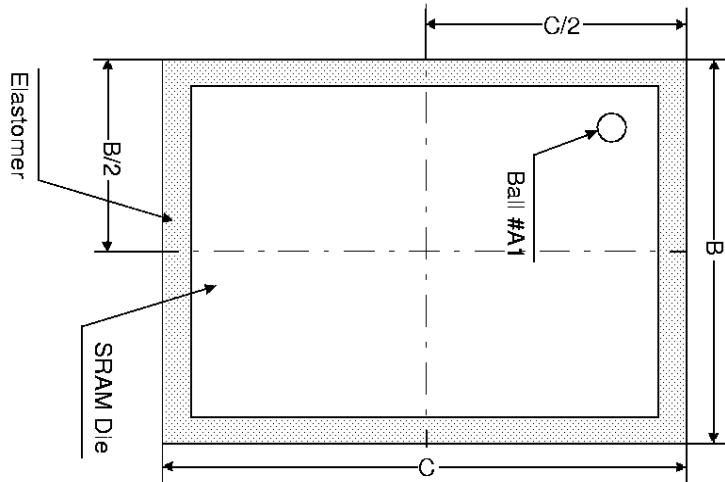
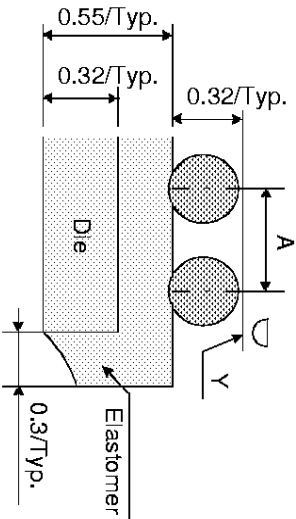|	Min	Typ	Max
A	–	0.75	–
B	6.10	6.20	6.30
B1	–	3.75	–
C	13.65	13.75	13.85
C1	–	5.25	–
D	0.30	0.35	0.40
E	–	0.80	0.81
E1	–	0.55	–
E2	–	0.25	–
Y	–	–	0.08

Bottom View

Side View

Top View

Detail A

Ball #A1

SRAM Die

Elastomer

Die

Notes.
1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

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