

February 2013

FDMC8321L

N-Channel Power Trench® MOSFET 40 V, 49 A, 2.5 m Ω

Features

- Max $r_{DS(on)} = 2.5 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 22 \text{ A}$
- Max $r_{DS(on)}$ = 4.1 m Ω at V_{GS} = 4.5 V, I_D = 18 A

Top

- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- Next Generation enhanced body diode technology, engineered for soft recovery
- 100% UIL tested
- RoHS Compliant



General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or convertional switching PWM contollers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed body diode reverse recovery performance.

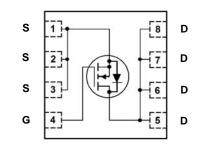
Applications

- Synchronous rectifier
- Load switch/Orring
- Motor switch





Bottom



Power 33

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Paramete	er		Ratings	Units
V _{DS}	Drain to Source Voltage			40	V
V _{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C		49	
I _D	-Continuous	T _A = 25 °C	(Note 1a)	22	Α
	-Pulsed			100	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	86	mJ
Б	Power Dissipation	T _C = 25 °C		40	w
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Temperatu	ire Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8321L	FDMC8321L	Power33	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		22		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V			1	μΑ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		-5		mV/°C
	r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 22 \text{ A}$		1.9	2.5	
r _{DS(on)}		$V_{GS} = 4.5 \text{ V}, I_D = 18 \text{ A}$		2.7	4.1	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 22 \text{ A}, T_J = 125 \text{ °C}$		2.8	3.7	
g _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 22 \text{ A}$		114		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		2930	3900	pF
C _{oss}	Output Capacitance			1000	1330	pF
C _{rss}	Reverse Transfer Capacitance			60	90	pF
R_g	Gate Resistance		0.1	0.7	2.5	Ω

Switching Characteristics

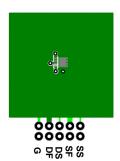
t _{d(on)}	Turn-On Delay Time		12	22	ns
t _r	Rise Time	$V_{DD} = 20 \text{ V}, I_D = 22 \text{ A},$	6.1	12	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_{GEN} = 6 Ω	32	51	ns
t _f	Fall Time		4.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V _{DD} = 20 V, I _D = 22 A	44	61	nC
$Q_{g(TOT)}$	Total Gate Charge at 5 V		21	32	nC
Q _{gs}	Total Gate Charge		7.7		nC
Q_{gd}	Gate to Drain "Miller" Charge		5.8		nC

Drain-Source Diode Characteristics

\/	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	0.69	1.2	\/
V _{SD} Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 22 \text{ A}$	(Note 2)	0.77	1.3	V	
t _{rr}	Reverse Recovery Time	I _F = 22 A, di/dt = 100 A/μs		41	65	ns
Q _{rr}	Reverse Recovery Charge			20	33	nC
NI 4						

Notes:

1. R_{BJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



53 °C/W when mounted on a 1 in² pad of 2 oz copper



125 °C/W when mounted on a minimum pad of 2 oz copper

^{2.} Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.

^{3.}Starting T $_{J}$ = 25 $^{\circ}\text{C};$ N-ch: L = 0.3 mH, I $_{AS}$ = 24 A, V $_{DD}$ = 36 V, V $_{GS}$ = 10 V.

Typical Characteristics $T_J = 25$ °C unless otherwise noted

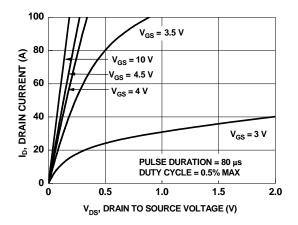


Figure 1. On Region Characteristics

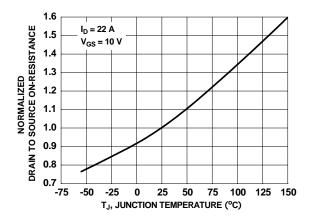


Figure 3. Normalized On Resistance vs Junction Temperature

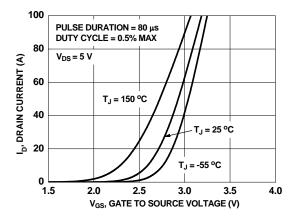


Figure 5. Transfer Characteristics

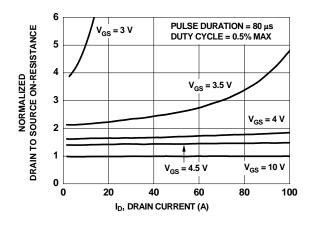


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

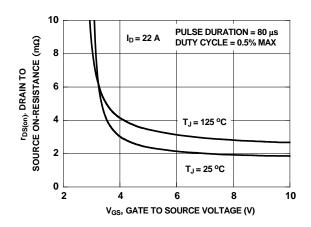


Figure 4. On-Resistance vs Gate to Source Voltage

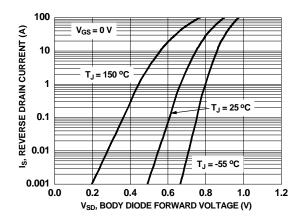


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

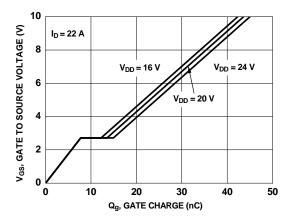


Figure 7. Gate Charge Characteristics

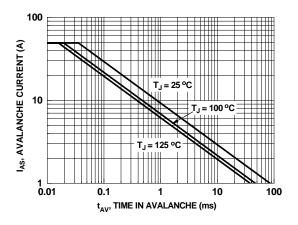


Figure 9. Unclamped Inductive Switching Capability

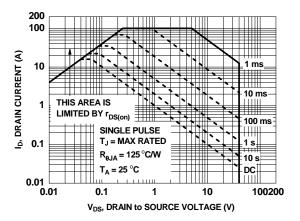


Figure 11. Forward Bias Safe Operating Area

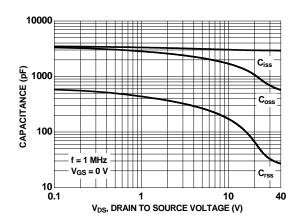


Figure 8. Capacitance vs Drain to Source Voltage

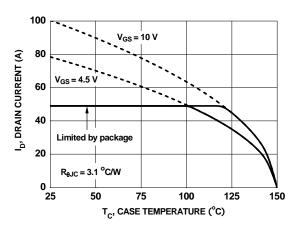


Figure 10. Maximum Continuous Drain Current vs Case Temperature

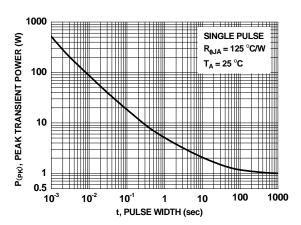


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

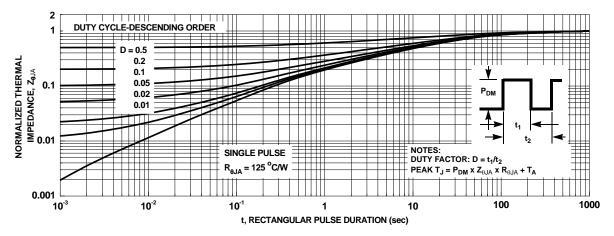
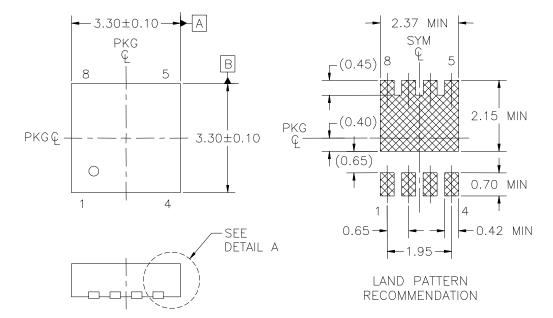
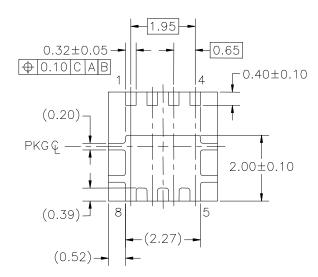
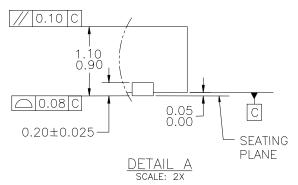


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout







PQFN08BREV1

NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08BREV1





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