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AK5702

4-Channel ADC with PLL & MIC-AMP

GENERAL DESCRIPTION

The AK5702 features a 4-channel ADC. Input circuits include a Microphone-Amplifier with programmable gain and an ALC (Auto Level Control) circuit, making it ideal for consumer microphone array applications. On-chip PLL and TDM audio format makes it easy to connect with DSP. The AK5702 has a software compatibility with stereo version, AK5701.

FEATURES

1. **Recording Function**
   - **4-Channel ADC**
   - **3:1 Stereo Input Selector**
   - **Full-differential or Single-ended Input**
   - **MIC Amplifier (+36dB/+30dB/+15dB/0dB)**
   - **Input Voltage: 1.8Vpp@AVDD=3.0V (= 0.6 x AVDD)**
   - **ADC Performance:**
     S/(N+D): 83dB, DR, S/N: 89dB@MGAIN=0dB
     S/(N+D): 83dB, DR, S/N: 87dB@MGAIN=+15dB
   - **Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)**
   - **Digital ALC**
   - **Input Digital Volume (+36dB ~ –54dB, 0.375dB Step, Mute)**
2. **Sampling Rate:**
   - **PLL Slave Mode (LRCK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (BCLK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (MCKI pin):**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **PLL Master Mode:**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **EXT Slave Mode:**
     7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs),
     7.35kHz ~ 13kHz (1024fs)
3. **PLL Input Clock:**
   - **MCKI pin:**
     27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz
   - **LRCK pin: 1fs**
   - **BCLK pin: 32fs/64fs**
4. **Master/Slave mode**
5. **Audio Interface Format: MSB First, 2's complement**
   - **DSP Mode, 16bit MSB justified, I^2S**
   - **Cascade TDM interface**
6. **μP I/F: 3-wire Serial or I2C Bus (Ver 1.0, 400kHz Mode)**
7. **Power Supply:**
   - **AVDD: 2.4 ~ 3.6V**
   - **DVDD: 1.6 ~ 3.6V (Stereo Mode)**
   - **DVDD: 2.0 ~ 3.6V (TDM128 Mode, 16bit x 8ch)**
   - **DVDD: 2.7 ~ 3.6V (TDM256 Mode, 32bit x 8ch)**
8. **Power Supply Current: 13 mA (EXT Slave Mode)**
9. **Ta = –30 ~ 85°C**
10. **Package: 32pin QFN (5mm x 5mm)**
11. **Register Compatible with AK5701**

■ Block Diagram

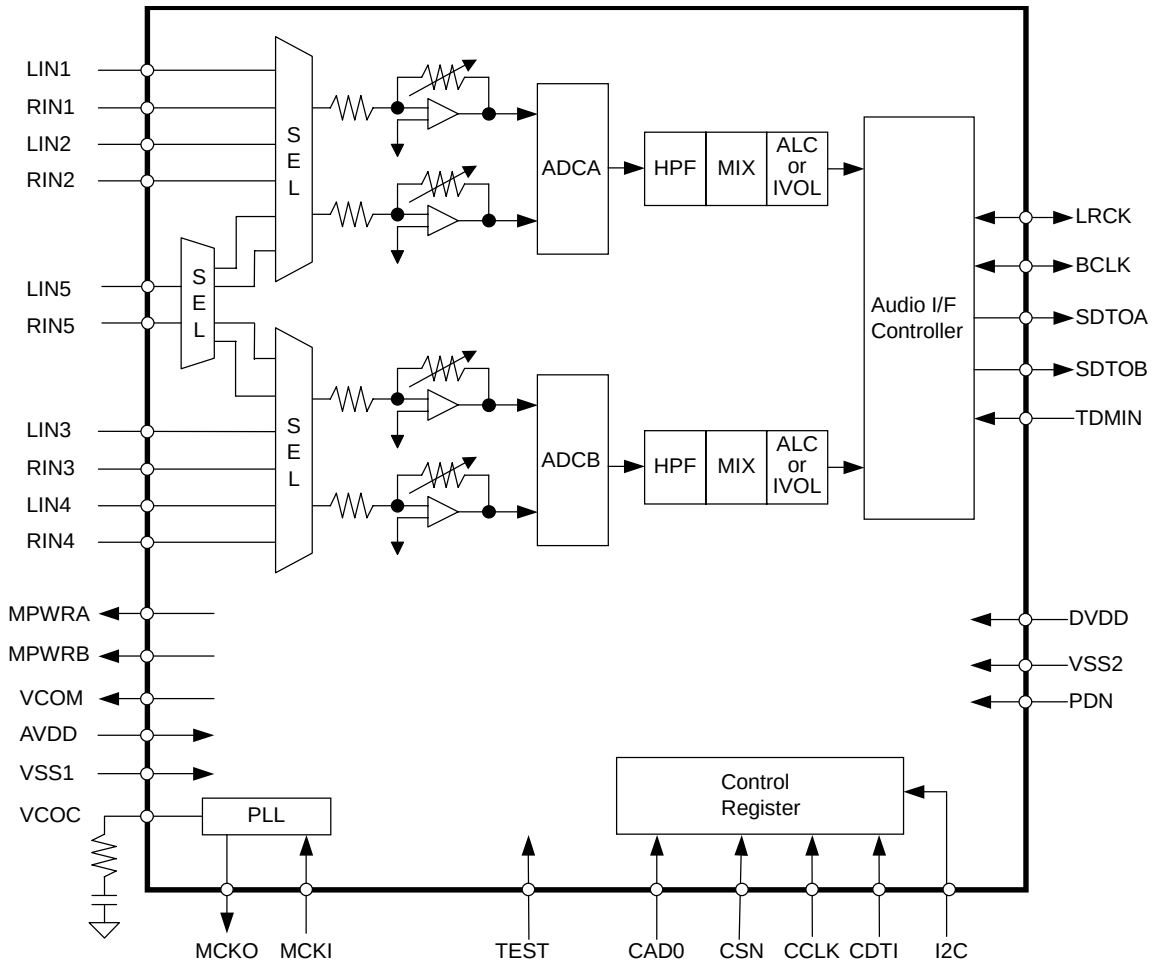
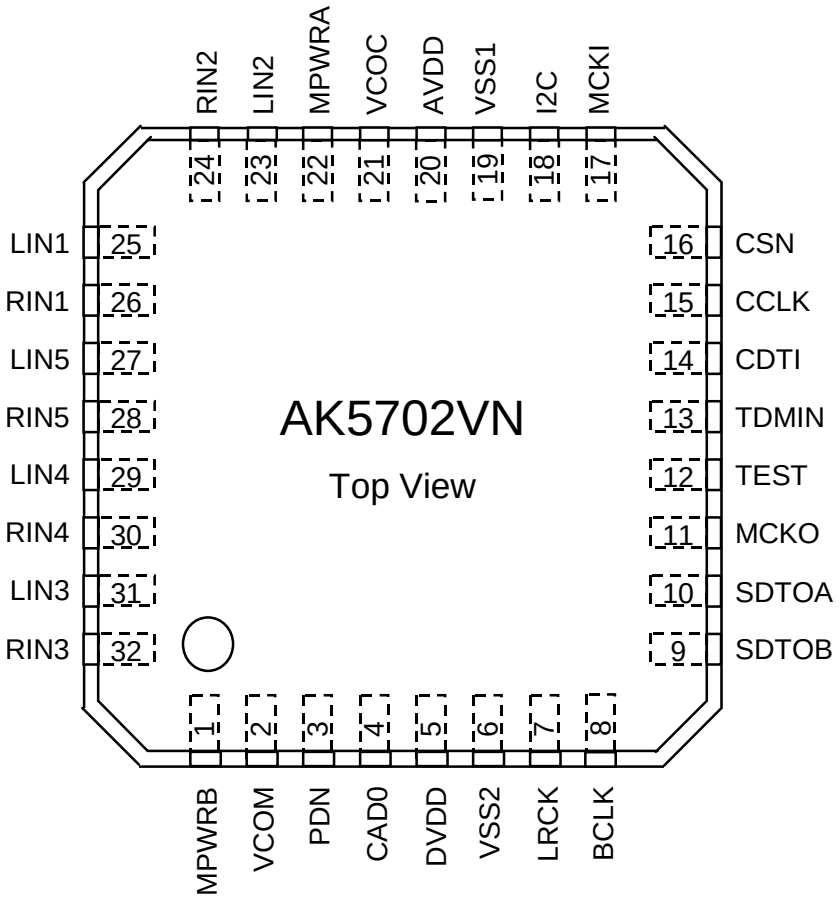


Figure 1. Block Diagram

■ Ordering Guide

AK5702VN	–30 ~ +85°C	32pin QFN (0.5mm pitch)
AKD5702	Evaluation board for AK5702	

■ Pin Layout



■ Comparison with AK5701

Function	AK5701	AK5702
# of ADC channel	2	4
Input Selector	2 stereo	3:1
Cascade TDM interface	No	Yes
Bypass mode	Yes	No
uP I/F	3-wire	3-wire or I2C
Package	24pin QFN (4mm x 4mm)	32pin QFN (5mm x 5mm)

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MPWRB	O	MIC Power Supply Pin
2	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs.
3	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initializes the control register.
4	CAD0	I	Chip Address 0 Pin
5	DVDD	-	Digital Power Supply Pin, 1.6 ~ 3.6V
6	VSS2	-	Digital Ground Pin
7	LRCK	I/O	Input / Output Channel Clock Pin
8	BCLK	I/O	Audio Serial Data Clock Pin
9	SDTOB	O	ADCB/TDM Audio Serial Data Output Pin
10	SDTOA	O	ADCA Audio Serial Data Output Pin
11	MCKO	O	Master Clock Output Pin
12	TEST	I	Test Pin This pin should be connected to the ground.
13	TDMIN	I	TDM Data Input Pin
14	CDTI	I	Control Data Input Pin (I2C pin = "L": 3-wire Serial Mode)
	SDA	I/O	Control Data Input Pin (I2C pin = "H": I^2C Bus Mode)
15	CCLK	I	Control Data Clock Pin (I2C pin = "L": 3-wire Serial Mode)
	SCL	I	Control Data Clock Pin (I2C pin = "H": I^2C Bus Mode)
16	CSN	I	Chip Select Pin (I2C pin = "L": 3-wire Serial Mode)
	CAD1	I	Chip Address 1 Select Pin (I2C pin = "H": I^2C Bus Mode)
17	MCKI	I	External Master Clock Input Pin
18	I2C	I	Control Mode Select Pin "H": I2C, "L": 3-wire serial
19	VSS1	-	Analog Ground Pin
20	AVDD	-	Analog Power Supply Pin, 2.4 ~ 3.6V
21	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to VSS1 with one resistor and capacitor in series.
22	MPWRA	O	MIC Power Supply Pin
23	LIN2	I	Lch Analog Input 2 Pin (MDIFA2 bit = "0": Single-ended Input)
	RINA–	I	Rch Negative Input A Pin (MDIFA2 bit = "1": Full-differential Input)
24	RIN2	I	Rch Analog Input 2 Pin (MDIFA2 bit = "0": Single-ended Input)
	RINA+	I	Rch Positive Input A Pin (MDIFA2 bit = "1": Full-differential Input)
25	LIN1	I	Lch Analog Input 1 Pin (MDIFA1 bit = "0": Single-ended Input)
	LINA+	I	Lch Positive Input A Pin (MDIFA1 bit = "1": Full-differential Input)
26	RIN1	I	Rch Analog Input 1 Pin (MDIFA1 bit = "0": Single-ended Input)
	LINA–	I	Lch Negative Input A Pin (MDIFA1 bit = "1": Full-differential Input)
27	LIN5	I	Lch Analog Input 5 Pin (INA5L bit or INB5L bit = "1": Single-ended Input)
28	RIN5	I	Rch Analog Input 5 Pin (INA5R bit or INB5R bit = "1": Single-ended Input)
29	LIN4	I	Lch Analog Input 4 Pin (MDIFB1 bit = "0": Single-ended Input)
	RINB-	I	Rch Negative Input B Pin (MDIFB1 bit = "1": Full-differential Input)
30	RIN4	I	Rch Analog Input 4 Pin (MDIFB1 bit = "0": Single-ended Input)
	RINB+	I	Rch Positive Input B Pin (MDIFB1 bit = "1": Full-differential Input)
31	LIN3	I	Lch Analog Input 3 Pin (MDIFB2 bit = "0": Single-ended Input)
	LINB+	I	Lch Positive Input B Pin (MDIFB2 bit = "1": Full-differential Input)
32	RIN3	I	Rch Analog Input 3 Pin (MDIFB2 bit = "0": Single-ended Input)
	LINB-	I	Lch Negative Input B Pin (MDIFB2 bit = "1": Full-differential Input)

Note 1. All input pins except analog input pins (LIN1-5, RIN1-5) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWRA, MPWRB, VCOC, LIN1/LINA+, RIN1/LINA−, LIN2/RINA−, RIN2/RINA+, LIN3/LINB+, RIN3/LINB−, LIN4/RINB−, RIN4/RINB+, RIN5, LIN5	These pins should be open.
Digital	SDTOA, SDTOB, MCKO	These pins should be open.
	MCKI, TDMIN	This pin should be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1, VSS2=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	−0.3	4.6	V
	Digital	DVDD	−0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	−0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	−30	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 3. LIN1/LINA+, RIN1/LINA−, LIN2/RINA−, RIN2/RINA+, LIN3/LINB+, RIN3/LINB−, LIN4/RINB−, RIN4/RINB+, LIN5/RIN5 pins
Note 4. PDN, CSN/CAD1, CCLK/SCL, CDTI/SDA, MCKI, LRCK, BCLK, TEST, TDMIN, I2C, CAD0 pins
Pull-up resistors at SDA and SCL pins should be connected to (DVDD+0.3) V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1, VSS2=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	2.4	3.0	3.6	V
(Note 5)	Digital (Stereo mode)	DVDD	1.6	3.0	AVDD	V
	(TDM128 mode)		2.0	3.0	AVDD	V
	(TDM256 mode)		2.7	3.0	AVDD	V

Note 2. All voltages with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 5. The power-up sequence between AVDD and DVDD is not critical. When only AVDD is powered OFF (Hi_Z or L), it should be done after the PDN pin = “L” or all power management bits (PMADAL, PMADAR, PMADBL, PMADBR, PMVCM, PMPLL, PMMPA, PMMPB) = “0”. DVDD should not be powerd OFF while AVDD is powered ON.

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=3.0V; VSS1, VSS2=0V; EXT Slave Mode; MCKI=11.2896MHz, fs=44.1kHz, BCLK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
MIC Amplifier: LIN1-5, RIN1-5 pins; MDIFA1-2 = MDIFB1-2 bits = "00" (Single-ended inputs)					
Input Resistance	LIN1-4, RIN1-4 pins				
	MGAIN1-0 bits = "00"	40	60	80	kΩ
	MGAIN1-0 bits = "01", "10" or "11"	20	30	40	kΩ
	LIN5, RIN5 pin				
	MGAIN1-0 bits = "00"	20	30	40	kΩ
	MGAIN1-0 bits = "01", "10" or "11" (Note 6)	10		27	kΩ
Gain	MGAIN1-0 bits = "00"	-	0	-	dB
	MGAIN1-0 bits = "01"	-	+15	-	dB
	MGAIN1-0 bits = "10"	-	+30	-	dB
	MGAIN1-0 bits = "11"	-	+36	-	dB
MIC Amplifier: LINA+/–, RINA+/–, LINB+/–, RINB+/– pins; MDIFA1-2 = MDIFB1-2 bits = "11" (Full-differential input)					
Input Voltage (Note 7)	MGAIN=+36dB	-	-	0.033	Vpp
	MGAIN=+30dB	-	-	0.066	Vpp
	MGAIN=+15dB	-	-	0.37	Vpp
	MGAIN=0dB	-	-	2.07	Vpp
MIC Power Supply: MPWRA, MPWRB pins					
Output Voltage (Note 8)		2.02	2.25	2.48	V
Load Resistance		0.5	-	-	kΩ
Load Capacitance		-	-	30	pF
ADC Analog Input Characteristics: LIN1-5, RIN1-5 pins (Single-ended inputs) → ADC → IVOL, MGAIN=+15dB, IVOL=0dB, ALC=OFF					
Resolution		-	-	16	Bits
Input Voltage (Note 9)	MGAIN=+36dB	-	0.028	-	Vpp
	MGAIN=+30dB	-	0.057	-	Vpp
	MGAIN=+15dB	0.27	0.32	0.37	Vpp
	MGAIN=0dB	1.53	1.80	2.07	Vpp
S/(N+D) (–0.5dBFS) (Note 10)		73	83	-	dB
D-Range (–60dBFS, A-weighted) (Note 11)		79	87	-	dB
S/N (A-weighted) (Note 11)		79	87	-	dB
Interchannel Isolation (Note 12)		80	90	-	dB
Interchannel Gain Mismatch	MGAIN=+36dB	-	0.2	-	dB
	MGAIN=+30dB	-	0.2	-	dB
	MGAIN=+15dB	-	0.2	1.0	dB
	MGAIN=0dB	-	0.2	0.5	dB
Power Supplies:					
Power Supply Current					
Power Up (PDN pin = "H") (Note 13)					
AVDD			10	15	mA
DVDD			3	5	mA
Power Down (PDN pin = "L") (Note 14)					
AVDD			1	100	μA
DVDD			1	100	μA

Note 6. When MGAIN1-0 bits = "01", "10", "11", the input resistance of typical refer to Table 24.

Note 7. The voltage difference between LIN+/RIN+ and LIN–/RIN– pins. AC coupling capacitor should be inserted in series at each input pin. Maximum input voltage of LINA+/–, RINA+/–, LINB+/– and RINB+/– pins is proportional to AVDD voltage, respectively. Vin = |(L/RIN+) – (L/RIN–)| = 0.123 x AVDD

Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ).

Note 9. Input voltage is proportional to AVDD voltage. Vin = 0.107 x AVDD (typ)@MGAIN1-0 bits = "01" (+15dB), Vin = 0.6 x AVDD (typ)@MGAIN1-0 bits = "00" (0dB).
Note 10. 83dB(typ)@MGAIN=0dB, 72dB(typ)@MGAIN=+30dB, 66dB (typ) @MGAIN=+36dB
Note 11. 89dB(typ)@MGAIN=0dB, 77dB(typ)@MGAIN=+30dB, 70dB (typ) @MGAIN=+36dB
Note 12. 100dB(typ)@MGAIN=0dB, 80dB(typ)@MGAIN=+30dB, 80dB(typ) @MGAIN=+36dB
Note 13. EXT Slave Mode (MCKI=11.2896MHz), PMADAL = PMADAR = PMADBL = PMADBR = PMVCM = PMMPA = PMMPB bits = "1" and PMPLL = M/S = MCKO bit = "0". MPWRA/B pins outputs 0mA.
PLL Master Mode (PMPLL = M/S = MCKO bits = "1"): AVDD= 11.0 mA(typ), DVDD= 3.5 mA(typ).
Note 14. All digital input pins are fixed to DVDD or VSS2.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V; fs=44.1kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 15)	±0.1dB	PB	0	-	17.4	kHz
	−1.0dB		-	20.0	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband (Note 15)		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	65	-	-	dB
Group Delay (Note 16)		GD	-	18	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFA1-0 = HPFB1-0 bits = "00"						
Frequency Response (Note 15)	−3.0dB	FR	-	3.4	-	Hz
	−0.5dB		-	10	-	Hz
	−0.1dB		-	22	-	Hz

Note 15. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=20kHz= 0.454*fs (@−1.0dB). Each response refers to that of 1kHz.
Note 16. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF.

DC CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage						
2.2V≤ DVDD ≤3.6V		VIH	70%DVDD	-	-	V
1.6V≤ DVDD <2.2V		VIH	80%DVDD	-	-	V
Low-Level Input Voltage						
2.2V≤ DVDD ≤3.6V		VIL	-	-	30%DVDD	V
1.6V≤ DVDD <2.2V		VIL	-	-	20%DVDD	V
High-Level Output Voltage	(Iout= −200μA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage						
Except SDA pin	(Iout= 200μA)	VOL	-	-	0.2	V
SDA pin, 2.0V≤DVDD≤3.6V	(Iout= 3mA)	VOL	-	-	0.4	V
SDA pin, 1.6V≤DVDD<2.0V	(Iout= 3mA)	VOL	-	-	20%DVDD	V
Input Leakage Current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 - 3.6V (Note 17); C_L=20pF; unless otherwise specified)

Parameter		Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
Stereo DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Stereo I2S, MSB Justified Mode: Duty Cycle		Duty	-	50	-	%
TDM128 Mode: Pulse Width High		tLRCKH	-	1/(8fs)	-	ns
TDM256 Mode: Pulse Width High		tLRCKH	-	1/(8fs)	-	ns
BCLK Output Timing						
Period	BCKO1-0 bit = "01"	tBCK	-	1/(32fs)	-	ns
	BCKO1-0 bit = "10"	tBCK	-	1/(64fs)	-	ns
	TDM1-0 bit = "01"	tBCK	-	1/(128fs)	-	ns
	TDM1-0 bit = "11"	tBCK	-	1/(256fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Stereo DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs – tBCK	ns
Stereo I2S, MSB Justified Mode: Duty Cycle		Duty	45	-	55	%
TDM128 Mode: Pulse Width High		tLRCKH	-	1/(128fs)	-	ns
TDM256 Mode: Pulse Width High		tLRCKH	-	1/(256fs)	-	ns
BCLK Input Timing						
Period	Stereo DSP Mode	tBCK	1/(64fs)	-	1/(32fs)	ns
	Stereo I2S, MSB Justified Mode	tBCK	1/(64fs)	-	1/(32fs)	ns
	TDM128 Mode	tBCK	-	1/(128fs)	-	ns
	TDM256 Mode	tBCK	-	1/(256fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Note 17. The voltage range of DVDD depends on the audio interface mode
Stereo Mode: DVDD = 1.6 ~ 3.6V
TDM128 Mode: DVDD = 2.0 ~ 3.6V
TDM256 Mode: DVDD = 2.7 ~ 3.6V

Parameter			Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = LRCK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
DSP Mode: Pulse Width High			tLRCKH	tBCK−60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle			Duty	45	-	55	%
BCLK Input Timing							
Period			tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High			tBCKH	0.4 x tBCK	-	-	ns
PLL Slave Mode (PLL Reference Clock = BCLK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
DSP Mode: Pulse Width High			tLRCKH	tBCK−60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle			Duty	45	-	55	%
BCLK Input Timing							
Period	PLL3-0 bits = “0010”		tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = “0011”		tBCK	-	1/(64fs)	-	ns
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High			tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	12.288	MHz
	512fs		fCLK	3.7632	-	13.312	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing							
Frequency	256fs		fs	7.35	-	48	kHz
	512fs		fs	7.35	-	26	kHz
	1024fs		fs	7.35	-	13	kHz
Stereo DSP Mode: Pulse Width High			tLRCKH	tBCK−60	-	1/fs – tBCK	ns
Stereo I2S, MSB Justified Mode: Duty Cycle			Duty	45	-	55	%
TDM128 Mode: Pulse Width High			tLRCKH	-	1/(128fs)	-	ns
TDM256 Mode: Pulse Width High			tLRCKH	-	1/(256fs)	-	ns
BCLK Input Timing							
Period		Stereo Mode	tBCK	312.5	-	-	ns
		TDM Mode	tBCK	78	-	-	ns
Pulse Width Low		Stereo Mode	tBCKL	130	-	-	ns
		TDM Mode	tBCKL	32	-	-	ns
Pulse Width High		Stereo Mode	tBCKH	130	-	-	ns
		TDM Mode	tBCKH	32	-	-	ns

Parameter			Symbol	min	typ	max	Units
External Master Mode							
MCKI Input Timing							
	Frequency	256fs	fCLK	1.8816	-	12.288	MHz
		512fs	fCLK	3.7632	-	13.312	MHz
		1024fs	fCLK	7.5264	-	13.312	MHz
	Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
	Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
	Frequency		fs	7.35	-	48	kHz
	Stereo DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
	Stereo I2S, MSB Justified Mode: Duty Cycle		Duty	-	50	-	%
	TDM128 Mode: Pulse Width High		tLRCKH	-	1/(8fs)	-	ns
	TDM256 Mode: Pulse Width High		tLRCKH	-	1/(8fs)	-	ns
BCLK Output Timing							
	Period	BCKO1-0 bit = "01"	tBCK	-	1/(32fs)	-	ns
		BCKO1-0 bit = "10"	tBCK	-	1/(64fs)	-	ns
		TDM1-0 bit = "01"	tBCK	-	1/(128fs)	-	ns
		TDM1-0 bit = "11"	tBCK	-	1/(256fs)	-	ns
	Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (Stereo DSP Mode)					
Master Mode					
LRCK "↑" to BCLK "↑" (Note 18)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
LRCK "↑" to BCLK "↓" (Note 19)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
BCLK "↑" to SDTO (BCKP bit = "0")	tBSD	–70	-	70	ns
BCLK "↓" to SDTO (BCKP bit = "1")	tBSD	–70	-	70	ns
Slave Mode					
LRCK "↑" to BCLK "↑" (Note 18)	tLRB	0.4 x tBCK	-	-	ns
LRCK "↑" to BCLK "↓" (Note 19)	tLRB	0.4 x tBCK	-	-	ns
BCLK "↑" to LRCK "↑" (Note 18)	tBLR	0.4 x tBCK	-	-	ns
BCLK "↓" to LRCK "↑" (Note 19)	tBLR	0.4 x tBCK	-	-	ns
BCLK "↑" to SDTO (BCKP bit = "0")	tBSD	-	-	80	ns
BCLK "↓" to SDTO (BCKP bit = "1")	tBSD	-	-	80	ns
Audio Interface Timing (Left justified & I^2S)					
Master Mode					
BCLK "↓" to LRCK Edge (Note 20)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	–70	-	70	ns
BCLK "↓" to SDTO	tBSD	–70	-	70	ns
Slave Mode					
LRCK Edge to BCLK "↑" (Note 20)	tLRB	50	-	-	ns
BCLK "↑" to LRCK Edge (Note 20)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	-	-	80	ns
BCLK "↓" to SDTO	tBSD	-	-	80	ns
Audio Interface Timing (TDM128 Mode)					
Master Mode					
BCLK "↓" to LRCK	tMBLR	-24	-	24	ns
BCLK "↓" to SDTOB (Note 21)	tBSD	-40	-	40	ns
TDMIN Hold Time	tTDMH	20	-	-	ns
TDMIN Setup Time	tTDMS	20	-	-	ns
Slave Mode					
LRCK Edge to BCLK "↑" (Note 20)	tLRB	40	-	-	ns
BCLK "↑" to LRCK Edge (Note 20)	tBLR	40	-	-	ns
BCLK "↓" to SDTOB (Note 21)	tBSD	-	-	40	ns
TDMIN Hold Time	tTDMH	20	-	-	ns
TDMIN Setup Time	tTDMS	20	-	-	ns
Audio Interface Timing (TDM256 Mode)					
Master Mode					
BCLK "↓" to LRCK	tMBLR	-12	-	12	ns
BCLK "↓" to SDTOB (Note 21)	tBSD	-20	-	20	ns
TDMIN Hold Time	tTDMH	10	-	-	ns
TDMIN Setup Time	tTDMS	10	-	-	ns
Slave Mode					
LRCK Edge to BCLK "↑" (Note 20)	tLRB	20	-	-	ns
BCLK "↑" to LRCK Edge (Note 20)	tBLR	20	-	-	ns
BCLK "↓" to SDTOB (Note 21)	tBSD	-	-	20	ns
TDMIN Hold Time	tTDMH	10	-	-	ns
TDMIN Setup Time	tTDMS	10	-	-	ns

Note 18. MSBS, BCKP bits = "00" or "11"
Note 19. MSBS, BCKP bits = "01" or "10"
Note 20. BCLK rising edge must not occur at the same time as LRCK edge.
Note 21. SDTOA is fixed to "L".

Parameter	Symbol	min	typ	max	Units
Control Interface Timing					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	200	-	-	ns
CSN Edge to CCLK "↑" (Note 22)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 22)	tCSH	50	-	-	ns
Control Interface Timing (I²C Bus mode) (Note 23)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 24)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 25)	tPD	150	-	-	ns
PMADAL or PMADAR or PMADBL or PMADBR "↑" to SDTO valid (Note 26)					
HPFA/B1-0 bits = "00"	tPDV	-	3088	-	1/fs
HPFA/B1-0 bits = "01"	tPDV	-	1552	-	1/fs
HPFA/B1-0 bits = "10"	tPDV	-	784	-	1/fs
HPFA/B1-0 bits = "11", INCA/B = "0"	tPDV	-	3088	-	1/fs
HPFA/B1-0 bits = "11", INCA/B = "1"	tPDV	-	1552	-	1/fs

Note 22. CCLK rising edge must not occur at the same time as CSN edge.
Note 23. I²C is a registered trademark of Philips Semiconductors.
Note 24. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 25. The AK5702 can be reset by the PDN pin = "L".
Note 26. This is the count of LRCK "↑" from the PMADAL, PMADAR, PMADBL, PMADBR bit = "1".

■ Timing Diagram

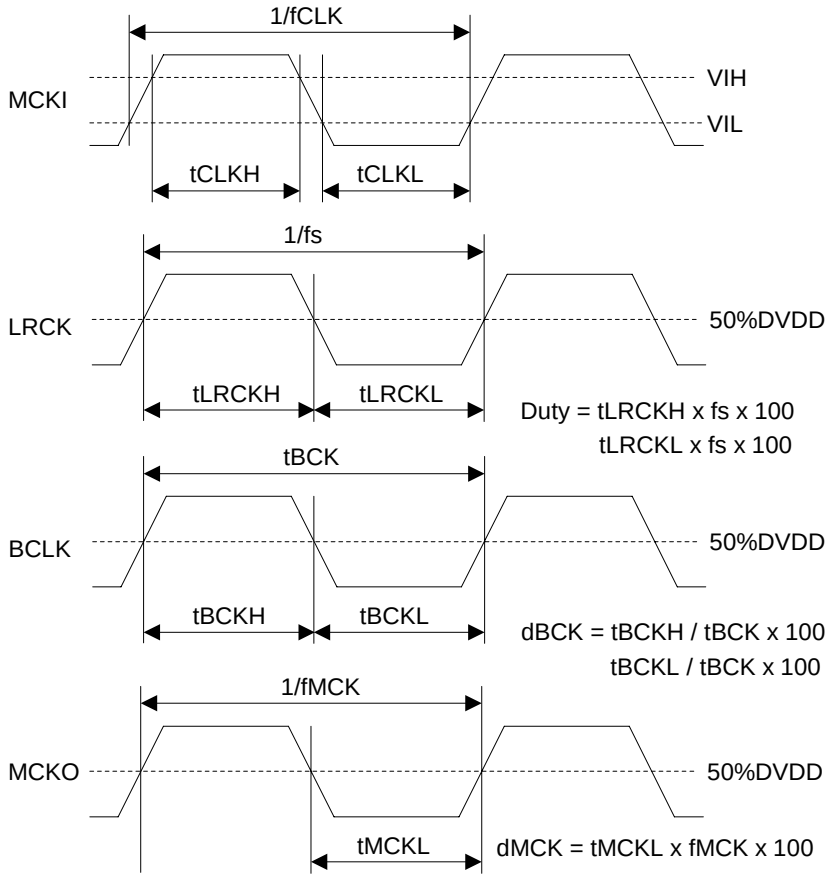


Figure 2. Clock Timing (PLL/EXT Master mode)

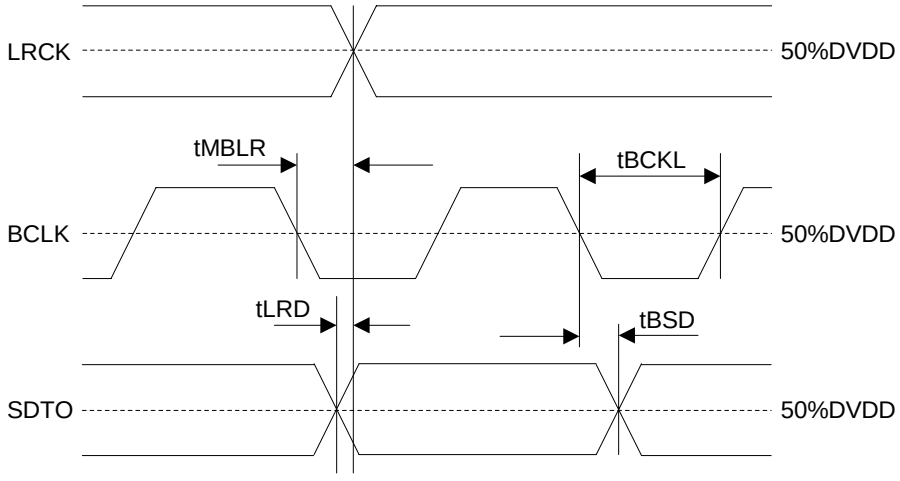


Figure 3. Audio Interface Timing (PLL/EXT Master mode & Normal mode)

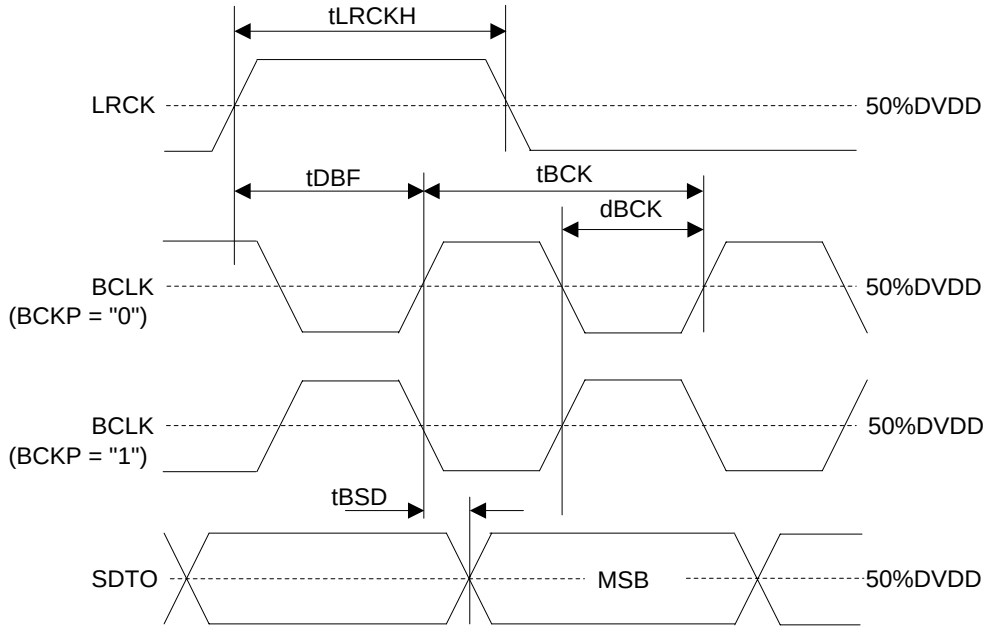


Figure 4. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = “0”)

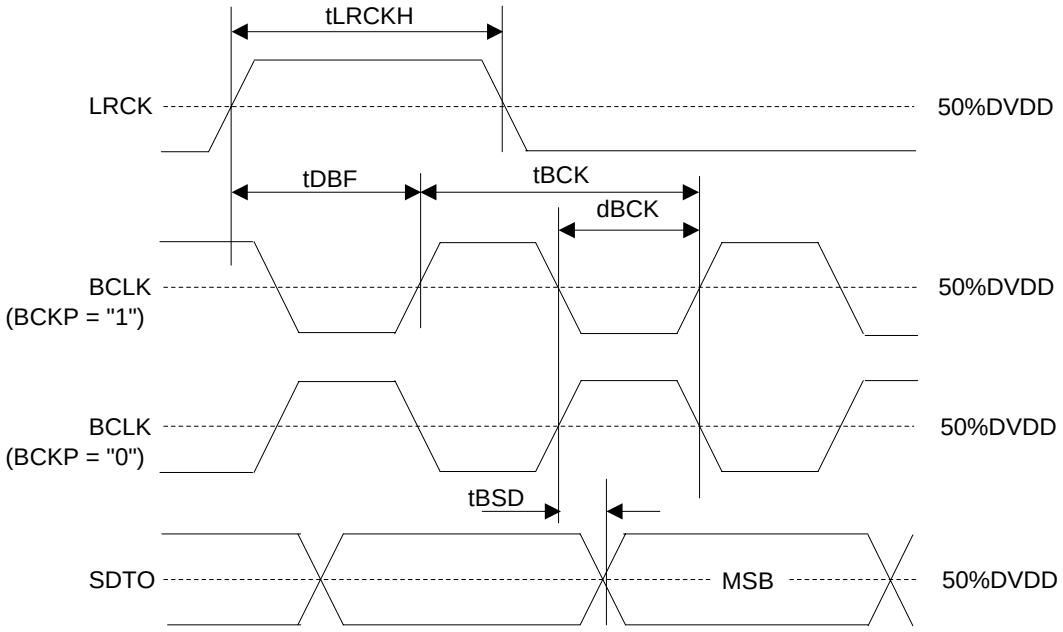


Figure 5. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = “1”)

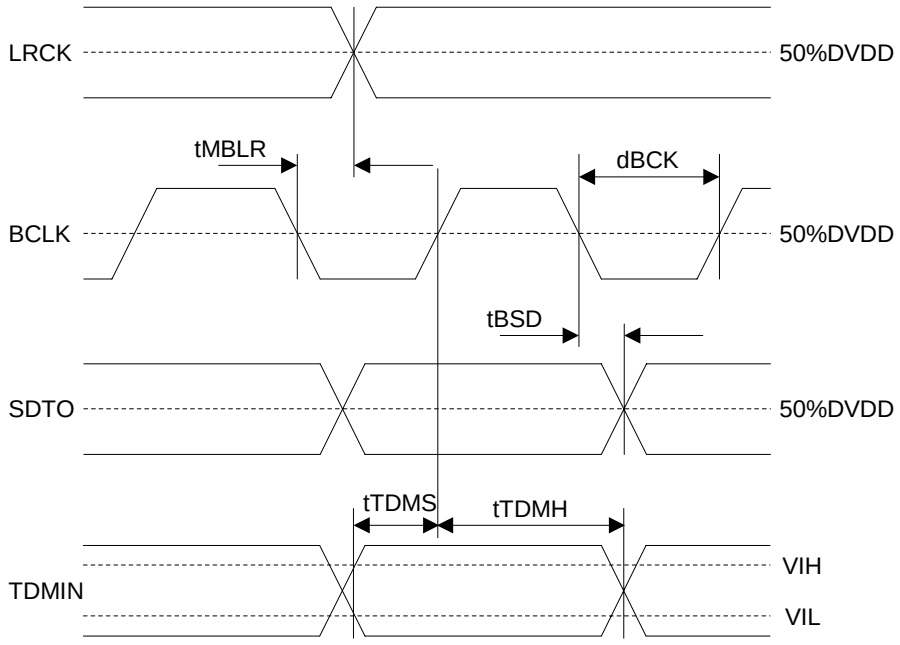


Figure 6. Audio Interface Timing (PLL/EXT Master mode & TDM mode)

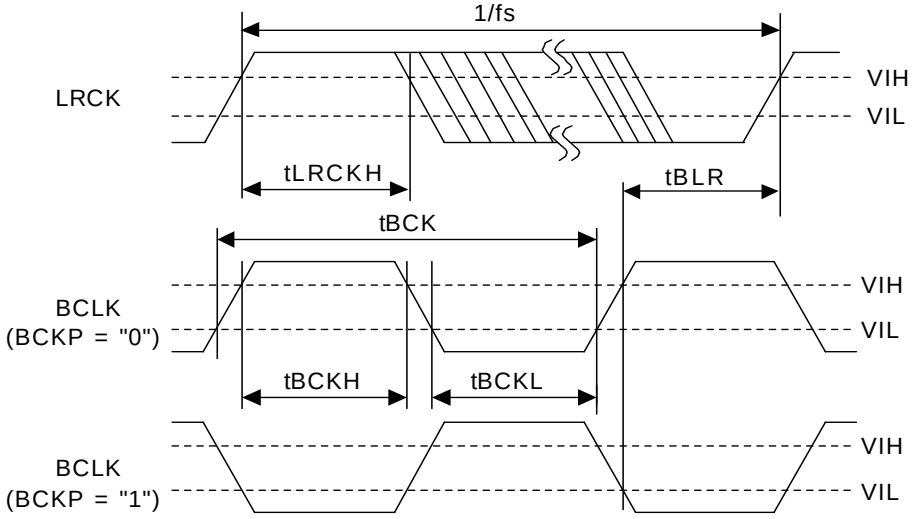


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BCLK pin & DSP mode; MSBS = 0)

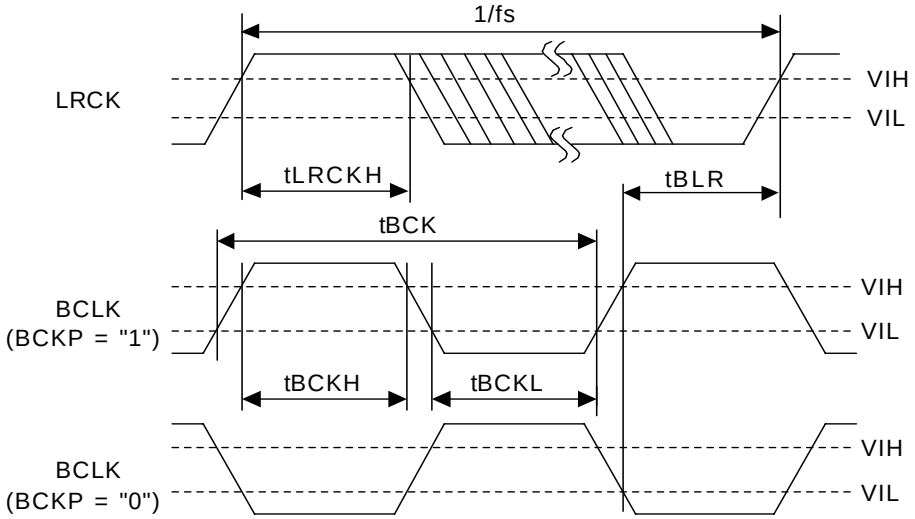


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BCLK pin & DSP mode; MSBS = 1)

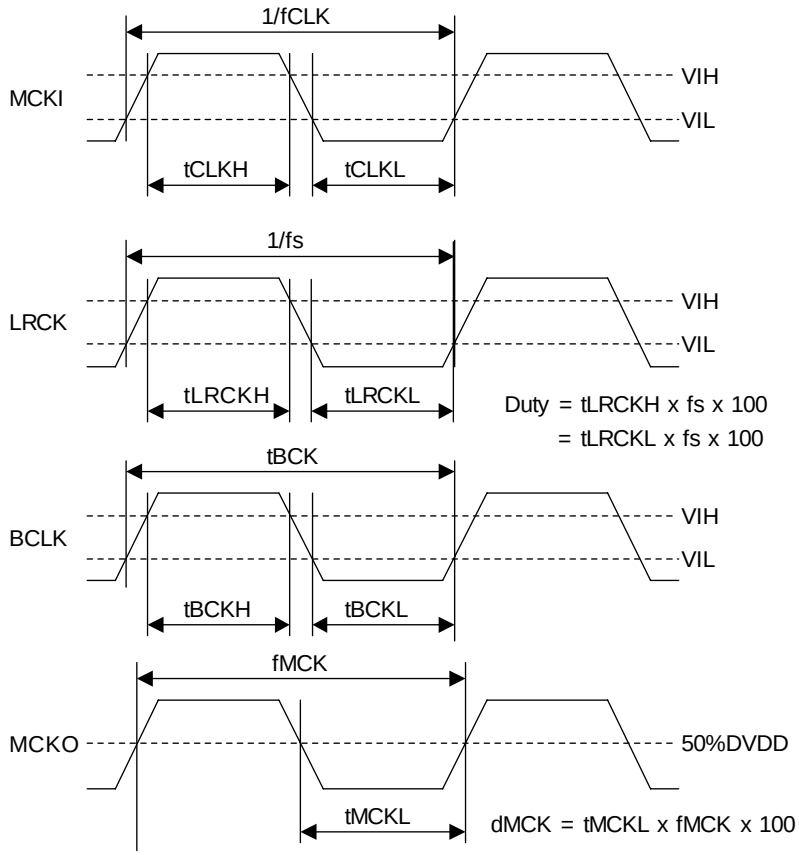


Figure 9. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin & Except DSP mode)

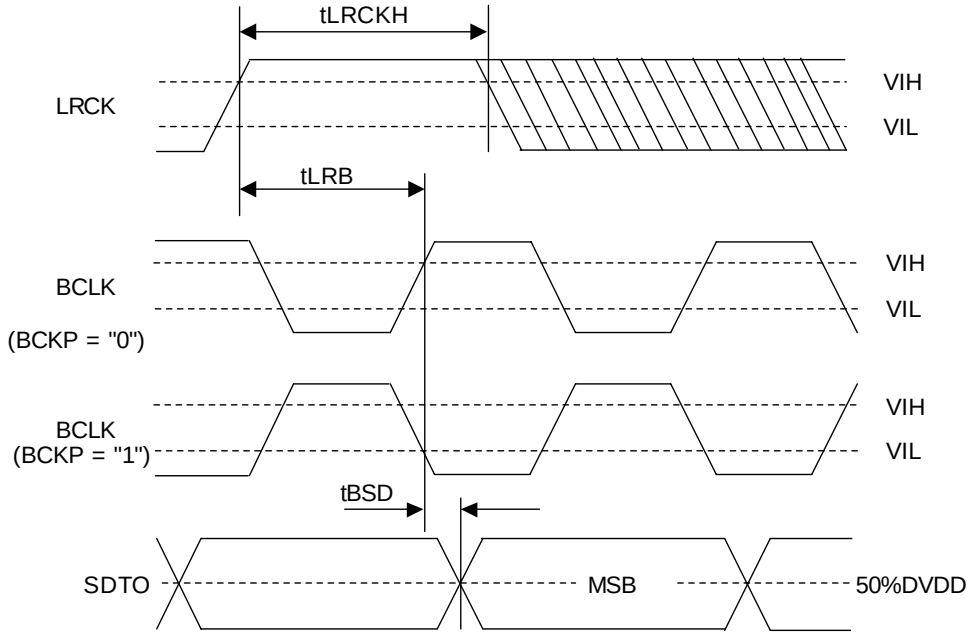


Figure 10. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS = 0)

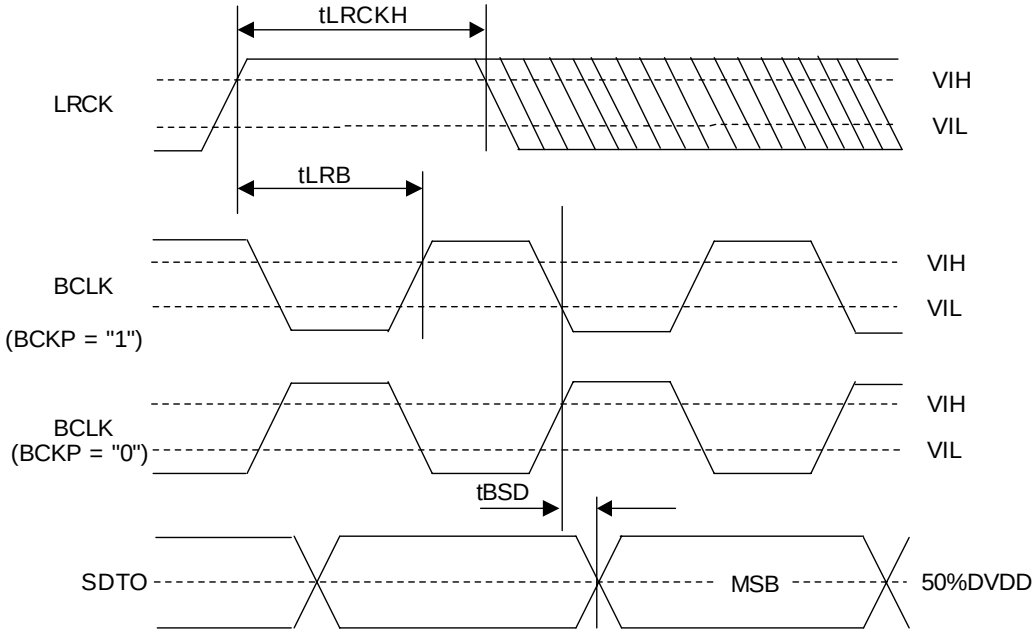


Figure 11. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS = 1)

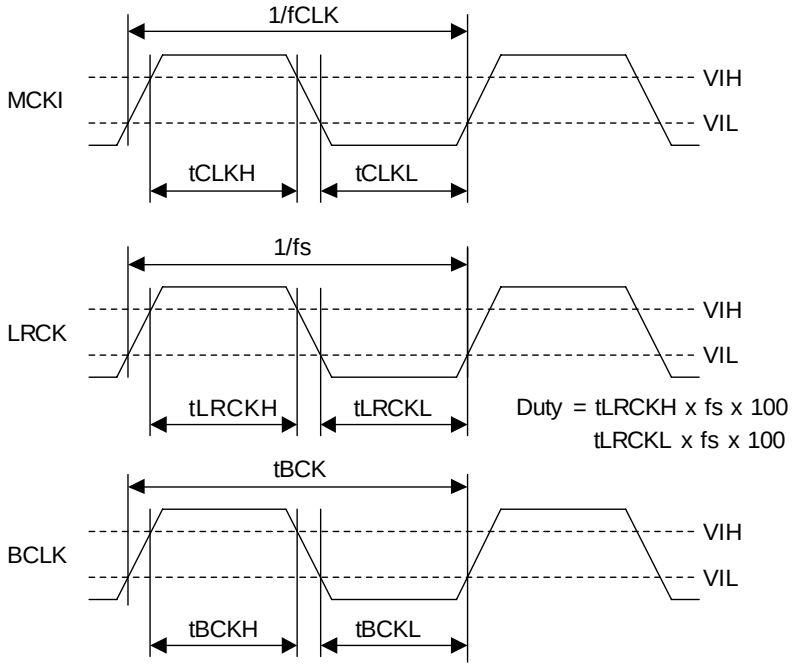


Figure 12. Clock Timing (EXT Slave mode)

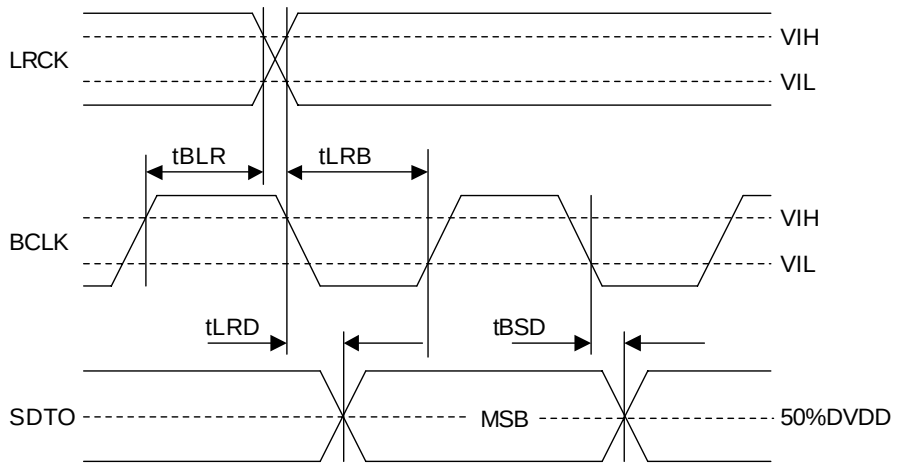


Figure 13. Audio Interface Timing (PLL/EXT Slave mode)

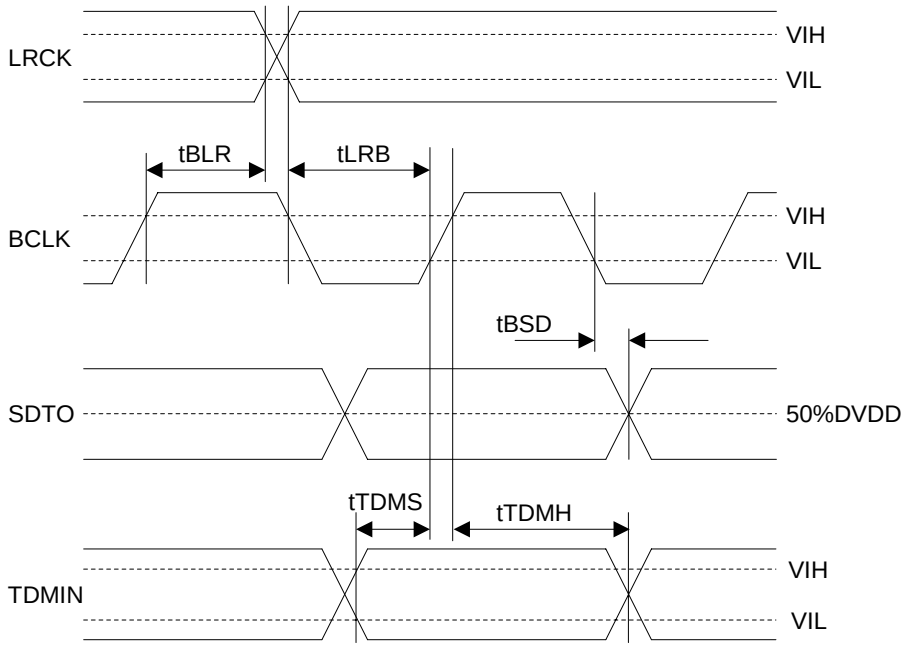


Figure 14. Audio Interface Timing (PLL/EXT Slave mode & TDM mode)

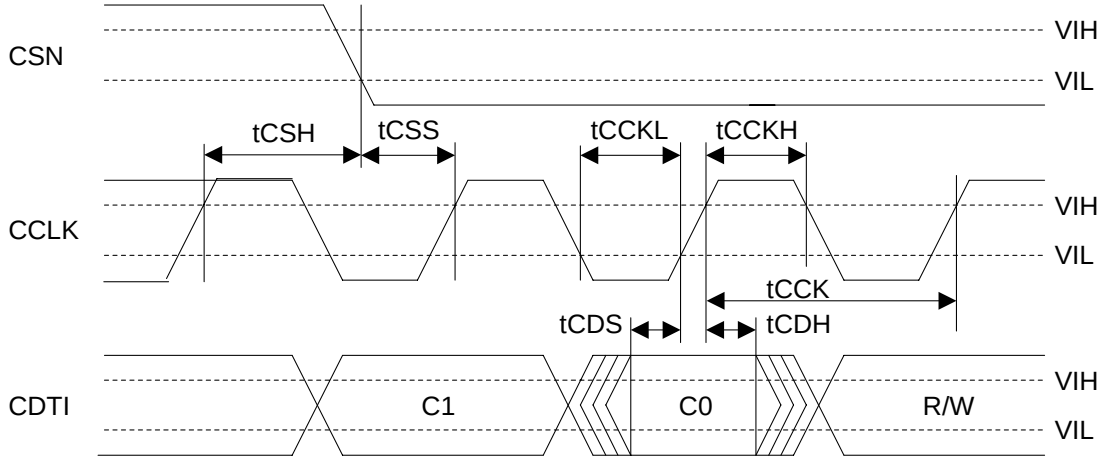


Figure 15. WRITE Command Input Timing

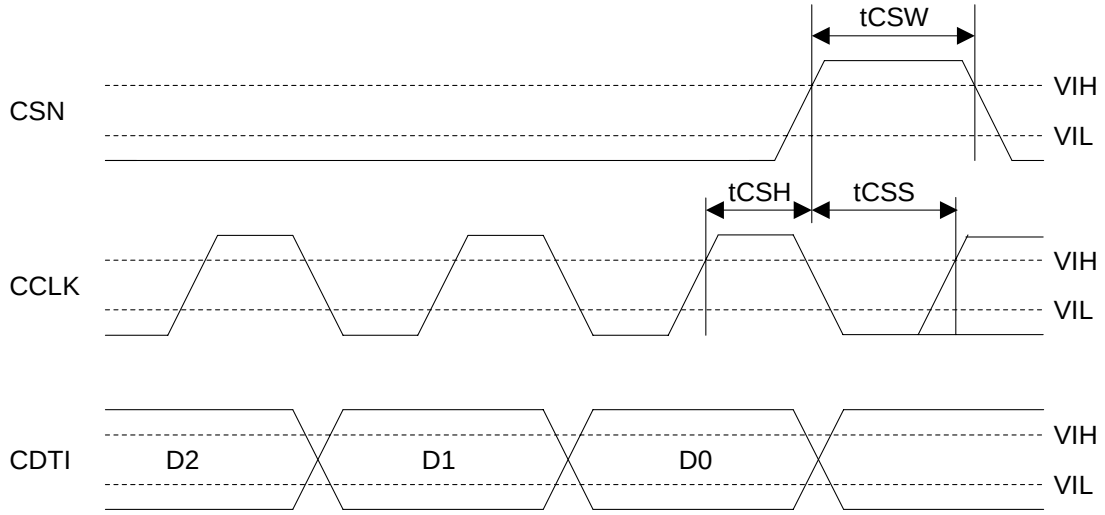


Figure 16. WRITE Data Input Timing

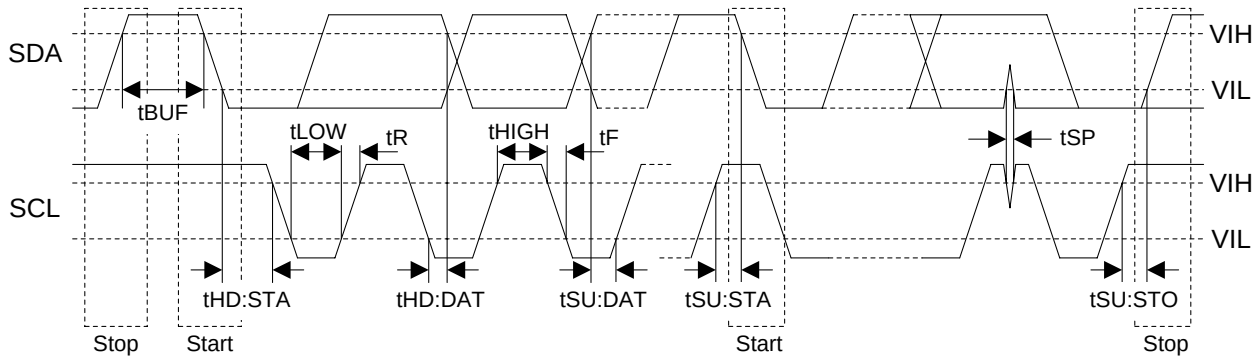


Figure 17. I^{2}CBUS Timing

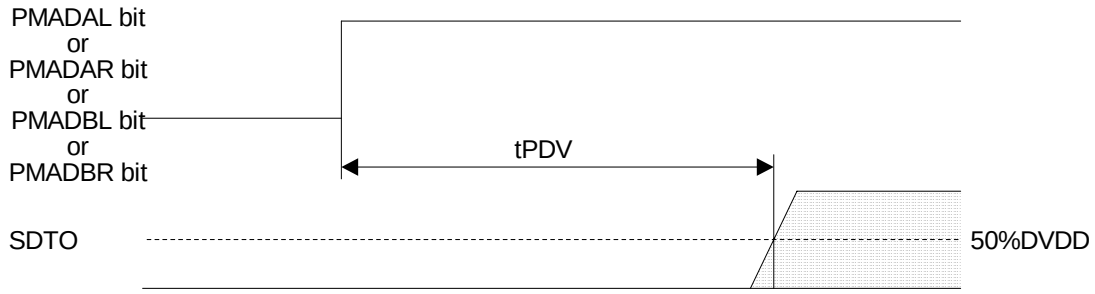


Figure 18. Power Down & Reset Timing 1

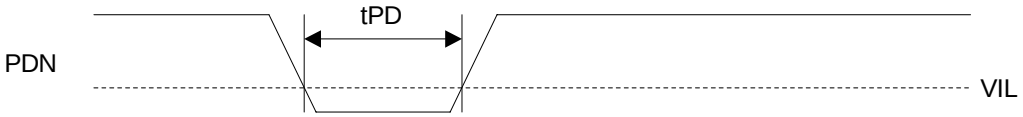


Figure 19. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1 and Table 2.)

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 27)	1	1	See Table 4	Figure 20
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	Figure 21
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BCLK pin)	1	0	See Table 4	Figure 22
EXT Slave Mode	0	0	x	Figure 23
EXT Master Mode (Note 28)	0	1	x	Figure 24

Note 27. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is "1".

Note 28. In case of EXT Master Mode, the register should be set as Figure 64.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BCLK pin	LRCK pin
PLL Master Mode	0	"L"	Selected by PLL3-0 bits	BCLK pin (Selected by BCKO1-0 bits)	LRCK pin (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	0	"L"	Selected by PLL3-0 bits	BCLK pin (≥ 32fs)	LRCK pin (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BCLK pin)	0	"L"	GND	BCLK pin (Selected by PLL3-0 bits)	LRCK pin (1fs)
EXT Slave Mode	0	"L"	Selected by FS1-0 bits	BCLK pin (≥ 32fs)	LRCK pin (1fs)
EXT Master Mode	0	"L"	Selected by FS1-0 bits	BCLK pin (Selected by BCKO1-0 bits)	LRCK pin (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK5702 is power-down mode (PDN pin = "L") and exits reset state, the AK5702 is slave mode. After exiting reset state, the AK5702 goes to master mode by changing M/S bit = "1".

When the AK5702 is used by master mode, LRCK and BCLK pins are a floating state until M/S bit becomes "1". LRCK and BICK pins of the AK5702 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state. When PDN pin is "H" and PMVCM bit becomes "L", LRCK, BCLK pin output "L" or "H". In this situation, it is possible to draw the current into pulled-down or pulled-up resister. This current can stop by setting M/S bit to "0".

PDN pin	PMVCM bit	M/S bit	Mode	LRCK,BCLK pin
L	L	L	Slave	Input
H	L	L	Slave	Input
H	L	H	Master	Output "L" or "H"
H	H	L	Slave	Input
H	H	H	Master	Output

Table 3. Select Master/Salve Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, whenever the AK5702 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 Bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	80ms	
2	0	0	1	0	BCLK pin	32fs	10k	4.7n	2ms	
							10k	10n	4ms	
3	0	0	1	1	BCLK pin	64fs	10k	4.7n	2ms	
							10k	10n	4ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	40ms	
8	1	0	0	0	MCKI pin	19.2MHz	10k	4.7n	40ms	
9	1	0	0	1	MCKI pin	12MHz (Note 29)	10k	4.7n	40ms	(default)
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
14	1	1	1	0	MCKI pin	13MHz	10k	220n	60ms	
15	1	1	1	1	MCKI pin	26MHz	10k	220n	60ms	
Others	Others				N/A					

Note 29. See Table 5 regarding the difference between PLL3-0 bits = "0110"(Mode 6) and "1001"(Mode 9). Clock jitter is lower in Mode9 than Mode6 respectively.

Table 4. Setting of PLL Mode (fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz 7.349918kHz (Note 30)	
5	0	1	0	1	11.025kHz 11.024877kHz (Note 30)	
6	0	1	1	0	14.7kHz 14.69984kHz (Note 30)	
7	0	1	1	1	22.05kHz 22.04975kHz (Note 30)	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz 29.39967kHz (Note 30)	
15	1	1	1	1	44.1kHz 44.0995kHz (Note 30)	(default)
Others	Others				N/A	

Note 30. In case of PLL3-0 bits = "1001"

Table 5. Setting of Sampling Frequency at PMPLL bit = "1" and Reference Clock=MCKI pin

When PLL reference clock input is LRCK or BCLK pin, the sampling frequency is selected by FS3 and FS2 bits (Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	Don't care	Don't care	7.35kHz ≤ fs ≤ 12kHz	
1	0	1	Don't care	Don't care	12kHz < fs ≤ 24kHz	
2	1	Don't care	Don't care	Don't care	24kHz < fs ≤ 48kHz	(default)
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" and Reference=LRCK/BCLK

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BCLK pins go to "L" and irregular frequency clock is output from MCKO pins at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", MCKO pin goes to "L" (Table 7).

In DSP Mode 0, BCLK and LRCK start to output corresponding to Lch data after PLL goes to lock state by setting PMPLL bit = "0" → "1". When MSBS bit = "0" and BCKP bit = "1" or MSBS bit = "1" and BCKP bit = "0" in DSP Mode 0, BCLK "H" time of the first pulse becomes shorter by 1/(256fs) than "H" time except for the first pulse.

When sampling frequency is changed, BCLK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BCLK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	See Table 9	See Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 9 is output from MCKO pin when PLL is locked. The ADC output invalid data when the PLL is unlocked.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except above case)	"L" Output	Invalid
PLL Lock	"L" Output	See Table 9

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to MCKI pin, the MCKO, BCLK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BCLK output frequency is selected among 32fs or 64fs, by BCKO1-0 bits (Table 10).

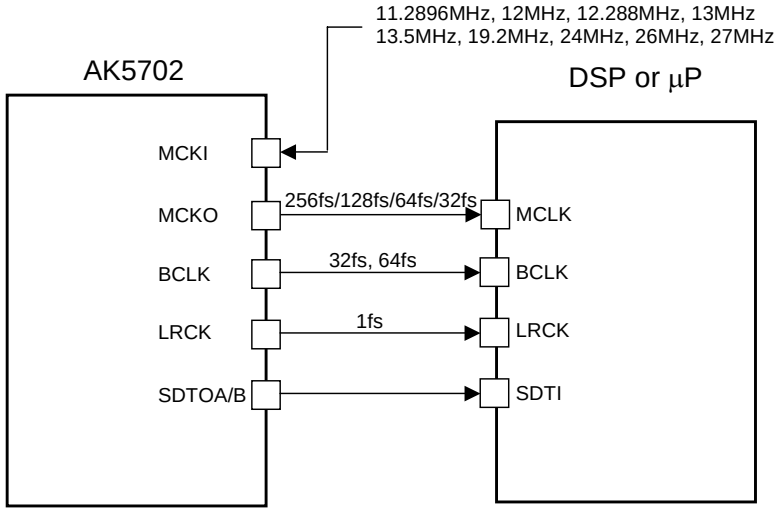


Figure 20. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO1 bit	BCKO0 bit	BCLK Output Frequency	
0	0	N/A	
0	1	32fs	(default)
1	0	64fs	
1	1	N/A	

Table 10. BCLK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to MCKI, BCLK or LRCK pin. The required clock to the AK5702 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL Slave Mode 1 (PLL reference clock: MCKI pin)

BCLK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

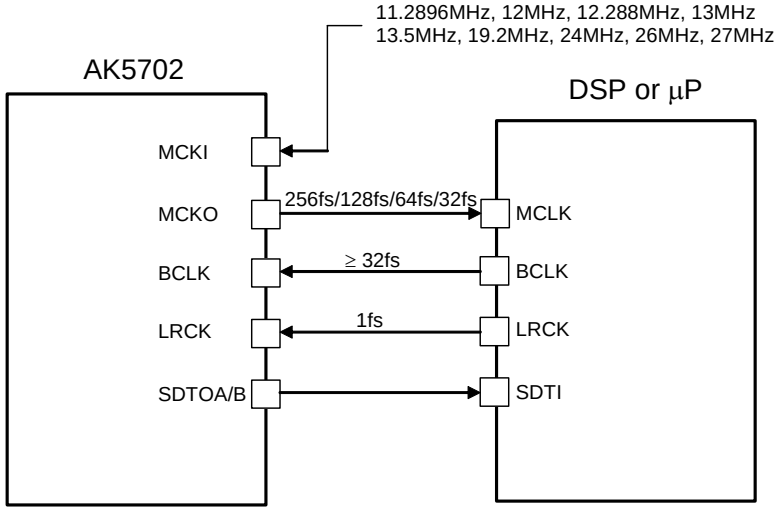


Figure 21. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

The external clocks (MCKI, BCLK and LRCK) should always be present whenever the ADC is in operation (PMADAL bit = "1" or PMADAR bit = "1" or PMADBL bit = "1" or PMADBR bit = "1"). If these clocks are not provided, the AK5702 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC should be in the power-down mode (PMADAL= PMADAR = PMADBL = PMADBR bits = "0").

b) PLL Slave Mode 2 (PLL reference clock: BCLK or LRCK pin)

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).

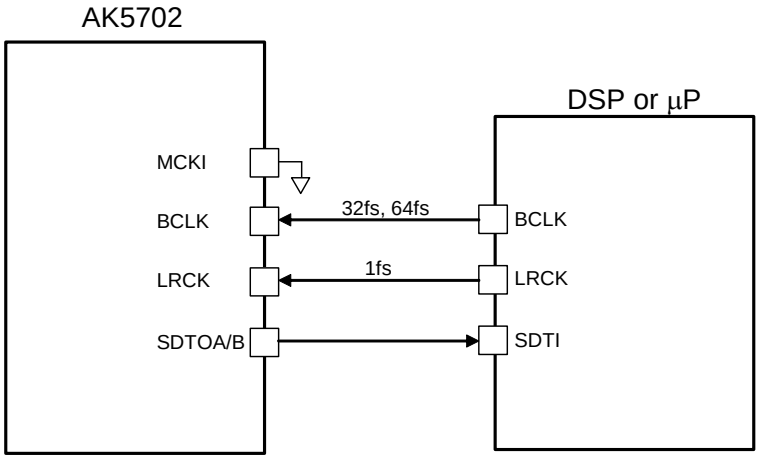


Figure 22. PLL Slave Mode 2 (PLL Reference Clock: LRCK or BCLK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK5702 becomes EXT mode. Master clock is input from MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BCLK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS3-0 bits (Table 11).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	00, 01, 11	0	0	256fs	7.35kHz ~ 48kHz	
1	00, 01, 11	0	1	1024fs	7.35kHz ~ 13kHz	
2	00, 01, 11	1	0	512fs	7.35kHz ~ 26kHz	
3	00, 01, 11	1	1	256fs	7.35kHz ~ 48kHz	(default)
4	10	Don't care	Don't care	N/A	-	

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

The external clocks (MCKI, BCLK and LRCK) should always be present whenever the ADC is in operation (PMADAL bit = "1" or PMADAR bit = "1" or PMADBL bit = "1" or PMADBR bit = "1"). If these clocks are not provided, the AK5702 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC should be in the power-down mode (PMADAL= PMADAR = PMADBL = PMADBR bits = "0").

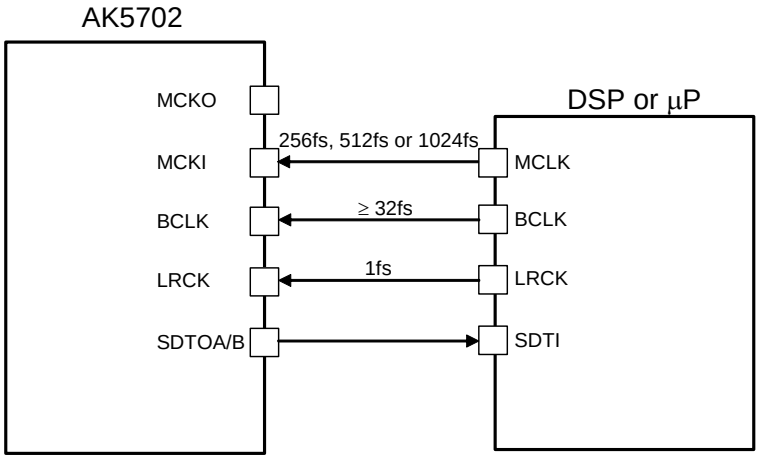


Figure 23. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1", TE3-0 bits = "0101", TMASTER bit = "1")

The AK5702 becomes EXT Master Mode by setting as Figure 63. Master clock is input from MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS3-0 bits (Table 12).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	00, 01, 11	0	0	256fs	7.35kHz ~ 48kHz	
1	00, 01, 11	0	1	1024fs	7.35kHz ~ 13kHz	
2	00, 01, 11	1	0	512fs	7.35kHz ~ 26kHz	
3	00, 01, 11	1	1	256fs	7.35kHz ~ 48kHz	(default)
4	10	Don't care	Don't care	N/A	-	

Table 12. MCKI Frequency at EXT Master Mode

MCKI should always be present whenever the ADC is in operation (PMADAL bit = "1" or PMADAR bit = "1" or PMADBL bit = "1" or PMADBR bit = "1"). If MCKI is not provided, the AK5702 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC should be in the power-down mode (PMADAL= PMADAR = PMADBL = PMADBR bits = "0").

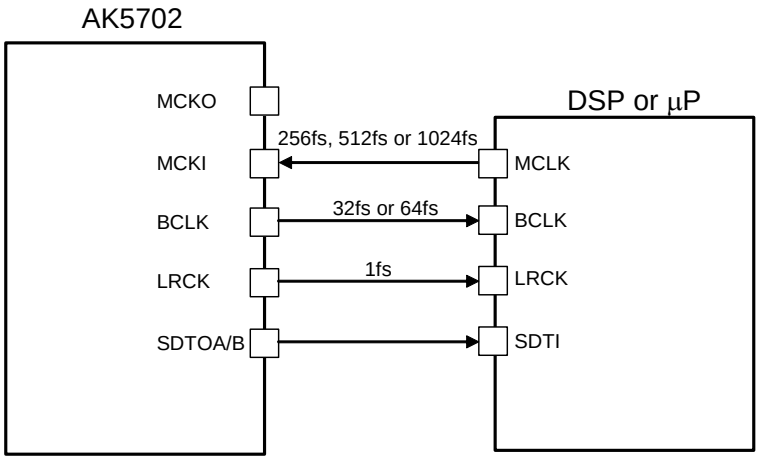


Figure 24. EXT Master Mode

BCKO1 bit	BCKO0 bit	BCLK Output Frequency	
0	0	N/A	
0	1	32fs	(default)
1	0	64fs	
1	1	N/A	

Table 13. BCLK Output Frequency at Master Mode

■ Audio Interface Format

Fore types of data format are available and are selected by setting the M/S, TDM1-0, DIF1-0 bits (Table 14, Table 15, Table 16). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. The SDTO is clocked out on the falling edge ("↓") of BCLK except DSP mode.
In TDM128 mode at master operation, BCLK becomes 128fs independent of select the BCLK1-0 bits.
In TDM256 mode at master operation, BCLK becomes 256fs independent of select the BCLK1-0 bits.
TDM mode dose not correspond the PLL Slave Mode2.

Mode	M/S	TDM1	TDM0	DIF1	DIF0	SDTOA/B	BCLK	Figure	
0	0	0	0	0	0	DSP Mode 0	32fs	Figure 25	
1	0	0	0	0	1	Reserved	-	-	
2	0	0	0	1	0	MSB justified	≥ 32fs	Figure 29	
3	0	0	0	1	1	I^2S compatible	≥ 32fs	Figure 30	(default)
4	1	0	0	0	0	DSP Mode 0	32fs	Figure 25	
5	1	0	0	0	1	Reserved	-	-	
6	1	0	0	1	0	MSB justified	32fs or 64fs	Figure 29	
7	1	0	0	1	1	I^2S compatible	32fs or 64fs	Figure 30	

Table 14. Audio Interface Format (Stereo Mode)

Mode	M/S	TDM1	TDM0	DIF1	DIF0	SDTOB	BCLK	Figure
8	0	0	1	0	0	Reserved	-	-
9	0	0	1	0	1	Reserved	-	-
10	0	0	1	1	0	MSB justified	128fs	Figure 31
11	0	0	1	1	1	I^2S compatible	128fs	Figure 32
12	1	0	1	0	0	Reserved	-	-
13	1	0	1	0	1	Reserved	-	-
14	1	0	1	1	0	MSB justified	128fs	Figure 31
15	1	0	1	1	1	I^2S compatible	128fs	Figure 32

Table 15. Audio Interface Format (TDM128 Mode, 8ch)

Mode	M/S	TDM1	TDM0	DIF1	DIF0	SDTOB	BCLK	Figure
16	0	1	1	0	0	Reserved	-	-
17	0	1	1	0	1	Reserved	-	-
18	0	1	1	1	0	MSB justified	256fs	Figure 33
19	0	1	1	1	1	I^2S compatible	256fs	Figure 34
20	1	1	1	0	0	Reserved	-	-
21	1	1	1	0	1	Reserved	-	-
22	1	1	1	1	0	MSB justified	256fs	Figure 33
23	1	1	1	1	1	I^2S compatible	256fs	Figure 34

Table 16. Audio Interface Format (TDM256 Mode, 8ch)

Belows are minimam voltage of DVDD at the audio interface respectivity.
Stereo Mode: DVDD = 1.6 ~ 3.6V
TDM128 Mode: DVDD = 2.0 ~ 3.6V
TDM256 Mode: DVDD = 2.7 ~ 3.6V

Note. In TDM mode at master operation, LRCK can be output by writing "0101" at TE3-0 bits and "1" at TMASTER bit.

In DSP mode 0, the audio I/F timing is changed by BCKP and MSBS bits.
When BCKP bit is "0", SDTO data is output by rising edge ("↑") of BCLK/BCLK.
When BCKP bit is "1", SDTO data is output by falling edge ("↓") of BCLK/BCLK.
MSB data position of SDTO can be shifted by MSBS bit. The shifted period is a half of BCLK/BCLK.

DIF1	DIF0	MSBS	BCKP	Audio Interface Format	Figure
0	0	0	0	MSB of SDTO is output by the rising edge ("↑") of the first BCLK after the rising edge ("↑") of LRCK.	Figure 25
		0	1	MSB of SDTO is output by the falling edge ("↓") of the first BCLK after the rising edge ("↑") of LRCK.	Figure 26
		1	0	MSB of SDTO is output by next rising edge ("↑") of the falling edge ("↓") of the first BCLK after the rising edge ("↑") of LRCK.	Figure 27
		1	1	MSB of SDTO is output by next falling edge ("↓") of the rising edge ("↑") of the first BCLK after the rising edge ("↑") of LRCK.	Figure 28

Table 17. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "−1" at 16bit data is converted to "−1" at 8-bit data. And when the DAC playbacks this 8-bit data, "−1" at 8-bit data will be converted to "−256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

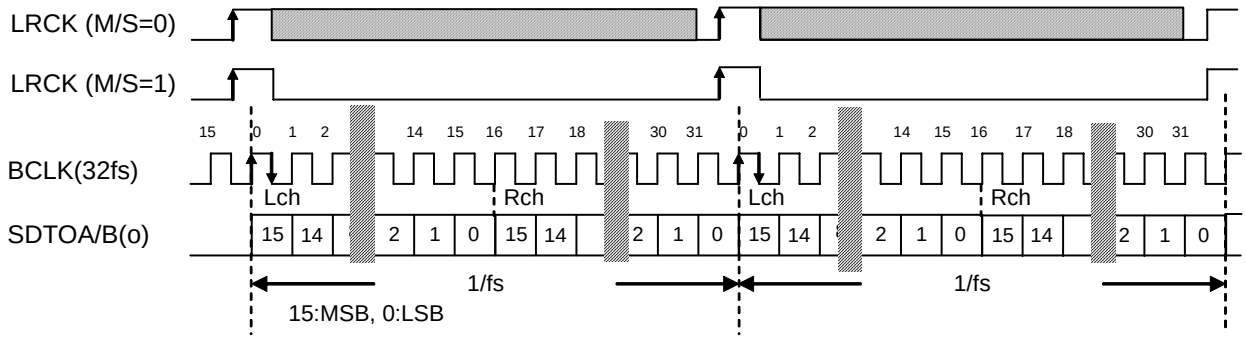


Figure 25. Mode 0, 4 Timing (Stereo Mode, DSP Mode 0, MSBS = "0", BCKP = "0")

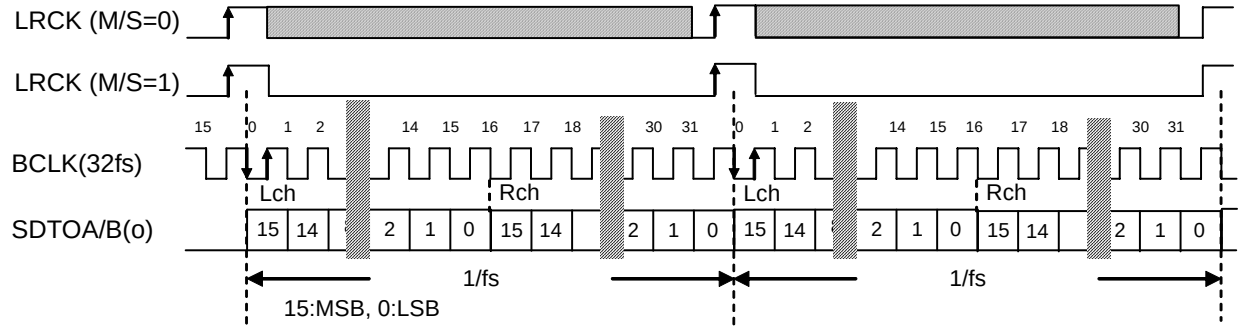


Figure 26. Mode 0, 4 Timing (Stereo Mode, DSP Mode 0, MSBS = "0", BCKP = "1")

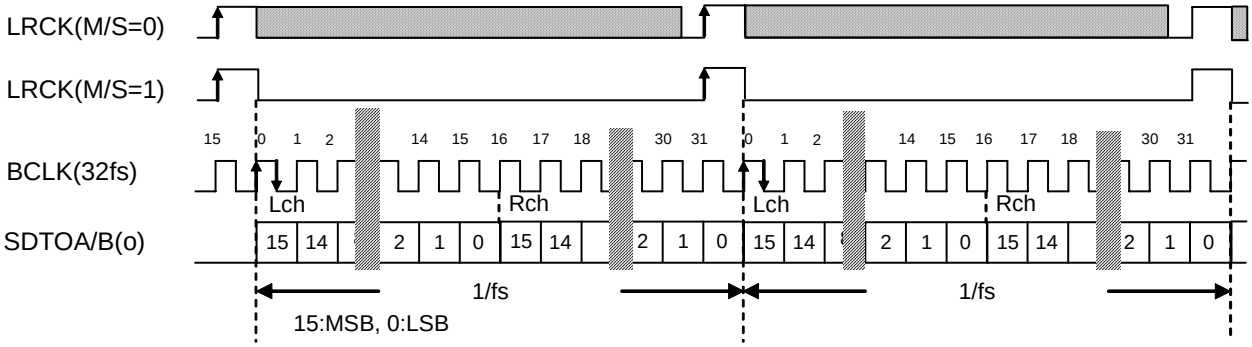


Figure 27. Mode 0, 4 Timing (Stereo Mode, DSP Mode 0, MSBS = "1", BCKP = "0")

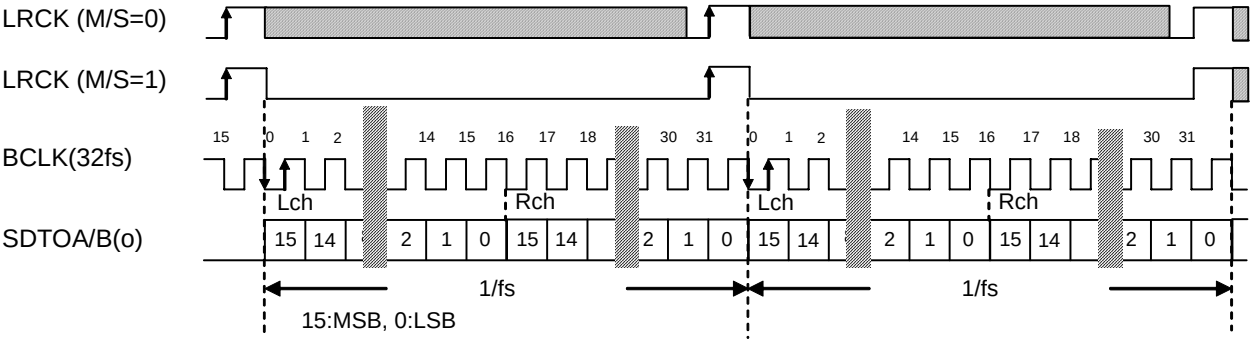


Figure 28. Mode 0, 4 Timing (Stereo Mode, DSP Mode 0, MSBS = "1", BCKP = "1")

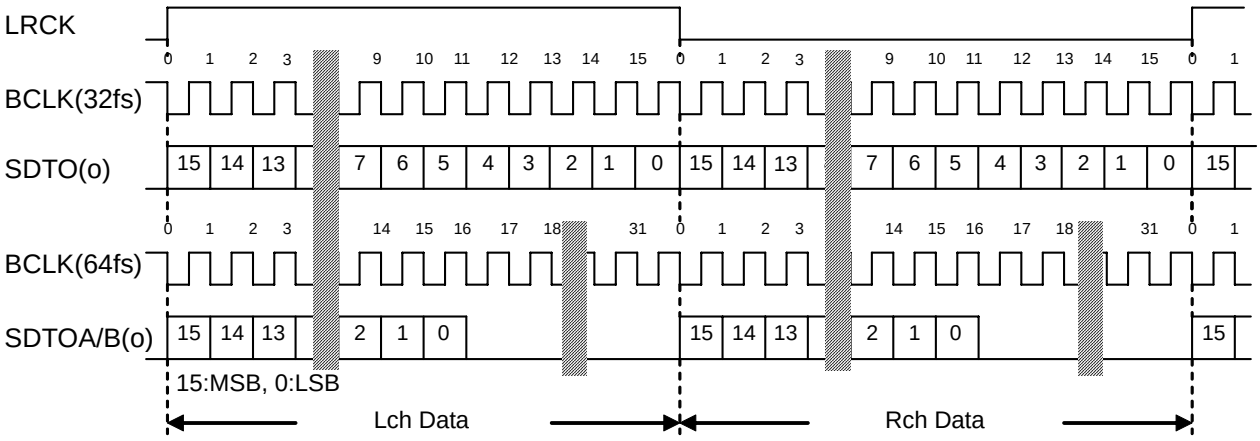


Figure 29. Mode 2, 6 Timing (Stereo Mode, MSB justified)

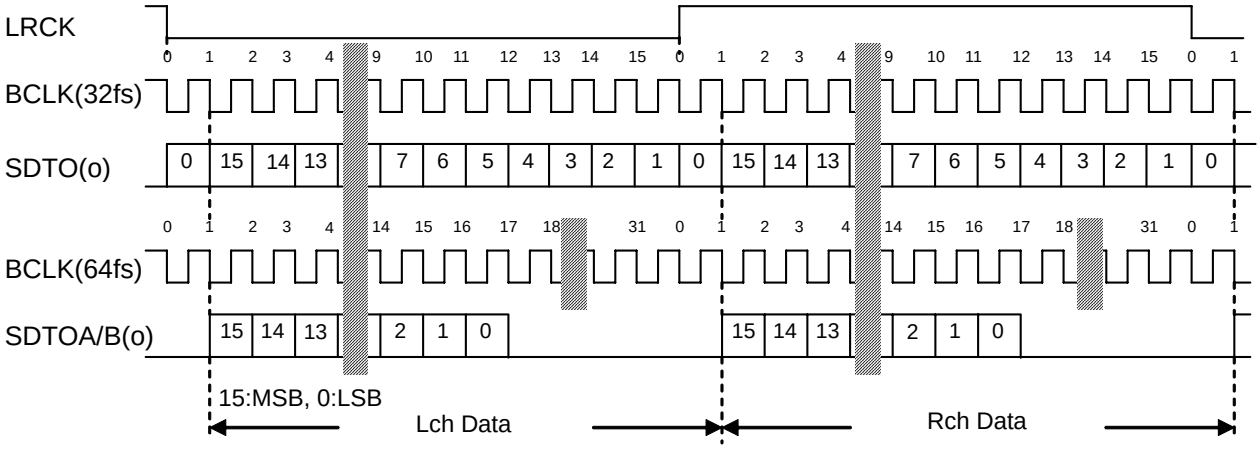


Figure 30. Mode 3, 7 Timing (Stereo Mode, I^2S compatible)

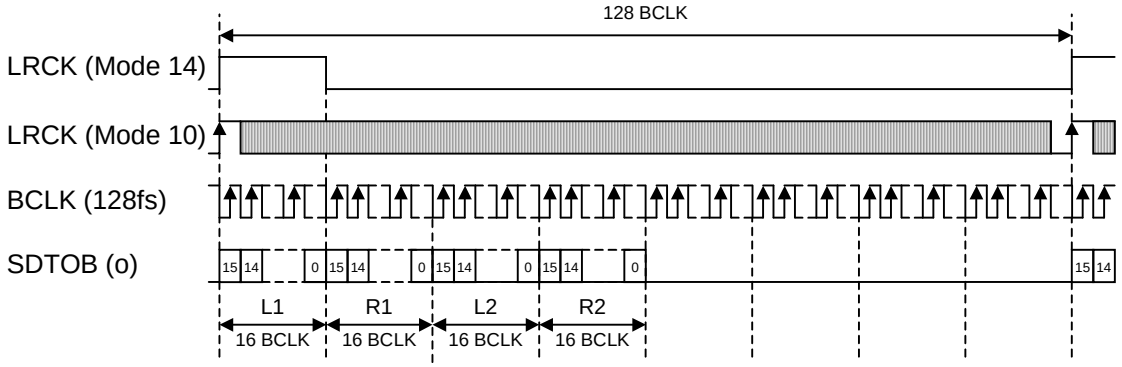


Figure 31. Mode 10, 14 Timing (TDM128 mode, MSB justified)

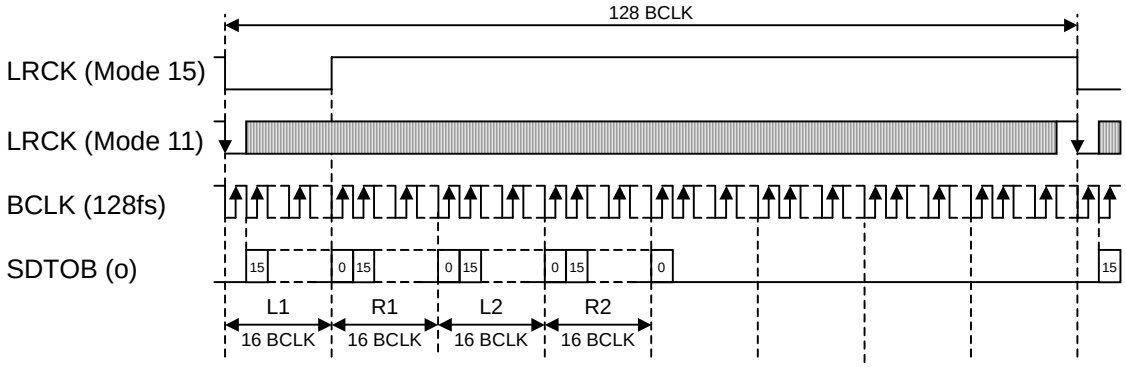


Figure 32. Mode 11, 15 Timing (TDM128 mode, I^2S compatible)

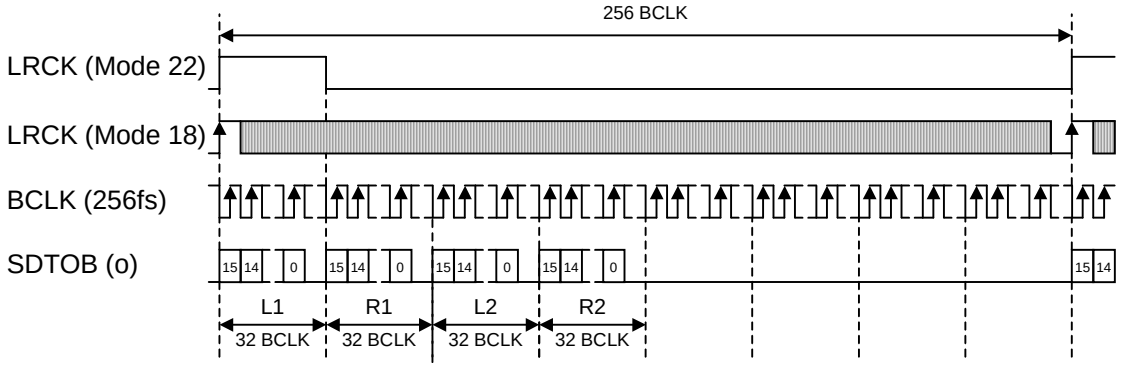


Figure 33. Mode 18, 22 Timing (TDM256 Mode, MSB justified)

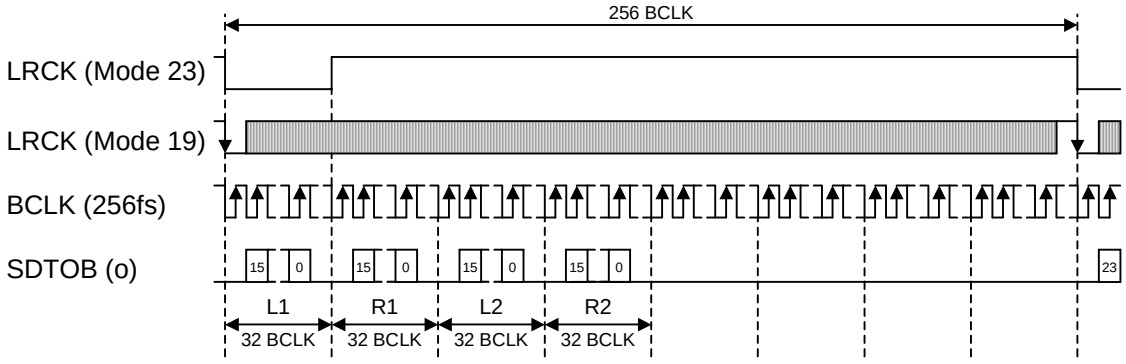


Figure 34. Mode 19, 23 Timing (TDM256 mode, I^2S compatible)

■ Cascade TDM Mode

The AK5702 supports cascading of up to two devices in a daisy chain configuration at TDM mode. In this mode, SDTOB pin of device #1 is connected to TDMIN pin of device #2. SDTOB pin of device #2 can output 8ch TDM data multiplexed with 4ch TDM data of device #1 and 4ch TDM data of device #2. Figure 35 and Figure 37 show a connection example of a daisy chain.

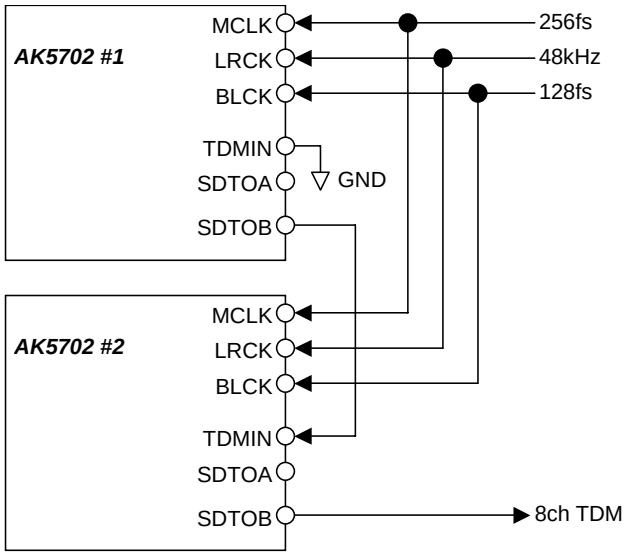


Figure 35. Cascade TDM Connection example (TDM128, MSB justified)

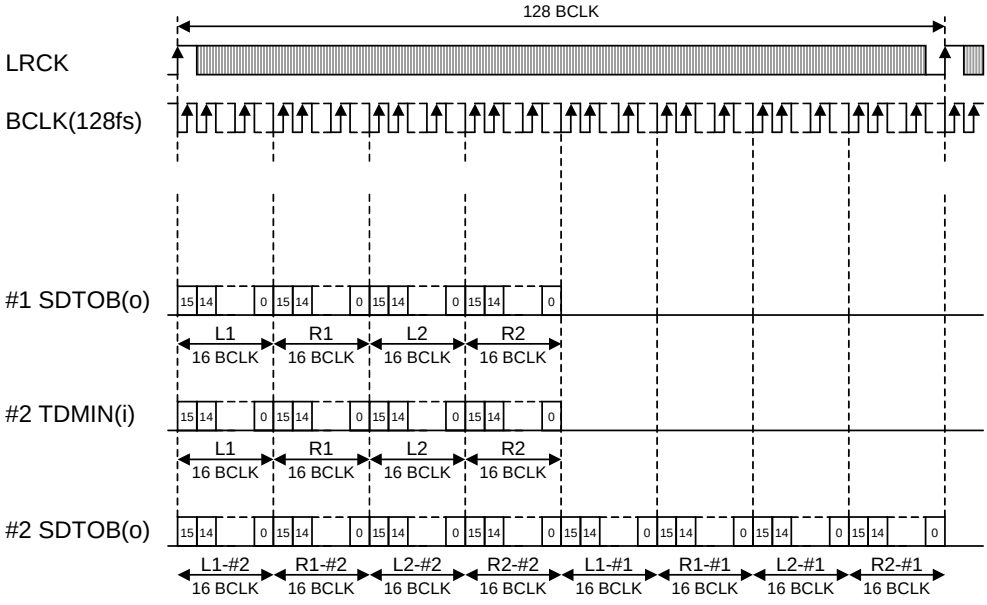


Figure 36. Cascade TDM128 Timing example

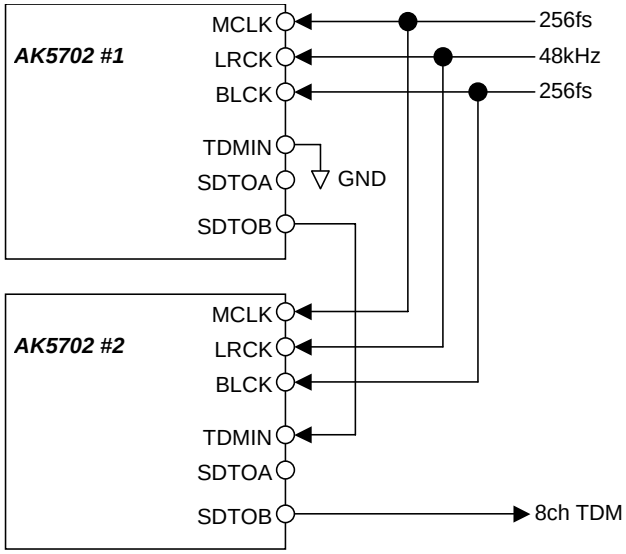


Figure 37. Cascade TDM Connection example (TDM256, MSB justified)

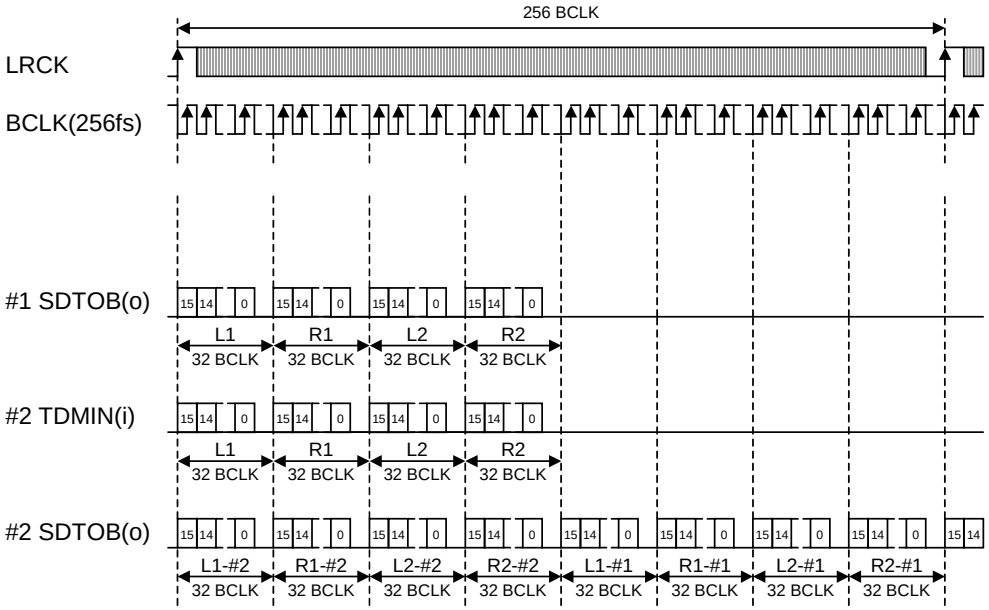


Figure 38. Cascade TDM256 Timing example

■ Mono/Stereo Selection

PMADAL, PMADAR and MIXA bits select mono or stereo mode of ADCA output data. PMADBL, PMADBR and MIXB bits select mono or stereo mode of ADCB output data. ALC operation (ALC bit = "1") or digital volume operation (ALC bit = "0") is applied to the data in Table 18 and Table 19.

PMADAL bit	PMADAR bit	MIXA bit	ADCA Lch data	ADCA Rch data	
0	0	x	All "0"	All "0"	(default)
0	1	x	Rch Input Signal	Rch Input Signal	
1	0	x	Lch Input Signal	Lch Input Signal	
1	1	0	Lch Input Signal	Rch Input Signal	
		1	(L+R)/2	(L+R)/2	

Table 18. ADCA Mono/Stereo Selection (x: Don't care)

PMADBL bit	PMADBR bit	MIXB bit	ADCB Lch data	ADCB Rch data	
0	0	x	All "0"	All "0"	(default)
0	1	x	Rch Input Signal	Rch Input Signal	
1	0	x	Lch Input Signal	Lch Input Signal	
1	1	0	Lch Input Signal	Rch Input Signal	
		1	(L+R)/2	(L+R)/2	

Table 19. ADCB Mono/Stereo Selection (x: Don't care)

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is selected by HPFA1-0 and HPFB1-0 bits (Table 20, Table 21) and scales with sampling rate (fs). The default value is 3.4Hz (@fs=44.1kHz).

HPFA1 bit	HPFA0 bit	fc			
		fs=44.1kHz	fs=22.05kHz	fs=11.025kHz	
0	0	3.4Hz	1.7Hz	0.85Hz	(default)
0	1	6.8Hz	3.4Hz	1.7Hz	
1	0	13.6Hz	6.8Hz	3.4Hz	
1	1	213.9Hz	109.7Hz	54.8Hz	

Table 20. ADCA Digital HPF Cut-off Frequency

HPFB1 bit	HPFB0 bit	fc			
		fs=44.1kHz	fs=22.05kHz	fs=11.025kHz	
0	0	3.4Hz	1.7Hz	0.85Hz	(default)
0	1	6.8Hz	3.4Hz	1.7Hz	
1	0	13.6Hz	6.8Hz	3.4Hz	
1	1	213.9Hz	109.7Hz	54.8Hz	

Table 21. ADCB Digital HPF Cut-off Frequency

■ MIC/LINE Input Selector

The AK5702 has input selector. When MDIF1 and MDIF2 bits are "0", INAL and INAR bits select LIN1/LIN2 and RIN1/RIN2, INBL and INBR bits select LIN3/LIN4 and RIN3/RIN4 respectively. INA5L and INA5R bits also select LIN5 and RIN5, respectively. Refer to Table 24 about the typical input resistance of LIN5, RIN5. When MDIF1 and MDIF2 bits are "1", LIN1, RIN1, LIN2 and RIN2 pins become LINA+, LINA−, RINA− and RINA+ pins, LIN3, RIN3, LIN4 and RIN4 pins become LINB+, LINB−, RINB− and RINB+ pins respectively. In this case, full-differential input is available (Figure 40).

MDIFA1 bit	MDIFA2 bit	INA5L bit	INAL	INA5R bit	INAR	Lch	Rch	
0	0	0	0	0	0	LIN1	RIN1	(default)
					1	LIN1	RIN2	
				1	x	LIN1	RIN5	
			1	0	0	LIN2	RIN1	
					1	LIN2	RIN2	
				1	x	LIN2	RIN5	
		1	x	0	0	LIN5	RIN1	
					1	LIN5	RIN2	
				1	x	LIN5	RIN5	
	1	0	0	x	x	LIN1	RINA+/−	
			1	x	x	N/A	N/A	
		1	x	x	x	LIN5	RINA+/−	
1	0	x	x	0	0	N/A	N/A	
					1	LINA+/−	RIN2	
				1	x	LINA+/−	RIN5	
	1	x	x	x	x	LINA+/−	RINA+/−	

Table 22. ADCA MIC/Line In Path Select

MDIFB1 bit	MDIFB2 bit	INB5L bit	INBL	INB5R bit	INBR	Lch	Rch	
0	0	0	0	0	0	LIN3	RIN3	(default)
					1	LIN3	RIN4	
				1	x	LIN3	RIN5	
			1	0	0	LIN4	RIN3	
					1	LIN4	RIN4	
				1	x	LIN4	RIN5	
		1	x	0	0	LIN5	RIN3	
					1	LIN5	RIN4	
				1	x	LIN5	RIN5	
	1	0	0	x	x	LIN3	RINB+/−	
			1	x	x	N/A	N/A	
		1	x	x	x	LIN5	RINB+/−	
1	0	x	x	0	0	N/A	N/A	
					1	LINB+/−	RIN4	
				1	x	LINB+/−	RIN5	
	1	x	x	x	x	LINB+/−	RINB+/−	

Table 23. ADCB MIC/Line In Path Select

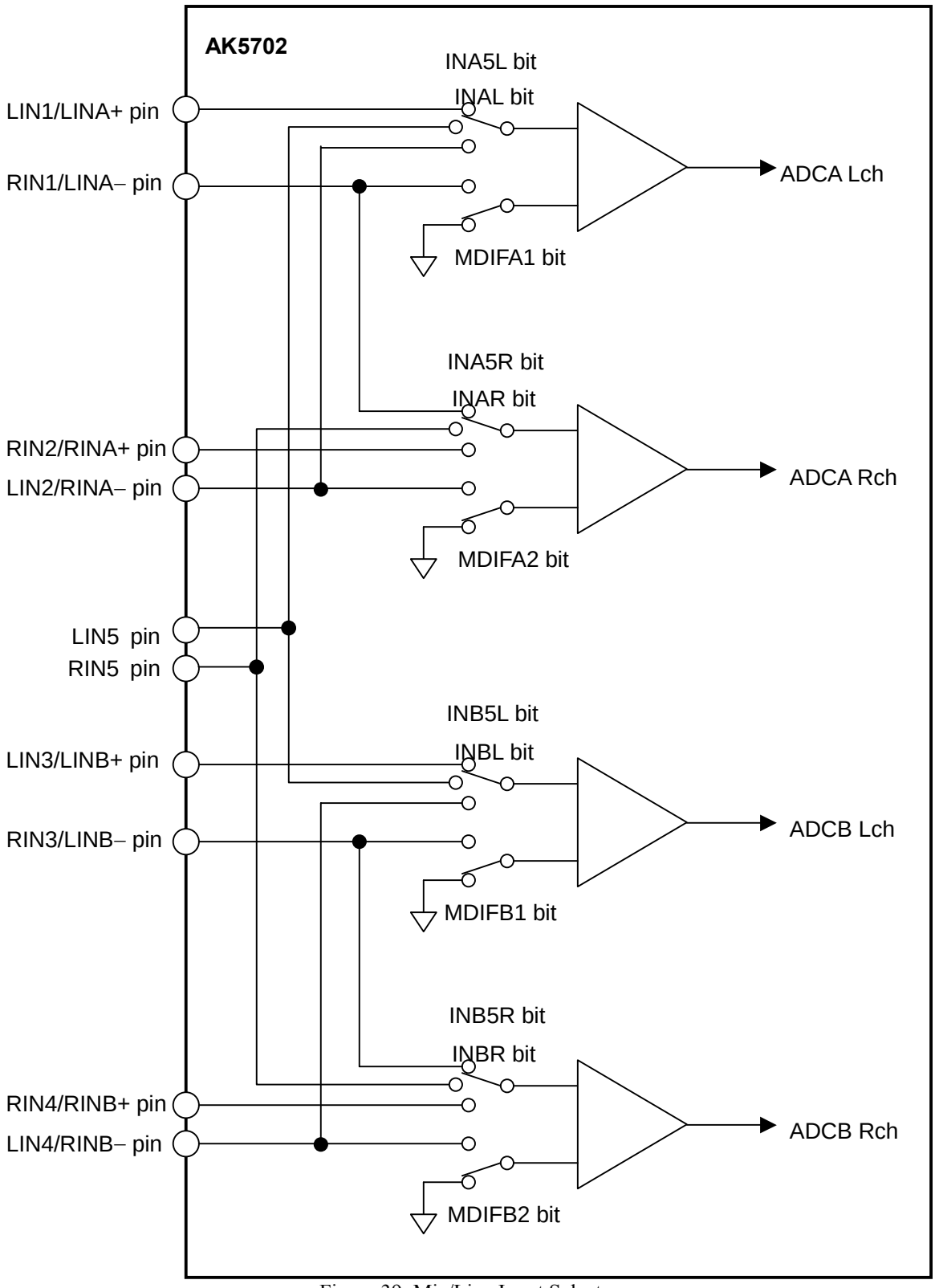


Figure 39. Mic/Line Input Selector

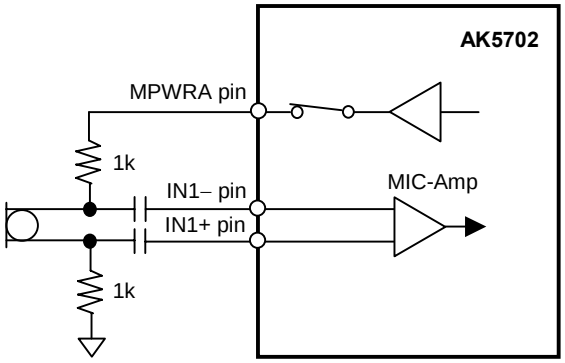


Figure 40. Connection Example for Full-differential Mic Input (MDIFA1/2 bits = "1")

MGAINA1-0 bits	MGAINB1-0 bits	ADCA Input	ADCB Input	Input Resistance (typ)
00	00	LIN5/RIN5	LIN5/RIN5	30kΩ
00	Don't care	LIN5/RIN5	LIN3-4/RIN3-4	
Don't care	00	LIN1-2/RIN1-2	LIN5/RIN5	
00	01,10,11	LIN5/RIN5	LIN5/RIN5	20kΩ
01,10,11	00	LIN5/RIN5	LIN5/RIN5	
01,10,11	Don't care	LIN5/RIN5	LIN3-4/RIN3-4	
Don't care	01,10,11	LIN1-2/RIN1-2	LIN5/RIN5	
01,10,11	01,10,11	LIN5/RIN5	LIN5/RIN5	15kΩ

Table 24. Input Resistance of LIN5, RIN5

■ MIC Gain Amplifier

The AK5702 has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAINA1-0, MGAINB1-0 bits (Table 25). The typical input impedance of LIN1-4 and RIN1-4 is 60kΩ(typ)@MGAINA1-0, MGAINB1-0 bits = "00" or 30kΩ(typ)@MGAIN1-0 bits = "01", "10" or "11". Refer to Table 24 about the typical input resistance of LIN5, RIN5.

MGAINA/B1 bit	MGAINA/B0 bit	Input Gain	
0	0	0dB	
0	1	+15dB	(default)
1	0	+30dB	
1	1	+36dB	

Table 25. Mic Input Gain

■ MIC Power

When PMMPA, PMMPB bits = "1", the MPWRA, MPWRB pins supplies power for the microphone. This output voltage is typically 0.75 x AVDD and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo mic, the load resistance is minimum 2kΩ for each channel. No capacitor must not be connected directly to MPWRA, MPWRB pins (Figure 41, Figure 42).

PMMPA/B bit	MPWRA/B pin	
0	Hi-Z	(default)
1	Output	

Table 26. MIC Power

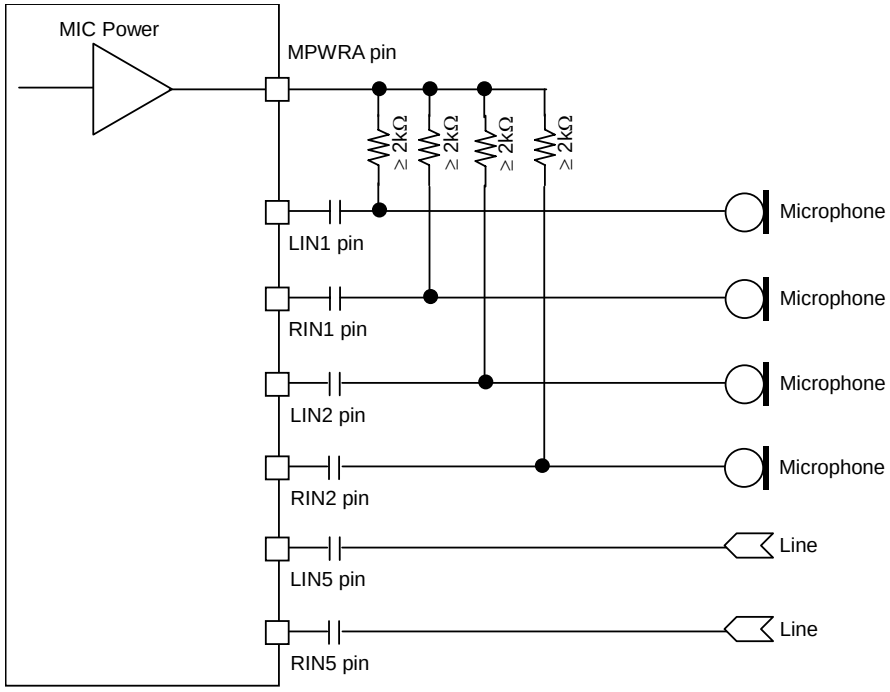


Figure 41. ADCA MIC Block Circuit MDIFA (MDIFA1=MDIFA2="0")

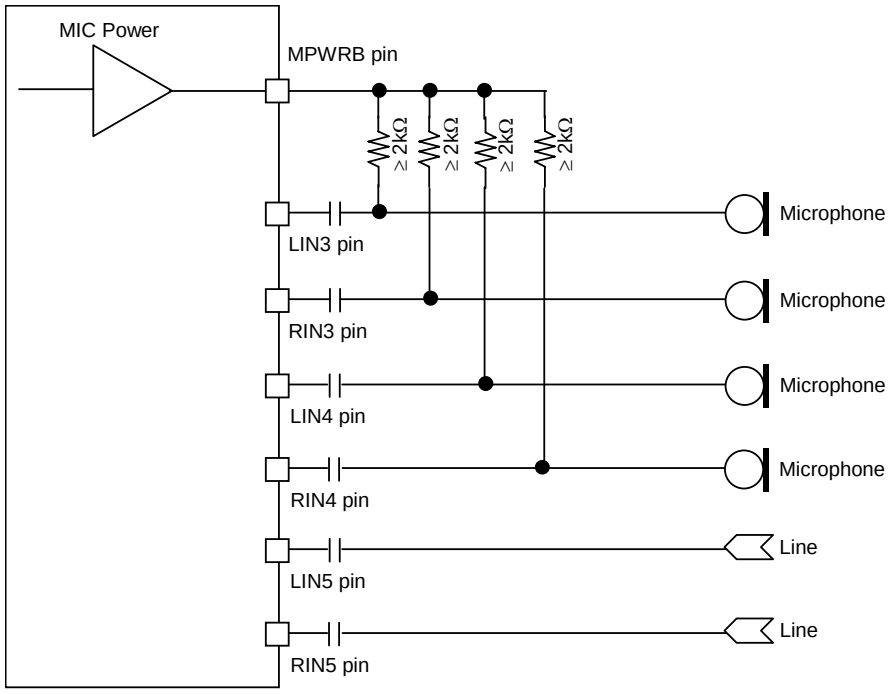


Figure 42. ADCB MIC Block Circuit MDIFB (MDIFB1=MDIFB2="0")

■ ALC Operation

When ALCA bit = "1", ALC operation is done for 2ch of ADCA. When ALCB bit = "1", ALC operation is done for 2ch of ADCB. Volumes of Lch and Rch always change in common during ALC operation. When ALC4 bit = "0", ALCA bit = ALCB bit = "1", ALC of ADCA and ADCB operate at the individual. When ALC4 bit = "1", regardless of the setting of ADCA bit and ADCB bit ,ALC operation is done for 4ch of ADCA and ADCB. Volumes of 4ch always change in common during 4ch Link ALC operation. During the 4ch Link ALC operation, the setting of ADCA resisters (LMTHA1-0, ZELMNA, LMATA1-0, ZTMA1-0, WTMA2-0, RGA1-0, REFA7-0, RFSTA1-0) are reflected to the setting of 4ch Link ALC resister, the set of ADCB (LMTHB1-0, ZELMNB, LMATB1-0, ZTMB1-0, WTMB2-0, RGB1-0, REFB7-0, RFSTB1-0) resisters are ignored.

1. ALC Limiter Operation

During the 2ch Link ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 28), the IVA/BL and IVA/BR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 29). During the 4ch Link ALC limiter operation, when even one of 4 channels of ADCA and ADCB exceeds the ALC limiter detection level (Table 28), the IVL and IVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step.

When ZELMNA/B bit = "0" (zero cross detection is enabled), the IVA/BL and IVA/BR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTMA/B1-0 bits set the zero crossing timeout periods of both ALC limiter and recovery operation (Table 30). When LFST bit = "1", if output level exceeds FS, volume is change to 1 step (Lch and Rch are change to same value) immediately (period: 1/fs), if output level dosen't exceed FS, volume is change to 1 step at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. When LFST bit = "1", LMATA/B 1-0 bits are recommended to set "00".

When ZELMNA/B bit = "1" (zero cross detection is disabled), IVA/BL and IVA/BR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless as the setting of LMATA/B1-0 bits.

The attenuation operation is done continuously until the input signal level becomes ALC limiter detection level (Table 27) or less. After completing the attenuation operation, unless operation is changed to manual, the operation repeats when the input signal level exceeds LMTHA/B1-0 bits.

Mode	ALC4	ALCB	ALCA	ALCB Operation	ALCA Operation	
0	0	0	0	Manual	Manual	(default)
1	0	0	1	Manual	2ch Link	
2	0	1	0	2ch Link	Manual	
3	0	1	1	2ch Link	2ch Link	
4	1	x	x	4ch Link	4ch Link	

Table 27. ALC mode

Note. ALC4 bit should be changed after ALCA=ALCB bits ="0" or PMADAL=PMADAR= PMADBL=PMADBR bits = "0". When ALC4 bit= "1", only either ADCA or ADCB should not be powered-down.

LMTHA/B1	LMTHA/B0	ALC Limier Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	(default)
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 28. ALC Limiter Detection Level / Recovery Counter Reset Level

ZELMNA/B	LMATA/B1	LMATA/B0	ALC Limiter ATT Step		
0	0	0	1 step	0.375dB	(default)
	0	1	2 step	0.750dB	
	1	0	4 step	1.500dB	
	1	1	8 step	3.000dB	
1	x	x	1step	0.375dB	

Table 29. ALC Limiter ATT Step

ZTMA/B1	ZTMA/B0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 30. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTMA/B2-0 bits (Table 31) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 28) during the wait time, the ALC recovery operation is done. The IVAL and IVAR values are automatically incremented by RGA/B1-0 bits (Table 32) up to the set reference level (Table 33) with zero crossing detection which timeout period is set by ZTMA/B1-0 bits (Table 30). Then the IVA/BL and IVA/BR are set to the same value for both channels. The ALC recovery operation is done at a period set by WTMA/B2-0 bits. If ZTMA/B1-0 is longer than WTMA/B2-0 and no zero crossing occurs, the ALC recovery operation is done at a period set by ZTMA/B1-0 bits.

For example, when the current IVOL value is 30H and RGA/B1-0 bits are set to "01", IVOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVOL value exceeds the reference level (REFA/B7-0), the IVOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTHA/B1-0) ≤ Output Signal < ALC limiter detection level (LMTHA/B1-0)"
during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTHA/B1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is setted by RFSTA/B1-0 bits (Table 34).

WTMA/B2	WTMA/B1	WTMA/B0		ALC Recovery Operation Waiting Period			
				8kHz	16kHz	44.1kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	
0	1	0	512/fs	64ms	32ms	11.6ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	

Table 31. ALC Recovery Operation Waiting Period

RGA/B1	RGA/B0	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 32. ALC Recovery GAIN Step

REFA/B7-0	GAIN(dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54.0		
00H	MUTE		

Table 33. Reference Level at ALC Recovery operation

RFSTA/B1 bit	RFSTA/B0 bit	Recovery Speed	
0	0	4 times	(default)
0	1	8 times	
1	0	16times	
1	1	N/A	

Table 34. Fast Recovery Speed Setting

3. Example of ALC Operation

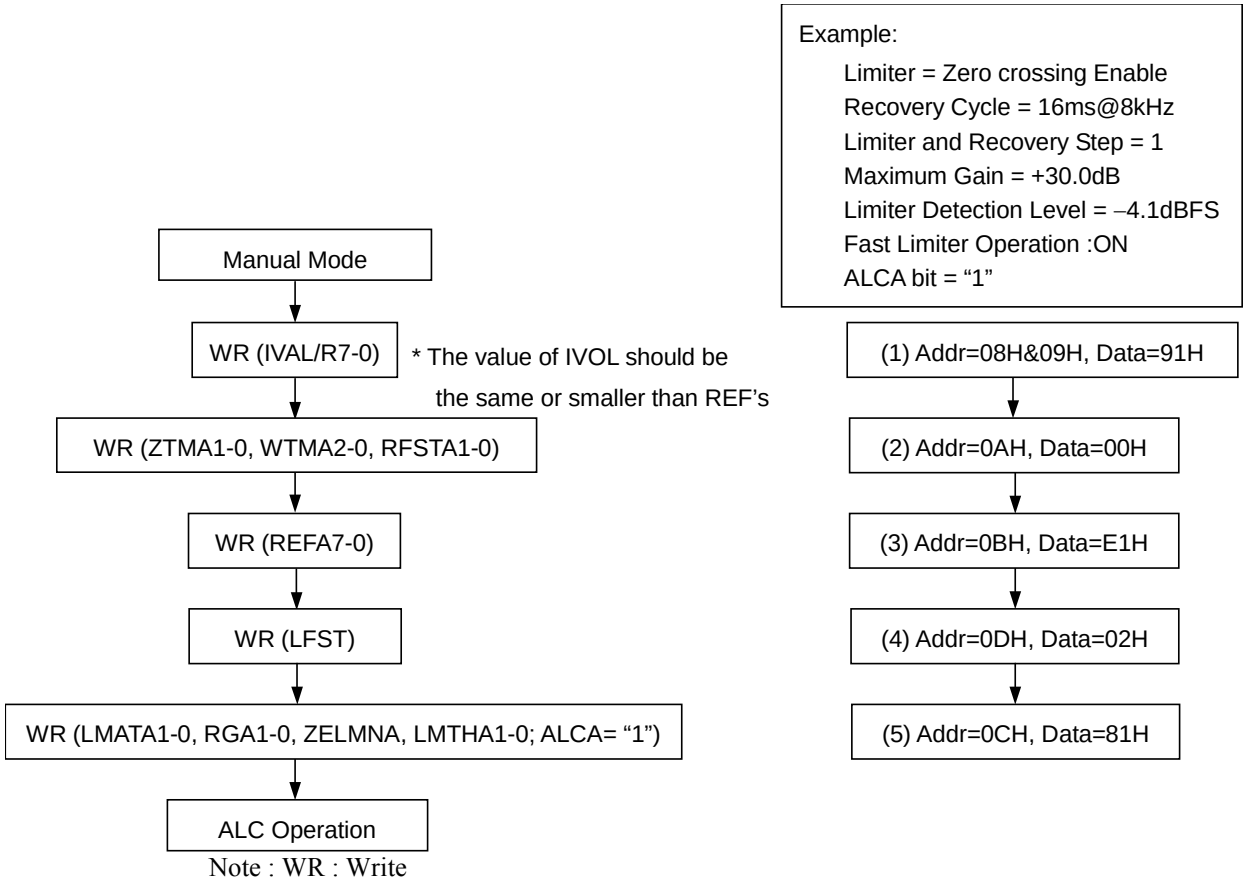
Table 35 shows the examples of the ALC setting for mic recording.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTHA/B1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMNA/B	Limiter zero crossing detection	0	Enable	0	Enable
ZTMA/B1-0	Zero crossing timeout period	00	16ms	11	23.2ms
WTMA/B2-0	Recovery waiting period *WTMA/B 2-0 bits should be the same data as ZTMA/B 1-0 bits	000	16ms	011	23.2ms
REFA/B7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVA/BL7-0, IVA/BR7-0	Gain of IVOL	91H	0dB	91H	0dB
LMATA/B1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGA/B1-0	Recovery GAIN step	00	1 step	00	1 step
RFSTA/B1_0	Fast Recovery Speed	00	4 times	00	4 times
ALCA/B	ALC enable	1	Enable	1	Enable

Table 35. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC4 bit = ALCA/B bit = “0” or PMADA/BL=PMADA/BR bits = “0”.

- **LMTHA/B1-0, LMATA/B1-0, WTMA/B2-0, ZTMA/B1-0, RGA/B1-0, REFA/B7-0, ZELMNA/B, LFST, RFSTA/B1-0**



Note : WR : Write

Figure 43. Registers set-up sequence at ALCA operation

■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC4 bit is "0" and ALCA/B bit is "0". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTMA/B1-0, LMTHA/B and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVA/BL7-0 and IVA/BR7-0 bits set the gain of the volume control (Table 36). The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTMA/B1-0 bits.

If IVA/BL7-0 or IVA/BR7-0 bits are written during PMADA/BL=PMADA/BR bits = "0", IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADA/BL or PMADA/BR bit is changed to "1".

IVA/BL7-0 IVA/BR7-0	GAIN (dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	–0.375		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 36. Input Digital Volume Setting

When writing to the IVA/BL7-0 and IVA/BR7-0 bits continuouslly, the control register should be written by an interval more than zero crossing timeout. If not, IVA/BL and IVA/BR are not changed since zero crossing counter is reset at every write operation. If the same register value as the previous write operation is written to IVA/BL and IVA/BR, this write operation is ignored and zero crossing counter is not reset. Therefore, IVA/BL and IVA/BR can be written by an interval less than zero crossing timeout.

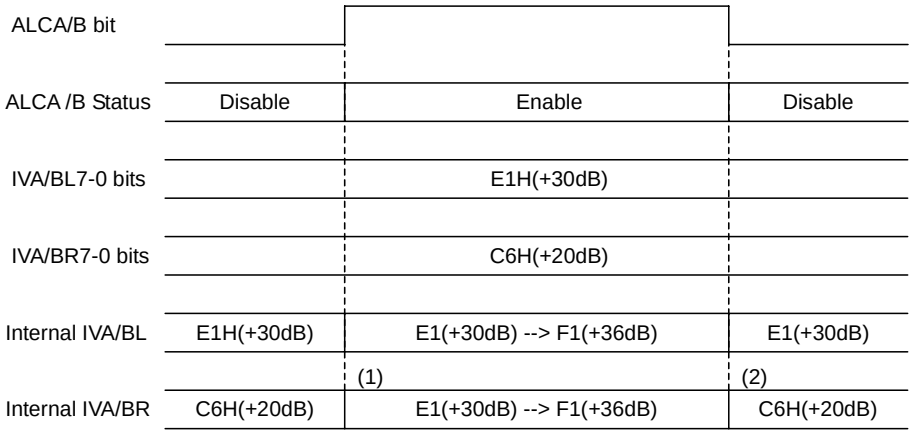


Figure 44. IVOL value during 2ch ALC operation

(1) The IVA/BL value becomes the start value if the IVA/BL and IVA/BR are different when the ALC starts. The wait time from ALC bit = "1" to ALC operation start by IVA/BL7-0 bits is at most recovery time (WTMA/B2-0 bits) plus zerocross timeout period (ZTMA/B1-0 bits).

(2) Writing to IVA/BL and IVA/BR registers (18H and 19H) is ignored during ALC operation. After ALC is disabled, the IVOL changes to the last written data by zero crossing or timeout. When ALC is enabled again, ALCA/B bit should be set to "1" by an interval more than zero crossing timeout period after ALCA/B bit = "0".

■ ALC 4ch Link Mode sequence

Figure 47 shows the 4ch Link ALC Mode sequence at ALCA bit = ALCB bit = "0"

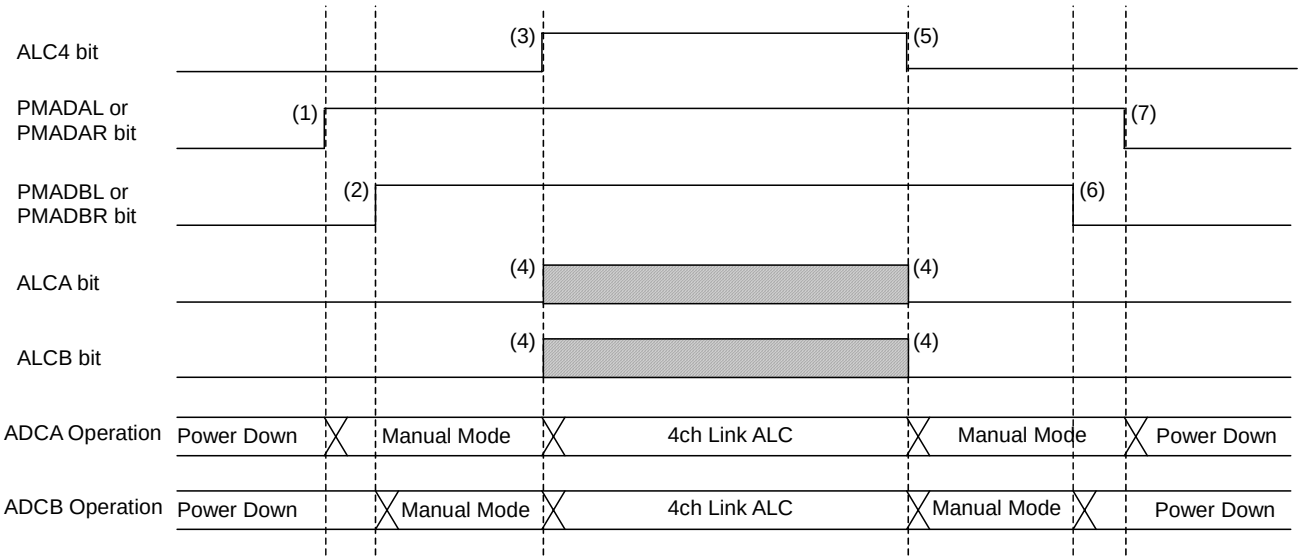


Figure 45. 4ch Link ALC Mode sequence

(1) ADCA is powered up by PMADAL bit or PMADAR bit is changed from "0" to "1".
(2) ADCB is powered up by PMADBL bit or PMADBR bit is changed from "0" to "1".
(3) Both ADCA and ADCB start 4ch Link ALC by ALC4 bit is changed from "0" to "1" at once. At this point the start value of ALC becomes Lch of ADCA (IVAL7-0 bits).
(4) When ALC4 bit = "1", ALCA bit and ALCB bit becomes invalid. But ALC4 bit should be "0", when it is changed.
(5) When ALC4 bit = "1" → "0", ADCA and ADCB become Manual Mode. 2ch link mode can be also set without power down operation by setting ALCA and ALCB bits = "1".
(6) ADCB is powered down by setting PMADBL bit or PMADBR bit "0".
(7) ADCA is powered down by setting PMADAL bit or PMADAR bit "0".

■ System Reset

Upon power-up, the AK5702 should be reset by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADAL or PMADAR or PMADBL or PMADBR bit is changed from "0" to "1". The initialization cycle time is 3088/fs=70.0ms@fs=44.1kHz when HPF1-0 bits are "00" (Table 37). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, "0". The ADC output reflects the analog input signal after the initialization cycle is complete.

(Note) The recommendaion values in Table 36 are the shortest cycle time that the offset does not occur. The initial data of ADC may have some offset by the external condition such as a use of microphone. If this offset isn't small, the longer initialization cycle should be selected as ADRSTbit="0" in order to prevent the offset data. Or, do not use the initial data of ADC.

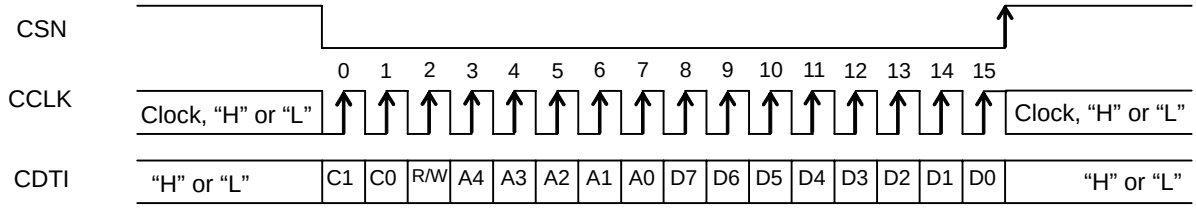
HPFA/B1 bit	HPFA/B0 bit	INCA/B bit	Init Cycle				
			Cycle	fs=44.1kHz	fs=22.05kHz	fs=11.025kHz	
0	0	0	3088/fs	70.0ms (Recommendation)	140.0ms	280.1ms	(default)
0	1	0	1552/fs	35.2ms	70.4ms (Recommendation)	140.8ms	
1	0	0	784/fs	17.8ms	35.6ms	71.1ms (Recommendation)	
1	1	0	3088/fs	70.0ms (Recommendation)	140.0ms	280.1ms	
1	1	1	1552/fs	35.2ms	70.4ms (Recommendation)	140.8ms	

Table 37. ADC Initialization Cycle

■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2C pin = "L")
Internal registers may be written by using the 3-wire μP interface pins (CSN, CCLK and CDTI).

The data on this interface consists of a 2-bit Chip address (2bits, "1x" x is designated by CAD0), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Address and data are latched on the 16th CCLK rising edge ("↑") after CSN falling edge("↓"). CSN should be set to "H" once after 16 CCLKs for each address. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by PDN pin = "L".



C1-C0: Chip Address (C1 = "1", C0 = CAD0)
R/W: READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A4-A0: Register Address
D7-D0: Control data

Figure 46. Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")
The AK5702 supports the fast-mode I²C-bus (max: 400kHz).

(2)-1. WRITE Operations
Figure 47 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 53). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pins (CAD1/0 pins) set these device address bits (Figure 48). If the slave address matches that of the AK5702, the AK5702 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 54). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5702. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 49). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 50). The AK5702 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 53).

The AK5702 can perform more than one byte write operation per sequence. After the receipt of the third byte the AK5702 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1CH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 55) except for the START and STOP conditions.

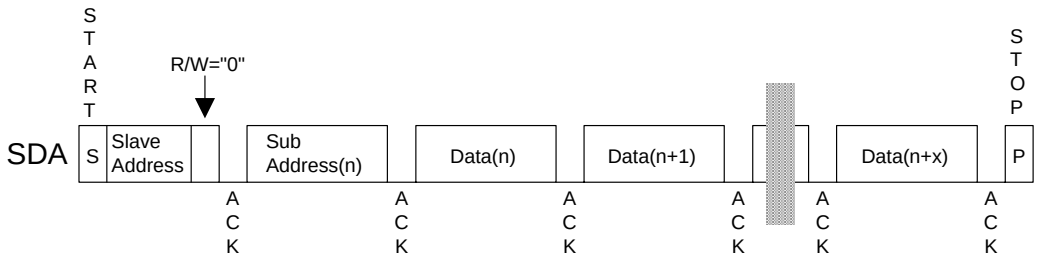


Figure 47. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins)
Figure 48. The First Byte

0	0	A5	A4	A3	A2	A1	A0

Figure 49. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 50. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK5702. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 1CH prior to generating a stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK5702 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK5702 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK5702 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK5702 ceases transmission.

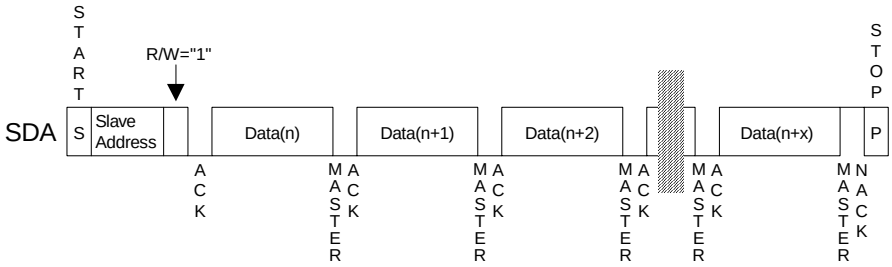


Figure 51. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK5702 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK5702 ceases transmission.

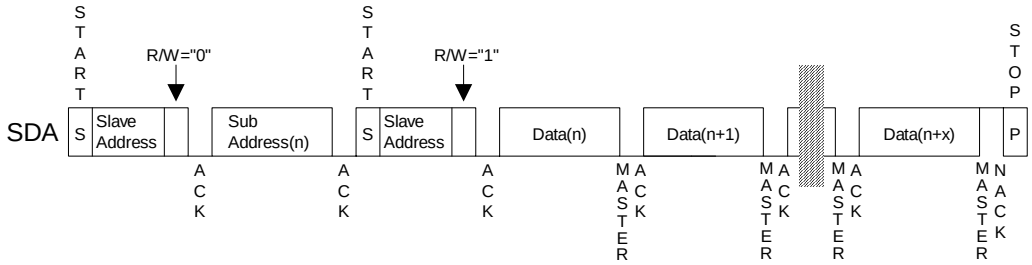


Figure 52. RANDOM ADDRESS READ

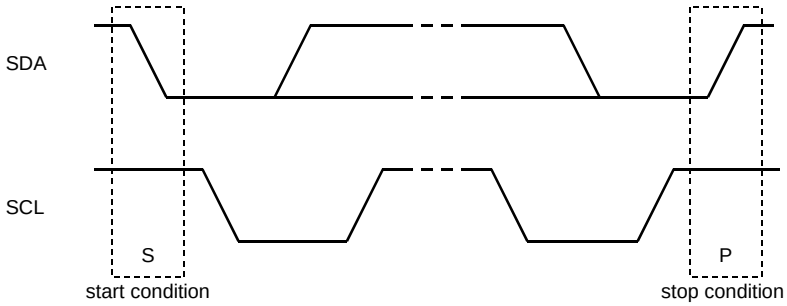


Figure 53. START and STOP Conditions

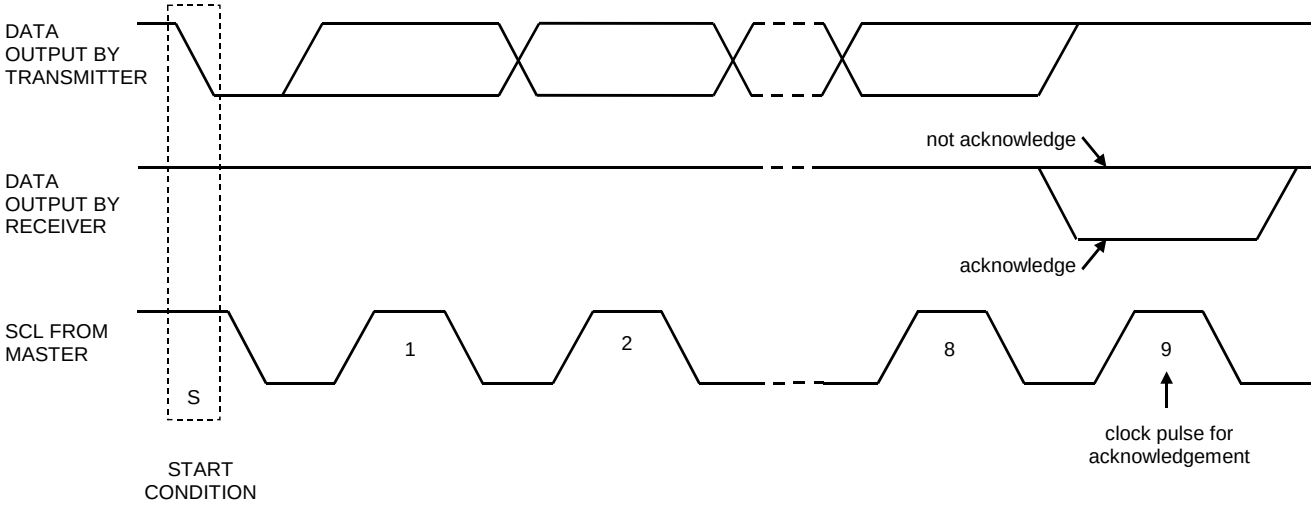


Figure 54. Acknowledge on the I^2C-Bus

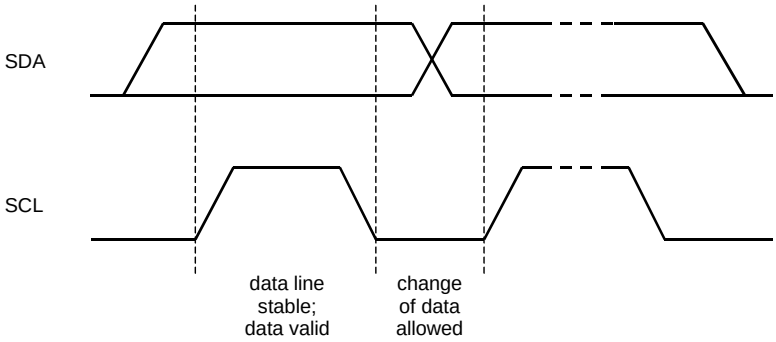


Figure 55. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	0	0	PMVCM	PMADAR	PMADAL
01H	PLL Control	0	0	PLL3	PLL2	PLL1	PLL0	M/S	PMPLL
02H	Signal Select	0	INA5R	INA5L	PMMPA	MDIFA2	MDIFA1	INAR	INAL
03H	Mic Gain Control	0	0	0	0	0	0	MGAINA1	MGAINA0
04H	Audio Format Select	TDM1	TDM0	1	MIXA	MSBS	BCKP	DIF1	DIF0
05H	fs Select	HPFA1	HPFA0	BCKO1	BCKO0	FS3	FS2	FS1	FS0
06H	Clock Output Select	INCA	0	0	0	0	MCKO	PS1	PS0
07H	Volume Control	0	0	0	0	0	0	0	IVOLAC
08H	Lch Input Volume Control	IVAL7	IVAL6	IVAL5	IVAL4	IVAL3	IVAL2	IVAL1	IVAL0
09H	Rch Input Volume Control	IVAR7	IVAR6	IVAR5	IVAR4	IVAR3	IVAR2	IVAR1	IVAR0
0AH	Timer Select	0	RFSTA1	RFSTA0	WTMA2	ZTMA1	ZTMA0	WTMA1	WTMA0
0BH	ALC Mode Control 1	REFA7	REFA6	REFA5	REFA4	REFA3	REFA2	REFA1	REFA0
0CH	ALC Mode Control 2	ALCA	ZELMNA	LMATA1	LMATA0	RGA1	RGA0	LMTHA1	LMTHA0
0DH	Mode Control 1	TE3	TE2	TE1	TE0	0	0	LFST	ALC4
0EH	Mode Control 2	0	0	0	0	0	0	TMASTER	0
0FH	Mode Control 3	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management	0	0	0	0	0	0	PMADBR	PMADBL
11H	PLL Control	0	0	0	0	0	0	0	0
12H	Signal Select	0	INB5R	INB5L	PMMPB	MDIFB2	MDIFB1	INBR	INBL
13H	Mic Gain Control	0	0	0	0	0	0	MGAINB1	MGAINB0
14H	Audio Format Select	0	0	1	MIXB	0	0	0	0
15H	fs Select	HPFB1	HPFB0	0	0	0	0	0	0
16H	Clock Output Select	INCB	0	0	0	0	0	0	0
17H	Volume Control	0	0	0	0	0	0	0	IVOLBC
18H	Lch Input Volume Control	IVBL7	IVBL6	IVBL5	IVBL4	IVBL3	IVBL2	IVBL1	IVBL0
19H	Rch Input Volume Control	IVBR7	IVBR6	IVBR5	IVBR4	IVBR3	IVBR2	IVBR1	IVBR0
1AH	Timer Select	0	RFSTB1	RFSTB0	WTMB2	ZTMB1	ZTMB0	WTMB1	WTMB0
1BH	ALC Mode Control 1	REFB7	REFB6	REFB5	REFB4	REFB3	REFB2	REFB1	REFB0
1CH	ALC Mode Control 2	ALCB	ZELMNB	LMATB1	LMATB0	RGB1	RGB0	LMTHB1	LMTHB0
1DH	Mode Control 1	0	0	0	0	0	0	0	0
1EH	Mode Control 2	0	0	0	0	0	0	0	0

Note 31. PDN pin = “L” resets the registers to their default values.
Note 32. “0” must be sent to the register written as “0” and “1” must be sent to the register written as “1”.
For the address 1FH, data must not be written.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	0	0	PMVCM	PMADAR	PMADAL
Default		0	0	0	0	0	0	0	0

PMADAL: MIC-AmpA Lch and ADCA Lch Power Management
0: Power down (default)
1: Power up

PMADAR: MIC-AmpA Rch and ADCA Rch Power Management
0: Power down (default)
1: Power up
When the PMADAL or PMADAR bit is changed from "0" to "1", the initialization cycle (3088/fs=70.0ms @fs= 44.1kHz, HPFA1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMVCM: VCOM Power Management
0: Power down (default)
1: Power up
When any blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be set to "0" only when PMADAL=PMADAR= PMADBL=PMADBR =PMPLL=PMMPA=PMMPB=MCKO bits = "0".

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When PMVCM, PMADAL, PMADAR, PMADBL, PMADBR, PMPLL, PMPLL, PMMPA,PMMPB and MCKO bits are "0", all blocks are powered-down. The register values remain unchanged.

When the all ADC is powered-down, external clocks may not be present. When one of the ADC is powered -up, external clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Control	0	0	PLL3	PLL2	PLL1	PLL0	M/S	PMPLL
Default		0	0	1	0	0	1	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power Down (default)
1: PLL Mode and Power up

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

PLL3-0: PLL Reference Clock Select (Table 4)
Default: "1001" (MCKI pin=12MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select	0	INA5R	INA5L	PMMPA	MDIFA2	MDIFA1	INAR	INAL
	Default	0	0	0	0	0	0	0	0

INAL: ADCA Lch Input Source Select
0: LIN1 pin (default)
1: LIN2 pin

INAR: ADCA Rch Input Source Select
0: RIN1 pin (default)
1: RIN2 pin

MDIFA1: ADCA Lch Input Type Select
0: Single-ended input (LIN1/LIN2/LIN5 pin: Default)
1: Full-differential input (LINA+/LINA– pin)

MDIFA2: ADCA Rch Input Type Select
0: Single-ended input (RIN1/RIN2/RIN5 pin: Default)
1: Full-differential input (RINA+/RINA– pin)

PMMPA: MPWRA pin Power Management
0: Power down: Hi-Z (default)
1: Power up

INA5L: ADCA Lch Input Source Select
0: LIN1 or LIN2 pin (default)
1: LIN5 pin

INA5R: ADCA Rch Input Source Select
0: RIN1 or RIN2 pin (default)
1: RIN5 pin

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mic Gain Control	0	0	0	0	0	0	MGAINA1	MGAINA0
	Default	0	0	0	0	0	0	0	1

MGAINA1-0: MIC-AmpA Gain Control (Table 25)
Default: “01” (+15dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Audio Format Select	TDM1	TDM0	1	MIXA	MSBS	BCKP	DIF1	DIF0
Default		0	0	1	0	0	0	1	1

DIF1-0: Audio Interface Format (Table 14)
Default: "11" (I^2S)

BCKP: BCLK/BCLK Polarity at DSP Mode (Table 17)
0: SDTO is output by the rising edge ("↑") of BCLK/BCLK. (default)
1: SDTO is output by the falling edge ("↓") of BCLK/BCLK.

MSBS: LRCK/LRCK Phase at DSP Mode (Table 17)
0: The rising edge ("↑") of LRCK/LRCK is half clock of BCLK/BCLK before the channel change. (default)
1: The rising edge ("↑") of LRCK/LRCK is one clock of BCLK/BCLK before the channel change.

MIXA: ADCA Output Data Select (Table 18)
0: Normal operation (default)
1: (L+R)/2

TDM1-0: TDM Format Select (Table 14, Table 15 Table 16)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	fs Select	HPFA1	HPFA0	BCKO1	BCKO0	FS3	FS2	FS1	FS0
Default		0	0	0	1	1	1	1	1

FS3-0: Sampling Frequency Select (Table 5 and Table 6) and MCKI Frequency Select (Table 11)
Default: "1111" (44.1kHz)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

BCKO1-0: BCLK Output Frequency Select at Master Mode (Table 10)
Default: "01" (32fs)

HPFA1-0: Offset Cancel HPF Cut-off Frequency and ADCA Initialization Cycle (Table 20, Table 37)
Default: "00" (fc=3.4Hz@fs=44.1kHz, Init Cycle=3088/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Clock Output Select	INCA	0	0	0	0	MCKO	PS1	PS0
Default		0	0	0	0	0	0	0	0

INCA: ADCA Initialization Cycle (Table 37)
0: When HPFA1-0 bits = "00", "01", "10", INCA bit is invalid, when HPFA1-0 bits = "11", ADCA Initialization Cycle becomes 3088/fs.
1: When HPFA1-0 bits = "00", "01", "10", INCA bit is invalid, when HPFA1-0 bits = "11", ADCA Initialization Cycle becomes 1552/fs.

PS1-0: MCKO Output Frequency Select (Table 9)
Default: "00" (256fs)

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Volume Control	0	0	0	0	0	0	0	IVOLAC
	Default	0	0	0	0	0	0	0	1

IVOLAC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLAC bit = "1", IVAL7-0 bits control both Lch and Rch volume level, while register values of IVAL7-0 bits are not written to IVAR7-0 bits. When IVOLC bit = "0", IVAL7-0 bits control Lch level and IVAR7-0 bits control Rch level, respectively.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Lch Input Volume Control	IVAL7	IVAL6	IVAL5	IVAL4	IVAL3	IVAL2	IVAL1	IVAL0
09H	Rch Input Volume Control	IVAR7	IVAR6	IVAR5	IVAR4	IVAR3	IVAR2	IVAR1	IVAR0
	Default	1	0	0	1	0	0	0	1

IVAL7-0, IVAR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 36)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Timer Select	0	RFSTA1	RFSTA0	WTMA2	ZTMA1	ZTMA0	WTMA1	WTMA0
	Default	0	0	0	0	0	0	0	0

WTM2-0: ALCA Recovery Waiting Period (Table 31)
Default: "00" (128/fs)
A period of recovery operation when any limiter operation does not occur during the ALCA operation.

ZTM1-0: ALCA Limiter/Recovery Operation Zero Crossing Timeout Period (Table 30)
Default: "00" (128/fs)
When the IVOL perform zero crossing or timeout, the IVOL value is changed by the μP WRITE operation, ALCA recovery operation.

RFSTA1-0: ALCA First recovery Speed (Table 34)
Default: "00" (4times)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	REFA7	REFA6	REFA5	REFA4	REFA3	REFA2	REFA1	REFA0
	Default	1	1	1	0	0	0	0	1

REFA7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 33)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	ALCA	ZELMNA	LMATA1	LMATA0	RGA1	RGA0	LMTHA1	LMTHA0
Default		0	0	0	0	0	0	0	0

LMTHA1-0: ALCA Limiter Detection Level / Recovery Counter Reset Level (Table 28)
Default: "00"

RGA1-0: ALCA Recovery GAIN Step (Table 32)
Default: "00"

LMATA1-0: ALCA Limiter ATT Step (Table 29)
Default: "00"

ZELMNA: Zero Crossing Detection Enable at ALCA Limiter Operation
0: Enable (default)
1: Disable

ALCA: ALC Enable
0: ALCA Disable (default)
1: ALCA Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Mode Control 1	TE3	TE2	TE1	TE0	0	0	LFST	ALC4
Default		1	0	1	0	0	0	0	0

ALC4: All ALCs Link Mode Enable
0: Disable (default)
1: All ALCs of 4-channel ADC operate at the same time.

LFST: ALC Limiter Operation Beyond FS
0: At the Individual Zero Crossing Points or at the Zero Crossing Timeout (default)
1: Immediately

TE3-0: EXT Master Mode Enable
When TE3-0 bits is set to "0101", the write operation to addr=0EH is enabled.
TE3-0 bits should be set to "1010" except for EXT Master Mode.
TE3-0 bits must not be set to the value except for "1010" and "0101".
Default: "1010"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Mode Control 2	0	0	0	0	0	0	TMASTER	0
Default		0	0	0	0	0	0	0	0

TMASTER: EXT Master Mode
The write operation to TMASTER bit is enabled when TE3-0 bits = "0101".
0: Except EXT Master Mode (default)
1: EXT Master Mode
In TDM mode at master operation, LRCK can be output by writing "1" at TMASTER bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management	0	0	0	0	0	0	PMADBR	PMADBL
Default		0	0	0	0	0	0	0	0

PMADBL: MIC-AmpB Lch and ADCB Lch Power Management
0: Power down (default)
1: Power up

PMADBR: MIC-AmpB Rch and ADCB Rch Power Management
0: Power down (default)
1: Power up
When the PMADBL or PMADBR bit is changed from "0" to "1", the initialization cycle (3088/fs=70.0ms @fs= 44.1kHz, HPFA1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Signal Select	0	INB5R	INB5L	PMMPB	MDIFB2	MDIFB1	INBR	INBL
Default		0	0	0	0	0	0	0	0

INBL: ADCB Lch Input Source Select
0: LIN3 pin (default)
1: LIN4 pin

INBR: ADCB Rch Input Source Select
0: RIN3 pin (default)
1: RIN4 pin

MDIFB1: ADCB Lch Input Type Select
0: Single-ended input (LIN3/LIN4/LIN5 pin: Default)
1: Full-differential input (LINB+/LINB– pin)

MDIFB2: ADCB Rch Input Type Select
0: Single-ended input (RIN3/RIN4/RIN5 pin: Default)
1: Full-differential input (RINB+/RINB– pin)

PMMPB: MPWRB pin Power Management
0: Power down: Hi-Z (default)
1: Power up

INB5L: ADCB Lch Input Source Select
0: LIN3 or LIN4 pin (default)
1: LIN5 pin

INB5R: ADCB Rch Input Source Select
0: RIN3 or RIN4 pin (default)
1: RIN5 pin

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Mic Gain Control	0	0	0	0	0	0	MGAINB1	MGAINB0
Default		0	0	0	0	0	0	0	1

MGAINB1-0: MIC-AmpB Gain Control (Table24)
Default: "01" (+15dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	Audio Format Select	0	0	1	MIXB	0	0	0	0
	Default	0	0	1	0	0	0	0	0

MIXB: ADCB Output Data Select (Table 19)
0: Normal operation (default)
1: (L+R)/2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	fs Select	HPFB1	HPFB0	0	0	0	0	0	0
	Default	0	0	0	0	0	0	0	0

HPFB1-0: Offset Cancel HPF Cut-off Frequency and ADCB Initialization Cycle (Table 21, Table 37)
Default: "00" (fc=3.4Hz@fs=44.1kHz, Init Cycle=3088/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Clock Output Select	INCB	0	0	0	0	0	0	0
	Default	0	0	0	0	0	0	0	0

INCB: ADCB Initialization Cycle (Table 37)
0: When HPFB1-0 bits = "00", "01", "10", INCA bit is invalid, when HPFB1-0 bits = "11", ADCB Initialization Cycle becomes 3088/fs.
1: When HPFB1-0 bits = "00", "01", "10", INCA bit is invalid, when HPFB1-0 bits = "11", ADCB Initialization Cycle becomes 1552/fs.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	Volume Control	0	0	0	0	0	0	0	IVOLBC
	Default	0	0	0	0	0	0	0	1

IVOLBC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLBC bit = "1", IVBL7-0 bits control both Lch and Rch volume level, while register values of IVBL7-0 bits are not written to IVBR7-0 bits. When IVOLC bit = "0", IVBL7-0 bits control Lch level and IVBR7-0 bits control Rch level, respectively.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Lch Input Volume Control	IVBL7	IVBL6	IVBL5	IVBL4	IVBL3	IVBL2	IVBL1	IVBL0
19H	Rch Input Volume Control	IVBR7	IVBR6	IVBR5	IVBR4	IVBR3	IVBR2	IVBR1	IVBR0
	Default	1	0	0	1	0	0	0	1

IVBL7-0, IVBR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 36)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Timer Select	0	RFSTB1	RFSTB0	WTMB2	ZTMB1	ZTMB0	WTMB1	WTMB0
	Default	0	0	0	0	0	0	0	0

WTM2-0: ALCB Recovery Waiting Period (Table 31)
Default: "00" (128/fs)
A period of recovery operation when any limiter operation does not occur during the ALCB operation.

ZTM1-0: ALCB Limiter/Recovery Operation Zero Crossing Timeout Period (Table 30)
Default: "00" (128/fs)
When the IVOL perform zero crossing or timeout, the IVOL value is changed by the μP WRITE operation, ALCB recovery operation.

RFSTB1-0: ALCB First recovery Speed (Table 34)
Default: "00"(4times)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	ALC Mode Control 1	REFB7	REFB6	REFB5	REFB4	REFB3	REFB2	REFB1	REFB0
	Default	1	1	1	0	0	0	0	1

REFB7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 33)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	ALC Mode Control 2	ALCB	ZELMNB	LMATB1	LMATB0	RGB1	RGB0	LMTHB1	LMTHB0
	Default	0	0	0	0	0	0	0	0

LMTHB1-0: ALCBB Limiter Detection Level / Recovery Counter Reset Level (Table 28)
Default: "00"

RGB1-0: ALCB Recovery GAIN Step (Table 32)
Default: "00"

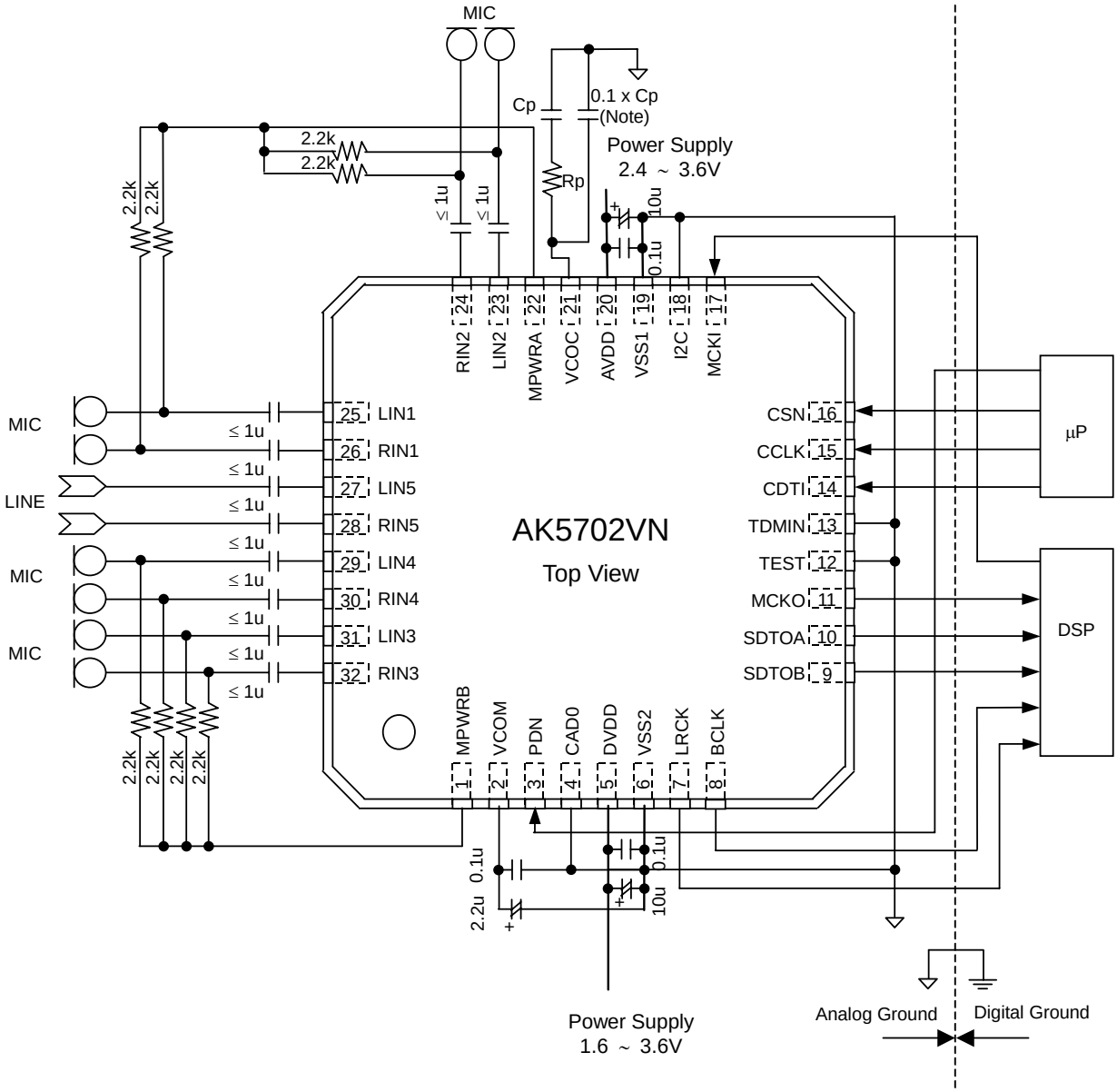
LMATB1-0: ALCB Limiter ATT Step (Table 29)
Default: "00"

ZELMNB: Zero Crossing Detection Enable at ALCB Limiter Operation
0: Enable (default)
1: Disable

ALCB: ALC Enable
0: ALCB Disable (default)
1: ALCB Enable

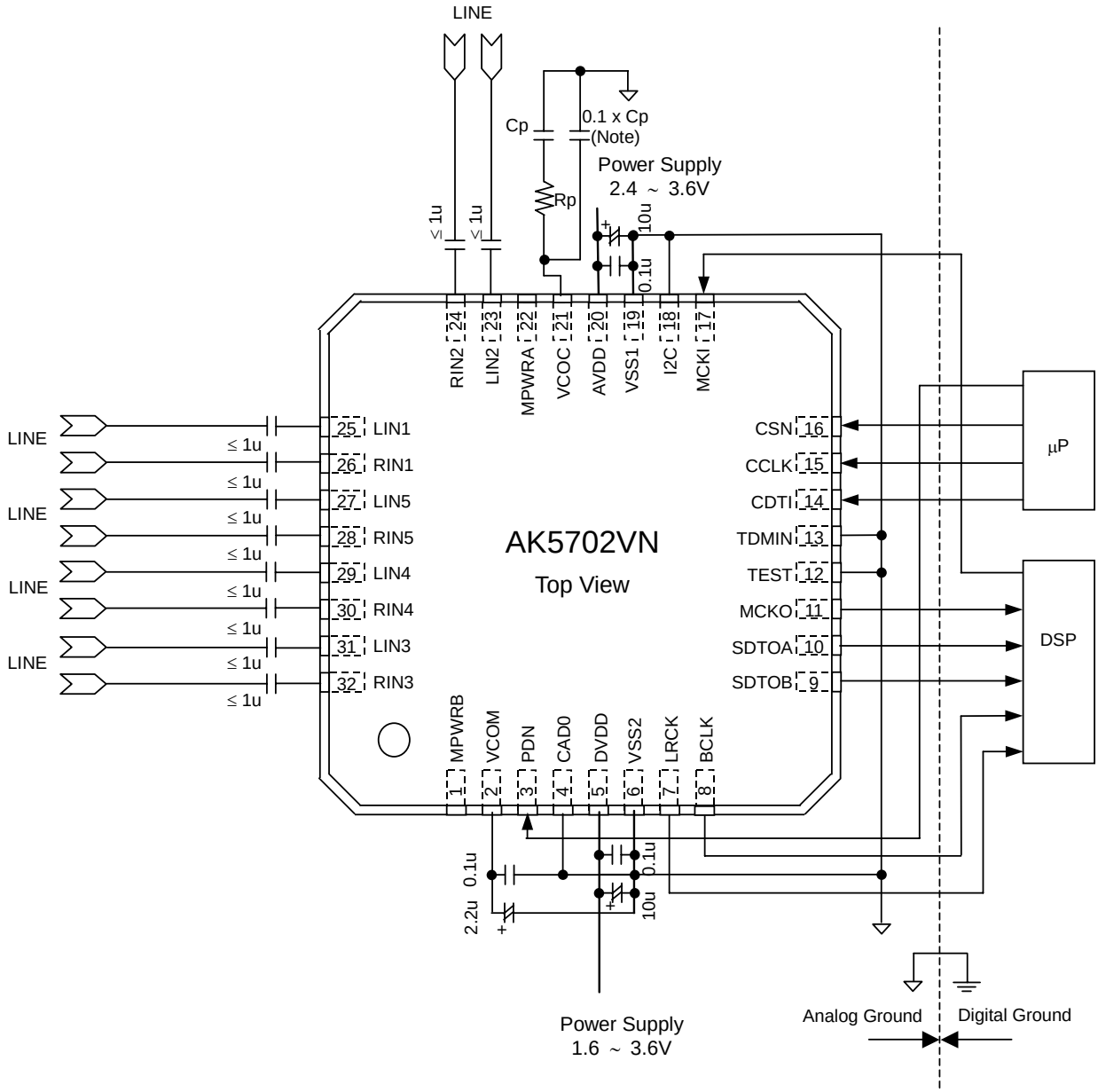
SYSTEM DESIGN

Figure 56, Figure 57, Figure 58shows the system connection diagram for the AK5702. An evaluation board [AKD5702] is available which demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:
- VSS1 and VSS2 of the AK5702 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK5702 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK5702 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 4. 0.1 x Cp in parallel with Cp+Rp improves PLL jitter characteristics.
- Mic input AC coupling capacitor should be 1μF or less to start the recording within 100ms.

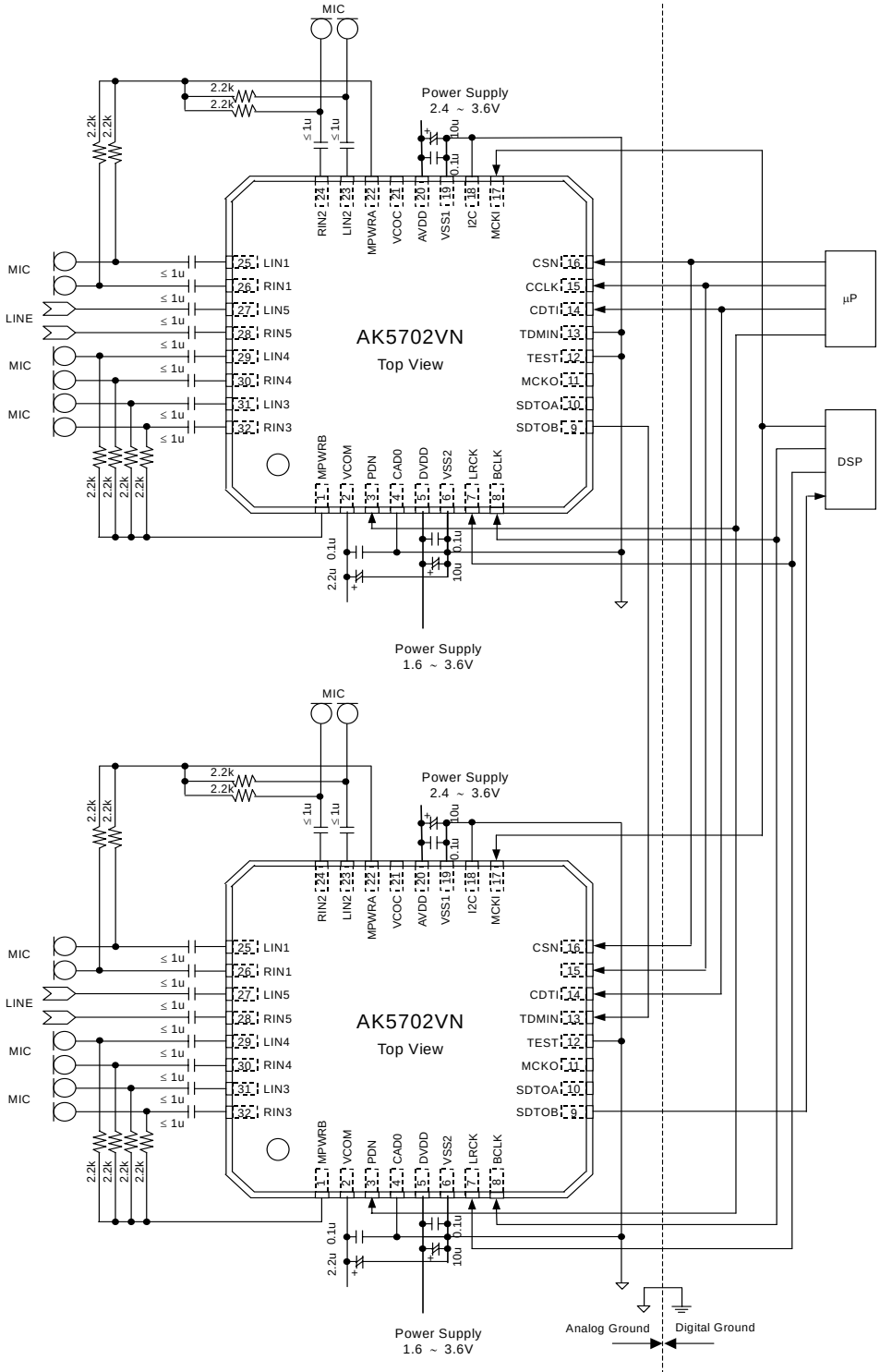
Figure 56. Typical Connection Diagram (MIC Input)



Notes:

- VSS1 and VSS2 of the AK5702 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK5702 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK5702 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 4. 0.1 x Cp in parallel with Cp+Rp improves PLL jitter characteristics.

Figure 57. Typical Connection Diagram (Line Input)



Notes:

- VSS1 and VSS2 of the AK5702 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK5702 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.

Figure 58. Typical Connection Diagram (Cascode TDM)

1. Grounding and Power Supply Decoupling

The AK5702 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from the system's analog supply. If AVDD and DVDD are supplied separately, the power-up sequence is not critical. VSS1 and VSS2 of the AK5702 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5702 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5702.

3. Analog Inputs

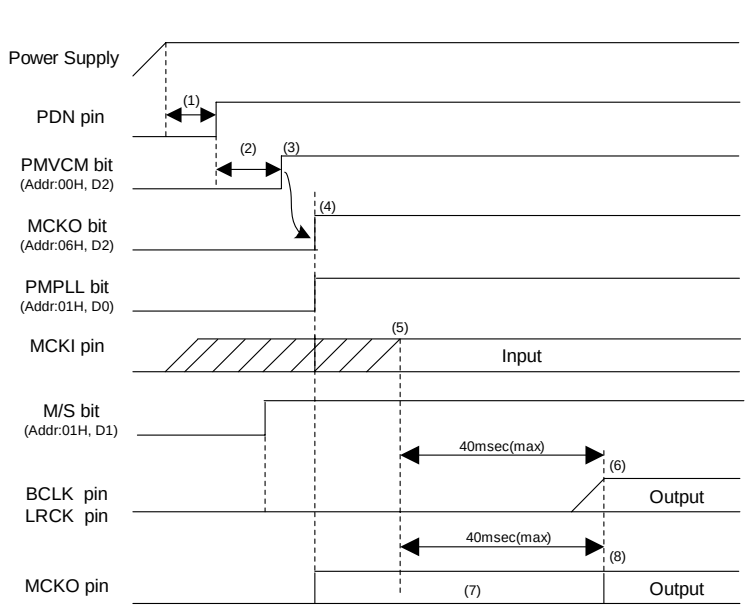
The analog inputs are single-ended or full-differential and input resistance is 60kΩ (typ)@MGAIN1-0 bits = "00", 30kΩ (typ)@MGAIN1-0 bits = "01", "10" or "11". The input signal range scales with 0.6 x AVDD Vpp(typ)@MGAIN 1-0 bits = "00" centered around the internal common voltage (0.5 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is fc = 1/ (2πRC). The ADC output data format is 2's complement. The DC offset including the ADC's own DC offset is removed by the internal HPF (fc=3.4Hz@ HPF1-0 bits = "00", fs=44.1kHz). The AK5702 can accept input voltages from VSS1 to AVDD at single-ended.

CONTROL SEQUENCE

■ Clock Set up

When ADC is powered-up, the clocks must be supplied.

1. PLL Master Mode.



Example:

Audio I/F Format: I2S
BCLK frequency at Master Mode: 64fs
Input Master Clock Select at PLL Mode: 11.2896MHz
MCKO: Enable
Sampling Frequency: 44.1kHz

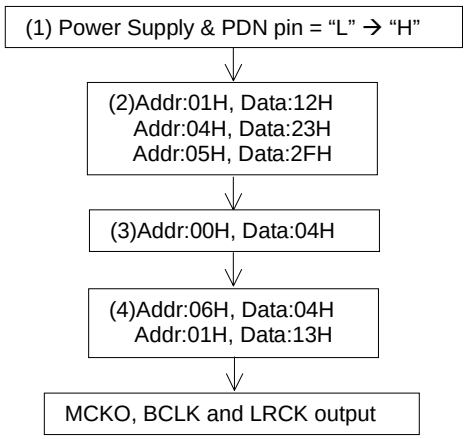


Figure 59. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5702.

(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0 and M/S bits should be set during this period as follows.
(2a) M/S bit = "1" and setting of PLL3-0, FS3-0, BCKO1-0 bits.
(2b) Setting of DIF1-0 bits.

(3) Power UpVCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.

(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(5) PLL operation starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source. PLL lock time is 40ms(max) at MCKI=12MHz (Table 4).

(6) The AK5702 starts to output the LRCK and BCLK clocks after the PLL becomes stable. Then normal operation starts.

(7) The invalid frequency is output from MCKO pin during this period if MCKO bit = "1".

(8) The normal clock is output from MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (LRCK or BCLK pin)

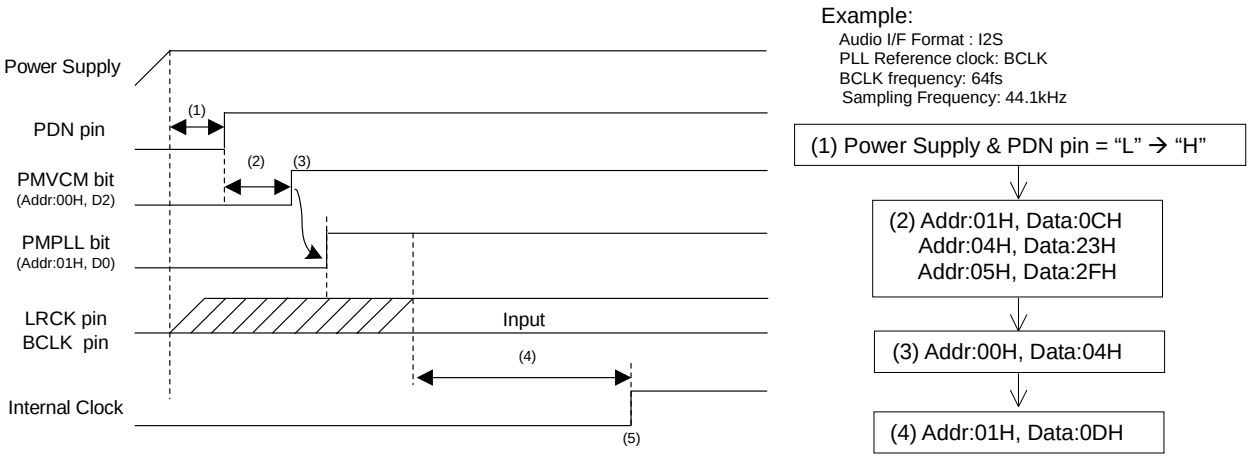


Figure 60. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5702.

(2) DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (LRCK or BCLK pin) is supplied. PLL lock time is 160ms(max) when LRCK is a PLL reference clock. PLL lock time is 2ms(max) when BCLK is a PLL reference clock and the external circuit at VCOC pin is 10k+4.7nF (Table 4).

(5) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

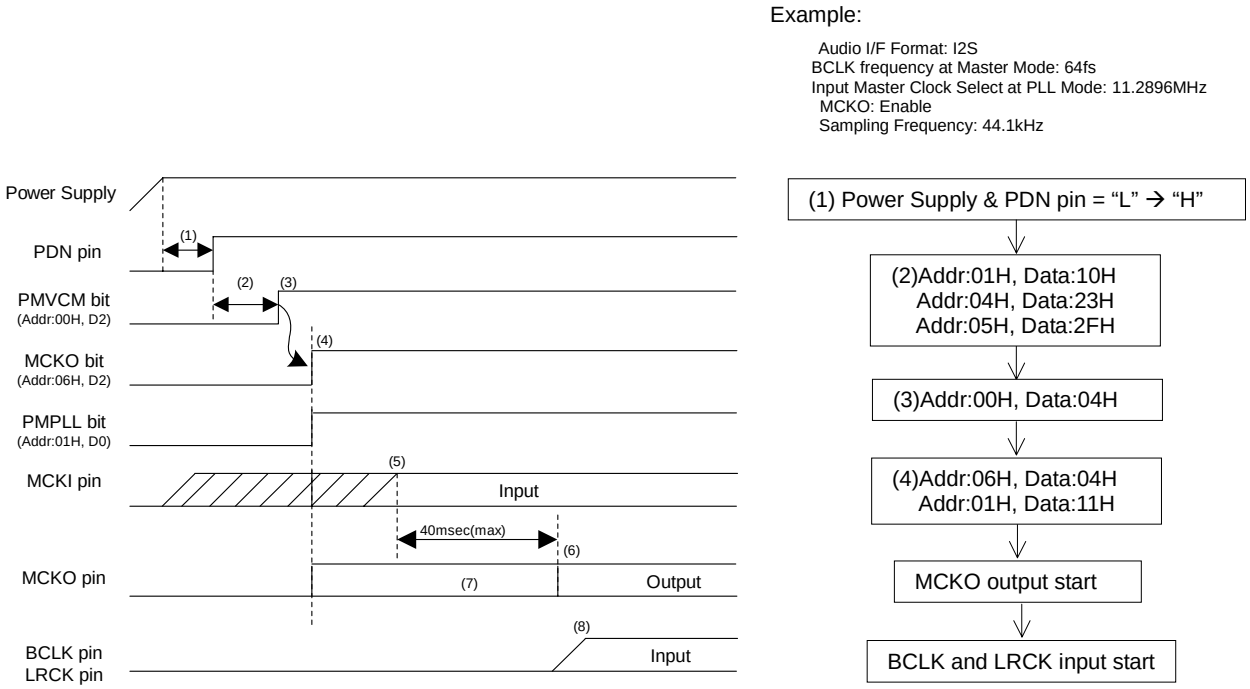


Figure 61. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5702.
(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0 and M/S bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Enable MCKO output: MCKO bit = "1"
(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.
PLL lock time is 40ms(max) at MCKI=12MHz (Table 4).
(6) The normal clock is output from MCKO after PLL is locked.
(7) The invalid frequency is output from MCKO during this period.
(8) BCLK and LRCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

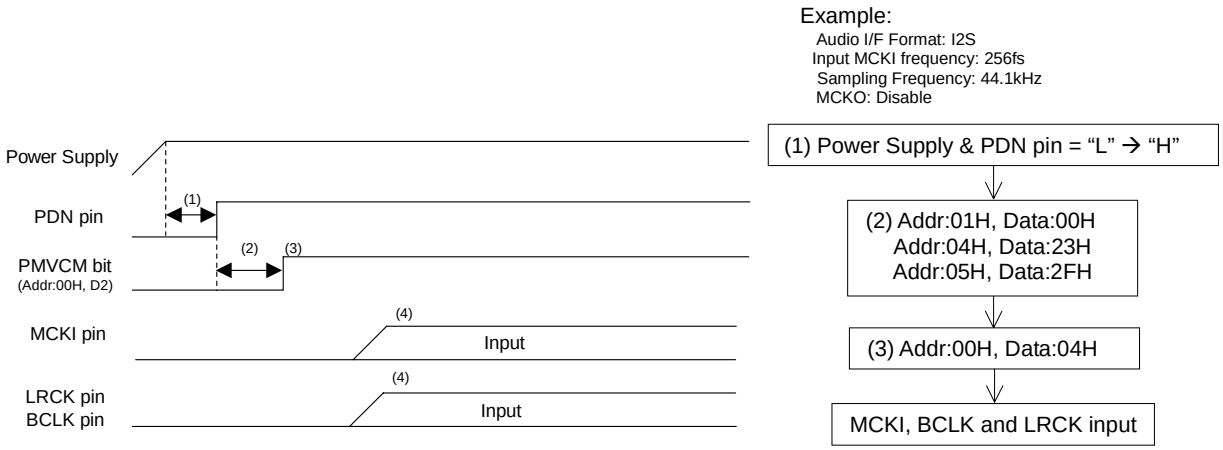


Figure 62. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5702.

(2) DIF1-0 and FS1-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) Normal operation starts after the MCKI, LRCK and BCLK are supplied.

5. EXT Master Mode

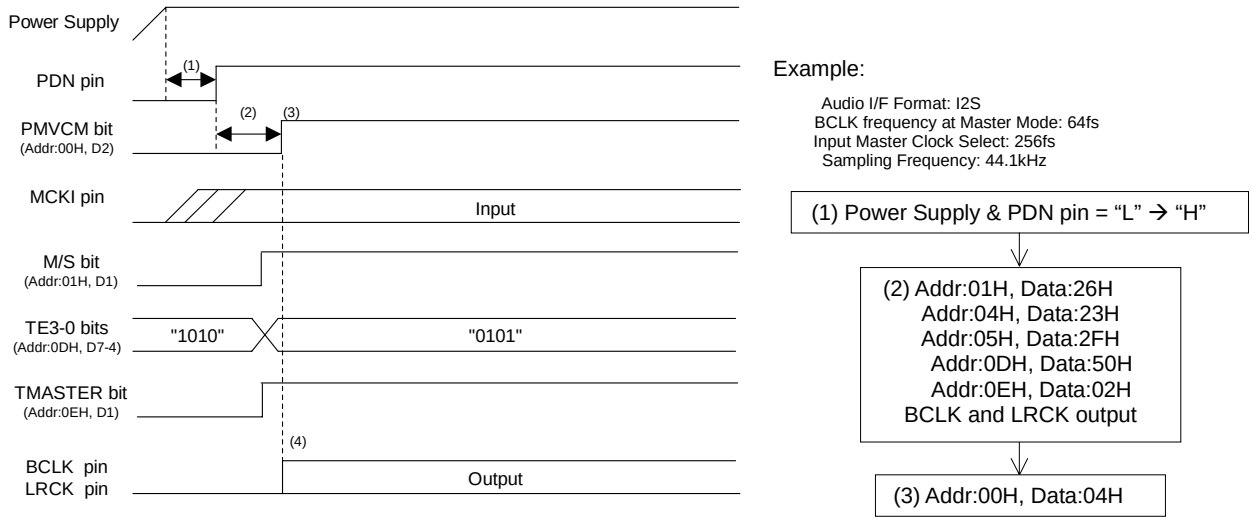


Figure 63. Clock Set Up Sequence (5)

<Example>
(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5702.
(2) DIF1-0, FS1-0, BCKO1-0, M/S, TE3-0 and TMASTER bits should be set during this period as follows.
(2a) M/S bit = "1", setting of FS3-0 and BCKO1-0 bits.
(2b) Setting of DIF1-0 bits.
(2c) TE3-0 bits = "0101"
(2d) TMASTER bit = "1"
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) BCLK and LRCK start to output.

When the clock mode is changed from EXT Master Mode to other modes, the register should be set as above table after PDN pin = "L" to "H" or TE3-0 bits = "1010".

■ MIC Input Recording (Stereo)

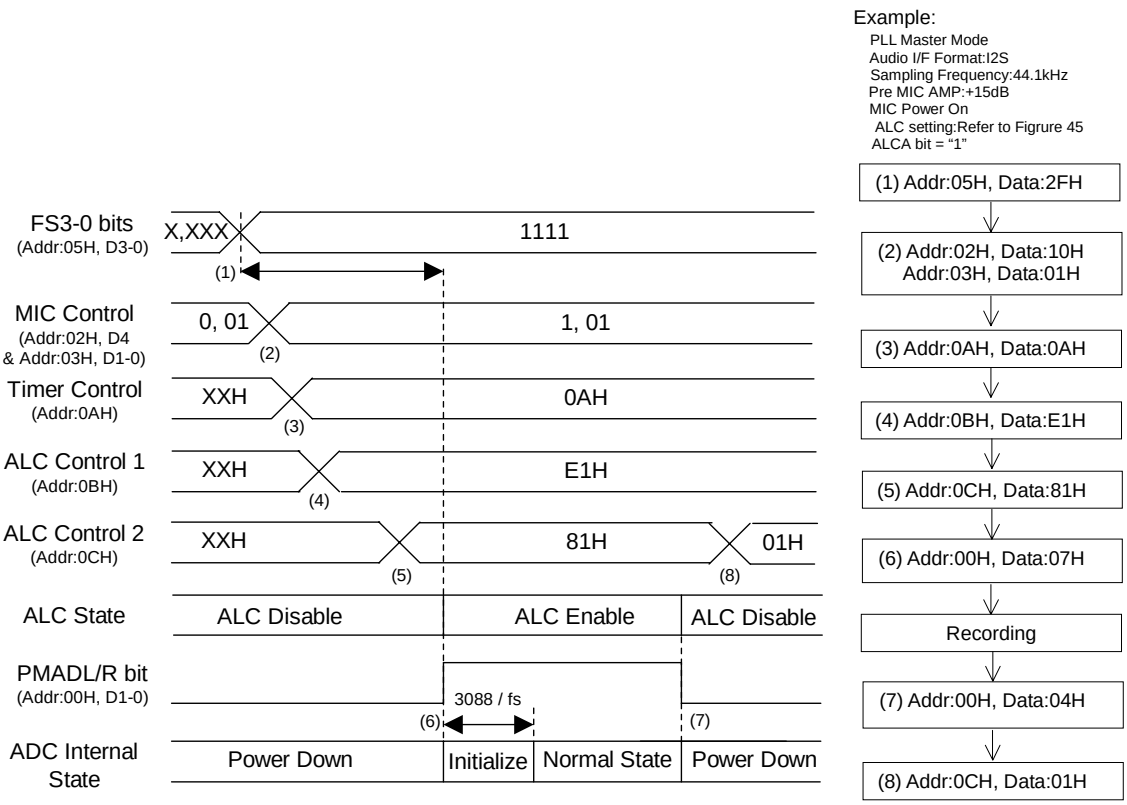


Figure 64. MIC Input Recording Sequence

<Example>

This sequence is an example of ALCA setting at fs=44.1kHz. If the parameter of the ALCA is changed, please refer to Figure 43.

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit). When the AK5702 is PLL mode, MIC and ADCA should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up MIC input (Addr: 02H&03H)

(3) Set up Timer Select for ALCA (Addr: 0AH)

(4) Set up REF value for ALCA (Addr: 0BH)

(5) Set up LMTHA1-0, RGA1-0, LMATA1-0 and ALCA bits (Addr: 0CH)

(6) Power Up MIC and ADCA: PMADAL = PMADAR bits = "0" → "1"
The initialization cycle time of ADCA is 3088/fs=70.0ms@fs=44.1kHz, HPFA1-0 bits = "00".
After the ALCA bit is set to "1" and MIC&ADC block is powered-up, the ALCA operation starts from IVOL default value (0dB).
To start the recording within 100ms, the following sequence is required.
(6a) PMVCM=PMMPA bits = "1".
(6b) Wait for 2ms, then PMPLL bit = "1".
(6c) Wait for 6ms, then PMADAL=PMADAR bits = "1".

(7) Power Down MIC and ADCA: PMADAL = PMADAR bits = "1" → "0"
When the registers for the ALC operation are not changed, ALCA bit may be keeping "1". The ALCA operation is disabled because the MIC&ADCA block is powered-down. If the registers for the ALCA operation are also changed when the sampling frequency is changed, it should be done after the AK5702 goes to the manual mode (ALC bit = "0") or MIC&ADCA block is powered-down (PMADAL=PMADAR bits = "0"). IVOL gain is not reset when PMADAL=PMADAR bits = "0", and then IVOL operation starts from the setting value when PMADAL or PMADAR bit is changed to "1".

(8) ALCA Disable: ALCA bit = "1" → "0"

■ Stop of Clock

Master clock can be stopped when ADC is not used.

1. PLL Master Mode

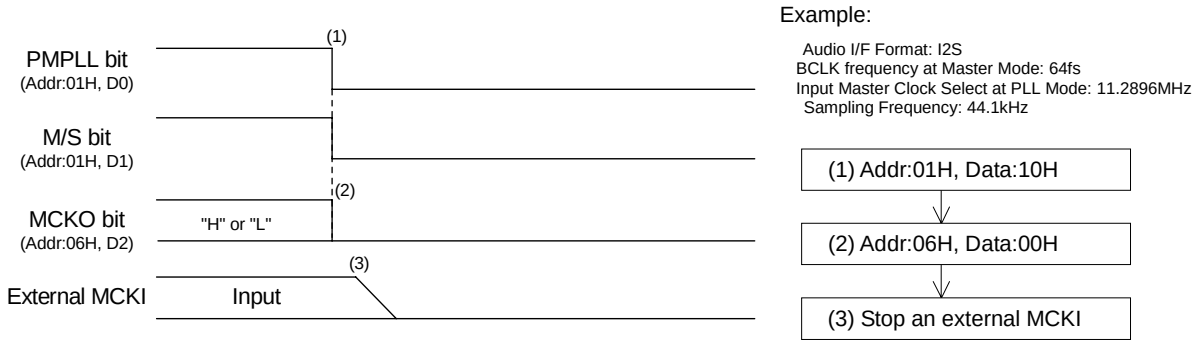


Figure 65. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL=M/S bits = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (LRCK, BCLK pin)

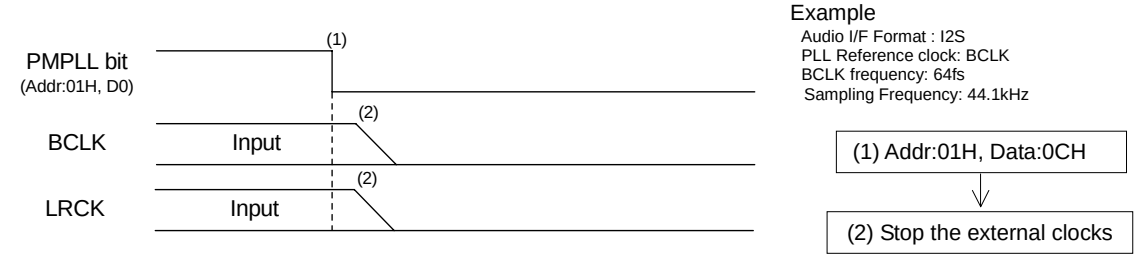


Figure 66. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BCLK and LRCK clocks

3. PLL Slave Mode (MCKI pin)

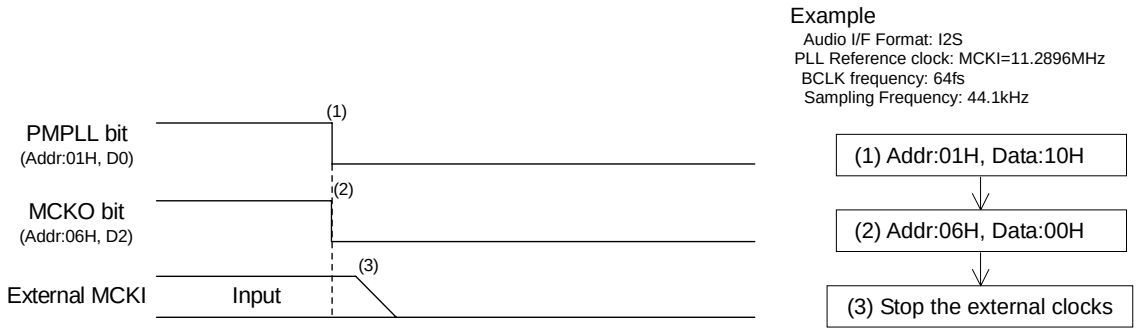


Figure 67. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO output: MCKO bit = "1" → "0"
(3) Stop the external master clock.

4. EXT Slave Mode

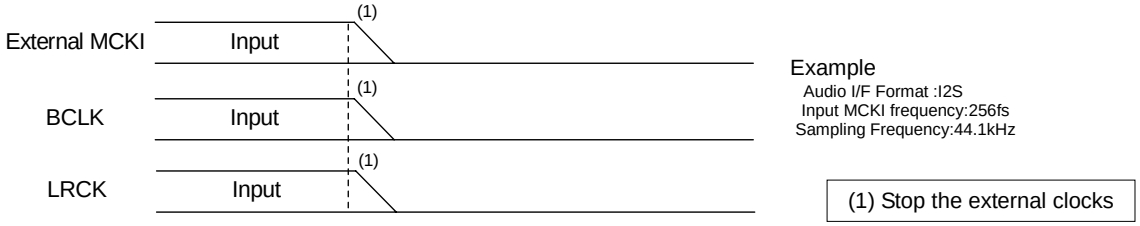


Figure 68. Clock Stopping Sequence (4)

<Example>
(1) Stop the external MCKI, BCLK and LRCK clocks.

5. EXT Master Mode

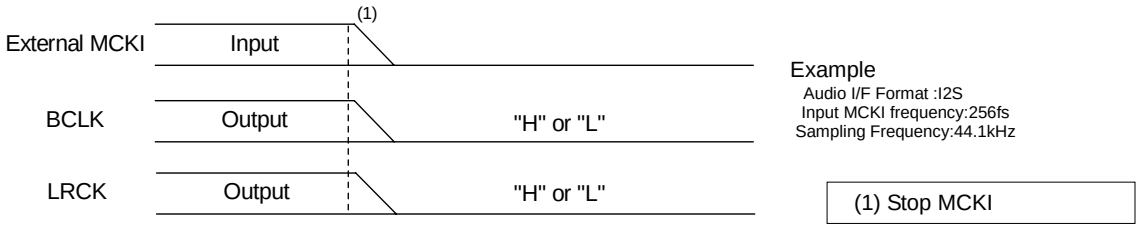


Figure 69. Clock Stopping Sequence (5)

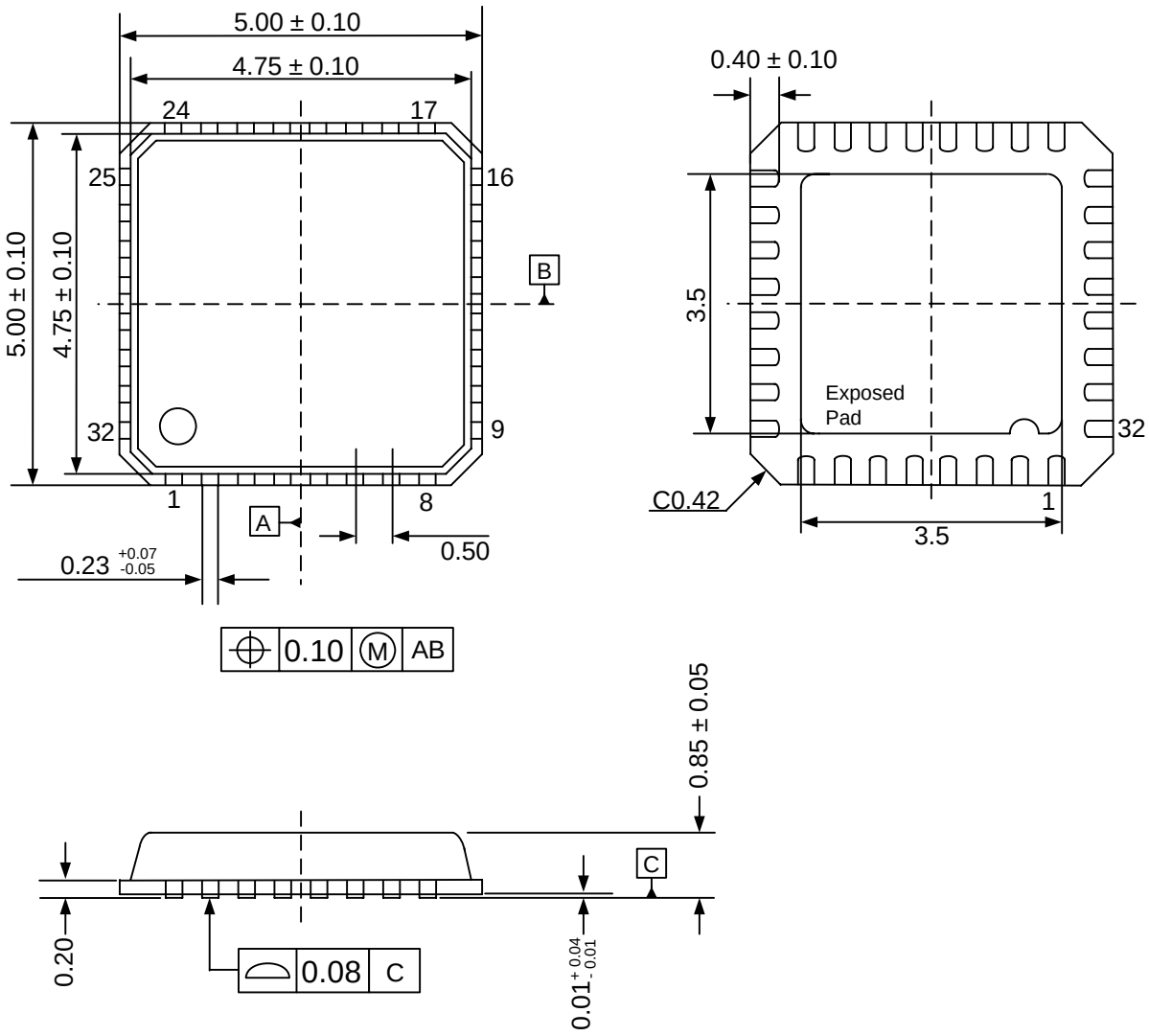
<Example>
(1) Stop MCKI. BCLK and LRCK are fixed to "H" or "L".

■ Power down

If the clocks are supplied, power down VCOM (PMVCM bit: “1” → “0”) after all blocks except for VCOM are powered-down and a master clock stops. The AK5702 is also powered-down by PDN pin = “L”. When PDN pin = “L”, the registers are initialized.

PACKAGE

● 32pin QFN (Unit: mm)

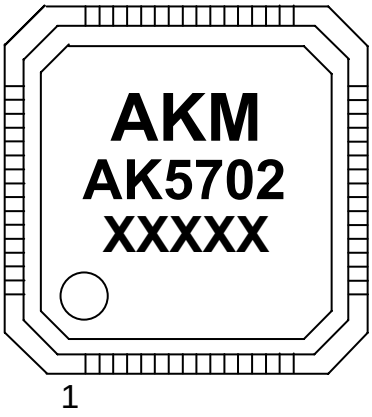


Note) The exposed pad on the bottom surface of the package must be open or connected to the ground.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXX: Date code identifier (5digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
07/06/07	00	First Edition		

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