

## 1. INTRODUCTION

The ST7556 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 102 segment and 65 common with 1 ICOM driver circuits. This chip is connected directly to a microprocessor, accepts 4-line serial interface (SPI) or 8-bit parallel interface, display data can store in an on-chip display data RAM of 66 x 102 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

## 2. FEATURES

### Driver Output Circuits

102 segment outputs / 65+1 common outputs

(external clock also possible)

### On-chip Display Data ram

- Capacity: 66X102=6,732 bits

- Voltage converter (x4)

- Voltage regulator (temperature gradient  
-0.05%/°C)

### Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line SPI (serial peripheral interface) available (only write operation)

- Voltage follower

- On-chip electronic contrast control function (128 steps)

- Liquid crystal driving voltage :

V<sub>0</sub> -V<sub>SS</sub> = max 12 V (external power supply)

### On-chip Low Power Analog Circuit

- Generation of LCD supply voltage (externally V<sub>out</sub> voltage supply is possible)
- Generation of intermediate LCD bias voltages
- Oscillator requires no external components

### External RESB (reset) pin

### Logic supply voltage range V<sub>DD</sub> -V<sub>SS</sub>

- 1.8 to 3.3V

**Temperature range: -30 to +85 degree**

## 3. PAD Arrangement (COG)

Chip Size: 10,310  $\mu\text{m}$   $\times$  1,150  $\mu\text{m}$

Bump Pitch:

PAD NO 1 ~ 148 , 250 ~ 272 : 75.5  $\mu\text{m}$  (com/seg) PAD NO 149 ~ 248 : 75  $\mu\text{m}$  (I/O) PAD NO 148 ~ 149 : 114  $\mu\text{m}$

PAD NO 248 ~ 249 : 93.5  $\mu\text{m}$  (Reset) PAD NO 249 ~ 250 : 95.9  $\mu\text{m}$  (Reset)

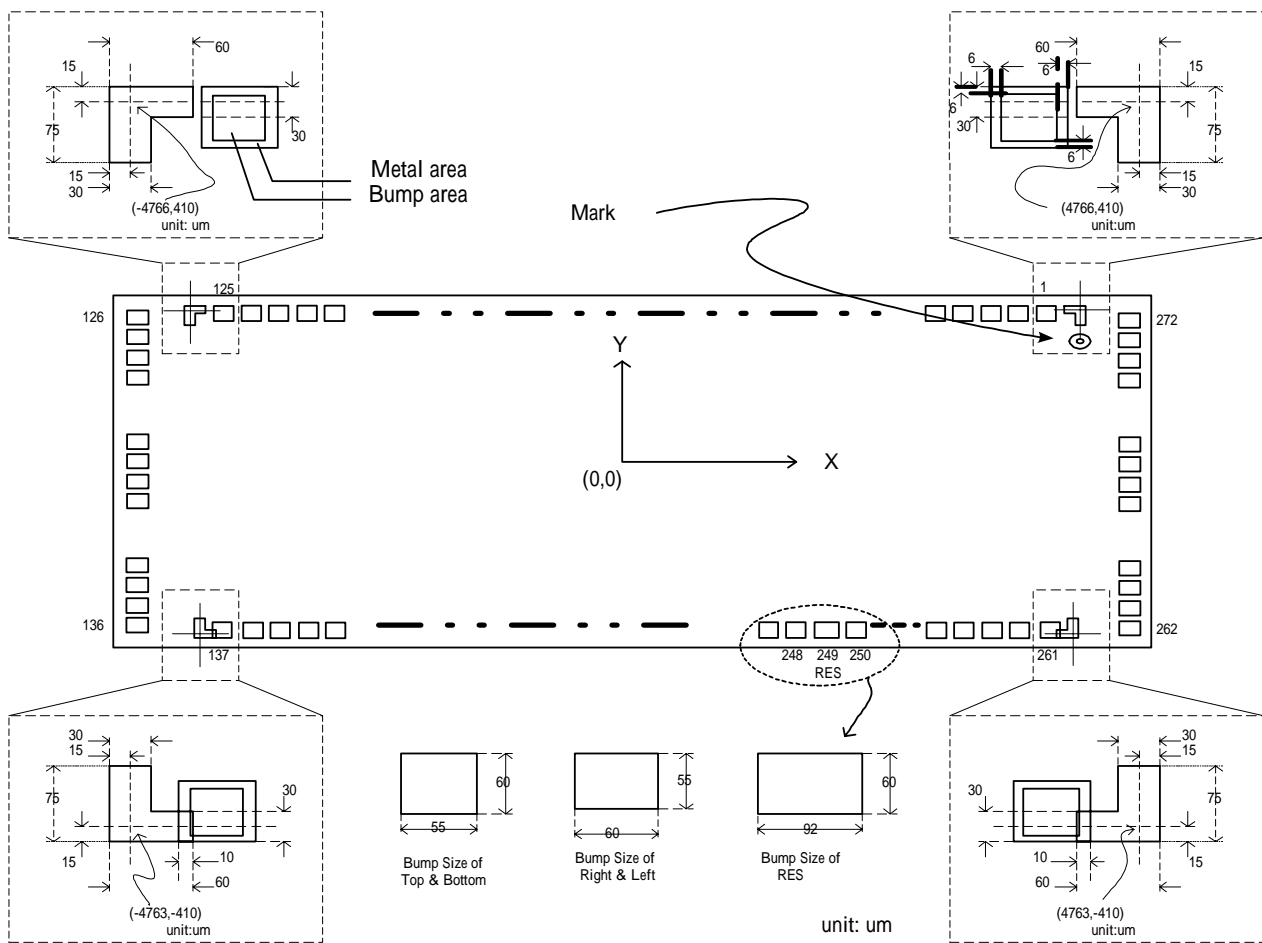
Bump Size:

PAD NO 1 ~ 125 , 137 ~ 248 , 250 ~ 261 : 55(x)  $\mu\text{m}$   $\times$  60(y)  $\mu\text{m}$  PAD NO 249 : 92(x)  $\mu\text{m}$   $\times$  60(y)  $\mu\text{m}$

PAD NO 126 ~ 136 , 262 ~ 272 : 60(x)  $\mu\text{m}$   $\times$  55(y)  $\mu\text{m}$

Bump Height: 17  $\mu\text{m}$

Chip Thickness: 635  $\mu\text{m}$



**Pad Center Coordinates (NORMAL, TMY=0)**

PAD NO.	PIN Name	X	Y
1	COM[42]	4681.0	389.0
2	COM[41]	4605.5	389.0
3	COM[40]	4530.0	389.0
4	COM[39]	4454.5	389.0
5	COM[38]	4379.0	389.0
6	COM[37]	4303.5	389.0
7	COM[36]	4228.0	389.0
8	COM[35]	4152.5	389.0
9	COM[34]	4077.0	389.0
10	COM[33]	4001.5	389.0
11	COM[32]	3926.0	389.0
12	Reserve	3850.5	389.0
13	SEG[0]	3775.0	389.0
14	SEG[1]	3699.5	389.0
15	SEG[2]	3624.0	389.0
16	SEG[3]	3548.5	389.0
17	SEG[4]	3473.0	389.0
18	SEG[5]	3397.5	389.0
19	SEG[6]	3322.0	389.0
20	SEG[7]	3246.5	389.0
21	SEG[8]	3171.0	389.0
22	SEG[9]	3095.5	389.0
23	SEG[10]	3020.0	389.0
24	SEG[11]	2944.5	389.0
25	SEG[12]	2869.0	389.0
26	SEG[13]	2793.5	389.0
27	SEG[14]	2718.0	389.0
28	SEG[15]	2642.5	389.0
29	SEG[16]	2567.0	389.0
30	SEG[17]	2491.5	389.0
31	SEG[18]	2416.0	389.0
32	SEG[19]	2340.5	389.0
33	SEG[20]	2265.0	389.0
34	SEG[21]	2189.5	389.0
35	SEG[22]	2114.0	389.0

PAD NO.	PIN Name	X	Y
36	SEG[23]	2038.5	389.0
37	SEG[24]	1963.0	389.0
38	SEG[25]	1887.5	389.0
39	SEG[26]	1812.0	389.0
40	SEG[27]	1736.5	389.0
41	SEG[28]	1661.0	389.0
42	SEG[29]	1585.5	389.0
43	SEG[30]	1510.0	389.0
44	SEG[31]	1434.5	389.0
45	SEG[32]	1359.0	389.0
46	SEG[33]	1283.5	389.0
47	SEG[34]	1208.0	389.0
48	SEG[35]	1132.5	389.0
49	SEG[36]	1057.0	389.0
50	SEG[37]	981.5	389.0
51	SEG[38]	906.0	389.0
52	SEG[39]	830.5	389.0
53	SEG[40]	755.0	389.0
54	SEG[41]	679.5	389.0
55	SEG[42]	604.0	389.0
56	SEG[43]	528.5	389.0
57	SEG[44]	453.0	389.0
58	SEG[45]	377.5	389.0
59	SEG[46]	302.0	389.0
60	SEG[47]	226.5	389.0
61	SEG[48]	151.0	389.0
62	SEG[49]	75.5	389.0
63	SEG[50]	0.0	389.0
64	SEG[51]	-75.5	389.0
65	SEG[52]	-151.0	389.0
66	SEG[53]	-226.5	389.0
67	SEG[54]	-302.0	389.0
68	SEG[55]	-377.5	389.0
69	SEG[56]	-453.0	389.0
70	SEG[57]	-528.5	389.0

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PAD NO.	PIN Name	X	Y
71	SEG[58]	-604.0	389.0
72	SEG[59]	-679.5	389.0
73	SEG[60]	-755.0	389.0
74	SEG[61]	-830.5	389.0
75	SEG[62]	-906.0	389.0
76	SEG[63]	-981.5	389.0
77	SEG[64]	-1057.0	389.0
78	SEG[65]	-1132.5	389.0
79	SEG[66]	-1208.0	389.0
80	SEG[67]	-1283.5	389.0
81	SEG[68]	-1359.0	389.0
82	SEG[69]	-1434.5	389.0
83	SEG[70]	-1510.0	389.0
84	SEG[71]	-1585.5	389.0
85	SEG[72]	-1661.0	389.0
86	SEG[73]	-1736.5	389.0
87	SEG[74]	-1812.0	389.0
88	SEG[75]	-1887.5	389.0
89	SEG[76]	-1963.0	389.0
90	SEG[77]	-2038.5	389.0
91	SEG[78]	-2114.0	389.0
92	SEG[79]	-2189.5	389.0
93	SEG[80]	-2265.0	389.0
94	SEG[81]	-2340.5	389.0
95	SEG[82]	-2416.0	389.0
96	SEG[83]	-2491.5	389.0
97	SEG[84]	-2567.0	389.0
98	SEG[85]	-2642.5	389.0
99	SEG[86]	-2718.0	389.0
100	SEG[87]	-2793.5	389.0
101	SEG[88]	-2869.0	389.0
102	SEG[89]	-2944.5	389.0
103	SEG[90]	-3020.0	389.0
104	SEG[91]	-3095.5	389.0
105	SEG[92]	-3171.0	389.0
106	SEG[93]	-3246.5	389.0

PAD NO.	PIN Name	X	Y
107	SEG[94]	-3322.0	389.0
108	SEG[95]	-3397.5	389.0
109	SEG[96]	-3473.0	389.0
110	SEG[97]	-3548.5	389.0
111	SEG[98]	-3624.0	389.0
112	SEG[99]	-3699.5	389.0
113	SEG[100]	-3775.0	389.0
114	SEG[101]	-3850.5	389.0
115	COMS1	-3926.0	389.0
116	COM[0]	-4001.5	389.0
117	COM[1]	-4077.0	389.0
118	COM[2]	-4152.5	389.0
119	COM[3]	-4228.0	389.0
120	COM[4]	-4303.5	389.0
121	COM[5]	-4379.0	389.0
122	COM[6]	-4454.5	389.0
123	COM[7]	-4530.0	389.0
124	COM[8]	-4605.5	389.0
125	COM[9]	-4681.0	389.0
126	COM[10]	-4998.5	381.5
127	COM[11]	-4998.5	306.0
128	COM[12]	-4998.5	230.5
129	COM[13]	-4998.5	155.0
130	COM[14]	-4998.5	79.5
131	COM[15]	-4998.5	4.0
132	COM[16]	-4998.5	-71.5
133	COM[17]	-4998.5	-147.0
134	COM[18]	-4998.5	-222.5
135	COM[19]	-4998.5	-298.0
136	COM[20]	-4998.5	-373.5
137	COM[21]	-4694.5	-389.0
138	COM[22]	-4619.0	-389.0
139	COM[23]	-4543.5	-389.0
140	COM[24]	-4468.0	-389.0
141	COM[25]	-4392.5	-389.0
142	COM[26]	-4317.0	-389.0

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PAD NO.	PIN Name	X	Y
143	COM[27]	-4241.5	-389.0
144	COM[28]	-4166.0	-389.0
145	COM[29]	-4090.5	-389.0
146	COM[30]	-4015.0	-389.0
147	COM[31]	-3939.5	-389.0
148	Reserve	-3864.0	-389.0
149	T9	-3750.0	-389.0
150	VDD	-3675.0	-389.0
151	VDD	-3600.0	-389.0
152	VDD	-3525.0	-389.0
153	VDD	-3450.0	-389.0
154	VDD	-3375.0	-389.0
155	VDD	-3300.0	-389.0
156	VDD2	-3225.0	-389.0
157	VDD2	-3150.0	-389.0
158	VDD2	-3075.0	-389.0
159	VDD2	-3000.0	-389.0
160	VDD2	-2925.0	-389.0
161	VDD2	-2850.0	-389.0
162	VDD2	-2775.0	-389.0
163	VDD2	-2700.0	-389.0
164	VDD2	-2625.0	-389.0
165	VDD2	-2550.0	-389.0
166	VDD2	-2475.0	-389.0
167	VDD2	-2400.0	-389.0
168	D7	-2325.0	-389.0
169	D7	-2250.0	-389.0
170	D6	-2175.0	-389.0
171	D6	-2100.0	-389.0
172	D5	-2025.0	-389.0
173	D5	-1950.0	-389.0
174	D4	-1875.0	-389.0
175	D4	-1800.0	-389.0
176	D3	-1725.0	-389.0
177	D3	-1650.0	-389.0
178	D2	-1575.0	-389.0

PAD NO.	PIN Name	X	Y
179	D2	-1500.0	-389.0
180	D1	-1425.0	-389.0
181	D1	-1350.0	-389.0
182	D0	-1275.0	-389.0
183	D0	-1200.0	-389.0
184	VDD	-1125.0	-389.0
185	T0	-1050.0	-389.0
186	T1	-975.0	-389.0
187	T2	-900.0	-389.0
188	T3	-825.0	-389.0
189	T4	-750.0	-389.0
190	T5	-675.0	-389.0
191	T6	-600.0	-389.0
192	T7	-525.0	-389.0
193	T8	-450.0	-389.0
194	VRS	-375.0	-389.0
195	ERD	-300.0	-389.0
196	ERD	-225.0	-389.0
197	RWR	-150.0	-389.0
198	RWR	-75.0	-389.0
199	A0	0.0	-389.0
200	A0	75.0	-389.0
201	CS	150.0	-389.0
202	CS	225.0	-389.0
203	IMS	300.0	-389.0
204	VDD	375.0	-389.0
205	PS	450.0	-389.0
206	T11	525.0	-389.0
207	T10	600.0	-389.0
208	VDD	675.0	-389.0
209	OSC	750.0	-389.0
210	OSC	825.0	-389.0
211	TMX	900.0	-389.0
212	TMY	975.0	-389.0
213	V0	1050.0	-389.0
214	V0	1125.0	-389.0

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PAD NO.	PIN Name	X	Y
215	V1	1200.0	-389.0
216	V2	1275.0	-389.0
217	V3	1350.0	-389.0
218	V4	1425.0	-389.0
219	VSS2	1500.0	-389.0
220	VSS2	1575.0	-389.0
221	VSS2	1650.0	-389.0
222	VSS2	1725.0	-389.0
223	VSS2	1800.0	-389.0
224	VSS2	1875.0	-389.0
225	VSS2	1950.0	-389.0
226	VSS2	2025.0	-389.0
227	VSS2	2100.0	-389.0
228	VSS2	2175.0	-389.0
229	VSS2	2250.0	-389.0
230	VSS2	2325.0	-389.0
231	VSS	2400.0	-389.0
232	VSS	2475.0	-389.0
233	VSS	2550.0	-389.0
234	VSS	2625.0	-389.0
235	VSS	2700.0	-389.0
236	VSS	2775.0	-389.0
237	VLCDIN	2850.0	-389.0
238	VLCDIN	2925.0	-389.0
239	VLCDIN	3000.0	-389.0
240	VLCDIN	3075.0	-389.0
241	VLCDIN	3150.0	-389.0
242	VLCDIN	3225.0	-389.0
243	VLCDOUT	3300.0	-389.0

PAD NO.	PIN Name	X	Y
244	VLCDOUT	3375.0	-389.0
245	VLCDOUT	3450.0	-389.0
246	VLCDOUT	3525.0	-389.0
247	VLCDOUT	3600.0	-389.0
248	VLCDOUT	3675.0	-389.0
249	RES	3768.5	-389.0
250	COMS2	3864.5	-389.0
251	COM[64]	3940.0	-389.0
252	COM[63]	4015.5	-389.0
253	COM[62]	4091.0	-389.0
254	COM[61]	4166.5	-389.0
255	COM[60]	4242.0	-389.0
256	COM[59]	4317.5	-389.0
257	COM[58]	4393.0	-389.0
258	COM[57]	4468.5	-389.0
259	COM[56]	4544.0	-389.0
260	COM[55]	4619.5	-389.0
261	COM[54]	4695.0	-389.0
262	COM[53]	4998.5	-373.5
263	COM[52]	4998.5	-298.0
264	COM[51]	4998.5	-222.5
265	COM[50]	4998.5	-147.0
266	COM[49]	4998.5	-71.5
267	COM[48]	4998.5	4.0
268	COM[47]	4998.5	79.5
269	COM[46]	4998.5	155.0
270	COM[45]	4998.5	230.5
271	COM[44]	4998.5	306.0
272	COM[43]	4998.5	381.5

**Pad Center Coordinates (REVERSE, TMY=1)**

PAD NO.	PIN Name	X	Y
1	COM[22]	4681.0	389.0
2	COM[23]	4605.5	389.0
3	COM[24]	4530.0	389.0
4	COM[25]	4454.5	389.0
5	COM[26]	4379.0	389.0
6	COM[27]	4303.5	389.0
7	COM[28]	4228.0	389.0
8	COM[29]	4152.5	389.0
9	COM[30]	4077.0	389.0
10	COM[31]	4001.5	389.0
11	Reserve	3926.0	389.0
12	Reserve	3850.5	389.0
13	SEG[0]	3775.0	389.0
14	SEG[1]	3699.5	389.0
15	SEG[2]	3624.0	389.0
16	SEG[3]	3548.5	389.0
17	SEG[4]	3473.0	389.0
18	SEG[5]	3397.5	389.0
19	SEG[6]	3322.0	389.0
20	SEG[7]	3246.5	389.0
21	SEG[8]	3171.0	389.0
22	SEG[9]	3095.5	389.0
23	SEG[10]	3020.0	389.0
24	SEG[11]	2944.5	389.0
25	SEG[12]	2869.0	389.0
26	SEG[13]	2793.5	389.0
27	SEG[14]	2718.0	389.0
28	SEG[15]	2642.5	389.0
29	SEG[16]	2567.0	389.0
30	SEG[17]	2491.5	389.0
31	SEG[18]	2416.0	389.0
32	SEG[19]	2340.5	389.0
33	SEG[20]	2265.0	389.0
34	SEG[21]	2189.5	389.0
35	SEG[22]	2114.0	389.0

PAD NO.	PIN Name	X	Y
36	SEG[23]	2038.5	389.0
37	SEG[24]	1963.0	389.0
38	SEG[25]	1887.5	389.0
39	SEG[26]	1812.0	389.0
40	SEG[27]	1736.5	389.0
41	SEG[28]	1661.0	389.0
42	SEG[29]	1585.5	389.0
43	SEG[30]	1510.0	389.0
44	SEG[31]	1434.5	389.0
45	SEG[32]	1359.0	389.0
46	SEG[33]	1283.5	389.0
47	SEG[34]	1208.0	389.0
48	SEG[35]	1132.5	389.0
49	SEG[36]	1057.0	389.0
50	SEG[37]	981.5	389.0
51	SEG[38]	906.0	389.0
52	SEG[39]	830.5	389.0
53	SEG[40]	755.0	389.0
54	SEG[41]	679.5	389.0
55	SEG[42]	604.0	389.0
56	SEG[43]	528.5	389.0
57	SEG[44]	453.0	389.0
58	SEG[45]	377.5	389.0
59	SEG[46]	302.0	389.0
60	SEG[47]	226.5	389.0
61	SEG[48]	151.0	389.0
62	SEG[49]	75.5	389.0
63	SEG[50]	0.0	389.0
64	SEG[51]	-75.5	389.0
65	SEG[52]	-151.0	389.0
66	SEG[53]	-226.5	389.0
67	SEG[54]	-302.0	389.0
68	SEG[55]	-377.5	389.0
69	SEG[56]	-453.0	389.0
70	SEG[57]	-528.5	389.0

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PAD NO.	PIN Name	X	Y
71	SEG[58]	-604.0	389.0
72	SEG[59]	-679.5	389.0
73	SEG[60]	-755.0	389.0
74	SEG[61]	-830.5	389.0
75	SEG[62]	-906.0	389.0
76	SEG[63]	-981.5	389.0
77	SEG[64]	-1057.0	389.0
78	SEG[65]	-1132.5	389.0
79	SEG[66]	-1208.0	389.0
80	SEG[67]	-1283.5	389.0
81	SEG[68]	-1359.0	389.0
82	SEG[69]	-1434.5	389.0
83	SEG[70]	-1510.0	389.0
84	SEG[71]	-1585.5	389.0
85	SEG[72]	-1661.0	389.0
86	SEG[73]	-1736.5	389.0
87	SEG[74]	-1812.0	389.0
88	SEG[75]	-1887.5	389.0
89	SEG[76]	-1963.0	389.0
90	SEG[77]	-2038.5	389.0
91	SEG[78]	-2114.0	389.0
92	SEG[79]	-2189.5	389.0
93	SEG[80]	-2265.0	389.0
94	SEG[81]	-2340.5	389.0
95	SEG[82]	-2416.0	389.0
96	SEG[83]	-2491.5	389.0
97	SEG[84]	-2567.0	389.0
98	SEG[85]	-2642.5	389.0
99	SEG[86]	-2718.0	389.0
100	SEG[87]	-2793.5	389.0
101	SEG[88]	-2869.0	389.0
102	SEG[89]	-2944.5	389.0
103	SEG[90]	-3020.0	389.0
104	SEG[91]	-3095.5	389.0
105	SEG[92]	-3171.0	389.0
106	SEG[93]	-3246.5	389.0

PAD NO.	PIN Name	X	Y
107	SEG[94]	-3322.0	389.0
108	SEG[95]	-3397.5	389.0
109	SEG[96]	-3473.0	389.0
110	SEG[97]	-3548.5	389.0
111	SEG[98]	-3624.0	389.0
112	SEG[99]	-3699.5	389.0
113	SEG[100]	-3775.0	389.0
114	SEG[101]	-3850.5	389.0
115	COMS1	-3926.0	389.0
116	COM[64]	-4001.5	389.0
117	COM[63]	-4077.0	389.0
118	COM[62]	-4152.5	389.0
119	COM[61]	-4228.0	389.0
120	COM[60]	-4303.5	389.0
121	COM[59]	-4379.0	389.0
122	COM[58]	-4454.5	389.0
123	COM[57]	-4530.0	389.0
124	COM[56]	-4605.5	389.0
125	COM[55]	-4681.0	389.0
126	COM[54]	-4998.5	381.5
127	COM[53]	-4998.5	306.0
128	COM[52]	-4998.5	230.5
129	COM[51]	-4998.5	155.0
130	COM[50]	-4998.5	79.5
131	COM[49]	-4998.5	4.0
132	COM[48]	-4998.5	-71.5
133	COM[47]	-4998.5	-147.0
134	COM[46]	-4998.5	-222.5
135	COM[45]	-4998.5	-298.0
136	COM[44]	-4998.5	-373.5
137	COM[43]	-4694.5	-389.0
138	COM[42]	-4619.0	-389.0
139	COM[41]	-4543.5	-389.0
140	COM[40]	-4468.0	-389.0
141	COM[39]	-4392.5	-389.0
142	COM[38]	-4317.0	-389.0



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PAD NO.	PIN Name	X	Y
143	COM[37]	-4241.5	-389.0
144	COM[36]	-4166.0	-389.0
145	COM[35]	-4090.5	-389.0
146	COM[34]	-4015.0	-389.0
147	COM[33]	-3939.5	-389.0
148	COM[32]	-3864.0	-389.0
149	T9	-3750.0	-389.0
150	VDD	-3675.0	-389.0
151	VDD	-3600.0	-389.0
152	VDD	-3525.0	-389.0
153	VDD	-3450.0	-389.0
154	VDD	-3375.0	-389.0
155	VDD	-3300.0	-389.0
156	VDD2	-3225.0	-389.0
157	VDD2	-3150.0	-389.0
158	VDD2	-3075.0	-389.0
159	VDD2	-3000.0	-389.0
160	VDD2	-2925.0	-389.0
161	VDD2	-2850.0	-389.0
162	VDD2	-2775.0	-389.0
163	VDD2	-2700.0	-389.0
164	VDD2	-2625.0	-389.0
165	VDD2	-2550.0	-389.0
166	VDD2	-2475.0	-389.0
167	VDD2	-2400.0	-389.0
168	D7	-2325.0	-389.0
169	D7	-2250.0	-389.0
170	D6	-2175.0	-389.0
171	D6	-2100.0	-389.0
172	D5	-2025.0	-389.0
173	D5	-1950.0	-389.0
174	D4	-1875.0	-389.0
175	D4	-1800.0	-389.0
176	D3	-1725.0	-389.0
177	D3	-1650.0	-389.0
178	D2	-1575.0	-389.0

PAD NO.	PIN Name	X	Y
179	D2	-1500.0	-389.0
180	D1	-1425.0	-389.0
181	D1	-1350.0	-389.0
182	D0	-1275.0	-389.0
183	D0	-1200.0	-389.0
184	VDD	-1125.0	-389.0
185	T0	-1050.0	-389.0
186	T1	-975.0	-389.0
187	T2	-900.0	-389.0
188	T3	-825.0	-389.0
189	T4	-750.0	-389.0
190	T5	-675.0	-389.0
191	T6	-600.0	-389.0
192	T7	-525.0	-389.0
193	T8	-450.0	-389.0
194	VRS	-375.0	-389.0
195	ERD	-300.0	-389.0
196	ERD	-225.0	-389.0
197	RWR	-150.0	-389.0
198	RWR	-75.0	-389.0
199	A0	0.0	-389.0
200	A0	75.0	-389.0
201	CS	150.0	-389.0
202	CS	225.0	-389.0
203	IMS	300.0	-389.0
204	VDD	375.0	-389.0
205	PS	450.0	-389.0
206	T11	525.0	-389.0
207	T10	600.0	-389.0
208	VDD	675.0	-389.0
209	OSC	750.0	-389.0
210	OSC	825.0	-389.0
211	TMX	900.0	-389.0
212	TMY	975.0	-389.0
213	V0	1050.0	-389.0
214	V0	1125.0	-389.0

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PAD NO.	PIN Name	X	Y
215	V1	1200.0	-389.0
216	V2	1275.0	-389.0
217	V3	1350.0	-389.0
218	V4	1425.0	-389.0
219	VSS2	1500.0	-389.0
220	VSS2	1575.0	-389.0
221	VSS2	1650.0	-389.0
222	VSS2	1725.0	-389.0
223	VSS2	1800.0	-389.0
224	VSS2	1875.0	-389.0
225	VSS2	1950.0	-389.0
226	VSS2	2025.0	-389.0
227	VSS2	2100.0	-389.0
228	VSS2	2175.0	-389.0
229	VSS2	2250.0	-389.0
230	VSS2	2325.0	-389.0
231	VSS	2400.0	-389.0
232	VSS	2475.0	-389.0
233	VSS	2550.0	-389.0
234	VSS	2625.0	-389.0
235	VSS	2700.0	-389.0
236	VSS	2775.0	-389.0
237	VLCDIN	2850.0	-389.0
238	VLCDIN	2925.0	-389.0
239	VLCDIN	3000.0	-389.0
240	VLCDIN	3075.0	-389.0
241	VLCDIN	3150.0	-389.0
242	VLCDIN	3225.0	-389.0
243	VLCDOUT	3300.0	-389.0

PAD NO.	PIN Name	X	Y
244	VLCDOUT	3375.0	-389.0
245	VLCDOUT	3450.0	-389.0
246	VLCDOUT	3525.0	-389.0
247	VLCDOUT	3600.0	-389.0
248	VLCDOUT	3675.0	-389.0
249	RES	3768.5	-389.0
250	COMS2	3864.5	-389.0
251	COM[0]	3940.0	-389.0
252	COM[1]	4015.5	-389.0
253	COM[2]	4091.0	-389.0
254	COM[3]	4166.5	-389.0
255	COM[4]	4242.0	-389.0
256	COM[5]	4317.5	-389.0
257	COM[6]	4393.0	-389.0
258	COM[7]	4468.5	-389.0
259	COM[8]	4544.0	-389.0
260	COM[9]	4619.5	-389.0
261	COM[10]	4695.0	-389.0
262	COM[11]	4998.5	-373.5
263	COM[12]	4998.5	-298.0
264	COM[13]	4998.5	-222.5
265	COM[14]	4998.5	-147.0
266	COM[15]	4998.5	-71.5
267	COM[16]	4998.5	4.0
268	COM[17]	4998.5	79.5
269	COM[18]	4998.5	155.0
270	COM[19]	4998.5	230.5
271	COM[20]	4998.5	306.0
272	COM[21]	4998.5	381.5

4. BLOCK DIAGRAM

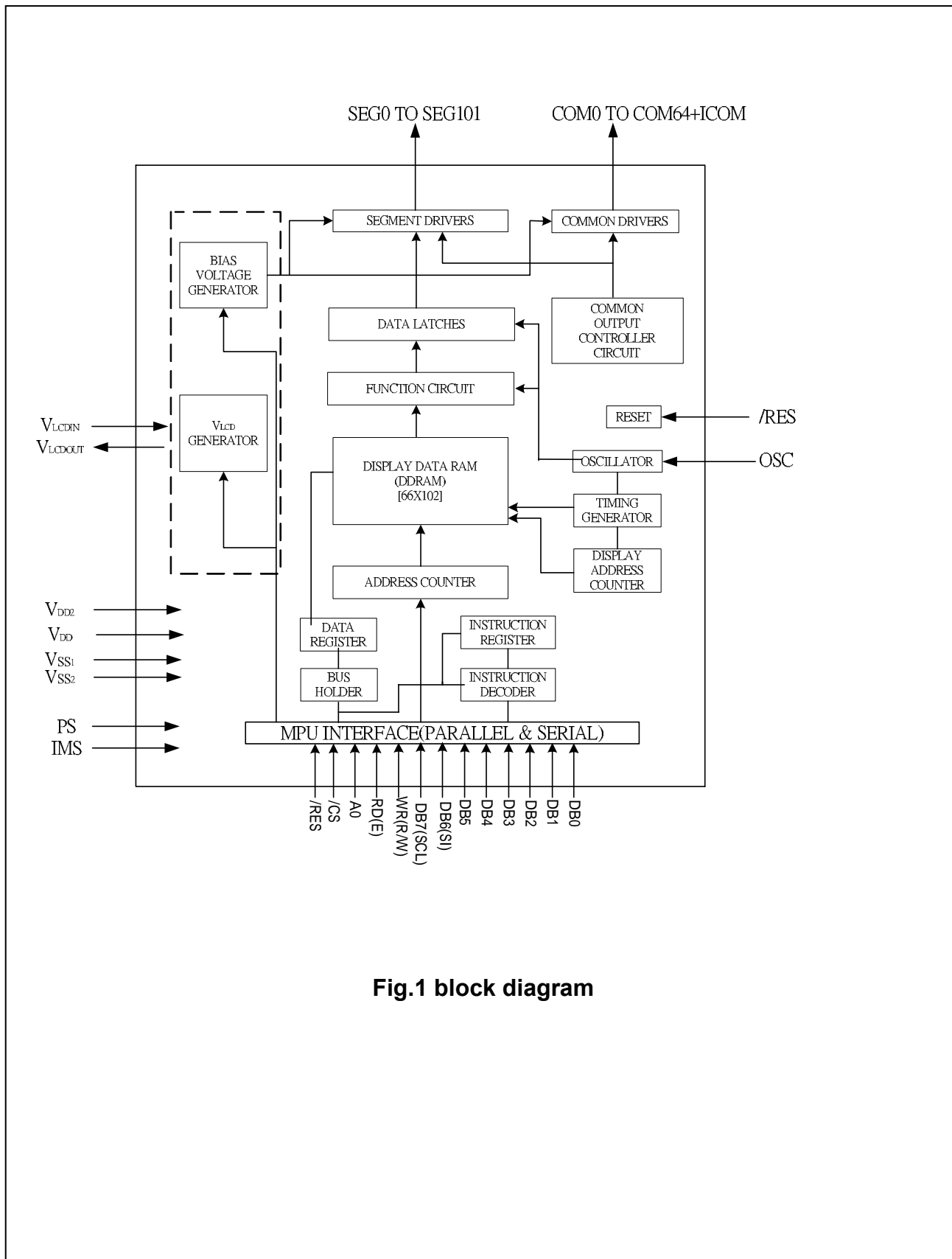


Fig.1 block diagram

5. PINNING DESCRIPTIONS

Pin Name	I/O	Description	No. of Pins																										
<b>LCD driver outputs</b>																													
SEG0 to SEG101	O	<p>LCD segment driver outputs This display data and the M signal control the output voltage of segment driver.</p> <table border="1"> <thead> <tr> <th rowspan="2">Display data</th> <th rowspan="2">M (Internal)</th> <th colspan="2">Segment drover output voltage</th> </tr> <tr> <th>Normal display</th> <th>Reverse display</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>VLCD</td> <td>V<sub>2</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td>V<sub>SS</sub></td> <td>V<sub>3</sub></td> </tr> <tr> <td>L</td> <td>H</td> <td>V<sub>2</sub></td> <td>VLCD</td> </tr> <tr> <td>L</td> <td>L</td> <td>V<sub>3</sub></td> <td>V<sub>SS</sub></td> </tr> <tr> <td colspan="2">Power save mode</td> <td>V<sub>SS</sub></td> <td>V<sub>SS</sub></td> </tr> </tbody> </table>	Display data	M (Internal)	Segment drover output voltage		Normal display	Reverse display	H	H	VLCD	V <sub>2</sub>	H	L	V <sub>SS</sub>	V <sub>3</sub>	L	H	V <sub>2</sub>	VLCD	L	L	V <sub>3</sub>	V <sub>SS</sub>	Power save mode		V <sub>SS</sub>	V <sub>SS</sub>	102
Display data	M (Internal)	Segment drover output voltage																											
		Normal display	Reverse display																										
H	H	VLCD	V <sub>2</sub>																										
H	L	V <sub>SS</sub>	V <sub>3</sub>																										
L	H	V <sub>2</sub>	VLCD																										
L	L	V <sub>3</sub>	V <sub>SS</sub>																										
Power save mode		V <sub>SS</sub>	V <sub>SS</sub>																										
COM0 to COM64	O	<p>LCD column driver outputs This internal scanning data and M signal control the output voltage of common driver.</p> <table border="1"> <thead> <tr> <th rowspan="2">Display data</th> <th rowspan="2">M(Internal)</th> <th colspan="2">Common drover output voltage</th> </tr> <tr> <th>Normal display</th> <th>Reverse display</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td colspan="2">V<sub>SS</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td colspan="2">VLCD</td> </tr> <tr> <td>L</td> <td>H</td> <td colspan="2">V<sub>1</sub></td> </tr> <tr> <td>L</td> <td>L</td> <td colspan="2">V<sub>4</sub></td> </tr> <tr> <td colspan="2">Power save mode</td> <td colspan="2">V<sub>SS</sub></td> </tr> </tbody> </table>	Display data	M(Internal)	Common drover output voltage		Normal display	Reverse display	H	H	V <sub>SS</sub>		H	L	VLCD		L	H	V <sub>1</sub>		L	L	V <sub>4</sub>		Power save mode		V <sub>SS</sub>		65
Display data	M(Internal)	Common drover output voltage																											
		Normal display	Reverse display																										
H	H	V <sub>SS</sub>																											
H	L	VLCD																											
L	H	V <sub>1</sub>																											
L	L	V <sub>4</sub>																											
Power save mode		V <sub>SS</sub>																											
COMS	O	<p>Common output for the icons The output signals of two pins are same. When not used, this pin should be left open.</p>	2																										
TMX	I	<p>Mirror X: SEG bi-direction selection TMX connect to VSS (MX=0):normal direction (SEG0→SEG101) TMX connect to VDD (MX=1):reverse direction (SEG101→SEG0)</p>	1																										
TMY	I	<p>Mirror Y: COM bi-direction selection TMY connect to VSS (MY=0):normal direction TMY connect to VDD (MY=1):reverse direction See pad center coordinates.</p>	1																										
<b>MICROPROCESSOR INTERFACE</b>																													
P/S	I	<p>Microprocessor interface select input pin P/S= "H " : parallel data input. P/S= "L " : serial data input. When P/S=" L ", D0 to D5 are fixed to " H ". RD (E) and WR(R/W) are fixed to "H ".</p>	1																										
IMS	I	<p>Input mode select</p> <table border="1"> <thead> <tr> <th>P/S</th> <th>IMS</th> <th>State</th> </tr> </thead> <tbody> <tr> <td>" H "</td> <td>" H "</td> <td>6800-series parallel MPU interface</td> </tr> <tr> <td>" H "</td> <td>" L "</td> <td>8080-series parallel MPU interface</td> </tr> <tr> <td>" L "</td> <td>" H "</td> <td>4 Pin-SPI MPU interface</td> </tr> <tr> <td>" L "</td> <td>" L "</td> <td>Do not use</td> </tr> </tbody> </table>	P/S	IMS	State	" H "	" H "	6800-series parallel MPU interface	" H "	" L "	8080-series parallel MPU interface	" L "	" H "	4 Pin-SPI MPU interface	" L "	" L "	Do not use	1											
P/S	IMS	State																											
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" H "	" L "	8080-series parallel MPU interface																											
" L "	" H "	4 Pin-SPI MPU interface																											
" L "	" L "	Do not use																											
CSB	I	<p>Chip select input pins Data/instruction I/O is enabled only when CSB is " L ". When chip select is non-active, DB0 to DB7 is high impedance.</p>	2																										
RESB	I	<p>Reset input pin When RESET is " L ", initialization is executed.</p>	1																										

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A0	I	It determines whether the data bits are data or a command. A0=" H ": Indicates that D0 to D7 are display data. A0=" L ": Indicates that D0 to D7 are control data.	2												
/WR(R/W)	I	Read/Write execution control pin <table border="1"> <thead> <tr> <th>IMS</th> <th>MPU type</th> <th>/WR(R/W)</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>6800-series</td> <td>R/W</td> <td>Read/Write control input pin R/W=" H ": read R/W=" L ": write</td> </tr> <tr> <td>L</td> <td>8080-series</td> <td>/WR</td> <td>Write enable clock input pin The data on D0 to D7 are latched at the rising edge of the /WR signal</td> </tr> </tbody> </table> <p>When in the serial interface must fixed to " H ".</p>	IMS	MPU type	/WR(R/W)	Description	H	6800-series	R/W	Read/Write control input pin R/W=" H ": read R/W=" L ": write	L	8080-series	/WR	Write enable clock input pin The data on D0 to D7 are latched at the rising edge of the /WR signal	2
IMS	MPU type	/WR(R/W)	Description												
H	6800-series	R/W	Read/Write control input pin R/W=" H ": read R/W=" L ": write												
L	8080-series	/WR	Write enable clock input pin The data on D0 to D7 are latched at the rising edge of the /WR signal												
/RD (E)	I	Read/Write execution control pin <table border="1"> <thead> <tr> <th>IMS</th> <th>MPU Type</th> <th>/RD (E)</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>6800-series</td> <td>E</td> <td>Read/Write control input pin R/W=" H ": When E is " H ", D0 to D7 are in an output status. R/W=" L ": The data on D0 to D7 are latched at the falling edge of the E signal.</td> </tr> <tr> <td>L</td> <td>8080-series</td> <td>/RD</td> <td>Read enable clock input pin When /RD is " L ", D0 to D7 are in an output status.</td> </tr> </tbody> </table> <p>When in the serial interface must fixed to " H ".</p>	IMS	MPU Type	/RD (E)	Description	H	6800-series	E	Read/Write control input pin R/W=" H ": When E is " H ", D0 to D7 are in an output status. R/W=" L ": The data on D0 to D7 are latched at the falling edge of the E signal.	L	8080-series	/RD	Read enable clock input pin When /RD is " L ", D0 to D7 are in an output status.	2
IMS	MPU Type	/RD (E)	Description												
H	6800-series	E	Read/Write control input pin R/W=" H ": When E is " H ", D0 to D7 are in an output status. R/W=" L ": The data on D0 to D7 are latched at the falling edge of the E signal.												
L	8080-series	/RD	Read enable clock input pin When /RD is " L ", D0 to D7 are in an output status.												
D5 to D0 D6 (SI) D7 (SCL)	I/O	<b>When the parallel interface selected (P/S=" H " ): 8-bit interface</b> 8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When chip select is not active, D0 to D7 is high impedance. <b>When the serial interface selected (P/S=" L " &amp; IMS="H"):</b> 4-line D7: serial input clock (SCL) D6: serial input data (SI) D5, D4, D3, D2, D1, D0: must fix to "H". When chip select is not active, D0 to D7 is high impedance.	16												
<b>LCD DRIVER SUPPLY</b>															
OSC	I	<b>When the on-chip oscillator is used, this input must be connected to VDD.</b> An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to VSS the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power Down Mode before stopping the clock.	2												
<b>Power Supply Pins</b>															
V <sub>SS1</sub>	<b>Power Supply</b>	Digital Ground. The 2 supply rails V <sub>SS1</sub> and V <sub>SS2</sub> must be connected together.	6												
V <sub>SS2</sub>	<b>Power Supply</b>	Analog Ground. The 2 supply rails V <sub>SS1</sub> and V <sub>SS2</sub> must be connected together.	12												
VDD	<b>Power Supply</b>	Digital Supply voltage. The 2 supply rails VDD and V <sub>DD2</sub> could be connected together. If Digital Option pin is high, must be this level	9												
V <sub>DD2</sub>	<b>Power</b>	Analog Supply voltage. The 2 supply rails VDD and V <sub>DD2</sub> could be connected together.	12												

## ST7556

	<b>Supply</b>		
V <sub>LCDOUT</sub>	<b>Power Supply</b>	If the internal voltage generator is used, the V <sub>LCDIN</sub> & V <sub>LCDOUT</sub> must be connected together and series one capacitor to VSS2. If an external supply is used this pin must be left open.	<b>6</b>
V <sub>LCDIN</sub>	<b>Power Supply</b>	If the internal voltage generator is used, the V <sub>LCDIN</sub> & V <sub>LCDOUT</sub> must be connected together. An external supply voltage can be supplied using the V <sub>LCDIN</sub> pad. This pad is for external multiple voltage input. In this case, VLCDOOUT has to be left open,	<b>6</b>
V0,V1, V2, V3, V4	<b>Power Supply</b>	This is a multi-level power supply for the liquid crystal. V <sub>LCDIN</sub> ≥V0 ≥V1≥V2≥V3≥V4≥VSS	<b>8</b>
VRS	<b>Power Supply</b>	Monitor Voltage Regulator level, must be left open.	<b>1</b>
<b>Test Pin</b>			
Test0~Test11	<b>T</b>	To test used. Test0~Test8 must floating Test9 could be connected out for monitor the VLCD(V0) voltage Test10 must connect to VSS Test11 must connect to VDD	<b>11</b>
Reserve Pin		ALL Reserve Pin must floating	

### ST7556 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
PS,IMS,OSC	No Limitation
T1~T8, VRS	Floating
VDD, Vdd2, Vss1, Vss2, Vlcdin , Vlcdout	<100Ω
V1 , V2 , V3 , V4	<500Ω
A0,/WR,/RD,CSB, D0 ...D7	<1KΩ
RESB	<10KΩ

## 6. FUNCTIONS DESCRIPTION

### MICROPROCESSOR INTERFACE

#### Chip Select Input

There is CSB pin for chip selection. The ST7556 can interface with an MPU when CSB is "L". When CSB is "H", these pins are set to any other combination, A0, /RD(E), and /WR(R/W) inputs are disabled and D0 to D7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

#### Parallel / Serial Interface

ST7556 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by P/S pin as shown in table 1.

**Table 1. Parallel/Serial Interface Mode**

Type	P/S	IMS	CSB	Interface mode
Parallel	H	H	CSB	6800-series MPU interface
		L		8080-series MPU interface
Serial	L	H	CSB	4-pin SPI interface
		L	---	Do not use

#### Parallel Interface (P/S = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by IMS as shown in table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in table 3.

**Table 2. Microprocessor Selection for Parallel Interface**

IMS	CSB	A0	/RD (E)	/WR (R/W)	DB0 to DB7	MPU bus
H	CSB	A0	E	R/W	DB0 to DB7	6800-series
L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

**Table 3. Parallel Data Transfer**

Common	6800-series		8080-series		Description
	E (/RD)	R/W (/WR)	/RD (E)	/WR (R/W)	
RS	H	H	L	H	Display data read out
	H	L	H	L	Display data write
	H	H	L	H	Register status read
	H	L	H	L	Writes to internal register (instruction)

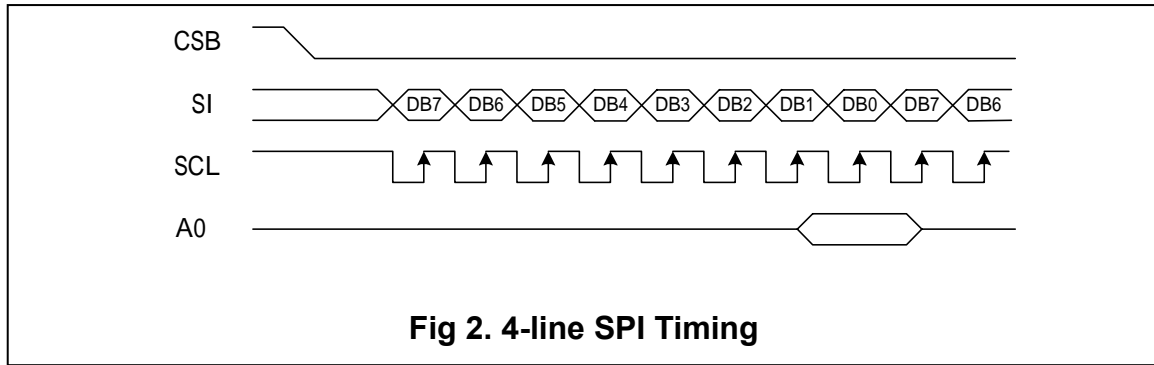
NOTE: When /RD (E) pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, /WR(R/W) as in case of 6800-series mode.

#### Serial Interface (P/S=" L ")

Serial Mode	P/S	IMS	CSB	A0	Description
4-line SPI interface	L	H	CSB	Used	Write only

#### IMS=" L ", P/S=" H ": 4-line SPI interface

When the ST7556 is active (CSB="L"), serial data (D6) and serial clock (D7) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (A0) Pin, based on the setting of P/S. When the A0 pin is used (IMS = "H"), data is display data when A0 is high, and command data when A0 is low. When A0 is not used (IMS = "L"), the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data direction command to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sending, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into D7 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string are handled as command data.



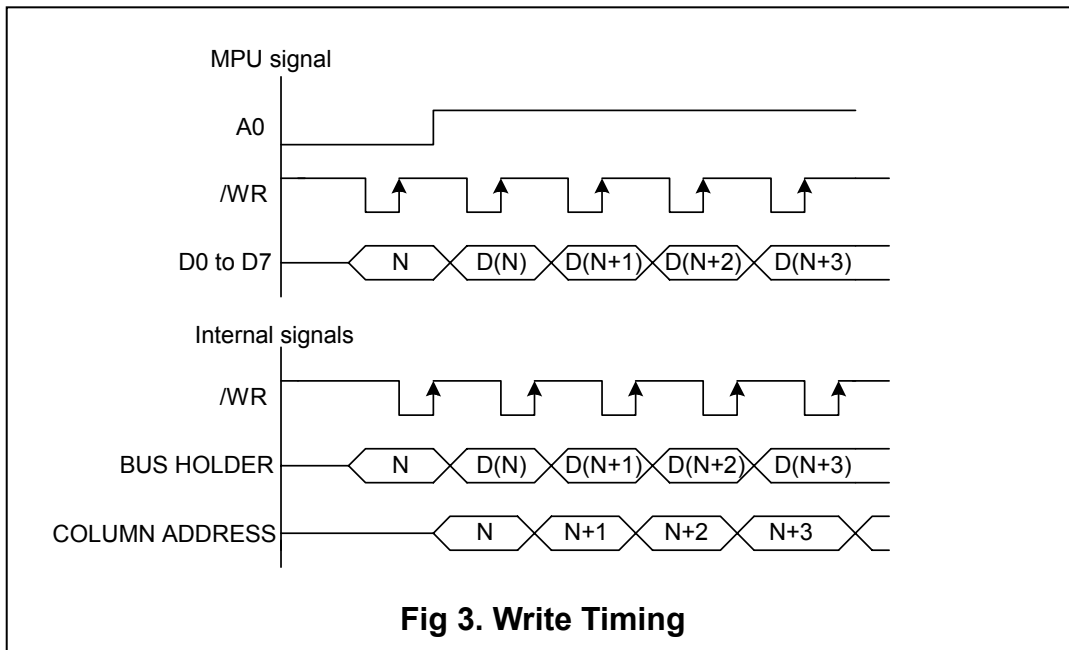
**Fig 2. 4-line SPI Timing**

**Busy Flag**

The Busy Flag indicates whether the ST7556 is operating or not. When D7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

**Data Transfer**

The ST7556 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 3. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 4. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.



**Fig 3. Write Timing**



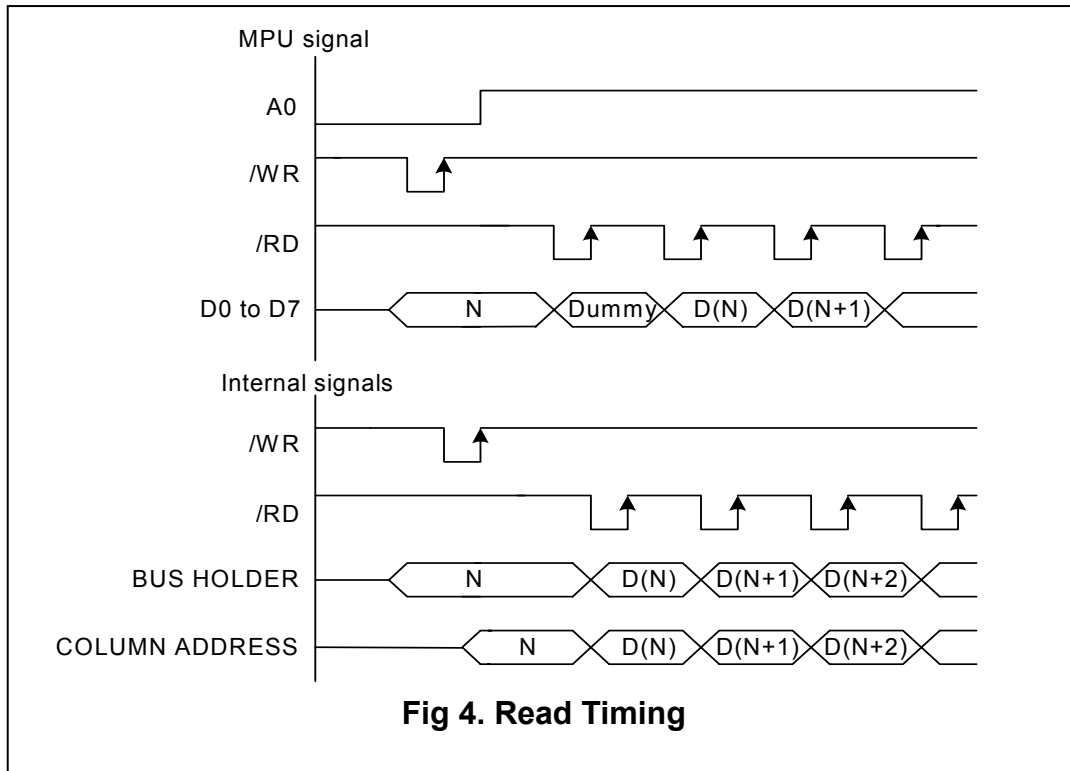


Fig 4. Read Timing

**DISPLAY DATA RAM (DDRAM)**

The ST7556 contains a 65X102 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 65(8 pageX8 +1) X102, and extra ICOM. There is a direct correspondence between X-address and column output number. It is 65-row by 102-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and 1 page of 1 line. Data is read from or written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

**Page Address Circuit**

This circuit is for providing a Page Address to Display Data RAM shown in figure 6. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data D0 is only valid.

**Column Address Circuit**

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 5. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

**ADDRESSING**

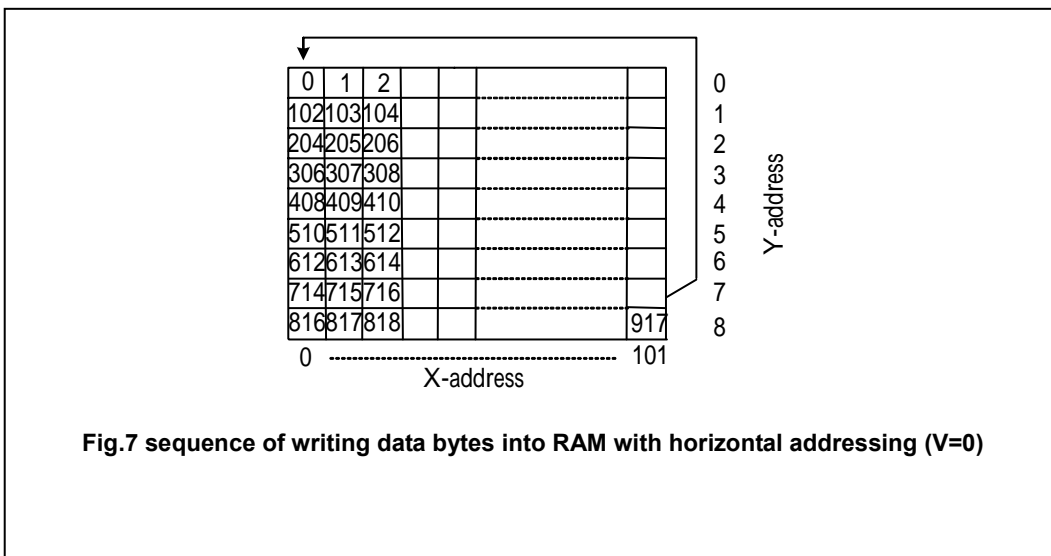
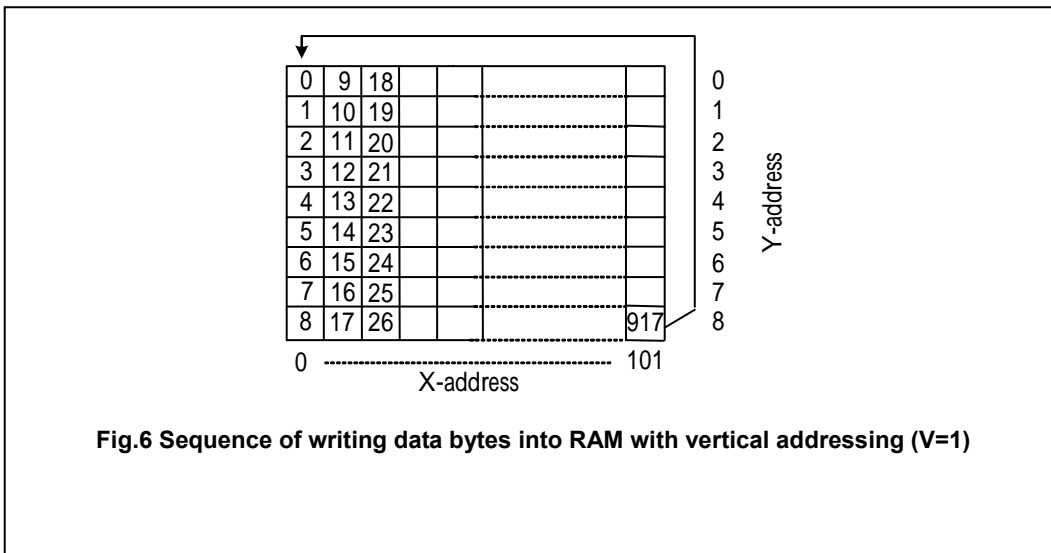
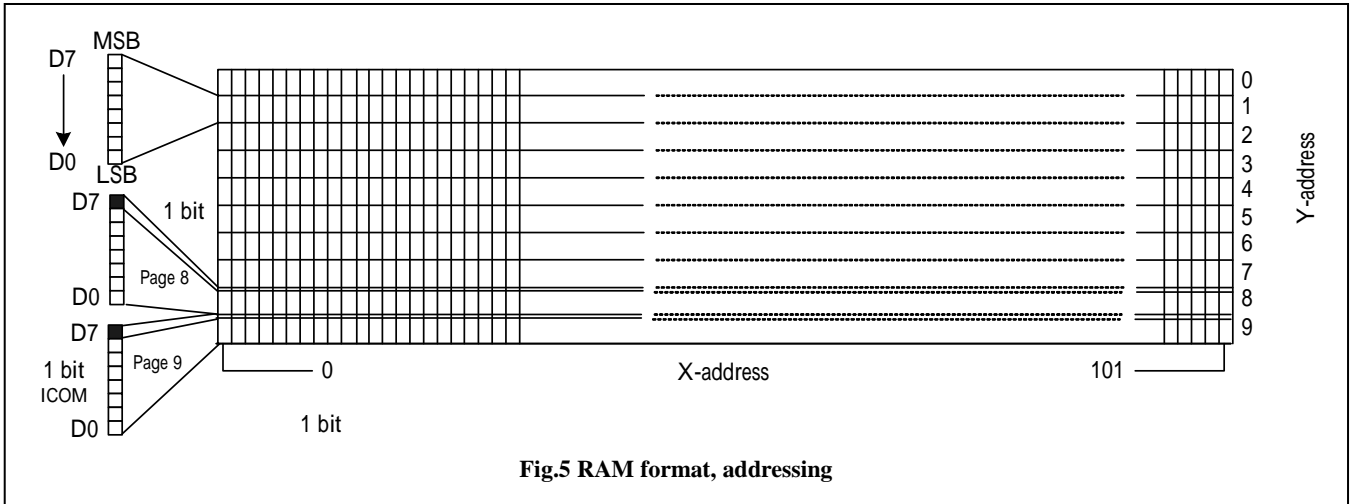
Data is downloaded in bytes into the RAM matrix of ST7556 as indicated in Figs.5, 6, 7. The display RAM has a matrix of 65 by 102 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101), Y 0 to 8 (1000). Addresses outside these ranges are not allowed.

In vertical addressing mode (V=1) the Y address increments after each byte (see Fig.7). After the last Y address (Y = 8) Y wraps around to 0 and X increments to address the next column.

In horizontal addressing mode (V=0) the X address increments after each byte (see Fig.6). After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 101, Y = 8) the address pointers wrap around to address (X = 0, Y =0)

## Data structure



# ST7556

Page Address				Data		Line Address		COM Output	
D3	D2	D1	D0						
0	0	0	0	D7				00H	COM0
				D6				01H	COM1
				D5				02H	COM2
				D4				03H	COM3
				D3				04H	COM4
				D2				05H	COM5
				D1				06H	COM6
				D0				07H	COM7
0	0	0	1	D7				08H	COM8
				D6				09H	COM9
				D5				0AH	COM10
				D4				0BH	COM11
				D3				0CH	COM12
				D2				0DH	COM13
				D1				0EH	COM14
				D0				0FH	COM15
0	0	1	0	D7				10H	COM16
				D6				11H	COM17
				D5				12H	COM18
				D4				13H	COM19
				D3				14H	COM20
				D2				15H	COM21
				D1				16H	COM22
				D0				17H	COM23
0	0	1	1	D7				18H	COM24
				D6				19H	COM25
				D5				1AH	COM26
				D4				1BH	COM27
				D3				1CH	COM28
				D2				1DH	COM29
				D1				1EH	COM30
				D0				1FH	COM31
0	1	0	0	D7				20H	COM32
				D6				21H	COM33
				D5				22H	COM34
				D4				23H	COM35
				D3				24H	COM36
				D2				25H	COM37
				D1				26H	COM38
				D0				27H	COM39
0	1	0	1	D7				28H	COM40
				D6				29H	COM41
				D5				2AH	COM42
				D4				2BH	COM43
				D3				2CH	COM44
				D2				2DH	COM45
				D1				2EH	COM46
				D0				2FH	COM47
0	1	1	0	D7				30H	COM48
				D6				31H	COM49
				D5				32H	COM50
				D4				33H	COM51
				D3				34H	COM52
				D2				35H	COM53
				D1				36H	COM54
				D0				37H	COM55
0	1	1	1	D7				38H	COM56
				D6				39H	COM57
				D5				3AH	COM58
				D4				3BH	COM59
				D3				3CH	COM60
				D2				3DH	COM61
				D1				3EH	COM62
				D0				3FH	COM63
1	0	0	0	D7				40H	COM64
1	0	0	1	D7				43H	ICON(COMS)

S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32	S33	S34	S35	S36	S37	S38	S39	S40	S41	S42	S43	S44	S45	S46	S47	S48	S49	S50	S51	S52	S53	S54	S55	S56	S57	S58	S59	S60	S61	S62	S63	S64	S65	S66	S67	S68	S69	S70	S71	S72	S73	S74	S75	S76	S77	S78	S79	S80	S81	S82	S83	S84	S85	S86	S87	S88	S89	S90	S91	S92	S93	S94	S95	S96	S97	S98	S99	S100	S101	S102	S103	S104	S105	S106	S107	S108	S109	S110	S111	S112	S113	S114	S115	S116	S117	S118	S119	S120	S121	S122	S123	S124	S125	S126	S127	S128	S129	S130	S131	S132	S133	S134	S135	S136	S137	S138	S139	S140	S141	S142	S143	S144	S145	S146	S147	S148	S149	S150	S151	S152	S153	S154	S155	S156	S157	S158	S159	S160	S161	S162	S163	S164	S165	S166	S167	S168	S169	S170	S171	S172	S173	S174	S175	S176	S177	S178	S179	S180	S181	S182	S183	S184	S185	S186	S187	S188	S189	S190	S191	S192	S193	S194	S195	S196	S197	S198	S199	S200	S201	S202	S203	S204	S205	S206	S207	S208	S209	S210	S211	S212	S213	S214	S215	S216	S217	S218	S219	S220	S221	S222	S223	S224	S225	S226	S227	S228	S229	S230	S231	S232	S233	S234	S235	S236	S237	S238	S239	S240	S241	S242	S243	S244	S245	S246	S247	S248	S249	S250	S251	S252	S253	S254	S255	S256	S257	S258	S259	S260	S261	S262	S263	S264	S265	S266	S267	S268	S269	S270	S271	S272	S273	S274	S275	S276	S277	S278	S279	S280	S281	S282	S283	S284	S285	S286	S287	S288	S289	S290	S291	S292	S293	S294	S295	S296	S297	S298	S299	S300	S301	S302	S303	S304	S305	S306	S307	S308	S309	S310	S311	S312	S313	S314	S315	S316	S317	S318	S319	S320	S321	S322	S323	S324	S325	S326	S327	S328	S329	S330	S331	S332	S333	S334	S335	S336	S337	S338	S339	S340	S341	S342	S343	S344	S345	S346	S347	S348	S349	S350	S351	S352	S353	S354	S355	S356	S357	S358	S359	S360	S361	S362	S363	S364	S365	S366	S367	S368	S369	S370	S371	S372	S373	S374	S375	S376	S377	S378	S379	S380	S381	S382	S383	S384	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396	S397	S398	S399	S400	S401	S402	S403	S404	S405	S406	S407	S408	S409	S410	S411	S412	S413	S414	S415	S416	S417	S418	S419	S420	S421	S422	S423	S424	S425	S426	S427	S428	S429	S430	S431	S432	S433	S434	S435	S436	S437	S438	S439	S440	S441	S442	S443	S444	S445	S446	S447	S448	S449	S450	S451	S452	S453	S454	S455	S456	S457	S458	S459	S460	S461	S462	S463	S464	S465	S466	S467	S468	S469	S470	S471	S472	S473	S474	S475	S476	S477	S478	S479	S480	S481	S482	S483	S484	S485	S486	S487	S488	S489	S490	S491	S492	S493	S494	S495	S496	S497	S498	S499	S500	S501	S502	S503	S504	S505	S506	S507	S508	S509	S510	S511	S512	S513	S514	S515	S516	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528	S529	S530	S531	S532	S533	S534	S535	S536	S537	S538	S539	S540	S541	S542	S543	S544	S545	S546	S547	S548	S549	S550	S551	S552	S553	S554	S555	S556	S557	S558	S559	S560	S561	S562	S563	S564	S565	S566	S567	S568	S569	S570	S571	S572	S573	S574	S575	S576	S577	S578	S579	S580	S581	S582	S583	S584	S585	S586	S587	S588	S589	S590	S591	S592	S593	S594	S595	S596	S597	S598	S599	S600	S601	S602	S603	S604	S605	S606	S607	S608	S609	S610	S611	S612	S613	S614	S615	S616	S617	S618	S619	S620	S621	S622	S623	S624	S625	S626	S627	S628	S629	S630	S631	S632	S633	S634	S635	S636	S637	S638	S639	S640	S641	S642	S643	S644	S645	S646	S647	S648	S649	S650	S651	S652	S653	S654	S655	S656	S657	S658	S659	S660	S661	S662	S663	S664	S665	S666	S667	S668	S669	S670	S671	S672	S673	S674	S675	S676	S677	S678	S679	S680	S681	S682	S683	S684	S685	S686	S687	S688	S689	S690	S691	S692	S693	S694	S695	S696	S697	S698	S699	S700	S701	S702	S703	S704	S705	S706	S707	S708	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720	S721	S722	S723	S724	S725	S726	S727	S728	S729	S730	S731	S732	S733	S734	S735	S736	S737	S738	S739	S740	S741	S742	S743	S744	S745	S746	S747	S748	S749	S750	S751	S752	S753	S754	S755	S756	S757	S758	S759	S760	S761	S762	S763	S764	S765	S766	S767	S768	S769	S770	S771	S772	S773	S774	S775	S776	S777	S778	S779	S780	S781	S782	S783	S784	S785	S786	S787	S788	S789	S790	S791	S792	S793	S794	S795	S796	S797	S798	S799	S800	S801	S802	S803	S804	S805	S806	S807	S808	S809	S810	S811	S812	S813	S814	S815	S816	S817	S818	S819	S820	S821	S822	S823	S824	S825	S826	S827	S828	S829	S830	S831	S832	S833	S834	S835	S836	S837	S838	S839	S840	S841	S842	S843	S844	S845	S846	S847	S848	S849	S850	S851	S852	S853	S854	S855	S856	S857	S858	S859	S860	S861	S862	S863	S864	S865	S866	S867	S868	S869	S870	S871	S872	S873	S874	S875	S876	S877	S878	S879	S880	S881	S882	S883	S884	S885	S886	S887	S888	S889	S890	S891	S892	S893	S894	S895	S896	S897	S898	S899	S900	S901	S902	S903	S904	S905	S906	S907	S908	S909	S910	S911	S912	S913	S914	S915	S916	S917	S918	S919	S920	S921	S922	S923	S924	S925	S926	S927	S928	S929	S930	S931	S932	S933	S934	S935	S936	S937	S938	S939	S940	S941	S942	S943	S944	S945	S946	S947	S948	S949	S950	S951	S952	S953	S954	S955	S956	S957	S958	S959	S960	S961	S962	S963	S964	S965	S966	S967	S968	S969	S970	S971	S972	S973	S974	S975	S976	S977	S978	S979	S980	S981	S982	S983	S984	S985	S986	S987	S988	S989	S990	S991	S992	S993	S994	S995	S996	S997	S998	S999	S1000	S1001	S1002	S1003	S1004	S1005	S1006	S1007	S1008	S1009	S1010	S1011	S1012	S1013	S1014	S1015	S1016	S1017	S1018	S1019	S1020	S1021	S1022	S1023	S1024	S1025	S1026	S1027	S1028	S1029	S1030	S1031	S1032	S1033	S1034	S1035	S1036	S1037	S1038	S1039	S1040	S1041	S1042	S1043	S1044	S1045	S1046	S1047	S1048	S1049	S1050	S1051	S1052	S1053	S1054	S1055	S1056	S1057	S1058	S1059	S1060	S1061	S1062	S1063	S1064	S1065	S1066	S1067	S1068	S1069	S1070	S1071	S1072	S1073	S1074	S1075	S1076	S1077	S1078	S1079	S1080	S1081	S1082	S
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## Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to VDD. An external clock signal, if used, is connected to this input.

## Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 102-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving waveform and internal timing signal are shown in Figure 8.

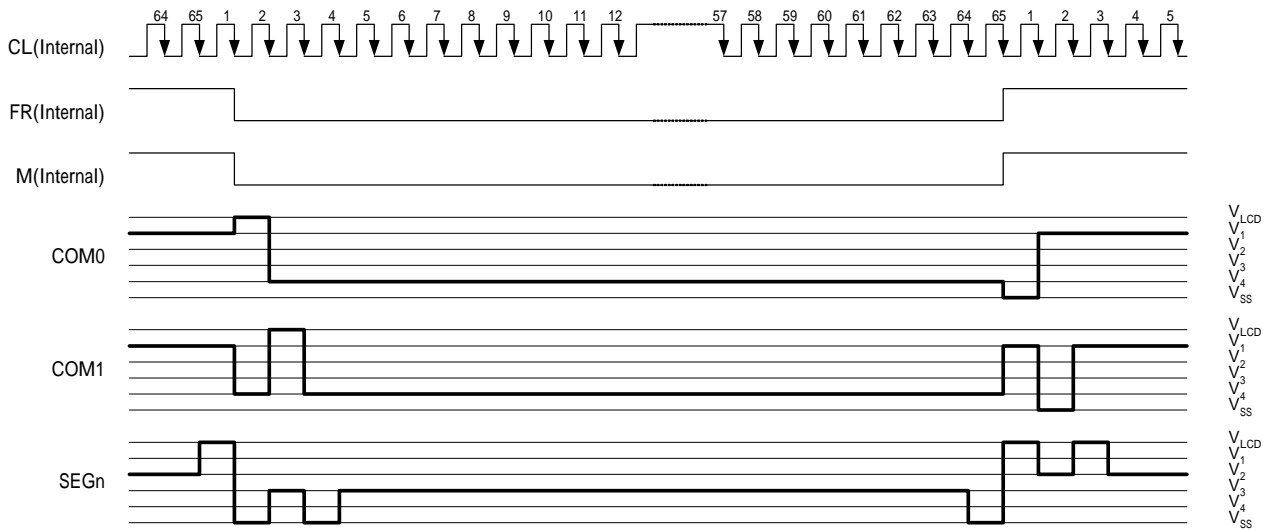


Fig 8. 2-frame AC Driving Waveform (Duty Ratio: 1/65)

## 7. RESET CIRCUIT

Setting RESB to “ L ” or Reset instruction can initialize internal function.

When RESB becomes “ L ”, following procedure is executed

Page address: 0

Column address: 0

Oscillator: OFF

Power down mode (PD = 1)

Horizontal addressing (V = 0)

normal instruction set (H = 0)

Display OFF (D = E = 0)

Address counter X [6:0] = 0, Y [2:0] = 0

Bias system (BS [2:0] = 0)

VLCD is equal to 0; the HV generator is switched off (VOP [6:0] = 0)

After power-on, RAM data are undefined

While RESB is “ L ” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB6. After DB6 becomes “ L ”, any instruction can be accepted. RESB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESB is essential before used.

## 8. INSTRUCTION TABLE

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
<b>H=0 or 1</b>											
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Reset	0	0	0	0	0	0	0	0	1	1	Internal reset
Function set	0	0	0	0	1	0	0	PD	V	H	Power-down; entry mode; Extended instruction control
Read status byte	0	1	PD	RST	BUSY	D	E	1	0	1	Read status byte
Read data	1	1	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Read data from RAM
Write data	1	0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Write data to RAM

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
<b>H=0</b>											
Display control	0	0	0	0	0	0	1	D	0	E	Set display configuration
Set Y address of RAM	0	0	0	1	0	0	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>	Sets Y address of RAM 0 Y 9
Set X address of RAM	0	0	1	X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Sets X address of RAM 0 X 101
<b>H=1</b>											
SW Internal register initial	0	0	0	0	0	0	1	1	1	0	S/W Internal register initial
	0	0	0	0	0	1	0	0	1	0	
Bias system	0	0	0	0	0	1	0	BS <sub>2</sub>	BS <sub>1</sub>	BS <sub>0</sub>	Sets bias system (BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	Do not use
Set V <sub>OP</sub>	0	0	1	V <sub>OP6</sub>	V <sub>OP5</sub>	V <sub>OP4</sub>	V <sub>OP3</sub>	V <sub>OP2</sub>	V <sub>OP1</sub>	V <sub>OP0</sub>	Write V <sub>OP</sub> to register

## 9. INSTRUCTION DESCRIPTION

**H="0" or "1"**

### Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status. This instruction cannot initialize the LCD power supply, which is initialized by the RESB pin.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

### Function Set

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	PD	V	H

Flag	Description
PD	All LCD outputs at VSS (display off), bias generator and VLCD generator off, VLCD can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written. PD=0:chip is active PD=1:chip is in power down mode
V	When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig13. When V = 1, the vertical addressing is selected. The data is written into the DDRAM as shown in Fig12
H	When H = 0 the commands ' display control ', ' set Y address ' and ' set X address ' can be performed, when H = 1 the others can be executed. The commands ' write data ' and ' function set ' can be executed in both cases. H=0:use basic instruction set H=1:use extended instruction set

### Read status byte

Indicates the internal status of the ST7556

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	RST	BUSY	D	E	1	0	1

Flag	Description
PD	PD=0:chip is active PD=1:chip is in power down mode
RST	Indicates the initialization is in progress by RESET signal 0: chip is active,1:chip is being reset
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes LOW. 0:chip is active;1:chip is being busy
D,E	D   E   The bits D and E select the display mode.
	0   0   Display blank
	0   1   All display segments on
	1   0   Normal mode
	1   1   Inverse video mode
D2~D0	ST7556 will return the fix data "101" as identification bit

### Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

# ST7556

H="0"

## Display Control

This bits D and E selects the display mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display off
	1	0	Normal display
	0	1	All display segments on
	1	1	Inverse video mode

## Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>

## X/Y Address range

Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>	CONTENT	ALLOWED X-RANGE
0	0	0	0	Page0 (display RAM)	0 to 101
0	0	0	1	Page1 (display RAM)	0 to 101
0	0	1	0	Page2 (display RAM)	0 to 101
0	0	1	1	Page3 (display RAM)	0 to 101
0	1	0	0	Page4 (display RAM)	0 to 101
0	1	0	1	Page5 (display RAM)	0 to 101
0	1	1	0	Page6 (display RAM)	0 to 101
0	1	1	1	Page7 (display RAM)	0 to 101
1	0	0	0	Page8 (display RAM)	0 to 101
1	0	0	1	Page9 (display RAM)	0 to 101

## Set X address of RAM

The X address points to the columns. The range of X is 0...101.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>

X <sub>6</sub>	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101



# ST7556

H="1"

## S/W initial internal register

The 1<sup>st</sup> Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	1	0

The 2<sup>nd</sup> Instruction

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	1	0

## System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS <sub>2</sub>	BS <sub>1</sub>	BS <sub>0</sub>

BS <sub>2</sub>	BS <sub>1</sub>	BS <sub>0</sub>	Bias	Recommend Duty
0	0	0	11	1:100
0	0	1	10	1:80
0	1	0	9	1:65/1:68
0	1	1	8	1:48
1	0	0	7	1/40:1/34
1	0	1	6	1/24
1	1	0	5	1:18/1:16
1	1	1	4	1:10/1:9/1:8

## LCD bias voltage

Symbol	Bias voltage for 1/8 bias	Symbol	Bias voltage for 1/8 bias
VLCDIN	VLCDIN	V3	2/8 X VLCDIN
V1	7/8 X VLCDIN	V4	1/8 X VLCDIN
V2	6/8 X VLCDIN	VSS	VSS

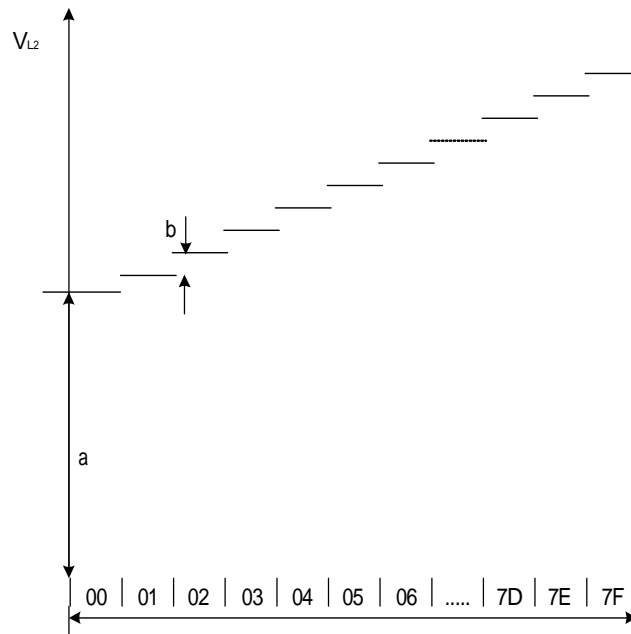
**Set VOP value:**

The operation voltage  $V_{LCD}$  can be set by software.

$$V_0 = (a + V_{OP} \times b) \tag{1}$$

**Typical values for parameter for the HV-Generator programming**

SYMBOL	VALUE	UNIT
a	6.75	V
b	0.03	V



VOP [6:0](programmed) {00 hex... 7F hex}

**Fig 13.  $V_{OP}$  programming of ST7556**

**Caution**

As the programming range for the internally generated VLCDIN allows values above the max allowed VLCDIN, the customer has to ensure while setting the VOP register that under all condition and including all tolerances the VLCD limit of max. 13V will never be exceeded. As VLCDIN increases with lower temperatures, care must be taken not to set a Vop generating a VLCDIN voltage that will exceed the maximum of 10.6V when operating at  $-30$  .

## 10. COMMAND DESCRIPTION

### Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

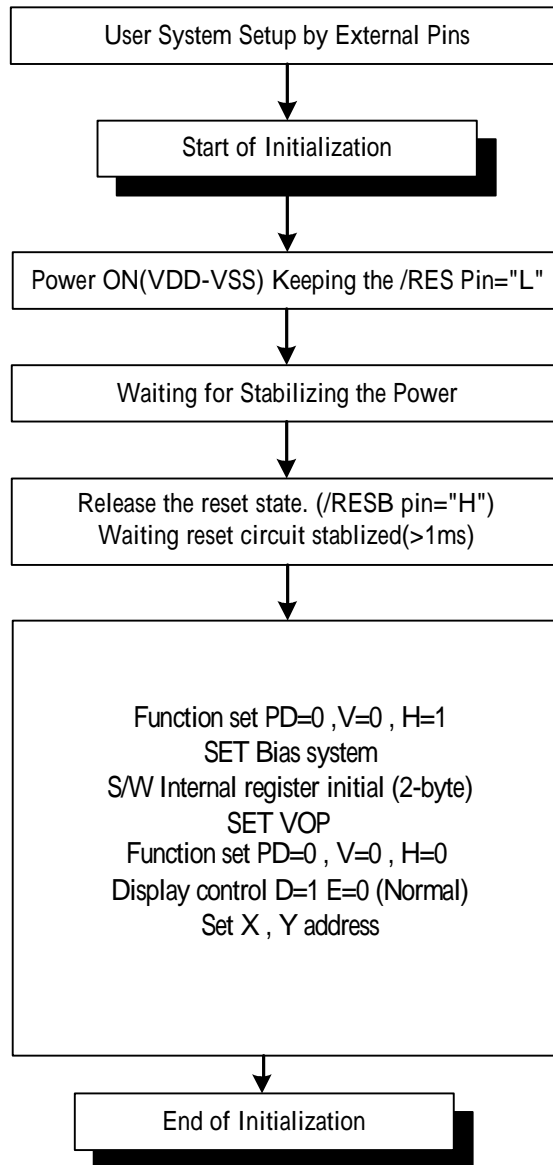


Fig 14. Initializing with the Built-in Power Supply Circuits

## Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits

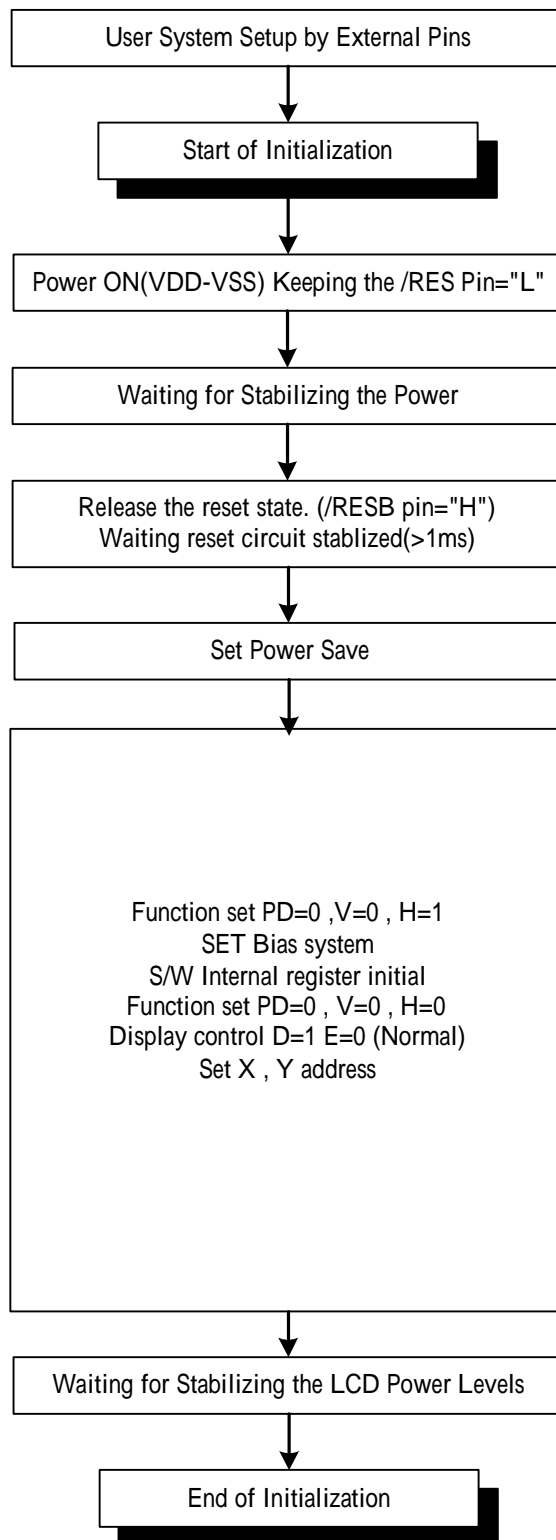


Fig 15. Initializing without Built-in Power Supply Circuits

## Referential Instruction Setup Flow: Data Displaying

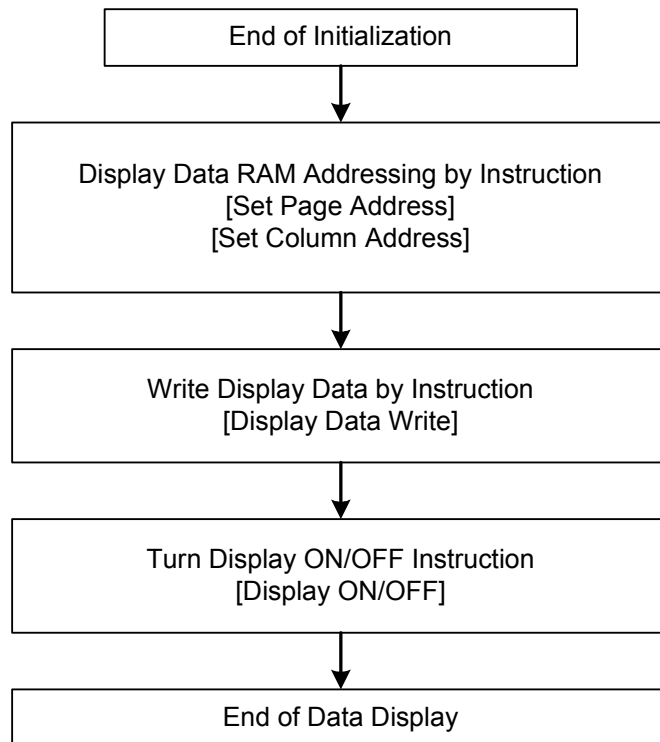


Figure 16.Data Displaying

## Referential Instruction Setup Flow: Power OFF

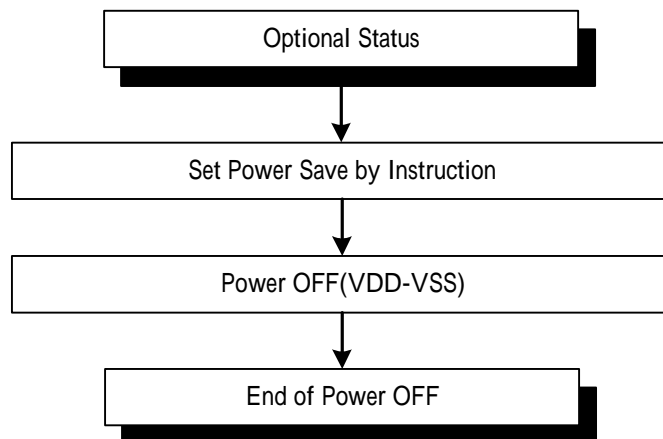
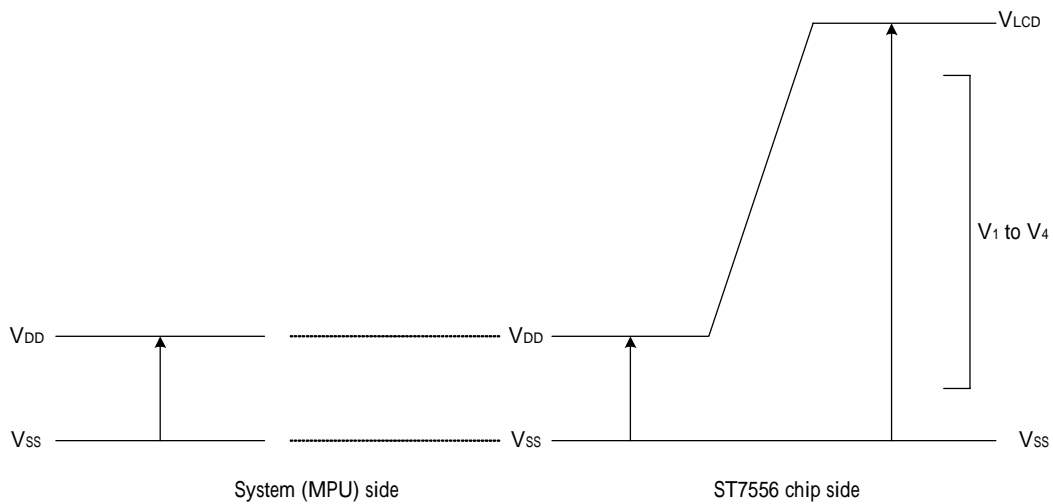


Figure 17. Power OFF

## 11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD, VDD2	-0.3 ~ +3.6	V
Power supply voltage	V0	3.0 ~ 12	V
Power supply voltage	VLCDIN	-0.3 ~ +13.5	V
Power supply voltage	V1, V2, V3, V4	0.3 to VLcdin	V
Input voltage	VIN	-0.5 to VDD+0.5	V
Output voltage	VO	-0.5 to VDD+0.5	V
Operating temperature	TOPR	-30 to +85	°C
Storage temperature	TSTR	-65 to +150	°C



### Notes

- Stresses above those listed under Limiting Values may cause permanent damage to the device.
  - Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V<sub>SS</sub> unless otherwise noted.
  - Insure that the voltage levels of V1, V2, V3, and V4 are always such that
- VLCD    V0    V1    V2    V3    V4    Vss

**12. DC CHARACTERISTICS**

$V_{DD} = 1.8\text{ V to }3.3\text{V}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{LCD} = 3.0\text{ to }13.0\text{V}$ ;  $T_{amb} = -30$  to  $+85$  ; unless otherwise specified.

Item	Symbol	Condition	Rating			Units	Applicable Pin	
			Min.	Typ.	Max.			
Operating Voltage (1)	VDD		1.8	—	3.3	V	Vss*1	
Operating Voltage (2)	VDD2	(Relative to VSS)	1.8	—	3.3	V	VSS2	
High-level Input Voltage	VIHC		0.7 x VDD	—	VDD	V	*2	
Low-level Input Voltage	VILC		VSS	—	0.3 x VDD	V	*2	
High-level Output Voltage	VOHC		0.7 x VDD	—	VDD	V	*3	
Low-level Output Voltage	VOLC		VSS	—	0.3 x VDD	V	*3	
Input leakage current	ILI	VIN = VDD or VSS	-1.0	—	1.0	μ A	*4	
Output leakage current	ILO	VIN = VDD or VSS	-3.0	—	3.0	μ A	*5	
Liquid Crystal Driver ON Resistance	RON	Ta = 25°C (Relative To VSS)	VLCDIN = 13.0 V	—	2.0	3.5	K	SEGn COMn *6
			VLCDIN = 8.0 V	—	3.2	5.4		
Oscillator Frequency	Internal Oscillator	fOSC	1/65 duty Ta = 25°C	—	80	84	kHz	*7
	External Input	fCL		—	80	84	kHz	OSC
	Frame frequency	fFRAME		—	77	80.3	Hz	

Item	Symbol	Condition	Rating			Units	Applicable Pin	
			Min.	Typ.	Max.			
Internal Power	Input voltage	VDD	(Relative To VSS)	1.8	—	3.3	V	
	Supply Step-up output voltage Circuit	VLCDOUT	(Relative To VSS)	—	—	13.5	V	VLCDOUT
	Voltage regulator Circuit Operating Voltage	VLCDIN	(Relative To VSS)	—	—	13.5	V	VLCDIN

Bare Dice Consumption Current : During Display, with the Internal Power Supply, Current consumed by total ICs when an external power supply(VDD,VDD2) is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDD,VDD2 = 3.0 V, V0 – VSS = 9.0 V 4X Booster 1/9 Bias	—	300	400	μ A	*8
Power Down	ISS	VDD=3.0V Ta = 25°C	—	0.01	2	μ A	

### Notes to the DC characteristics

1. The maximum possible  $V_{LCD}$  voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.
4. If external  $V_{LCDIN}$ , the display load current is not transmitted to  $I_{DD}$ .
5.  $V_{OUT}$  external voltage applied to VLCDIN pin; VLCDIN disconnected from VLCDOUT (no connect)

### References for items market with \*

- \*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.
- \*2 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.
- \*3 The D0 to D7, and OSC terminals.
- \*4 The A0,/RD (E), /WR ,/(R/W), CSB, IMS, OSC, P/S, /DOF, RESB ,and MODE terminals.
- \*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.
- \*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.  
 $RON = 0.1 \text{ V} / \Delta I$  (Where  $\Delta I$  is the current that flows when 0.1 V is applied while the power supply is ON.)
- \*7 The relationship between the oscillator frequency and the frame rate frequency.
- \*8,9It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.



### 13. TIMING CHARACTERISTICS

#### System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

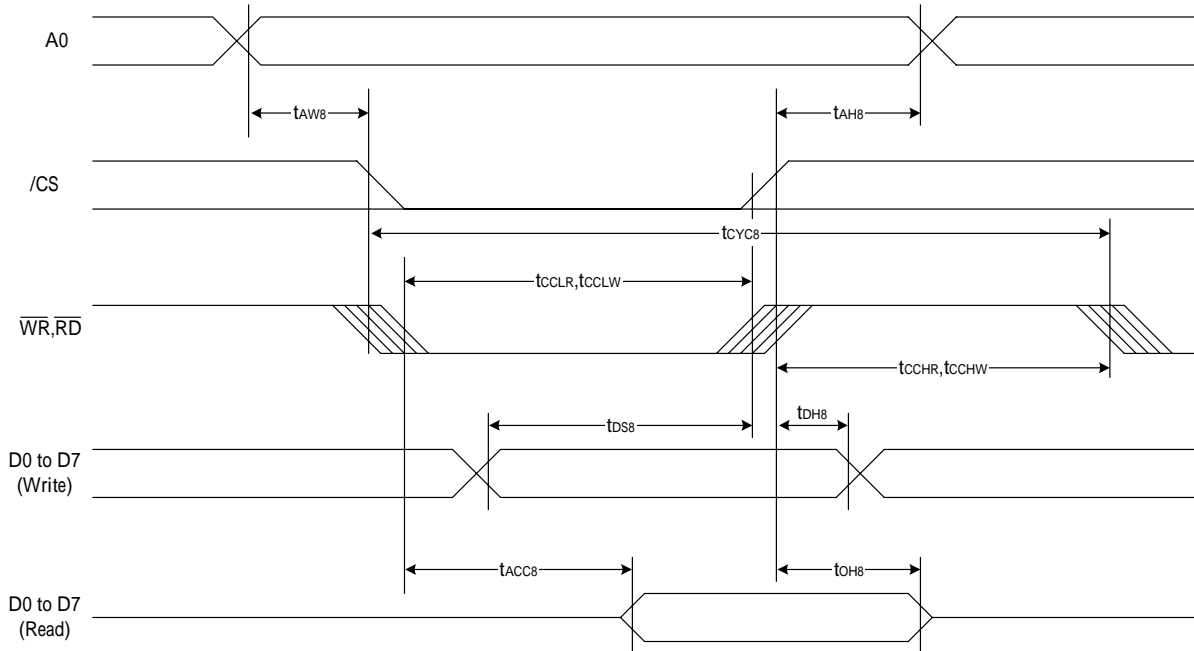


Figure 18.

(VDD = 3.3V , Ta = -30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V , Ta = 30~85°C )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		15	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V , Ta = 30~85°C )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280	—	
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Address hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) (tCYC8 – tCCLW – tCCHW) for (tr + tf) (tCYC8 – tCCLR – tCCHR) are specified.

\*2 All timing is specified using 20% and 80% of VDD as the reference.

\*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

## System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

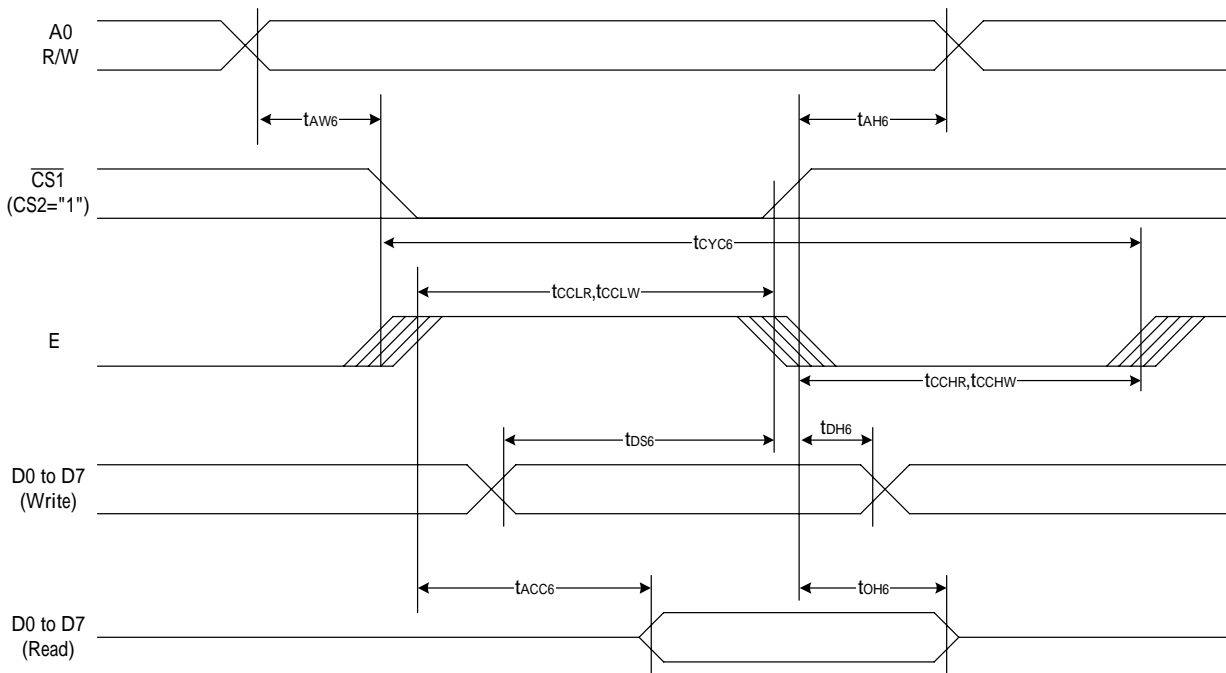


Figure 19.

(V<sub>DD</sub> = 3.3 V , T<sub>a</sub> = 30~85°C )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =30~85°C )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		15	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD =1.8V , Ta =30~85°C )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		30	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Address hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) (tCYC6 – tEWLW – tEWHW) for (tr + tf) (tCYC6 – tEWLR – tEWHR) are specified.

\*2 All timing is specified using 20% and 80% of VDD as the reference.

\*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

## SERIAL INTERFACE (4-Line Interface)

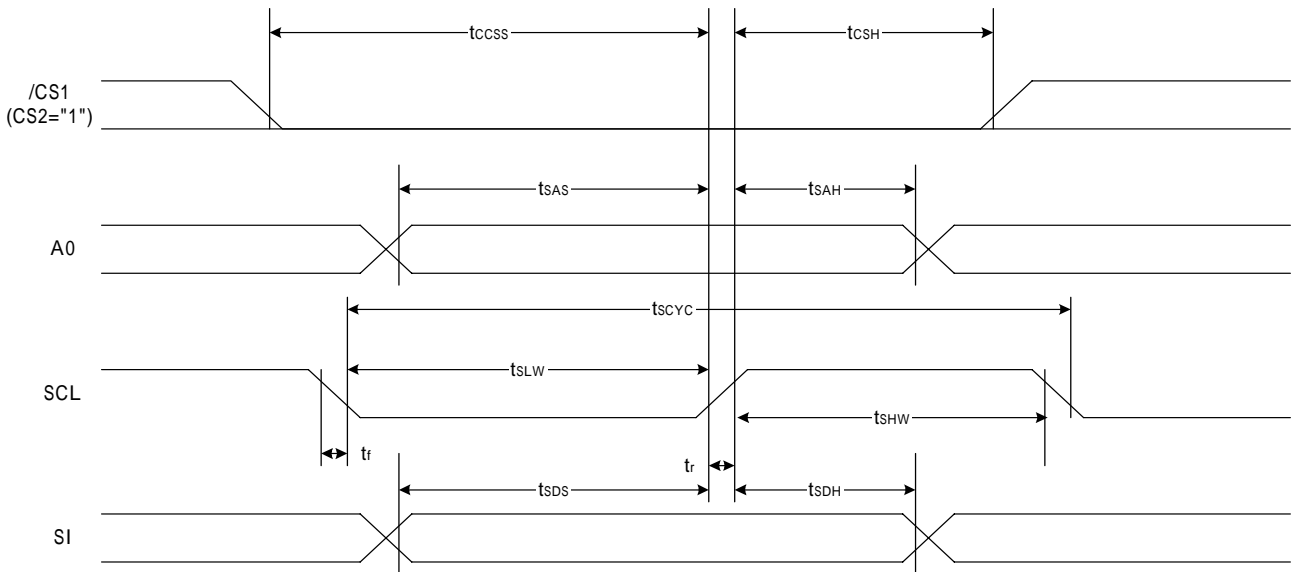


Fig 20.

( $V_{DD}=3.3V, T_a=30\sim 85$  )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL "H" pulse width		tSHW		25	—	
SCL "L" pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		140	—	

( $V_{DD}=2.7V, T_a=30\sim 85$  )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		50	—	
SCL "L" pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		160	—	

(V<sub>DD</sub>=1.8V, Ta=30~85 )

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		200	—	

\*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

\*2 All timing is specified using 20% and 80% of VDD as the standard.

## 14. RESET TIMING

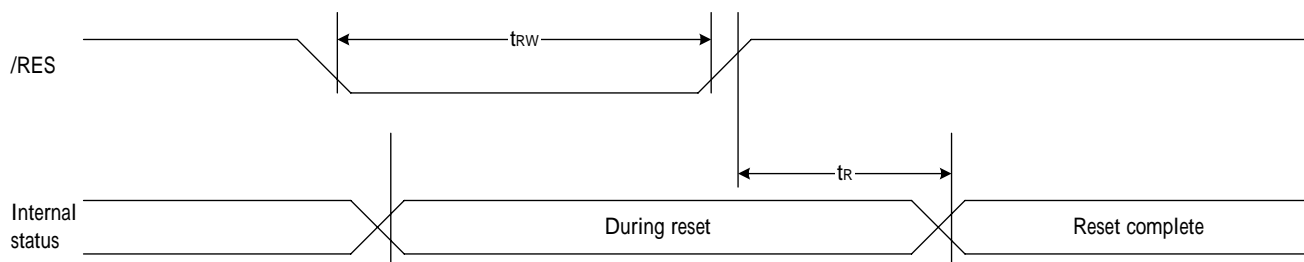


Fig 21.

(VDD = 3.3V , Ta = -30 to 85°C )

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset "L" pulse width	RESB	tRW		1	—	—	us

(VDD = 2.7V , Ta = -30 to 85°C )

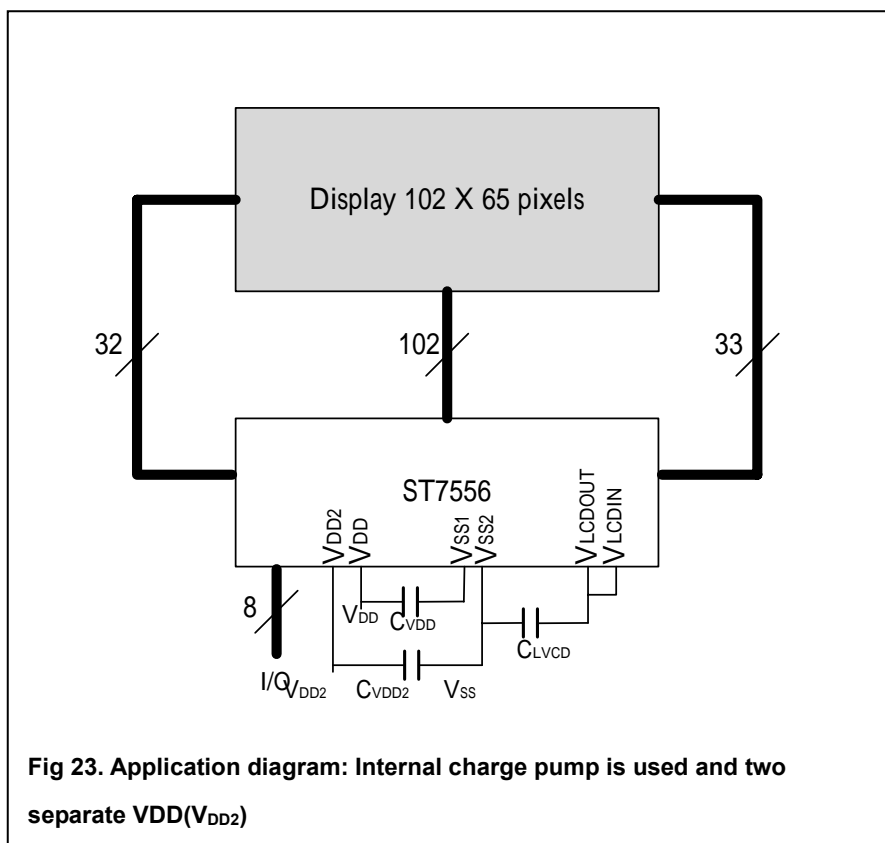
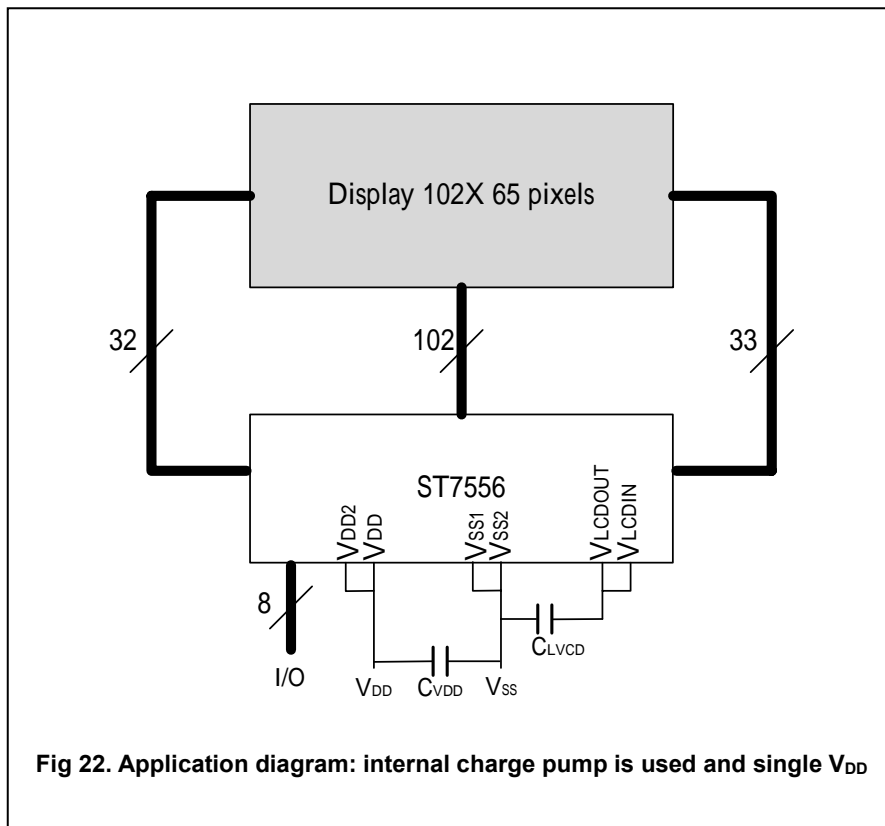
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset "L" pulse width	RESB	tRW		1.5	—	—	us

(VDD = 1.8V , Ta = -30 to 85°C )

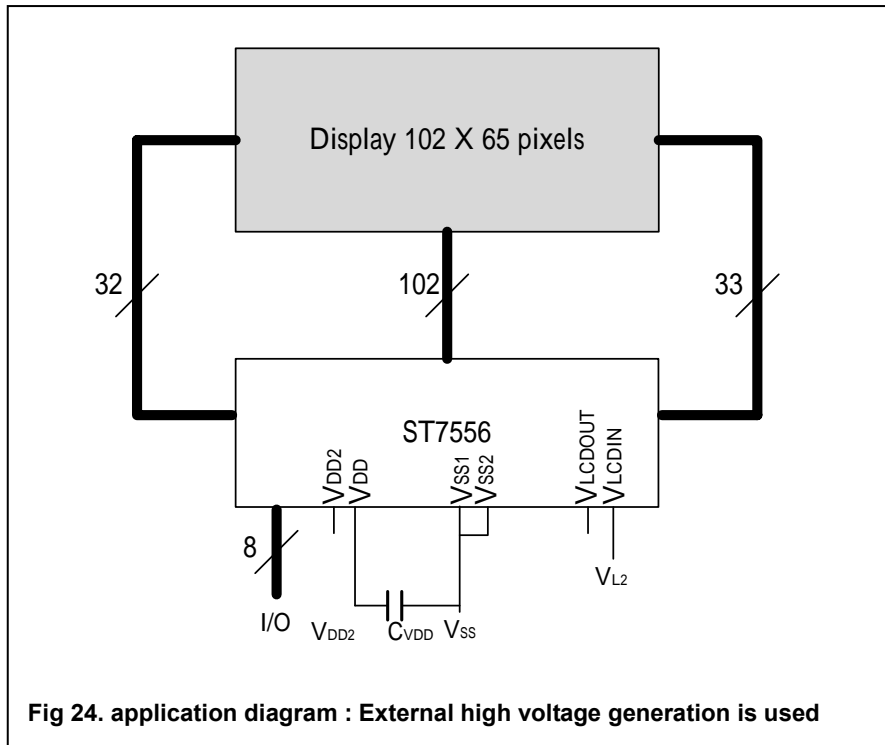
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset "L" pulse width	RESB	tRW		2.0	—	—	us

## 15. APPLICATION INFORMATION

The pinning of the ST7556 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 64x102 pixels.







The required minimum value for the external capacitors in an application with the ST7556 are:

$$C_{VLCD} = \text{min. } 100\text{nF} \quad C_{VDD,2} = \text{min. } 1.0 \mu\text{F}$$

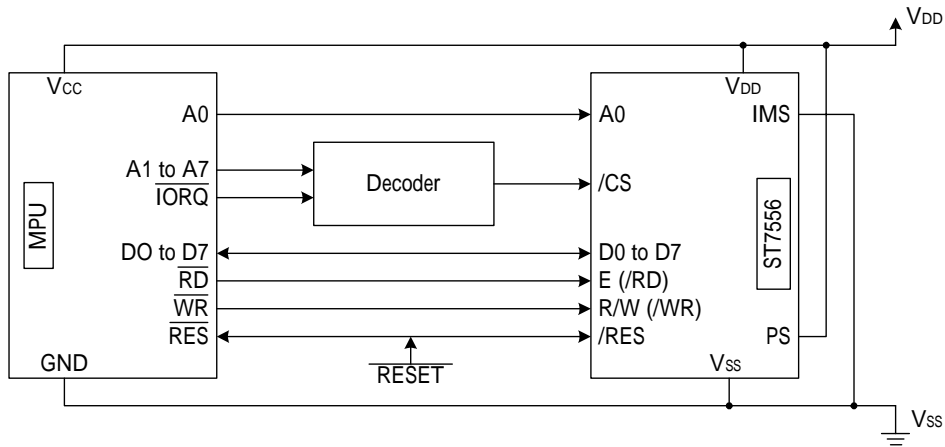
Higher capacitor values are recommended for ripple reduction.

## 16. THE MPU INTERFACE (REFERENCE EXAMPLES)

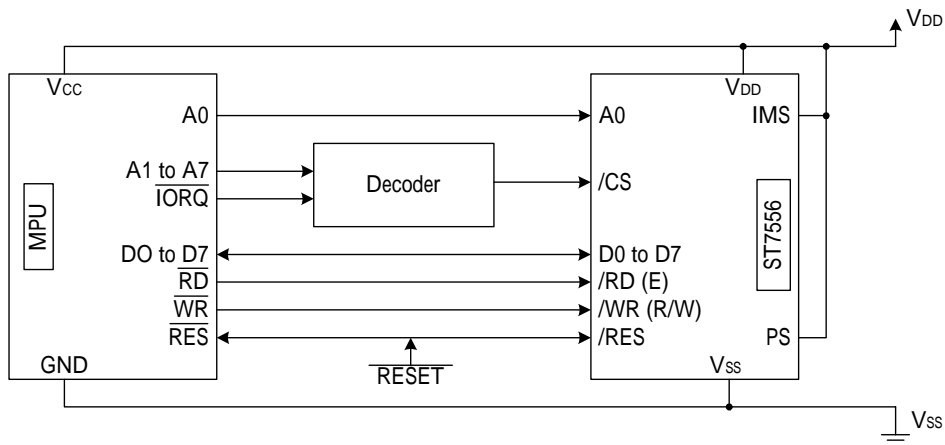
The ST7556 Series can be connected to either 80X86 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7556 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7556 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

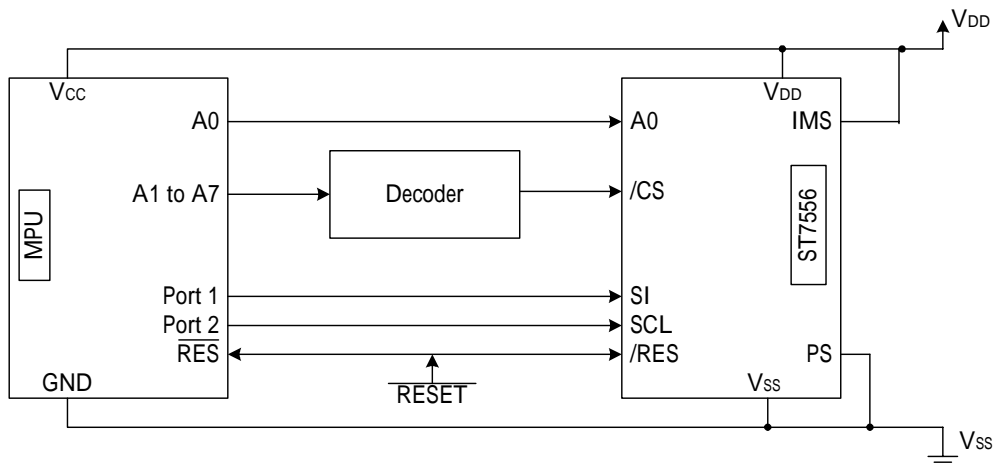
### (1) 8080 Series MPUs



### (2) 6800 Series MPUs



### (3) Using the Serial Interface (4-line interface)



17. ST7556 Application Note (96x65)

