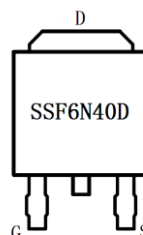
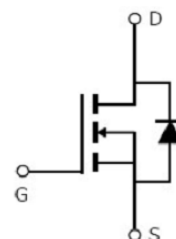


Main Product Characteristics:

V_{DSS}	400V
$R_{DS(on)}$	0.85Ω (typ.)
I_D	5.5A


TO-252

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	5.5	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	3.5	
I_{DM}	Pulsed Drain Current②	22	
$P_D @ TC = 25^\circ C$	Power Dissipation③	50	W
	Linear Derating Factor	0.4	W/°C
V_{DS}	Drain-Source Voltage	400	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=22mH	345	mJ
I_{AS}	Avalanche Current @ L=22mH	5.6	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

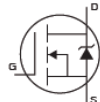
Thermal Resistance

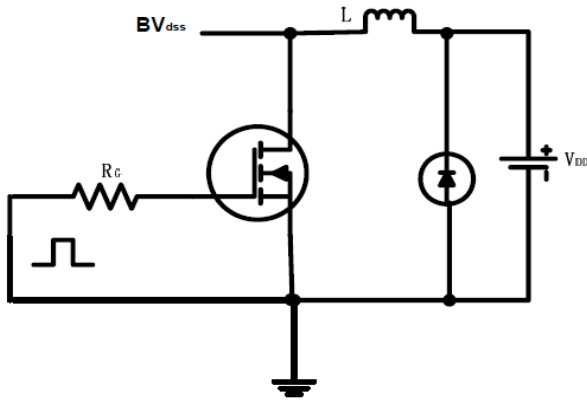
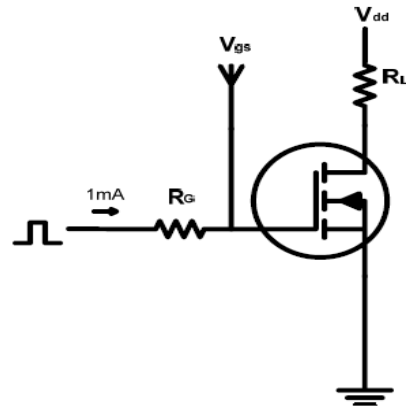
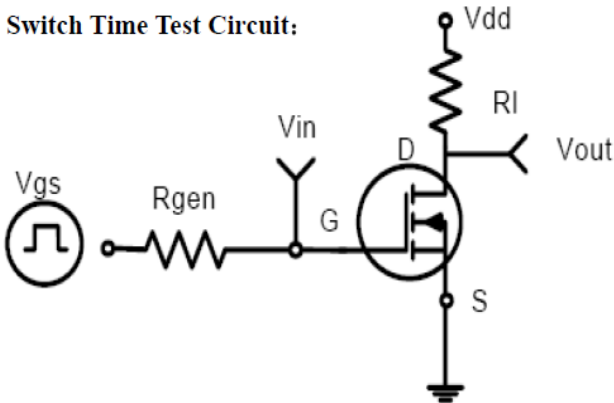
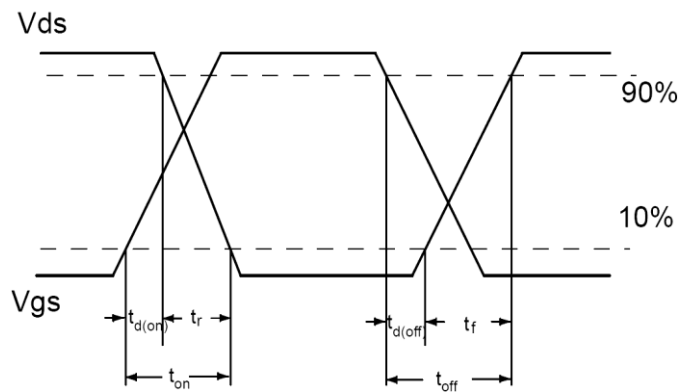
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	2.5	°C/W
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ^④	—	110	°C/W

Electrical Characterizes @ $T_A=25^\circ C$ unless otherwise specified

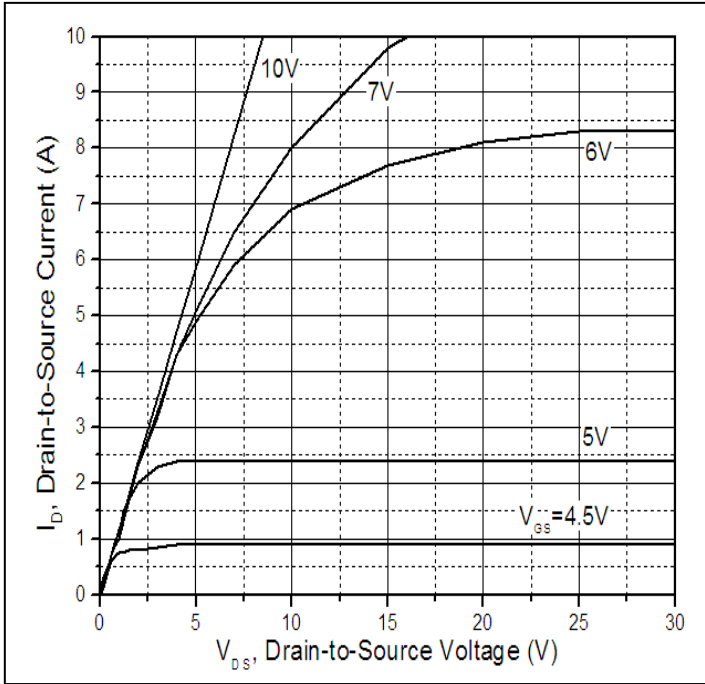
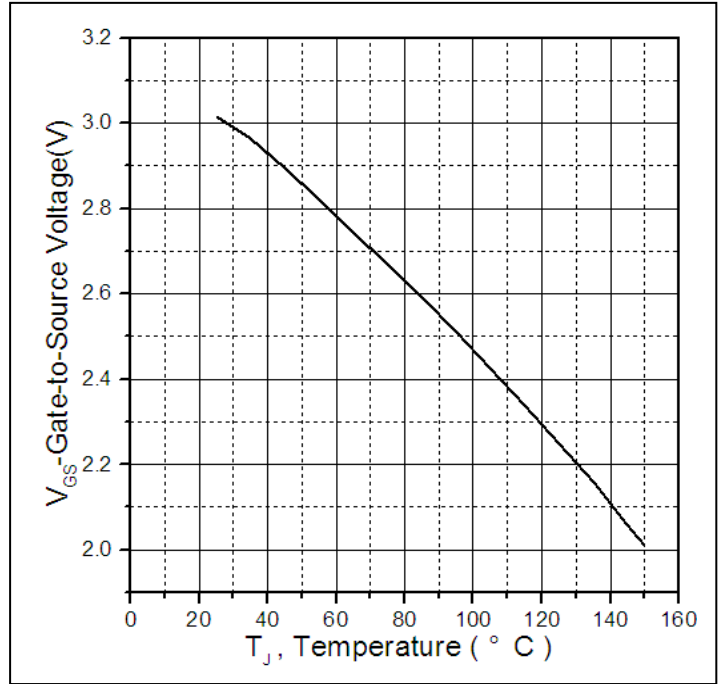
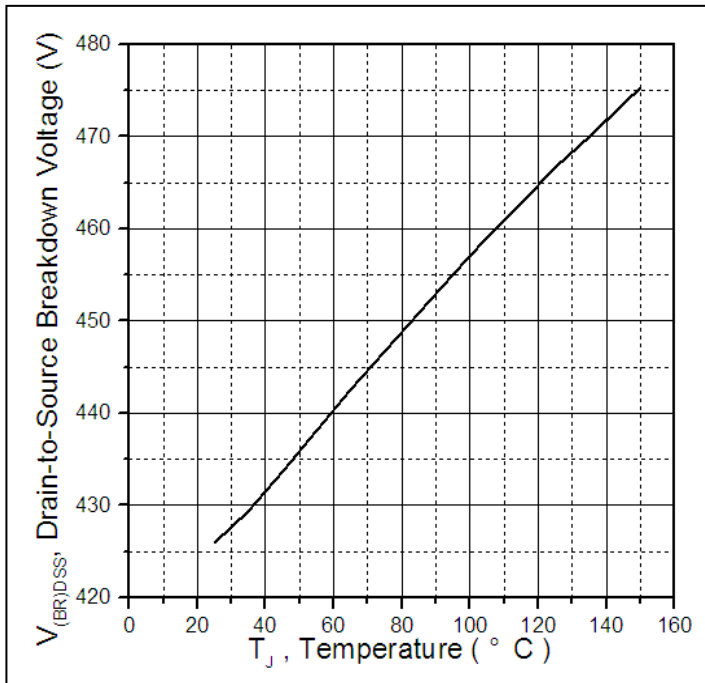
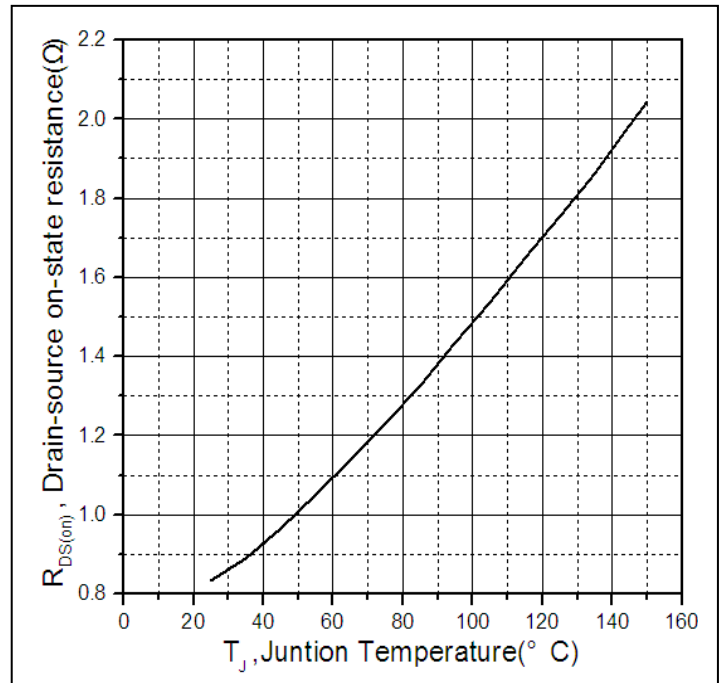
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	400	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.85	1.0	Ω	$V_{GS}=10V, I_D = 2.75A$
		—	1.75	—		$T_J = 125^\circ C$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.25	—		$T_J = 125^\circ C$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 400V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ C$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30V$
		—	—	-100		$V_{GS} = -30V$
Q_g	Total gate charge	—	16.1	—	nC	$I_D = 5.5A,$ $V_{DS}=320V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	3.9	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	6.0	—		
$t_{d(on)}$	Turn-on delay time	—	11.3	—	ns	$V_{GS}=10V, V_{DS}=200V,$ $R_{GEN}=25\Omega, I_D=5.5A$
t_r	Rise time	—	18.0	—		
$t_{d(off)}$	Turn-Off delay time	—	37.9	—		
t_f	Fall time	—	18.9	—		
C_{iss}	Input capacitance	—	643	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	79.0	—		$V_{DS} = 25V$
C_{rss}	Reverse transfer capacitance	—	5.14	—		$f = 1MHz$

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	22	A	
V_{SD}	Diode Forward Voltage	—	0.89	1.4	V	$I_S=5.5A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	267	—	ns	$T_J = 25^\circ C, I_F = 5.5A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	1644	—	nC	

Test circuits and Waveforms
EAS test circuits:

Gate charge test circuit:

Switch Time Test Circuit:

Switch Waveforms:

Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$

Typical electrical and thermal characteristics

Figure 1. Typical Output Characteristics

Figure 2. Gate to source cut-off voltage

Figure 3. Drain-to-Source Breakdown Voltage vs. Case Temperature

Figure 4. Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

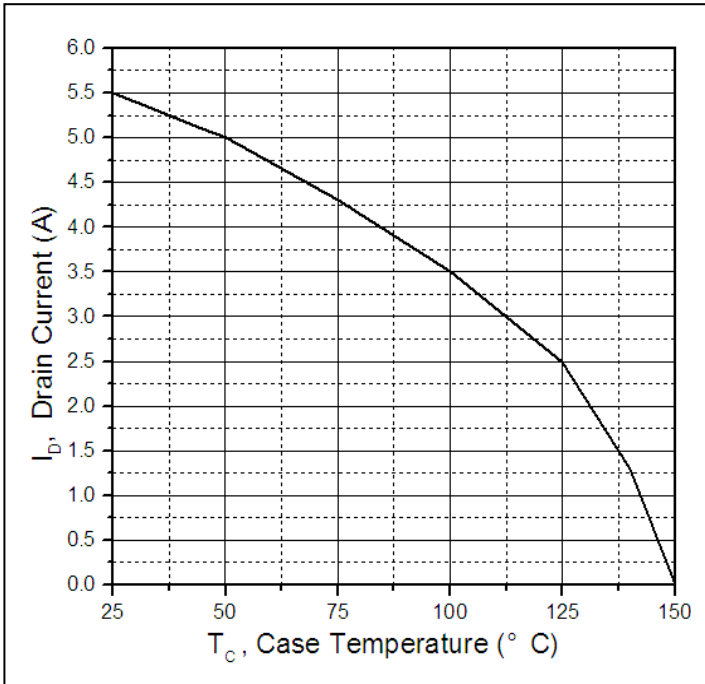


Figure 5. Maximum Drain Current Vs. Case Temperature

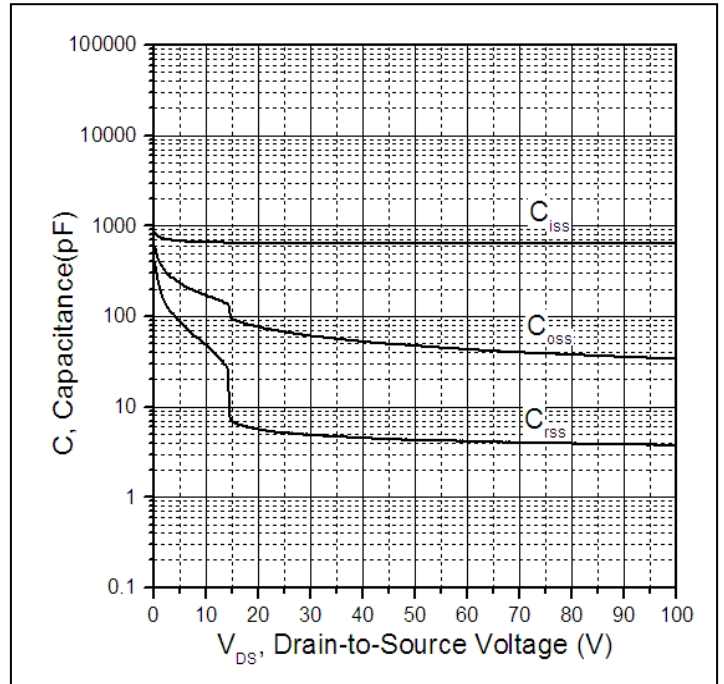


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

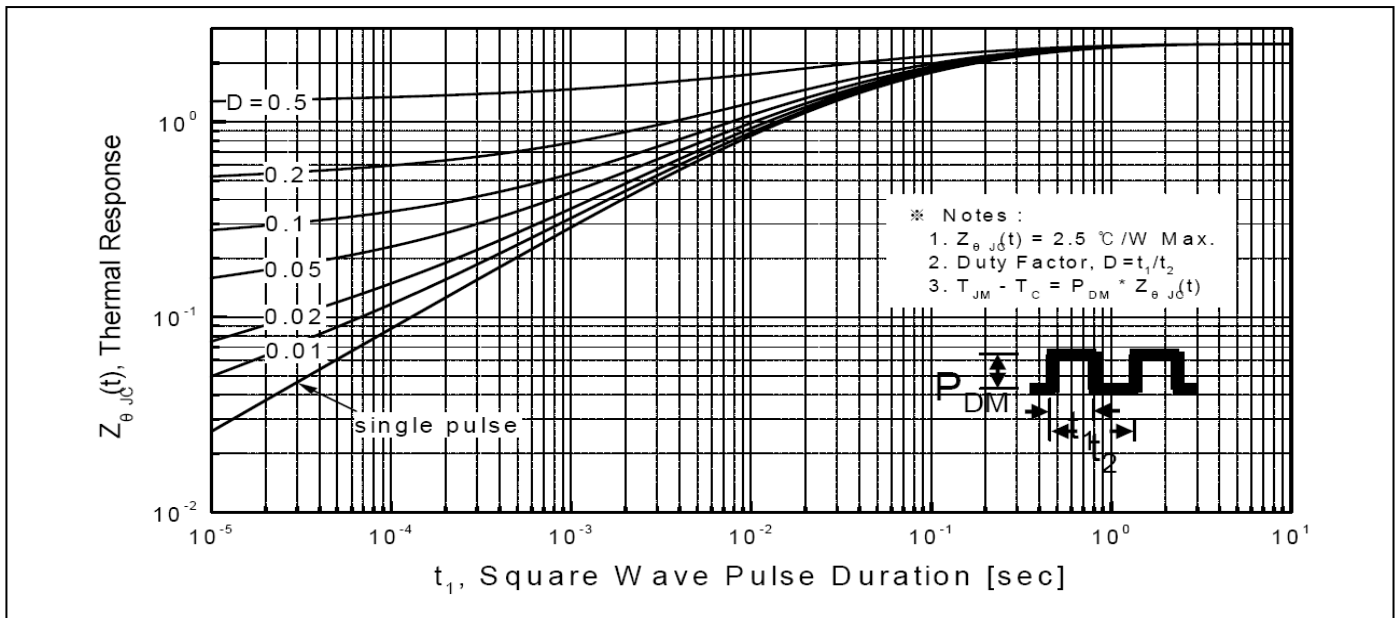
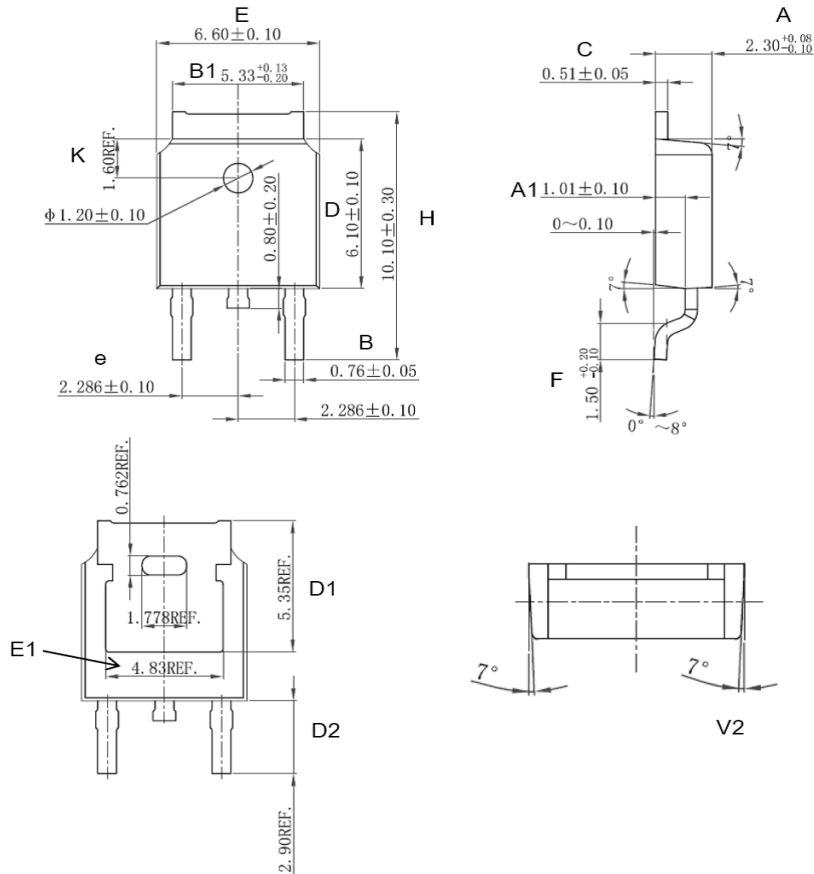


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:
TO-252 PACKAGE OUTLINE DIMENSION


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A1	0.910	1.010	1.110	0.036	0.040	0.044
B	0.710	0.760	0.810	0.028	0.030	0.032
B1	5.130	5.330	5.460	0.202	0.210	0.215
C	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1	5.350 (REF)			0.211 (REF)		
D2	2.900 (REF)			0.114 (REF)		
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	4.83 (REF)			0.190 (REF)		
e	2.186	2.286	2.386	0.086	0.090	0.094
H	9.800	10.100	10.400	0.386	0.398	0.409
F	1.400	1.500	1.700	0.055	0.059	0.067
K	1.600 (REF)			0.063 (REF)		
V2	8° (REF)			8° (REF)		

Ordering and Marking Information
Device Marking: SSF6N40D

Package (Available)
TO-252 (DPAK)
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit
Option1:

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO-252	2500	2	5000	7	35000

Option2:

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO-252	2500	1	2500	10	25000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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Customer Service**Worldwide Sales and Service:**

Sales@silikron.com

Technical Support:

Technical@silikron.com

Suzhou Silikron Semiconductor Corp.

11A, 428 Xinglong Street, Suzhou Industrial Park, P.R.China

TEL: (86-512) 62560688

FAX: (86-512) 65160705

E-mail: Sales@silikron.com