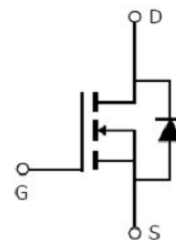


**Main Product Characteristics:**

$V_{DSS}$	100V
$R_{DS(on)}$	13.8mohm(typ.)
$I_D$	75A <sup>①</sup>


**D2PAK**

**Marking and pin Assignment**

**Schematic diagram**
**Features and Benefits:**

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


**Description:**

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

**Absolute max Rating:**

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	75	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	65	
$I_{DM}$	Pulsed Drain Current ②	300	
$P_D @ TC = 25^\circ C$	Power Dissipation ③	273	W
	Linear Derating Factor	1.8	W/°C
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=0.3mH	153	mJ
$I_{AS}$	Avalanche Current @ L=0.3mH	32	A
$T_J T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C

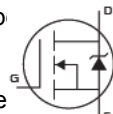
## Thermal Resistance

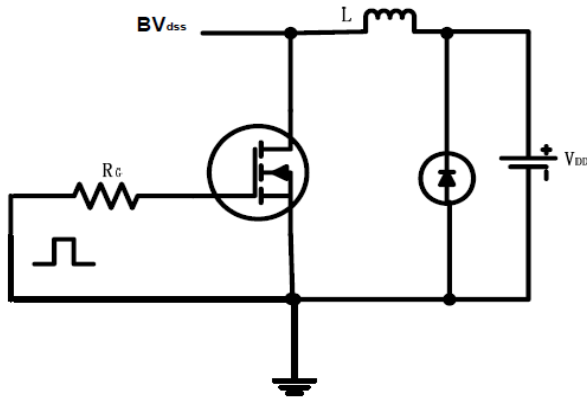
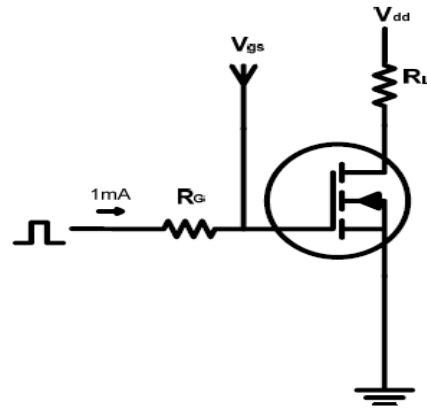
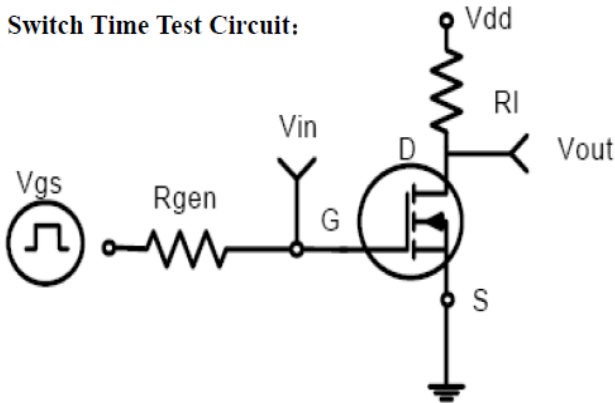
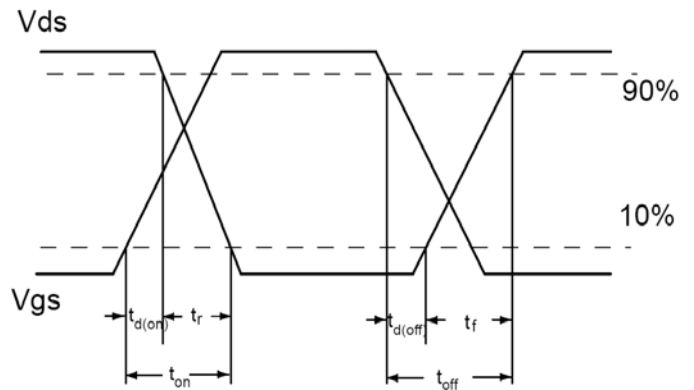
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.55	°C/W
$R_{\theta JA}$	Junction-to-ambient ( $t \leq 10s$ )④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

## Electrical Characterizes @ $T_A=25^\circ\text{C}$ unless otherwise specified

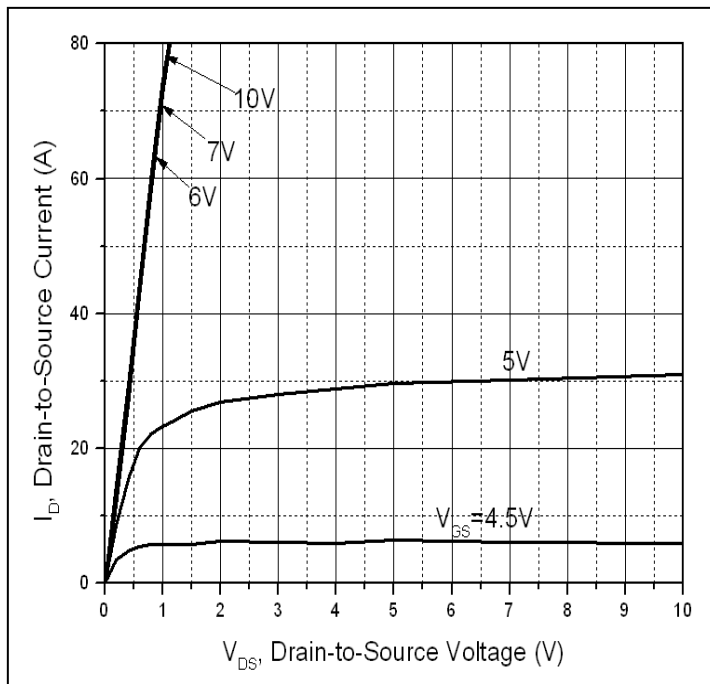
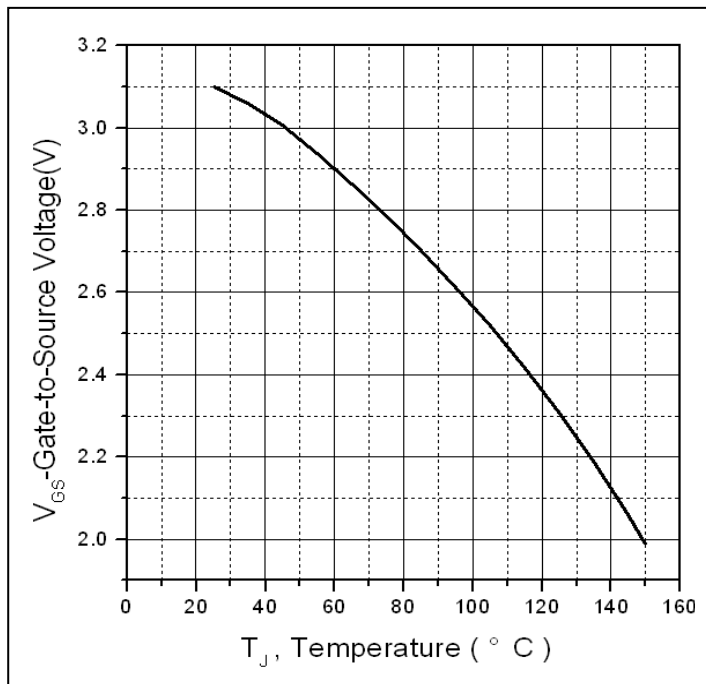
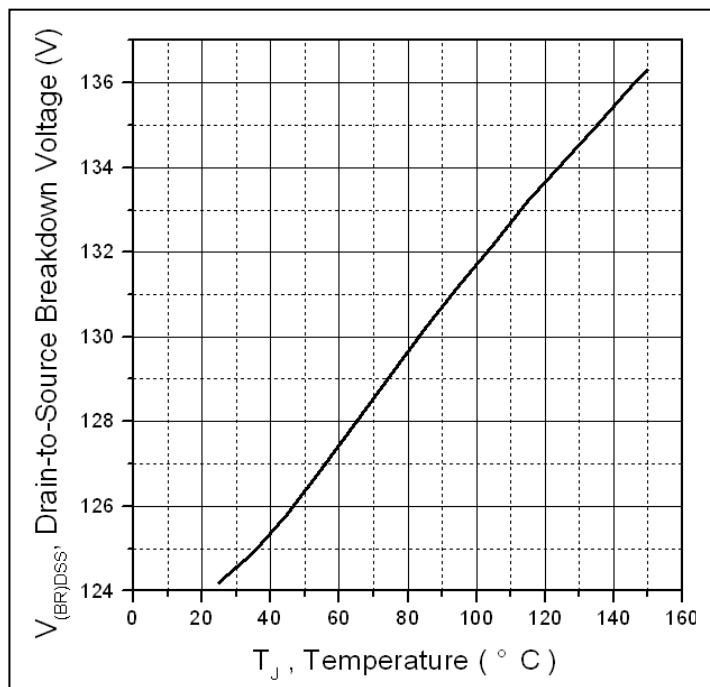
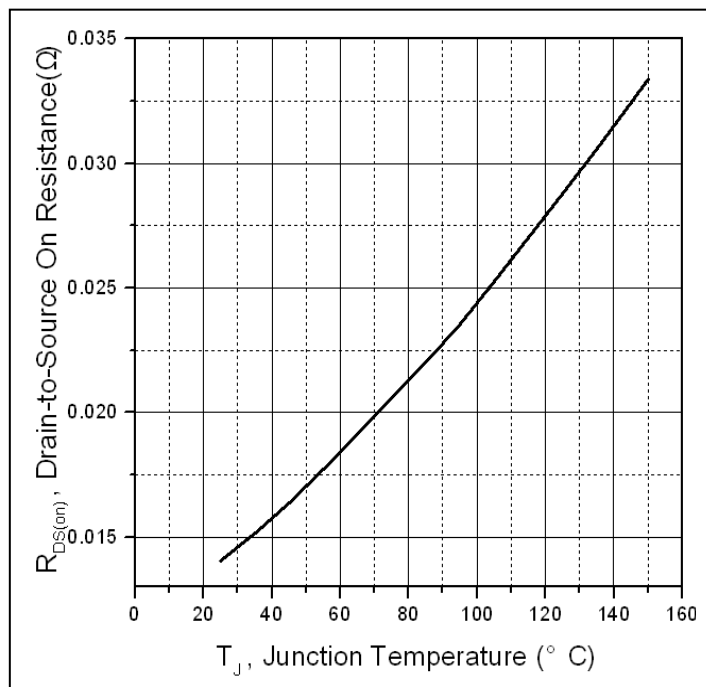
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	13.8	16	mΩ	$V_{GS}=10V, I_D = 30A$ $T_J = 125^\circ\text{C}$
		—	28.8	—		
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$ $T_J = 125^\circ\text{C}$
		—	2.3	—		
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 100V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$
		—	—	50		
$I_{GSS}$	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$ $V_{GS} = -20V$
		-100	—	—		
$Q_g$	Total gate charge	—	92	—	nC	$I_D = 50A,$ $V_{DS}=35V,$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source charge	—	21	—		
$Q_{gd}$	Gate-to-Drain("Miller") charge	—	31	—		
$t_{d(on)}$	Turn-on delay time	—	17	—	ns	$V_{GS}=10V, V_{DS}=30V,$ $R_L=15\Omega,$ $R_{GEN}=2.5\Omega$ $I_D=2.0A$
$t_r$	Rise time	—	14	—		
$t_{d(off)}$	Turn-Off delay time	—	53	—		
$t_f$	Fall time	—	12	—		
$C_{iss}$	Input capacitance	—	4415	—	pF	$V_{GS} = 10V$ $V_{DS} = 25V$ $f = 1\text{MHz}$
$C_{oss}$	Output capacitance	—	60	—		
$C_{rss}$	Reverse transfer capacitance	—	30	—		

## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	75 ①	A	MOSFET symb showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	300	A	
$V_{SD}$	Diode Forward Voltage	—	0.85	1.3	V	$I_S=30A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	—	47	—	ns	$T_J = 25^\circ\text{C}, I_F = 35A, di/dt = 100A/\mu s$
$Q_{rr}$	Reverse Recovery Charge	—	116	—	nC	

**Test circuits and Waveforms**
**EAS test circuits:**

**Gate charge test circuit:**

**Switch Time Test Circuit:**

**Switch Waveforms:**

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max junction temperature.
- ③ The power dissipation PD is based on max junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)} = 175^\circ\text{C}$ .

**Typical electrical and thermal characteristics**

**Figure 1: Typical Output Characteristics**

**Figure 2. Gate to source cut-off voltage**

**Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature**

**Figure 4: Normalized On-Resistance Vs. Case Temperature**

Typical electrical and thermal characteristics

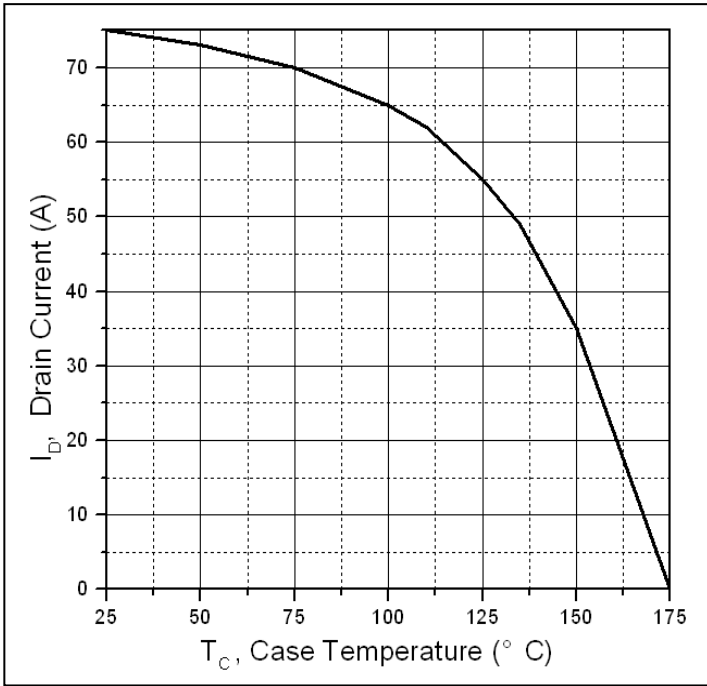


Figure 5. Maximum Drain Current Vs. Case Temperature

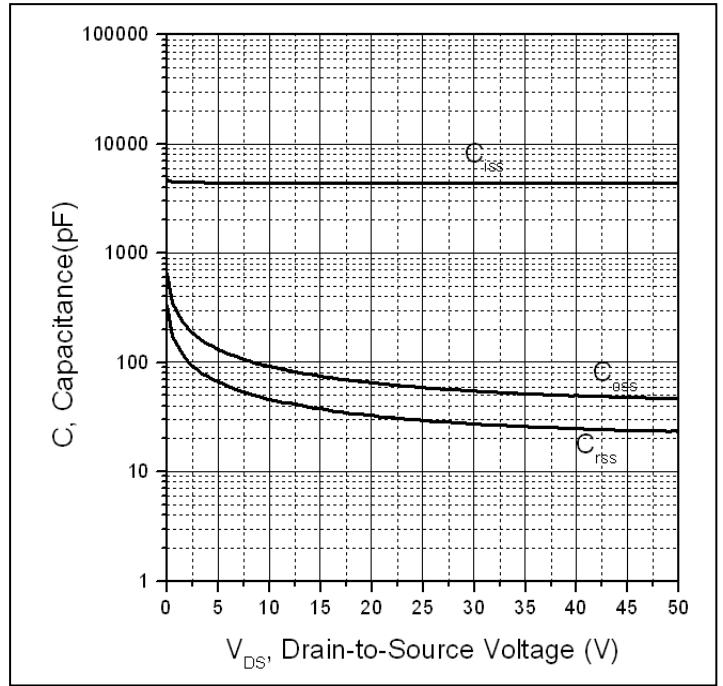


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

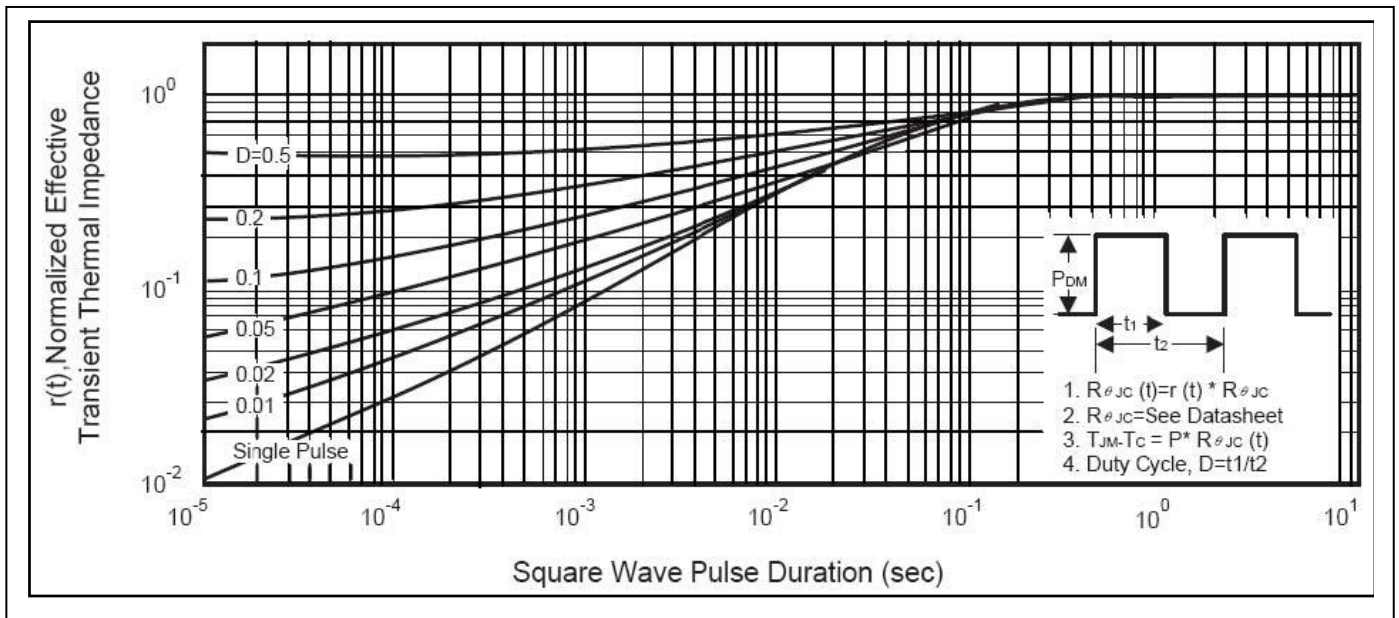
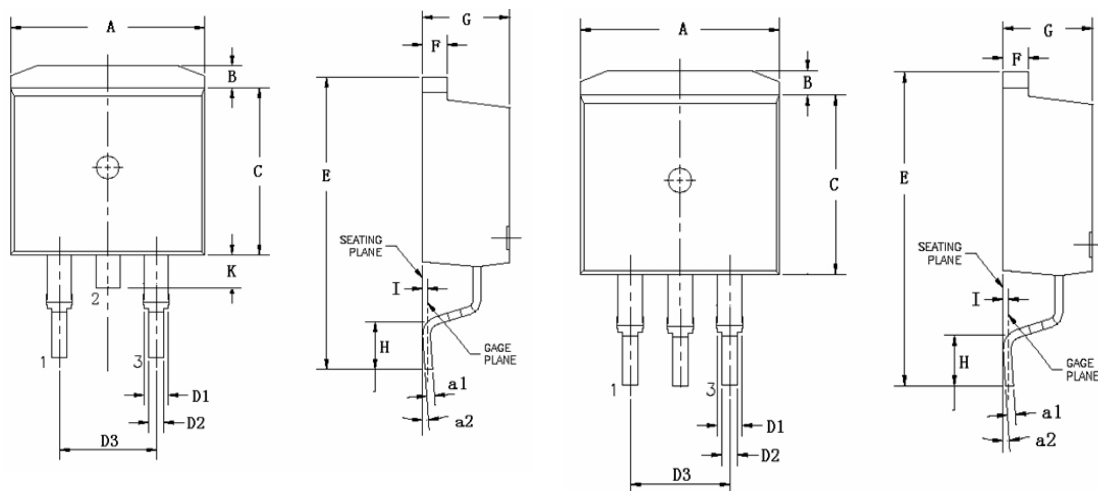


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Mechanical Data:**
**D2PAK PACKAGE OUTLINE DIMENSION**


Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	9.660	10.280	0.380	0.405
B	1.020	1.320	0.040	0.052
C	8.590	9.400	0.338	0.370
D1	1.140	1.400	0.045	0.055
D2	0.700	0.950	0.028	0.037
D3	5.080 (TYP)		0.200 (TYP)	
E	15.090	15.390	0.594	0.606
F	1.150	1.400	0.045	0.055
G	4.300	4.700	0.169	0.185
H	2.290	2.790	0.090	0.110
I	0.250 (TYP)		0.010 (TYP)	
K	1.300	1.600	0.051	0.063
a1	0.450	0.650	0.018	0.026
a2	0°	8°	1°	8°

**Ordering and Marking Information**
**Device Marking: SSF1016A**

**Package (Available)**  
**D2PAK**  
**Operating Temperature Range**  
**C : -55 to 175 °C**

**Devices per Unit**

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
D2PAK	50	20	1000	6	6000

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to $175^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ or $175^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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