5-bit DAC, Synchronous PWM Power Regulator with Dual Linear Controllers

FEATURES

- Provides 3 Regulated Voltages for Microprocessor Core, Clock and GTL Power.
- Simple Voltage-Mode PWM Control.
- Dual N-Channel MOSFET Synchronous Driver.
- Operates from +3.3V, +5V and +12V Inputs.
- Fast Transient Response.
- Full 0% to 100% Duty Ratios.
- ±1.0% Output Voltage for VCORE and ±2.0% Output Voltage Reference for VCLK and VGTL.
- TTL Compatible 5-bit Digital-to-Analog Core Output Voltage Selection. Range from 1.3V to 3.5V.
  - 0.1V Steps from 2.1V to 3.5V.
  - 0.05V Steps from 1.3V to 2.05V.
- Adjustable Current Limit without External Sense Resistor.
- Microprocessor Core Voltage Protection against Shorted MOSFET.
- Power Good Output Voltage Monitor.
- Over-Voltage and Over-Current Fault Monitors.
- 200KHz Free-Running Oscillator Programmable up to 350KHz.

APPLICATIONS

- Full Motherboard Power Regulation for Computers.
- Power Integrations for 3 Output Power System.

DESCRIPTION

The SS6571 combines a synchronous voltage mode controller with two linear controllers as well as the monitoring and protection functions in this chip. The PWM controller regulates the microprocessor core voltage with a synchronous rectified buck converter. One linear controller regulates power for the GTL bus and the other linear controller provides power for the clock driver circuit or memory (1.8V)

An integrated 5 bit D/A converter that adjusts the core PWM output voltage from 2.1V to 3.5V in 0.1V increments and from 1.3V to 2.05V in 0.05V increments. The linear regulator uses an internal driver device to provide 2.5V±2.5%. The linear controller drives with an external N-channel MOSEFET to provide 1.5V±2.5%.

This chip monitors all the output voltages. Power Good signal is issued when the core voltage is within ±10% of the DAC setting and the other levels are above their under-voltage levels. Over-voltage protection for the core output uses the lower N-channel MOSFET to prevent output voltage above 115% of the DAC setting.

The PWM over-current function monitors the output current by using the voltage drop across the upper MOSFET's $R_{DS(on)}$, eliminating the need for a current sensing resistor.

ORDERING INFORMATION

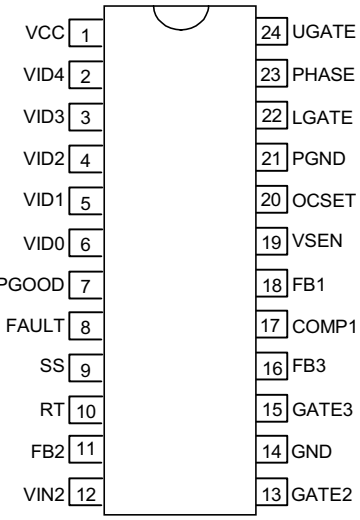
SS6571CXXX

- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGING TYPE
  S: SMALL OUTLINE

Example: SS6571CSTR
→ in SO-24 Package & Taping & Reel Packing Type

PIN CONFIGURATION

SO-24
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... +15V

PGOOD, FAULT and GATE Voltage ..... GND -0.3V to V_{CC} +0.3V

Input, Output , or I/O Voltage ..... GND -0.3V to 7V

Recommended Operating Conditions

- Supply Voltage; VCC ..... +12V±10%
- Ambient temperature Range ..... 0°C~70°C
- Junction Temperature Range ..... 0°C~100°C

Thermal Information

Thermal Resistance, θ_{JA}

- SOIC package ..... 100°C/W
- SOIC package (with 3in^2 of copper) ..... 90°C/W

Maximum Junction Temperature (Plastic Package) ..... 150°C

Maximum Storage Temperature Range ..... -65°C ~ 150°C

Maximum Lead Temperature (Soldering 10 sec) ..... 300°C

TEST CIRCUIT

Refer to APPLICATION CIRCUIT.

ELECTRICAL CHARACTERISTICS (V_{cc}=12V, T_J=25°C, Unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC SUPPLY CURRENT						
Supply Current	UGATE, LGATE, GATE2 and GATE3 open	I_{CC}		1.8	5	mA
POWER ON RESET						
Rising VCC Threshold	V_{OCSET}=4.5V	VCC_{THR}	8.6	9.5	10.4	V
Falling VCC Threshold	V_{OCSET}=4.5V	VCC_{THF}	8.2	9.2	10.2	V
Rising VIN2 Under-Voltage Threshold		$VIN2_{THR}$	2.5	2.6	2.7	V
VIN2 Under-Voltage Hysteresis		$VIN2_{HYS}$		130		mV
Rising V_{OCSET1} Threshold		V_{OCSETH}		1.3		V
OSCILLATOR						
Free Running Frequency	RT=Open	F	170	200	230	KHz
Ramp. Amplitude	RT=open	ΔV_{OSC}		1.3		V_{P-P}
REFERENCE AND DAC						
DAC (VID0~VID4) Input Low Voltage		VID_L			0.8	V
DAC (VID0~VID4) Input High Voltage		VID_H	2			V
DACOUT Voltage Accuracy	VDAC=1.3V~3.5V		-1.0		+1.0	%
FB2 Reference Voltage		V_{REF2}	1.245	1.270	1.295	V
FB3 Reference Voltage		V_{REF3}	1.250	1.275	1.300	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
LINEAR CONTROLLER						
Regulation	0 < $I_{GATE2/3}$ < 10mA		-2.5		+2.5	%
Under-Voltage Level	FB2/3 falling	$FB2/3_{UV}$		70	80	%
PWM CONTROLLER ERROR AMPLIFIER						
DC GAIN				76		dB
Gain Bandwidth Product		GBWP		11		MHz
Slew Rate	COMP1=10pF	SR		6		V/µS
PWM CONTROLLER GATE DRIVER						
Upper Drive Source	VCC=12V, V_{UGATE}=11V	R_{UGH}		5.2	6.5	Ω
Upper Drive Sink	VCC=12V, V_{UGATE} =1V	R_{UGL}		3.3	5	Ω
Lower Drive Source	VCC=12V, V_{LGATE}=11V	R_{LGH}		4.1	6	Ω
Lower Drive Sink	VCC=12V, V_{LGATE}=1V	R_{LGL}		3	5	Ω
PROTECTION						
V_{OUT1} Voltage Over-Voltage Trip	VSEN Rising	OVP	112	115	118	%
OCSET Current Source	V_{OCSET}=4.5V_{DC}	I_{OCSET}	170	200	230	µA
FAULT Sourcing Current	V_{FAULT}=10V	I_{OVP}	10	16		mA
Soft-Start Current		I_{SS}		11		µA
Chip Shutdown Soft Start Threshold					1.0	V
POWER GOOD						
V_{OUT1} Upper Threshold	VSEN Rising		109	110.5	112	%
V_{OUT1} Under-Voltage	VSEN Falling		90.5	92	93.5	%
V_{OUT1} Hysteresis (VSEN/DACOUT)	Upper and Lower Thresh-old			3		%
P_{GOOD} Voltage Low	I_{PGOOD}=-4mA	V_{PGOOD}			0.5	V

TYPICAL PERFORMANCE CHARACTERISTICS

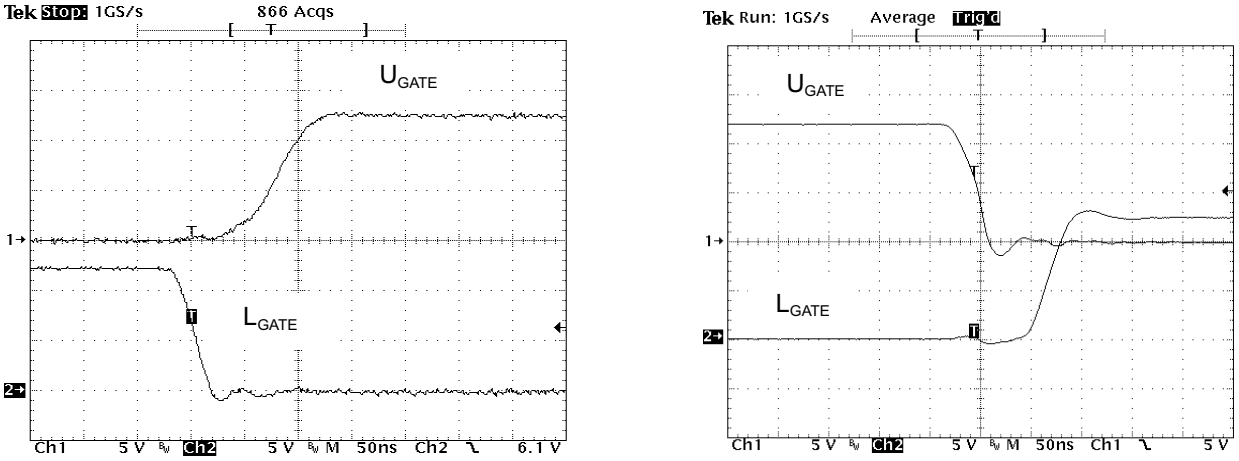


FIG.1 The gate drive waveforms

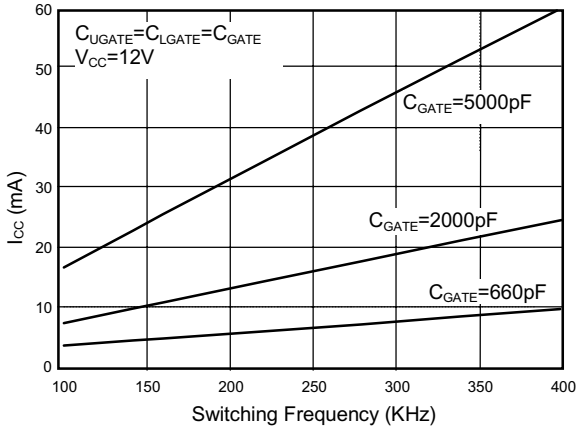


FIG. 2 Bias Supply Current VS. Frequency

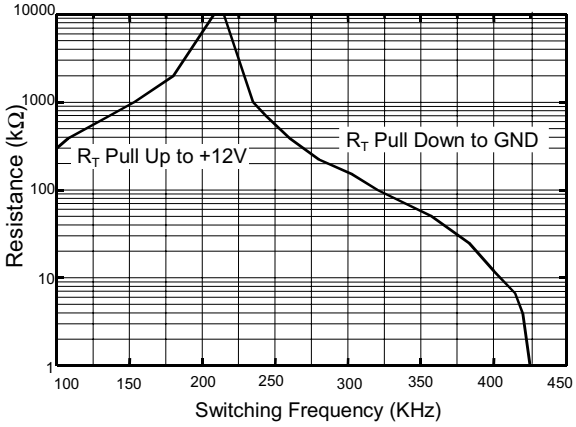


FIG. 3 R_T Resistance VS. Frequency

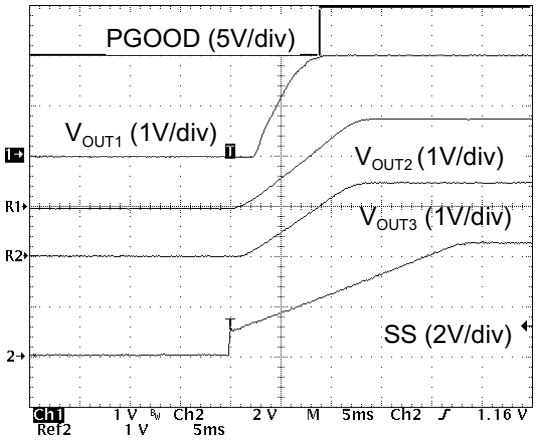


FIG.4-1 Circuit 1---Soft Start Interval with 3 Outputs and PGOOD

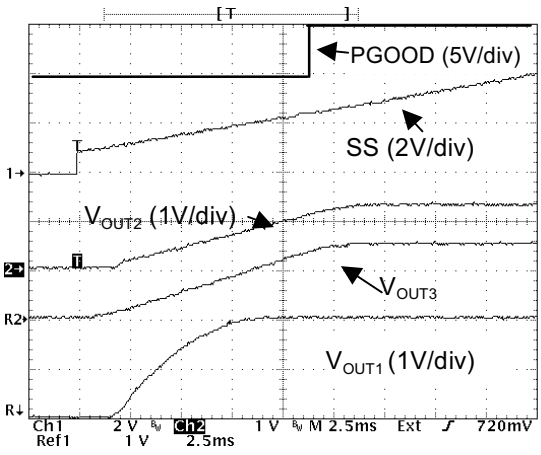


FIG.4-2 Circuit 2---Soft Start Interval with 3 Outputs and PGOOD

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

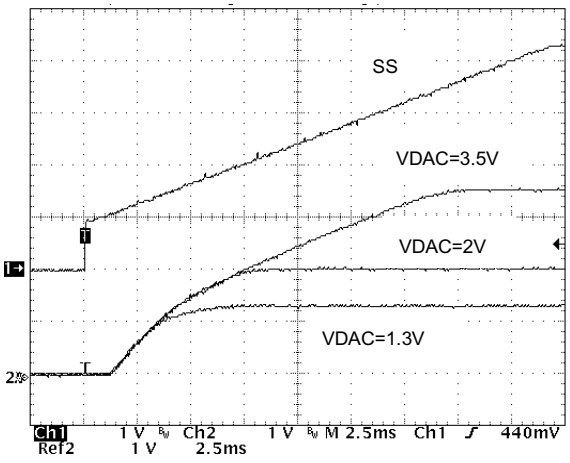


FIG. 5 Soft Start Initiates PWM Output

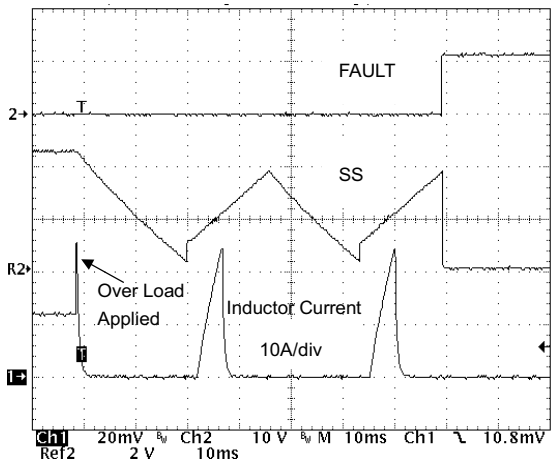


FIG. 6 Over-Current Operation on Inductor

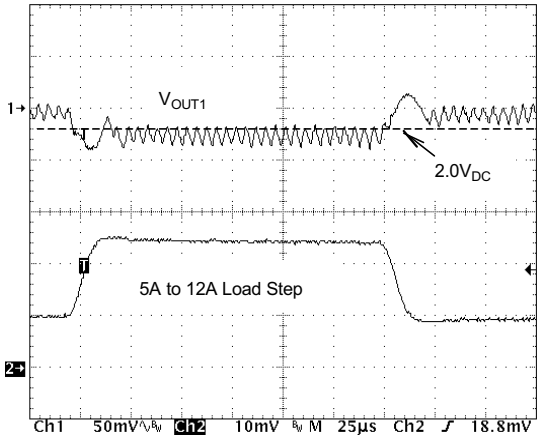


FIG. 7 Transient Response of PWM Output

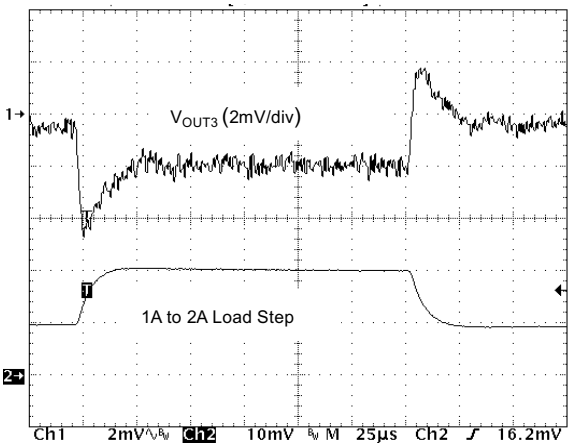


FIG. 8 Transient Response of Linear Controller

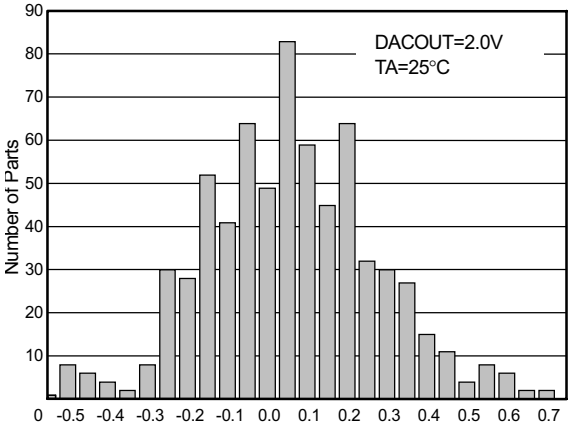


FIG. 9 DACOUT Voltage Accuracy (%)

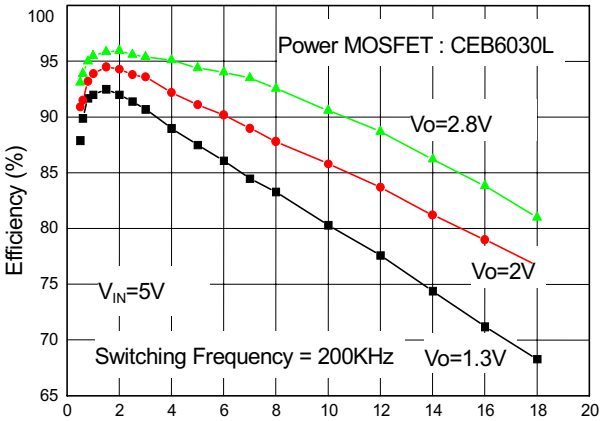


FIG.10 Efficiency vs. Load Current (A)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

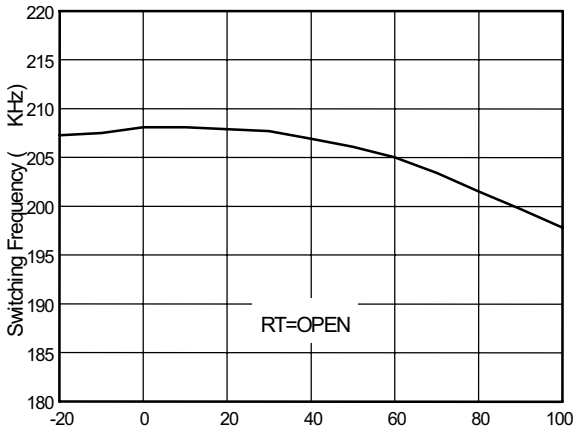


FIG.11 Oscillator Frequency vs. Temperature (°C)

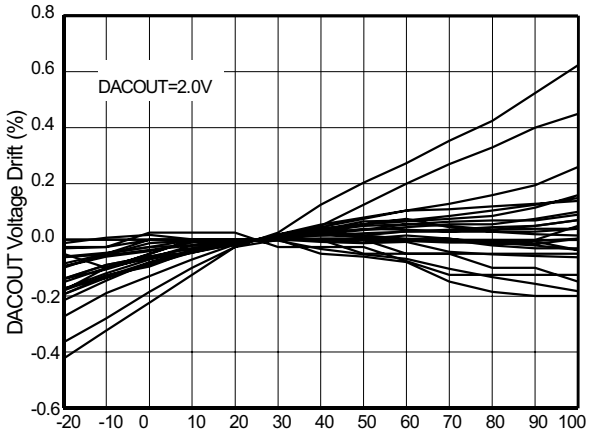


FIG.12 Temperature Drift of 24 Different Parts

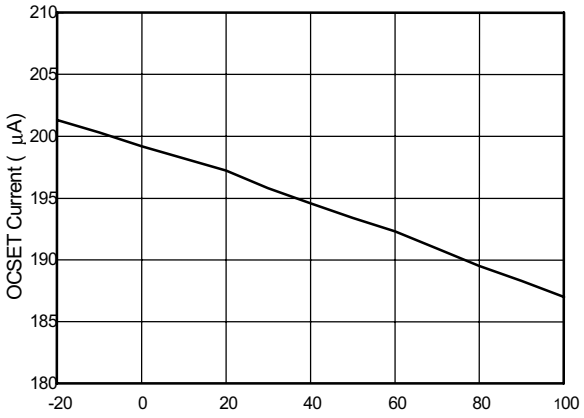


FIG.13 OCSET Current vs.Temperature (°C)

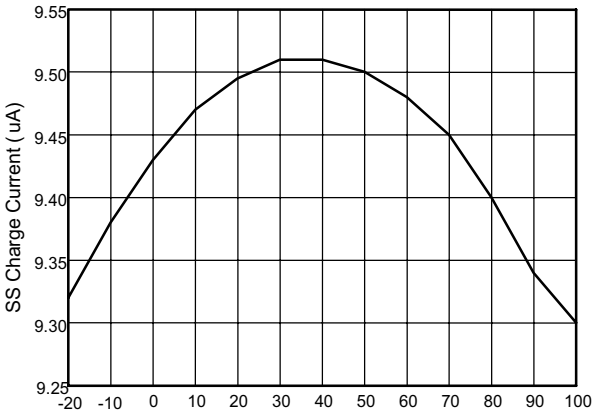


FIG.14 SS Current vs. Temperature (°C)

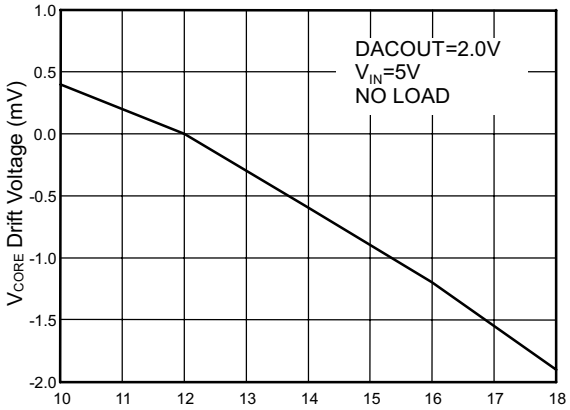


FIG.15 Vcore Drift vs. VCC (V)

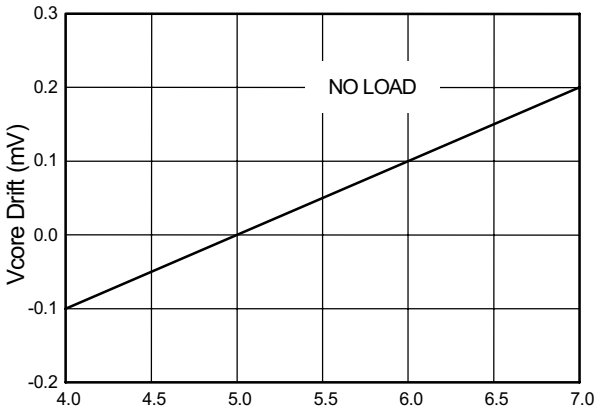
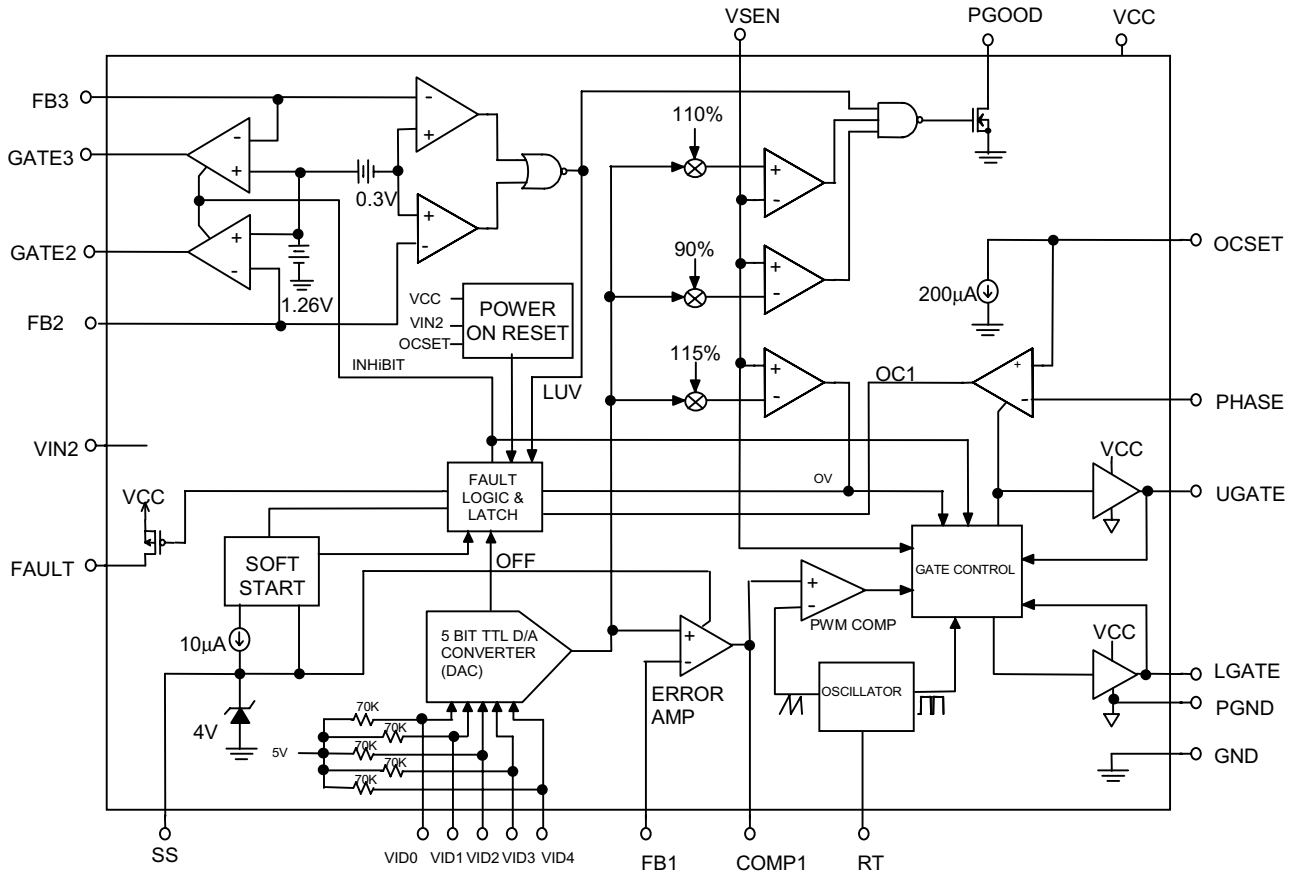


FIG.16 Vcore Drift vs. VIN (V)

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin 1: VCC: The chip power supply pin. It also provides the gate bias charge for all the MOSFETs controlled by the IC. Recommended supply voltage is 12V.

Pin 2: VID4:
Pin 3: VID3:
Pin 4: VID2:
Pin 5: VID1:
Pin 6: VID0:

5bit DAC voltage select pin. TTL inputs used to set the internal voltage reference VDAC. When left open, these pins are internally pulled up to 5V and provide logic ones. The level of VDAC sets the converter output voltage as well as the PGOOD and OVP thresholds.

Table 1 specifies the VDAC voltage for the 32 combinations of DAC inputs.

Pin 7: PGOOD: Power good indicator pin. PGOOD is an open drain output. This pin is pulled low when the converter output is ±10% out of the VDAC reference voltage and the other outputs are below their under-voltage thresholds. The PGOOD output is open for VID codes that inhibit operation. See Table 1.

Pin 8: FAULT: This pin is low during normal operation, but it is pulled to VCC in the event of an over-voltage or over-current condition.

Pin 9: SS: Soft-start pin. Connect a capacitor from this pin to ground. This capacitor, along with an internal 10μA (typically) current source, sets the soft-start interval of the converter.
Pulling this pin low will shut down the IC.

Pin 10: RT: Frequency adjustment pin. Connecting a resistor (RT) from this pin to GND, increasing the frequency. Connecting a resistor (RT) from this pin to VCC, decreasing the frequency by the following figure (Fig.3).

Pin 11: FB2: Connect this pin to a resistor divider to set the linear controller output voltage.

Pin 12: VIN2: This pin is used to monitor the 3.3V supply. If, following a start-up cycle, the voltage drops below 2.6V (typically), the chip shuts down. A new soft-start cycle is initiated upon return of the 3.3V supply above the under-voltage threshold.

Pin 13: GATE2: Linear Controller output drive pin. This pin can drive either a Darlington NPN transistor or a N-channel MOSFET.

Pin 14: GND: Signal GND for IC. All voltage levels are measured with respect to this pin.

Pin 15: GATE3: Linear Controller output drive pin. This pin can drive either a Darlington NPN transistor or a N-channel MOSFET.

Pin 16: FB3: Negative feedback pin for the linear controller error amplifier connect this pin to a resistor divider to set the linear controller output voltage.

Pin 17: COMP1: External compensation pin. This pin is connected to error amplifier output and PWM comparator. An RC network is connected to FB1 in to compensate the voltage control feedback loop of the converter.

Pin 18: FB1: The error amplifier inverting input pin. the FB1 pin and COMP1 pin are used to compensate the voltage-control feedback loop.

Pin 19: VSEN: Converter output voltage sense pin. Connect this pin to the converter output. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over-voltage protection function.

Pin 20: OCSET: Current limit sense pin. Connect a resistor R_{OCSET} from this pin to the drain of the external high-side N-MOSFET. R_{OCSET}, an internal 200μA current source (I_{OCSET}), and the upper N-MOSFET on-resistance ($R_{DS(ON)}$) set the over-current trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

Pin 21: PGND: Driver power GND pin. PGND should be connected to a low impedance ground plane in close to lower N-MOSFET source.

Pin 22: LGATE: Lower N-MOSFET gate drive pin.

Pin 23: PHASE: Over-current detection pin. Connect the PHASE pin to source of the external high-side N-MOSFET. This pin detects the voltage drop across the high-side N-MOSFET $R_{DS(ON)}$ for over-current protection.

Pin 24: UGATE: External high-side N-MOSFET gate drive pin. Connect UGATE to gate of the external high-side N-MOSFET.

APPLICATIONS INFORMATION

The SS6571 is designed for microprocessor computer applications with 3.3V and 5V power, and 12V bias input. This IC has one PWM controller and two linear controllers. The PWM controller is designed to regulate the microprocessor core voltage (V_{OUT1}) by driving 2 MOSFETs (Q1 and Q2) in a synchronous rectified buck converter configuration. The core voltage is regulated to a level programmed by the 5 bit D/A converter. One integrated linear controller supplies the 2.5V clock power (V_{OUT2}). The other linear controller drive an external MOSFET(Q3) to supply the GTL bus power(V_{OUT3})

The Power-On Reset (POR) function continually monitors the input supply voltage +12V at VCC pin, the 5V input voltage at OCSET pin, and the 3.3V input at VIN2 pin. The POR function initiates soft-start operation after all three input supply voltage exceed their POR thresholds.

Soft-Start

The POR function initiates the soft-start sequence. Initially, the voltage on SS pin rapidly increases to approximate 1V. Then an internal 10μA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. As the SS pin voltage slews from 1V to 4V, the PWM error amplifier reference input (Non-inverting terminal) and output (COMP1 pin) is clamped to a level proportional to the SS pin voltage. As the SS pin voltage slew from 1V to 4V, the output clamp generates PHASE pulses of increasing width that charge the output capacitors. Additionally both linear regulator's reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a controlled output voltage smooth rise.

Fig.4 and Fig.5 show the soft-start sequence for the typical application. The internal oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse width on PHASE pin increases. The interval of increasing pulse width continues until output reaches sufficient voltage to transfer control to the input reference clamp.

Each linear output (VOUT2 and VOUT3) initially follows a ramp. When each output reaches sufficient voltage the input reference clamp slows the rate of output voltage rise. The PGOOD signal toggles 'high' when all output voltage levels have exceeded their undervoltage levels.

Fault Protection

All three outputs are monitored and protected against extreme overload. A sustained overload on any output or over-voltage on PWM output disable all converters and drive the FAULT pin to VCC.

A simplified schematic is shown in figure 17. An over-voltage detected on VSEN immediately sets the fault latch. A sequence of three over-current fault signals also sets the fault latch. An undervoltage event on either linear output (FB2 or FB3) is ignored until the soft-start interval. Cycling the

bias input voltage (+12V) off then on reset the counter and the fault latch.

Over-Voltage Protection

During operation, a short on the upper PWM MOSFET (Q1) causes V_{OUT1} to increase. When the output exceed the over-voltage threshold of 115% of DACOUT, the FAULT pin is set to fault latch and turns Q2 on as required in order to regulate V_{OUT1} to 115% of DACOUT. The fault latch raises the FAULT pin close to VCC potential.

A separate over-voltage circuit provides protection during the initial application of power. For voltage on VCC pin below the power-on reset (and above 4V), should VSEN exceed 0.7V, the lower MOSFET (Q2) is driven on as needed to regulate V_{OUT1} to 0.7V.

Over-Current Protection

All outputs are protected against excessive over-current. The PWM controller uses upper MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. Both the linear regulator and controller monitor FB2 and FB3 for under-voltage to protect against excessive current.

When the voltage across Q1 ($I_D \cdot R_{DS(ON)}$) exceeds the level ($200\mu A \cdot R_{OCSET}$), this signal inhibit all outputs. Discharge soft-start capacitor (Css) with 10μA current sink, and increments the counter. Css recharges and initiates a soft-start cycle again until the counter increments to 3. This sets the fault latch to disable all outputs. Fig. 6 illustrates the over-current protection until an over load on OUT1.

Should excessive current cause FB2 or FB3 to fall below the linear under-voltage threshold, the LUV signal sets the over-current latch if Css is fully charged. Cycling the bias input power off then on reset the counter and the fault latch.

The over-current function for PWM controller will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

The OC trip point varies with MOSFET's temperature. To avoid over-current tripping in the normal operating load range, determine the R_{OCSET} resistor from the equation above with:

1. The maximum $R_{DS(ON)}$ at the highest junction.
2. The minimum I_{OCSET} from the specification table.
3. Determine $I_{PEAK} > I_{OUT(MAX)}$ + (inductor ripple current) /2.

PWM OUT1 Voltage Program

The output voltage of the PWM converter is programmed to discrete levels between 1.3V to 3.5V. The VID pins program an internal voltage reference (DACOUT) through a TTL compatible 5 bit digital to analog converter. The VID pins can be left open for a logic 1 input, because they are internally pulled up to 5V by a 70kΩ resistor. Changing the VID inputs during operation is not recommended. All VID pin combinations resulting in an INHIBIT disable the IC and the open collector at the PGOOD pin.

Shutdown

Holding the SS pin low with an open drain or collector signal turns off all three regulators.

The VID codes resulting in an INHIBIT as shown in Table 1 also shut down the IC.

Table 1 V_{OUT1} Voltage Program (0=connected to GND, 1=open or connected to 5V)

For all package version											
PIN NAME					DACOUT	PIN NAME					DACOUT
VID4	VID3	VID2	VID1	VID0	VOLTAGE	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	1	1	1	1.30V	1	1	1	1	1	INHIBIT
0	1	1	1	0	1.35V	1	1	1	1	0	2.1 V
0	1	1	0	1	1.40V	1	1	1	0	1	2.2 V
0	1	1	0	0	1.45V	1	1	1	0	0	2.3 V
0	1	0	1	1	1.50V	1	1	0	1	1	2.4 V
0	1	0	1	0	1.55V	1	1	0	1	0	2.5 V
0	1	0	0	1	1.60V	1	1	0	0	1	2.6 V
0	1	0	0	0	1.65V	1	1	0	0	0	2.7 V
0	0	1	1	1	1.70V	1	0	1	1	1	2.8 V
0	0	1	1	0	1.75V	1	0	1	1	0	2.9 V
0	0	1	0	1	1.80 V	1	0	1	0	1	3.0 V
0	0	1	0	0	1.85 V	1	0	1	0	0	3.1 V
0	0	0	1	1	1.90 V	1	0	0	1	1	3.2 V
0	0	0	1	0	1.95 V	1	0	0	1	0	3.3 V
0	0	0	0	1	2.00 V	1	0	0	0	1	3.4 V
0	0	0	0	0	2.05 V	1	0	0	0	0	3.5 V

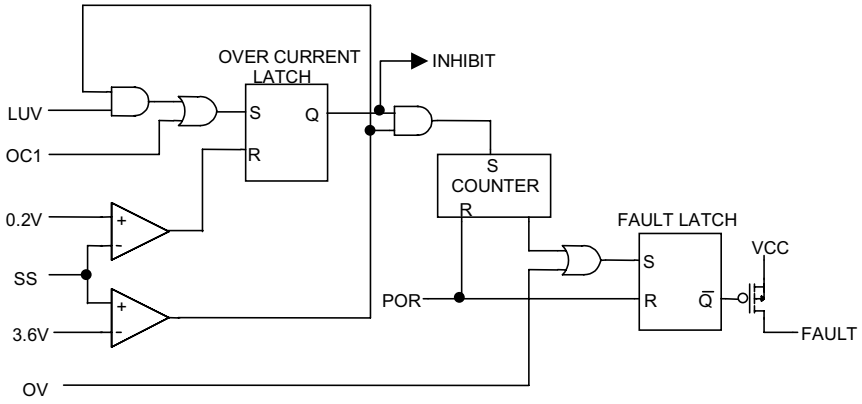


Fig. 17 Simplified Schematic of Fault Logic

Layout Considerations

Any inductance in the switched current path generates a large voltage spike during the switching interval. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component selection and tight layout of critical components, and short, wide metal trace minimize the voltage spike.

1) A ground plane should be used. Locate the input capacitors (C_{IN}) close to the power switches. Minimize the loop formed by C_{IN}, the upper MOSFET (Q1) and the lower MOSFET (Q2) as possible. Connections should be as wide as short as possible to minimize loop inductance.

2) The connection between Q1, Q2 and output inductor should be as wide as short as practical. Since this connection has fast voltage transitions will easily induce EMI.

3) The output capacitor (C_{OUT}) should be located as close the load as possible. Because minimize the transient load magnitude for high slew rate requires low inductance and resistance in circuit board

4) The SS6571 is best placed over a quiet ground plane area. The GND pin should be connected to the groundside of the output capacitors. Under no circumstances should GND be returned to a ground inside the C_{IN}, Q1, Q2 loop. The GND and PGND pins should be shorted right at the IC. This help to minimize internal ground disturbances in the IC and prevents differences in ground potential from disrupting internal circuit operation.

5) The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 1A current. Locate C_{OUT2} close to the SS6571.

6) The Vcc pin should be decoupled directly to GND by a 1uF ceramic capacitor, trace lengths should be as short as possible.

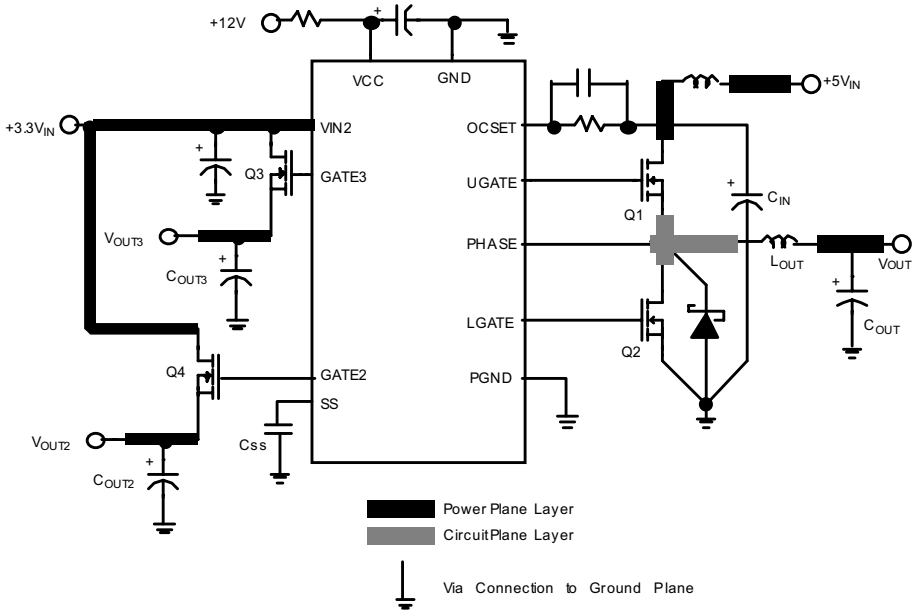


Fig. 18 Printed circuit board power planes and islands

A multi-layer printed circuit board is recommended. Figure 18 shows the connections of the critical components in the converter. The C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer.

PWM Output Capacitors

The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demand.

The ESR (equivalent series resistance) and ESL (equivalent series inductance) parameters rather than actual capacitance determine the buck capacitor values. For a given transient load magnitude, the output voltage transient change due to the output capacitor can be note by the following equation:

$$\Delta V_{OUT} = ESR \times \Delta I_{OUT} + ESL \times \frac{\Delta I_{OUT}}{\Delta T}, \text{ where}$$

ΔI_{OUT} is transient load current step.

After the initial transient, the ESL dependent term drops off. Because the strong relationship between output capacitor ESR and output load transient, the output capacitor is usually chosen for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed for energy storage.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. In most case, multiple electrolytic capacitors of small case size are better than a single large case capacitor.

Output Inductor Selection

Inductor value and type should be chosen based on output slew rate requirement, output ripple requirement and expected peak current. Inductor value is primarily controlled by the required current response time. The SS6571 will provide either 0% or 100% duty cycle in response to a load transient. The response time to a transient is different for the application of load and remove of load.

$$t_{RISE} = \frac{L \times \Delta I_{OUT}}{V_{IN} - V_{OUT}}, \quad t_{FALL} = \frac{L \times \Delta I_{OUT}}{V_{OUT}}.$$

Where ΔI_{OUT} is transient load current step.

In a typical 5V input, 2V output application, a 3μH inductor has a 1A/μS rise time, resulting in a 5μS delay in responding to a 5A load current step. To optimize performance, different combinations of input and output voltage and expected loads may require different inductor value. A smaller value of inductor will improve the transient response at the expense of increase output ripple voltage and inductor core saturation rating.

Peak current in the inductor will be equal to the maximum output load current plus half of inductor ripple current. The ripple current is approximately equal to:

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f \times L \times V_{IN}};$$

f = SS6571 oscillator frequency.

The inductor must be able to withstand peak current without saturation, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss

Input Capacitor Selection

Most of the input supply current is supplied by the input bypass capacitor, the resulting RMS current flow in the input capacitor will heat it up. Use a mix of input bulk capacitors to control the voltage overshoot across the upper MOSFET.

The ceramic capacitance for the high frequency decoupling should be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedance. The buck capacitors to supply the RMS current is approximate equal to:

$$I_{RMS} = (1-D)\times\sqrt{D}\times\sqrt{I^2_{OUT} + \frac{1}{12}\times\left(\frac{V_{IN}\times D}{f\times L}\right)^2}$$

$$\text{, where } D = \frac{V_{OUT}}{V_{IN}}$$

The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage.

PWM MOSFET Selection

In high current PWM application, the MOSFET power dissipation, package type and heatsink are the dominant design factors. The conduction loss is the only component of power dissipation for the lower MOSFET, since it turns on into near zero voltage. The upper MOSFET has conduction loss and switching loss. The gate charge losses are proportional to the switching frequency and are dissipated by the SS-6571. However, the gate charge increases the switching interval, t_{SW} which increase the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

$$P_{UPPER} = I_{OUT}{}^2\times R_{DS(ON)}\times D + \frac{I_{OUT}\times V_{IN}\times t_{SW}\times f}{2}$$

$$P_{LOWER} = I_{OUT}{}^2\times R_{DS(ON)}\times(1-D)$$

The equations above do not model power loss due to the reverse recovery of the lower MOSFET's body diode.

The $R_{DS(ON)}$ is different for the two previous equations even if the type devices is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Logic level MOSFETs should be selected based on on-resistance considerations, $R_{DS(ON)}$ should be chosen base on input and output voltage, allowable power dissipation and maximum required output current. Power dissipation should be calculated based primarily on required efficiency or allowable thermal dissipation.

Rectifier Schottky diode is a clamp that prevent the loss parasitic MOSFET body diode from conducting during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode's rated reverse breakdown voltage must be greater than twice the maximum input voltage.

Linear Controller MOSFET Selection

The power dissipated in a linear regulator is :

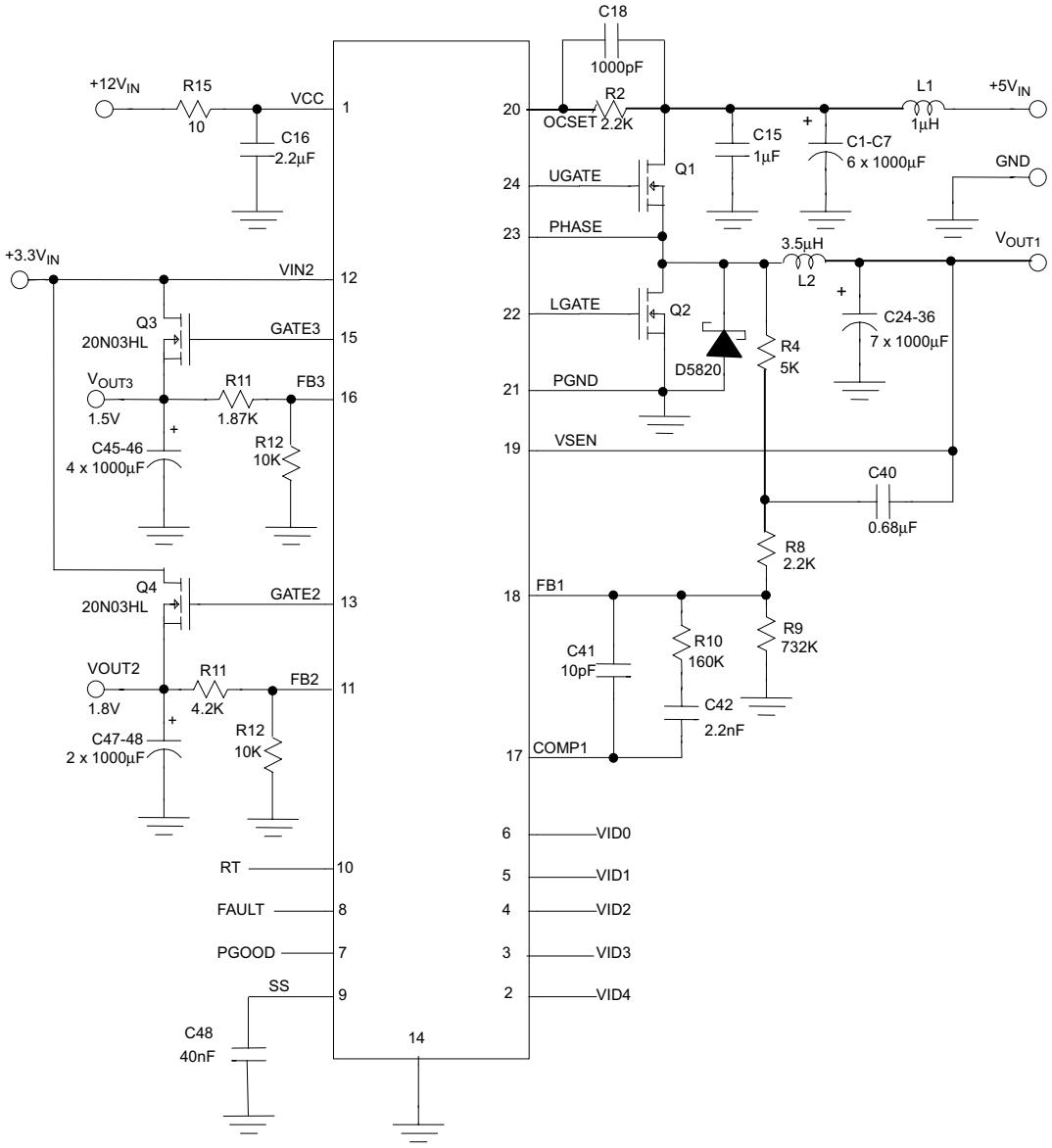
$$P_{LINEAR} = I_{OUT}\times(V_{IN2} - V_{OUT})$$

Select a package and heatsink that maintains junction temperature below the maximum rating while operation at the highest expected ambient temperature.

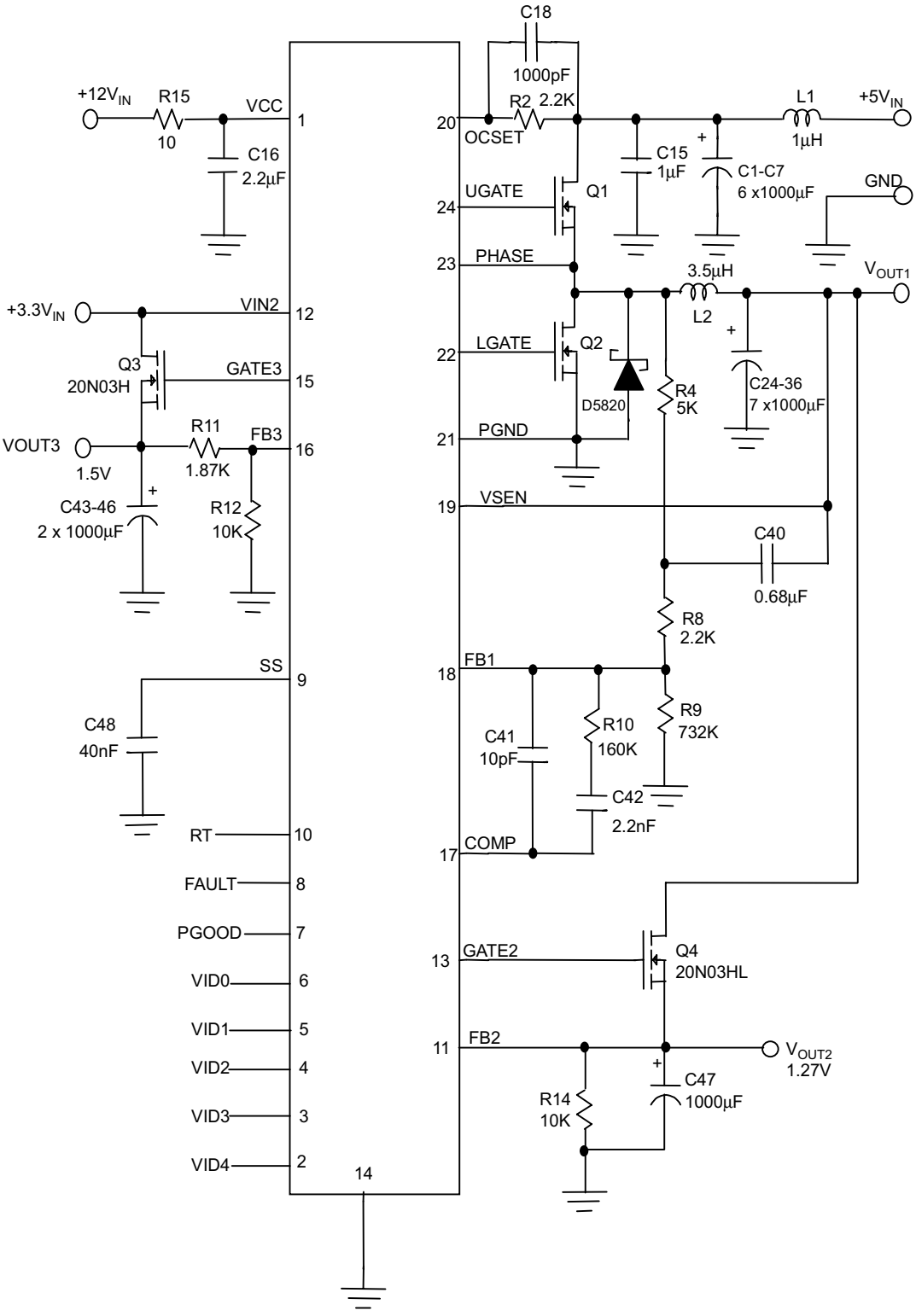
Linear Output Capacitor

The output capacitors for the linear controller provide dynamic load current. The linear controller uses dominant pole compensation integrated in the error amplifier and is insensitive to output capacitor selection. C_{OUT2} and C_{OUT3} should be selected for transient load regulation.

APPLICATION CIRCUIT



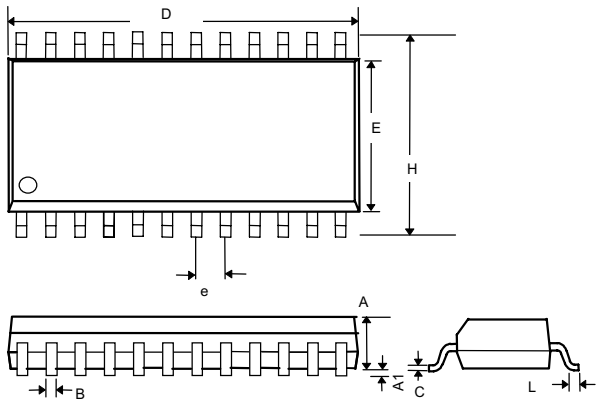
Circuit 1 Motherboard Power application Circuit



Circuit 2 Power Integration for 3-Output Power System

PHYSICAL DIMENSIONS

- **24 LEAD PLASTIC SO (300 mil) (unit: mm)**



SYMBOL	MIN	MAX
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	15.20	15.60
E	7.40	7.60
e	1.27(TYP)	
H	10.00	10.65
L	0.40	1.27