Freescale Semiconductor
Technical Data

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MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Hardware Specifications

This document provides an overview of the *MPC*8309 *PowerQUICC II Pro* processor features. The MPC8309 is a cost-effective, highly integrated communications processor that addresses the requirements of several networking applications including residential gateways, modem/routers, industrial control, and test and measurement applications. The MPC8309 extends current PowerQUICC offerings, adding higher CPU performance, additional functionality, and faster interfaces, while addressing the requirements related to time-to-market, price, power consumption, and board real estate. This document describes the electrical characteristics of MPC8309.

To locate published errata or updates for this document, refer to the MPC8309 product summary page on our website listed on the back cover of this document or contact your local Freescale sales office.

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1 Overview

The MPC8309 incorporates the e300c3 (MPC603e-based) core built on Power Architecture® technology, which includes 16 KB of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8309 also includes a 32-bit PCI controller, two DMA engines and a 16/32-bit DDR2 memory controller with 8-bit ECC.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8309. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8309 is shown in the following figure.

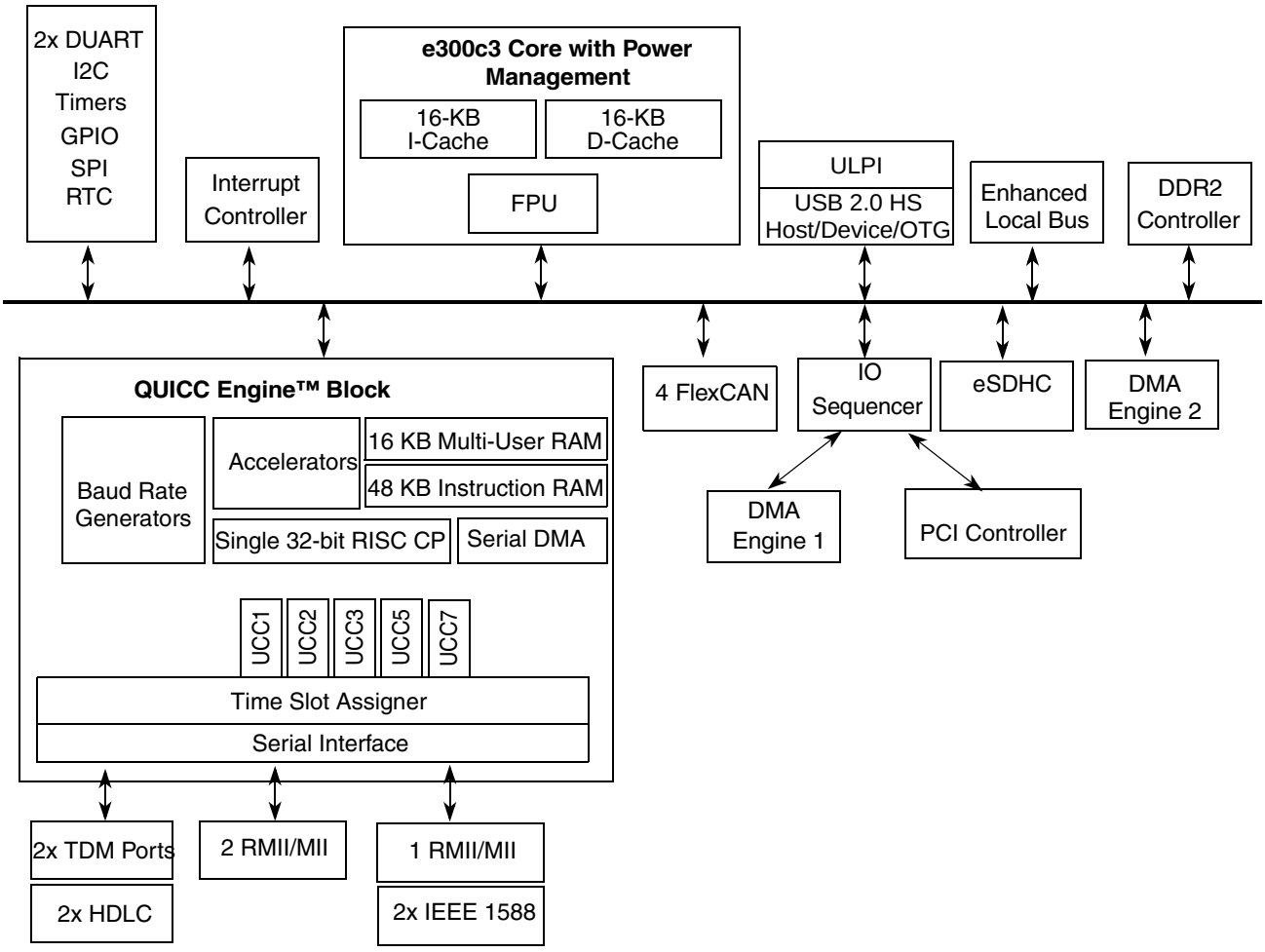


Figure 1. MPC8309 block diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8309 provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 Features

The major features of the device are as follows:

- e300c3 Power Architecture processor core
  - Enhanced version of the MPC603e core
  - High-performance, superscalar processor core with a four-stage pipeline and low interrupt latency times
  - Floating-point, dual integer units, load/store, system register, and branch processing units
  - 16-KB instruction cache and 16-KB data cache with lockable capabilities
  - Dynamic power management
  - Enhanced hardware program debug features
  - Software-compatible with Freescale processor families implementing Power Architecture technology
  - Separate PLL that is clocked by the system bus clock
  - Performance monitor
- QUICC Engine block
  - 32-bit RISC controller for flexible support of the communications peripherals with the following features:
    - One clock per instruction
    - Separate PLL for operating frequency that is independent of system's bus and e300 core frequency for power and performance optimization
    - 32-bit instruction object code
    - Executes code from internal IRAM
    - 32-bit arithmetic logic unit (ALU) data path
    - Modular architecture allowing for easy functional enhancements
    - Slave bus for CPU access of registers and multiuser RAM space
    - 48 KB of instruction RAM
    - 16 KB of multiuser data RAM
    - Serial DMA channel for receive and transmit on all serial channels
  - Five unified communication controllers (UCCs) supporting the following protocols and interfaces:
    - 10/100 Mbps Ethernet/IEEE Std. 802.3® through MII and RMII interfaces.
    - IEEE Std. 1588™ support
    - HDLC/Transparent (bit rate up to QUICC Engine operating frequency / 8)
    - HDLC Bus (bit rate up to 10 Mbps)
    - Asynchronous HDLC (bit rate up to 2 Mbps)
    - Two TDM interfaces supporting up to 128 QUICC multichannel controller channels, each running at 64 kbps

For more information on QUICC Engine sub-modules, see *QUICC Engine Block Reference Manual with Protocol Interworking*.

- DDR SDRAM memory controller
  - Programmable timing supporting DDR2 SDRAM
  - Integrated SDRAM clock generation
  - Supports 8-bit ECC
  - 16/32-bit data interface, up to 333-MHz data rate
  - 14 address lines
  - The following SDRAM configurations are supported:
    - Up to two physical banks (chip selects), 512-MB addressable space for 32 bit data interface
    - 64-Mbit to 2-Gbit devices with x8/x16/x32 data ports (no direct x4 support)
  - One 16-bit device or two 8-bit devices on a 16-bit bus, or two 16-bit devices or four 8-bit devices on a 32-bit bus Support for up to 16 simultaneous open pages for DDR2
  - Two clock pair to support up to 4 DRAM devices
  - Supports auto refresh
  - On-the-fly power management using CKE
- Enhanced local bus controller (eLBC)
  - Multiplexed 26-bit address and 8-/16-bit data operating at up to 66 MHz
  - Eight chip selects supporting eight external slaves
    - Four chip selects dedicated
    - Four chip selects offered as multiplexed option
  - Supports boot from parallel NOR Flash and parallel NAND Flash
  - Supports programmable clock ratio dividers
  - Up to eight-beat burst transfers
  - 16- and 8-bit ports, separate $\overline{\text{LWE}}$ for each 8 bit
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Variable memory block sizes for FCM, GPCM, and UPM mode
  - Default boot ROM chip select with configurable bus width (8 or 16)
  - Provides two Write Enable signals to allow single byte write access to external 16-bit eLBC slave devices
- Integrated programmable interrupt controller (IPIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for external and internal discrete interrupt sources
  - Programmable highest priority request
  - Six groups of interrupts with programmable priority

  - External and internal interrupts directed to host processor
  - Unique vector number for each interrupt source
- PCI interface
  - Designed to comply with *PCI Local Bus Specification, Revision 2.3*
  - 32-bit PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - Not 5-V compatible
  - Support for host and agent modes
  - Support for PCI-to-memory and memory-to-PCI streaming
  - Memory pre-fetching of PCI read accesses and support for delayed read transactions
  - Support for posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration, supporting three masters on PCI
  - Arbiter support for two-level priority request/grant signal pairs
  - Support for accesses to all PCI address spaces
  - Support for parity
  - Selectable hardware-enforced coherency
  - Address translation units for address mapping between host and peripheral
  - Mapping from an external 32-/64-bit address space to the internal 32-bit local space
  - Support for dual address cycle (DAC) (as a target only)
  - Internal configuration registers accessible from PCI
  - Selectable snooping for inbound transactions
  - Four outbound Translation Address Windows
    - Support for mapping 32-bit internal local memory space to an external 32-bit PCI address space and translating that address within the PCI space
  - Four inbound Translation Address Windows corresponding to defined PCI BARs
    - The first BAR is 32-bits and dedicated to on-chip register access
    - The second BAR is 32-bits for general use
    - The remaining two BARs may be 32- or 64-bits and are also for general use
- Enhanced secure digital host controller (eSDHC)
  - Compatible with the *SD Host Controller Standard Specification Version 2.0* with test event register support
  - Compatible with the *MMC System Specification Version 4.2*
  - Compatible with the *SD Memory Card Specification Version 2.0* and supports the high capacity SD memory card
  - Compatible with the *SD Input/Output (SDIO) Card Specification, Version 2.0*
  - Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, and RS-MMC cards
  - Card bus clock frequency up to 33.33 MHz.

- — Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
  - – Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
- — Supports block sizes of 1 ~ 4096 bytes

- Universal serial bus (USB) dual-role controller
  - — Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - — Supports operation as a stand-alone USB host controller
  - — Supports operation as a stand-alone USB device
  - — Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - — Full implementation of the CAN protocol specification version 2.0B
  - — Up to 64 flexible message buffers of zero to eight bytes data length
  - — Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - — Selectable backwards compatibility with previous FlexCAN module version
  - — Programmable loop-back mode supporting self-test operation
  - — Global network time, synchronized by a specific message
  - — Independent of the transmission medium (an external transceiver is required)
  - — Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - — Two-wire interface
  - — Multiple-master support
  - — Master or slave I^2C mode support
  - — On-chip digital filtering rejects spikes on the bus
  - — I^2C1 can be used as the boot sequencer
- DMA Engine1
  - — Support for the DMA engine with the following features:
    - – Sixteen DMA channels
    - – All data movement via dual-address transfers: read from source, write to destination
    - – Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - – Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - – Explicit software initiation
      - – Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - – Support for fixed-priority and round-robin channel arbitration
    - – Channel completion reported via optional interrupt requests
  - — Support for scatter/gather DMA processing
- IO Sequencer

- Direct memory access (DMA) controller (DMA Engine 2)
  - Four independent fully programmable DMA channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Misaligned transfer capability for source/destination address
  - Data chaining and direct mode
  - Interrupt on completed segment, error, and chain
- DUART
  - Supports 2 DUART
  - Each has two 2-wire interfaces (RxD, TxD)
    - The same can be configured as one 4-wire interface (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI)
  - Master or slave support
- Power management controller (PMC)
  - Supports core doze/nap/sleep/ power management
  - Exits low power state and returns to full-on mode when
    - The core internal time base unit invokes a request to exit low power state
    - The power management controller detects that the system is not idle and there are outstanding transactions on the internal bus or an external interrupt.
- Parallel I/O
  - General-purpose I/O (GPIO)
    - 56 parallel I/O pins multiplexed on various chip interfaces
    - Interrupt capability
- System timers
  - Periodic interrupt timer
  - Software watchdog timer
  - Eight general-purpose timers
- Real time clock (RTC) module
  - Maintains a one-second count, unique over a period of thousands of years
  - Two possible clock sources:
    - External RTC clock (RTC_PIT_CLK)
    - CSB bus clock
- IEEE Std. 1149.1™ compliant JTAG boundary scan

2 Electrical characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8309. The MPC8309 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC electrical characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute maximum ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute maximum ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1} AV_{DD2} AV_{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.98	V	—
PCI, Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN, USB and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	2
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.2 Power supply voltage specification

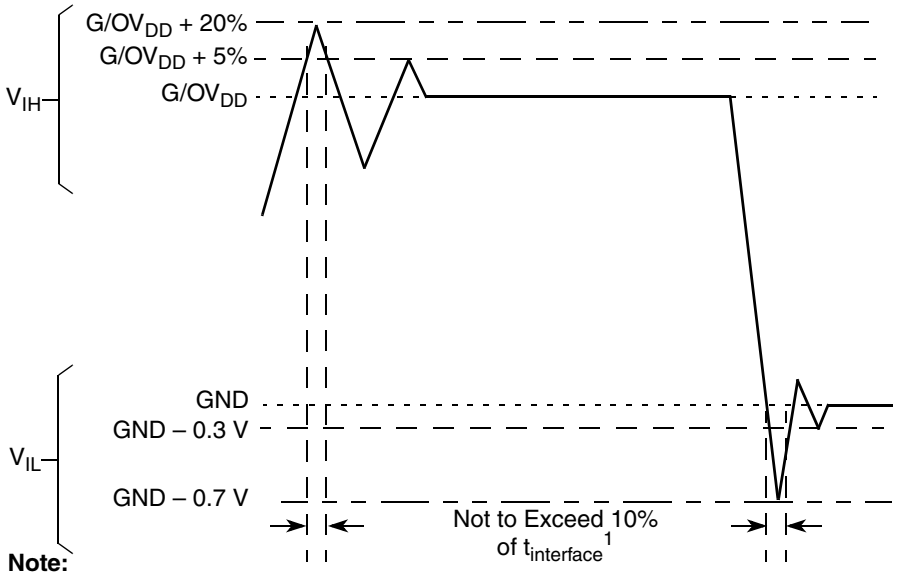
The following table provides the recommended operating conditions for the MPC8309. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended operating conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV_{DD1} AV_{DD2} AV_{DD3}	1.0 V ± 50 mV	V	1
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V ± 100 mV	V	1
PCI, Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN,USB and JTAG I/O voltage	OV_{DD}	3.3 V ± 300 mV	V	1, 3
Junction temperature	T_A/T_J	0 to 105	°C	2

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A(Ambient Temperature); maximum temperature is specified with T_J(Junction Temperature).
3. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8309



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot voltage for GV_{DD}/OV_{DD}

2.1.3 Output driver characteristics

The following table provides information on the characteristics of the output driver strengths.

Table 3. Output drive capability

Driver Type	Output Impedance (Ω)	Supply Voltage (V)
Local bus interface utilities signals	42	OV_{DD} = 3.3
PCI Signal	25	
DDR2 signal	18	GV_{DD} = 1.8
DUART, system control, I2C, SPI, JTAG	42	OV_{DD} = 3.3
GPIO signals	42	OV_{DD} = 3.3

2.1.4 Input capacitance specification

The following table describes the input capacitance for the SYS_CLK_IN pin in the MPC8309.

Table 4. Input capacitance specification

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input capacitance for all pins except SYS_CLK_IN and QE_CLK_IN	C_I	6	8	pF	—
Input capacitance for SYS_CLK_IN and QE_CLK_IN	C_{ICLK_IN}	10	—	pF	1

Note:
1. The external clock generator should be able to drive 10 pF.

2.2 Power sequencing

The device does not require the core supply voltage (V_{DD}) and I/O supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

NOTE

There is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

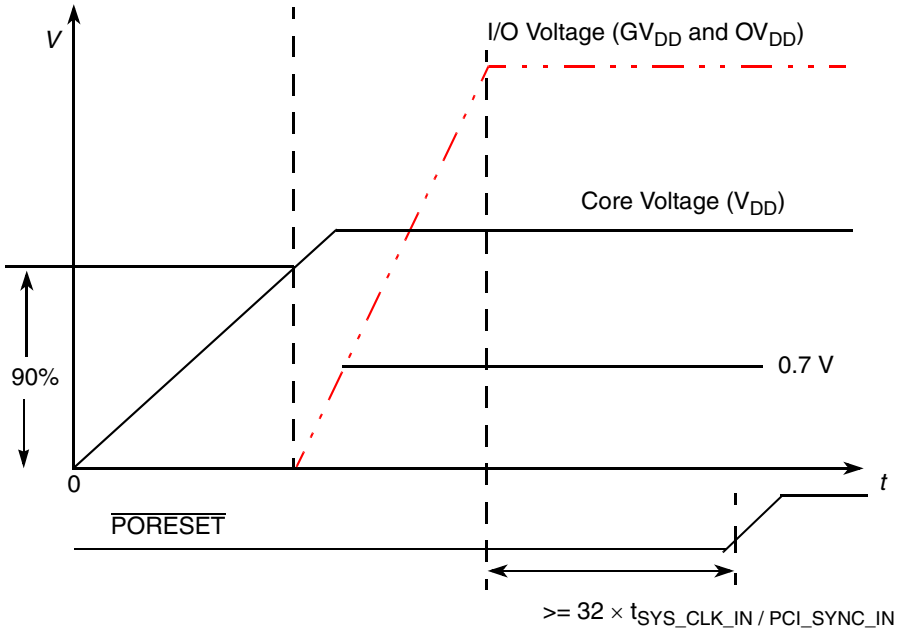


Figure 3. MPC8309 Power-Up sequencing example

3 Power characteristics

The typical power dissipation for this family of MPC8309 devices is shown in the following table.

Table 5. MPC8309 Power dissipation

Core Frequency (MHz)	QUICC Engine Frequency (MHz)	CSB Frequency (MHz)	Typical	Maximum	Unit	Note
266	233	133	0.341	0.920	W	1, 2, 3
333	233	133	0.361	0.938	W	1, 2, 3
400	233	133	0.381	0.969	W	1,2,3
417	233	167	0.429	1.003	W	1,2,3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}), but it does include V_{DD} and AV_{DD} power. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, WC process, a junction T_J = 105°C, and a smoke test code.

The following table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O power dissipation

Interface	Parameter	GV_{DD} (1.8 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 1.8 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 16 bits	0.149	—	W	—
Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 26 bits	—	0.415	W	1
QUICC Engine block and other I/Os	TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, PCI, SPI, Timer output, FlexCAN, eSDHC				

Note:
1. Typical I/O power is based on a nominal voltage of V_{DD} = 3.3V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

4 Clock input timing

This section provides the clock input DC and AC electrical characteristics for the MPC8309.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of OV_{DD}; fall time refers to transitions from 90% to 10% of OV_{DD}.

4.1 DC electrical characteristics

The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 7. SYS_CLK_IN DC electrical characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0.5 V ≤ V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±50	μA

4.2 AC electrical characteristics

The primary clock source for the MPC8309 can be one of two inputs, SYS_CLK_IN or PCI_SYNC_IN, depending on whether the device is configured in PCI host or agent mode. The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) AC timing specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 8. SYS_CLK_IN AC timing specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1
SYS_CLK_IN cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	1.1	—	2.8	ns	2
PCI_SYNC_IN rise and fall time	t_{PCH}, t_{PCL}	1.1	—	2.8	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

5 RESET initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8309. The following table provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET initialization timing specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of PORESET with stable clock applied to SYS_CLK_IN or PCI_SYNC_IN (in agent mode)	32	—	$t_{SYS\_CLK\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1

Table 9. RESET initialization timing specifications (continued)

Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$	4	—	$t_{SYS\_CLK\_IN}$	1, 2
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
2. POR configuration signals consist of CFG_RESET_SOURCE[0:3].

The following table provides the PLL lock times.

Table 10. PLL lock times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

5.1 Reset signals DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 reset signals mentioned in Table 9.

Table 11. Reset signals DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8309. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC electrical characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8309 when GV_{DD}(typ) = 1.8 V.

The following table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC electrical characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MVREF is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 13. DDR2 SDRAM capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.100 V, f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR2 SDRAM AC electrical characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM input AC timing specifications

This table provides the input AC timing specifications for the DDR2 SDRAM (GV_{DD}(typ) = 1.8 V).

Table 14. DDR2 SDRAM input AC timing specifications for 1.8-V interface

At recommended operating conditions with GV_{DD} of 1.8 V± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.25	V	—
AC input high voltage	V_{IH}	MVREF + 0.25	—	V	—

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 15. DDR2 SDRAM input AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

The following figure shows the input timing diagram for the DDR controller.

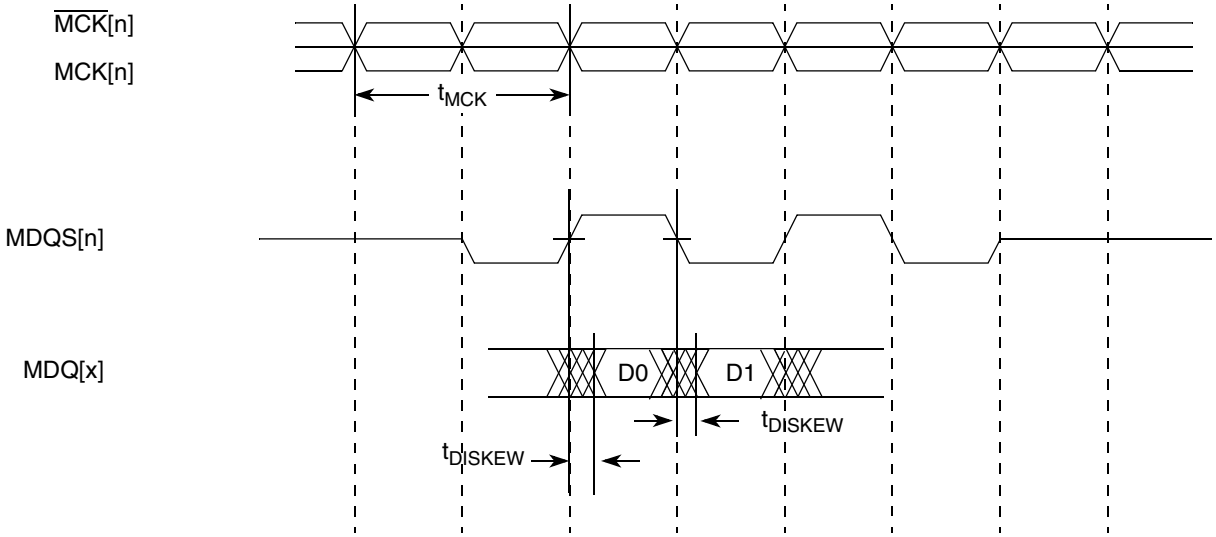


Figure 4. DDR input timing diagram

6.2.2 DDR2 SDRAM output AC timing specifications

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

Table 16. DDR2 SDRAM output AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK cycle time, (MCK/$\overline{MCK}$ crossing)	t_{MCK}	5.988	8	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			

Table 16. DDR2 SDRAM output AC timing specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
$\overline{MCS}$ output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.4 2.5	 — 	ns	3
$\overline{MCS}$ output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.4 2.5	 — 	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.8 0.9	 — 	ns	5
MDQ/MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100	 — 	ps	5
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjusts in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. t_{DDKHMP} follows the symbol conventions described in note 1.

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

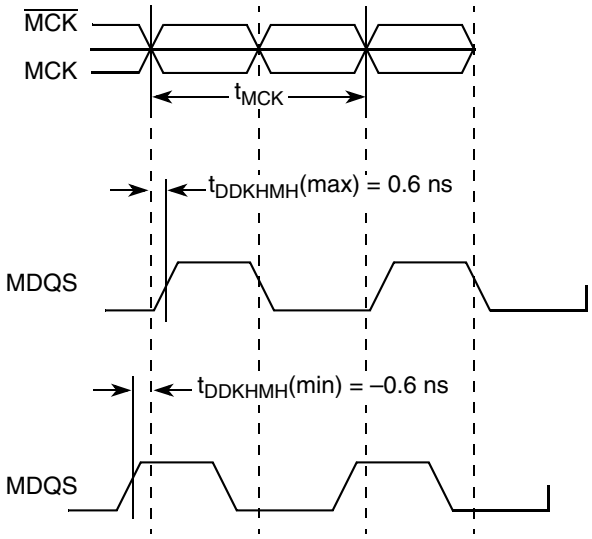


Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

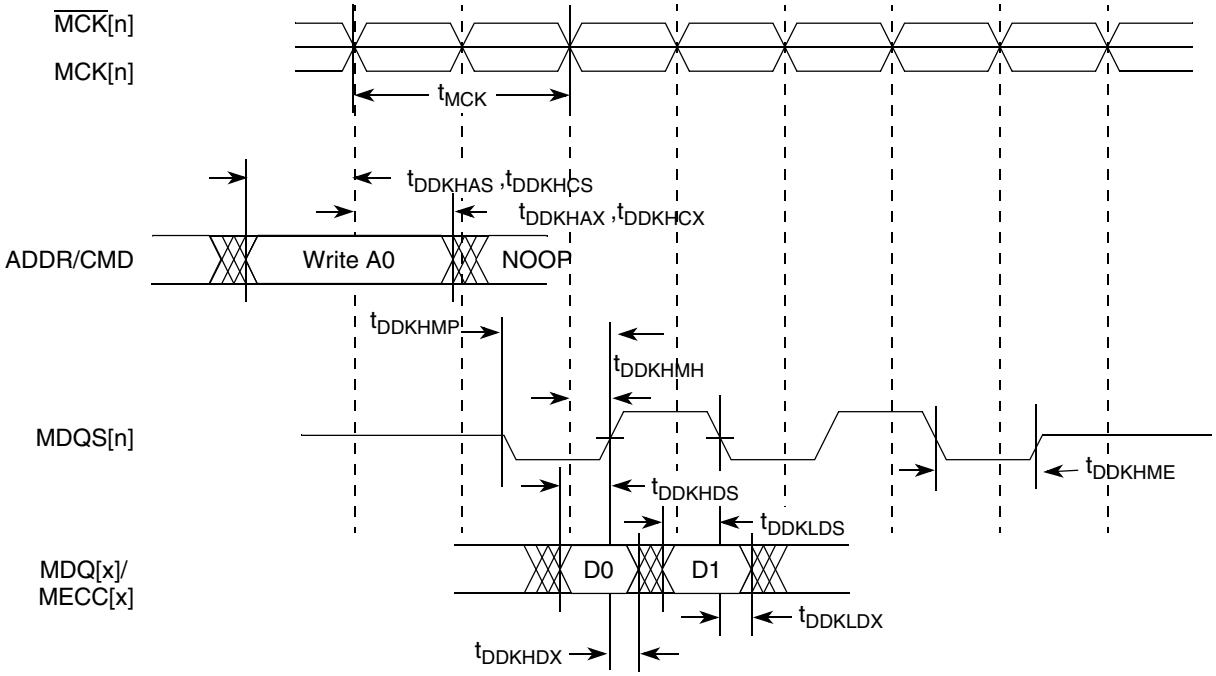


Figure 6. DDR2 SDRAM output timing diagram

7 Enhanced local bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface of the MPC8309.

7.1 Enhanced local bus DC electrical characteristics

The following table provides the DC electrical characteristics for the enhanced local bus interface.

Table 17. Enhanced local bus DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	μA

7.2 Enhanced local bus AC electrical specifications

The following table describes the general timing parameters of the enhanced local bus interface of MPC8309.

Table 18. Enhanced local bus general timing parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t_{LBOTOT}	3	—	ns	—
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3	ns	—
LALE output fall to LCLK negative edge	$t_{LALETOT}$	–5.0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

The following figure provides the AC test load for the local bus.

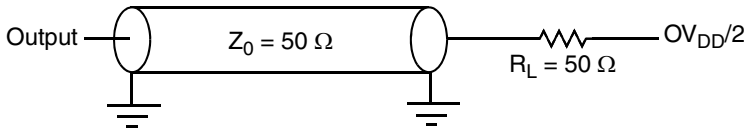


Figure 7. Enhanced local bus ac test load

The following figures show the local bus signals. These figures have been given indicate timing parameters only and do not reflect actual functional operation of interface.

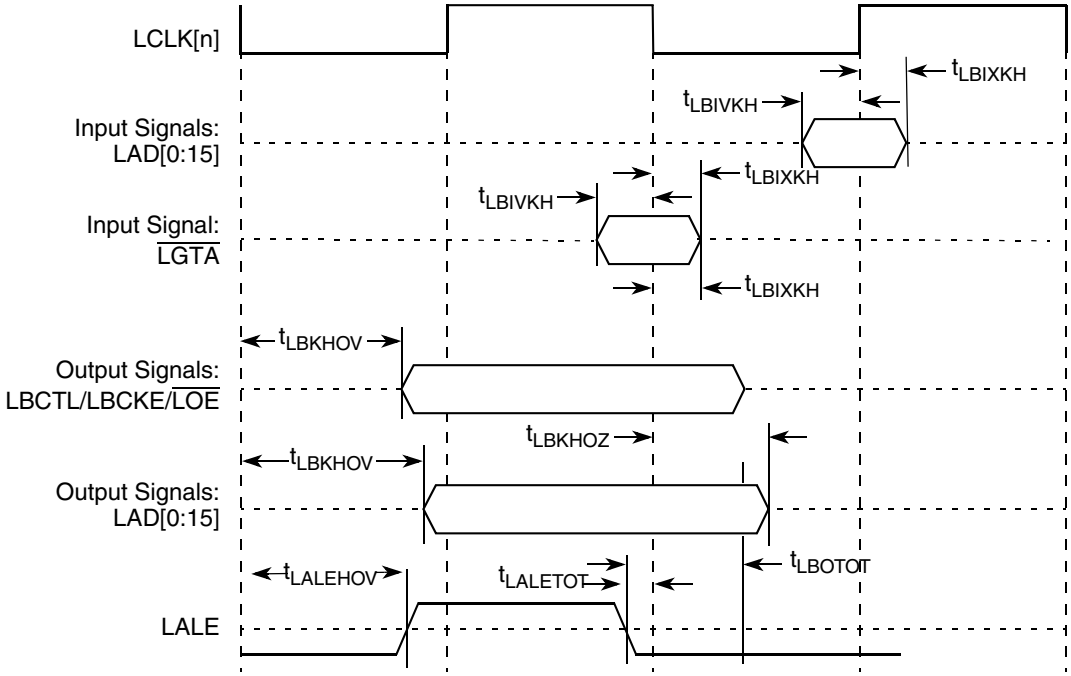


Figure 8. Enhanced local bus signals

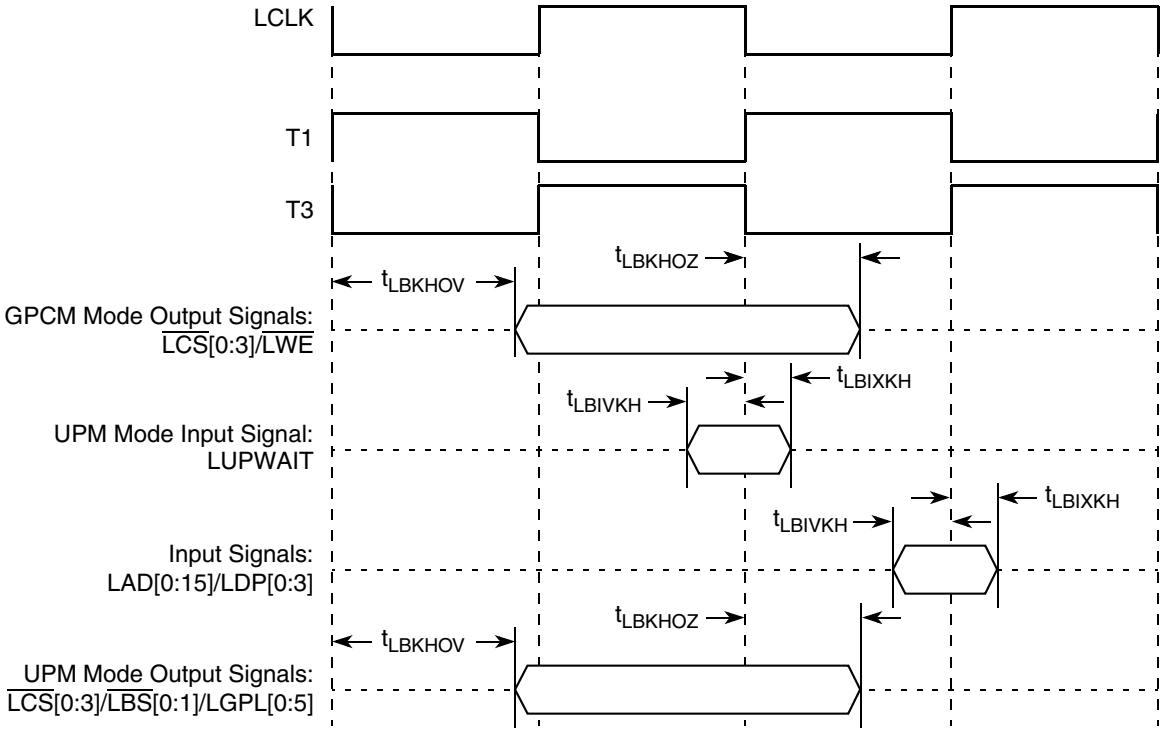


Figure 9. Enhanced local bus signals, GPCM/UPM signals for LCRR[CLKDIV] = 2

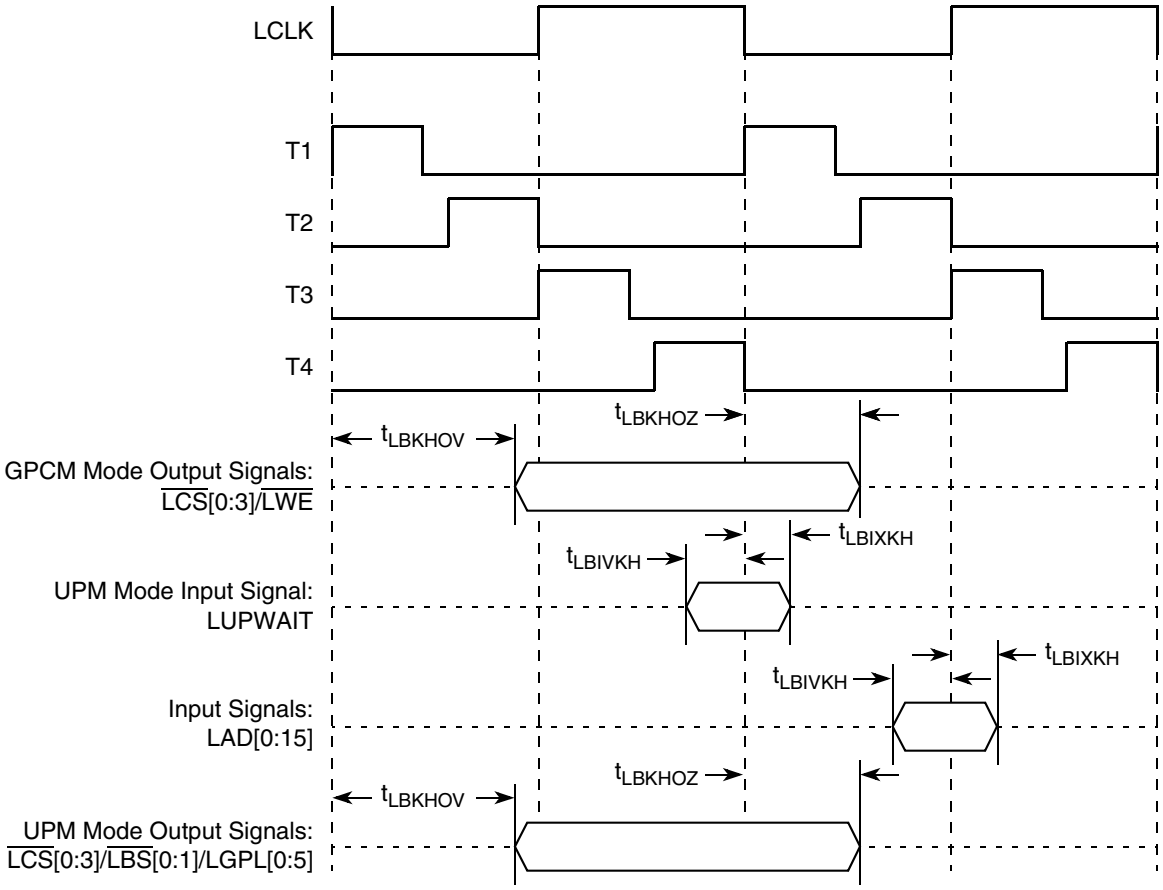


Figure 10. Enhanced local bus signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

8 Ethernet and MII management

This section provides the AC and DC electrical characteristics for Ethernet interfaces.

8.1 Ethernet controller (10/100 Mbps)—MII/RMII electrical characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC (management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet management interface electrical characteristics."

8.1.1 DC electrical characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in the following table.

Table 19. MII and RMII DC electrical characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC timing specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC timing specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII transmit AC timing specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII transmit AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

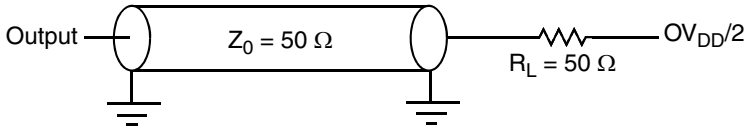


Figure 11. AC test load

The following figure shows the MII transmit AC timing diagram.

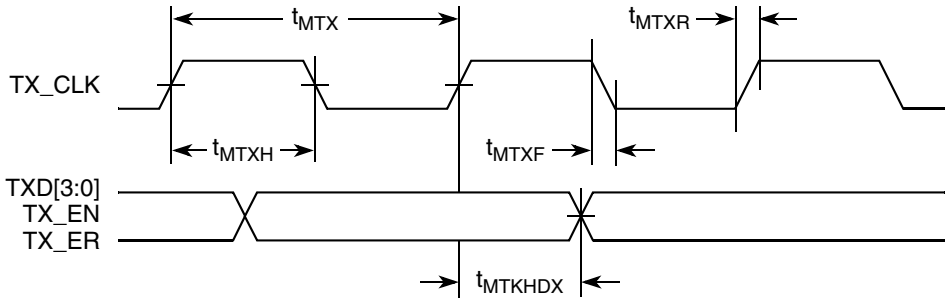


Figure 12. MII transmit AC timing diagram

8.2.1.2 MII receive AC timing specifications

The following table provides the MII receive AC timing specifications.

Table 21. MII receive AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII receive AC timing diagram.

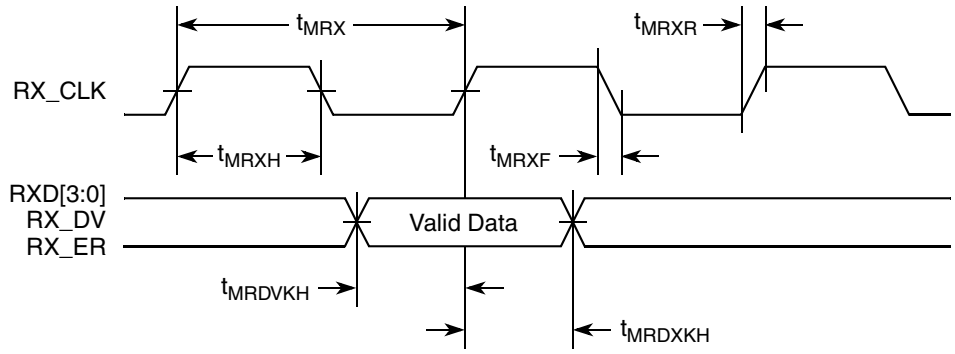


Figure 13. MII receive AC timing diagram

8.2.2 RMII AC timing specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII transmit AC timing specifications

The following table provides the RMII transmit AC timing specifications.

Table 22. RMII transmit AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	13	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

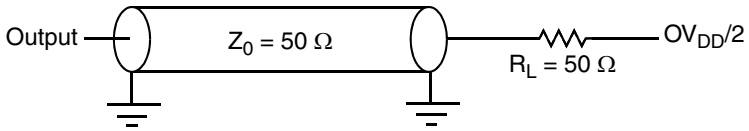


Figure 14. AC test load

The following figure shows the RMII transmit AC timing diagram.

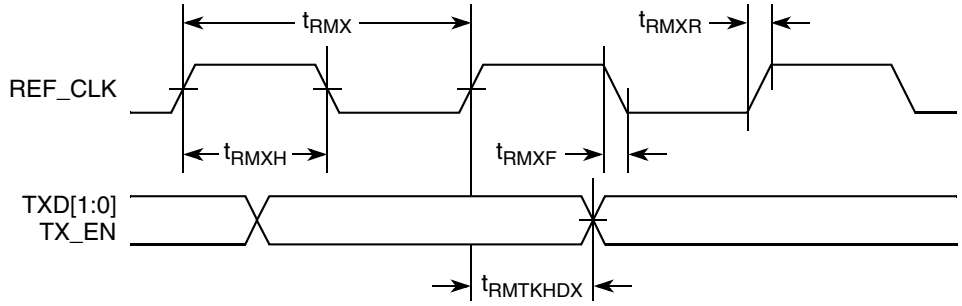


Figure 15. RMII transmit AC timing diagram

8.2.2.2 RMII receive AC timing specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII receive AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the RMII receive AC timing diagram.

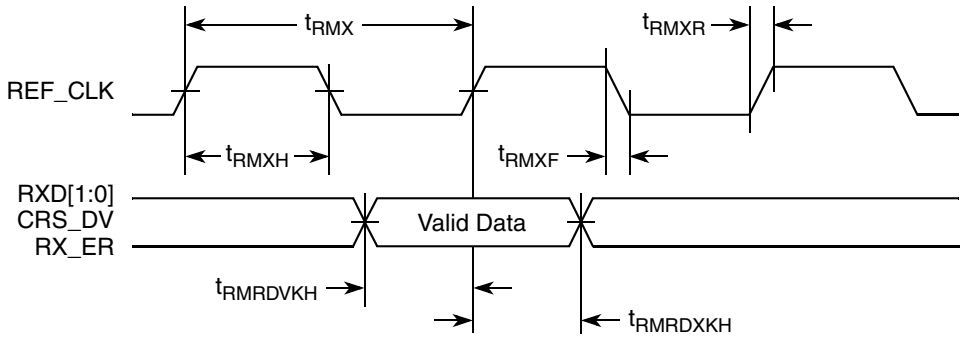


Figure 16. RMII receive AC timing diagram

8.3 Ethernet management interface electrical characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet controller (10/100 Mbps)—MII/RMII electrical characteristics."

8.3.1 MII management DC electrical characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII management DC electrical characteristics when powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII management AC electrical specifications

The following table provides the MII management AC timing specifications.

Table 25. MII management AC timing specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

Table 25. MII management AC timing specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	8.5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII management AC timing diagram.

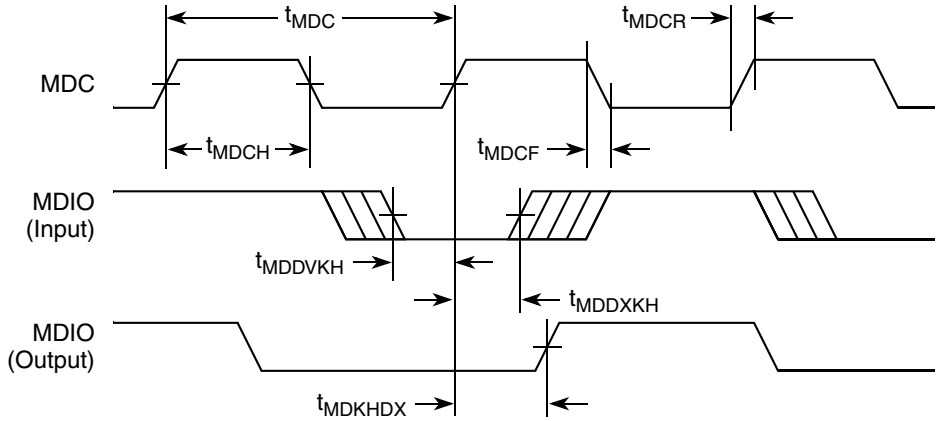


Figure 17. MII management interface timing diagram

8.3.3 IEEE 1588 DC Specifications

The IEEE 1588 DC timing specifications are given in the following table.

Table 26. IEEE 1588 DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	unit
Output high voltage	V_{OH}	I_{OH} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2mA	—	0.4	V

Table 26. IEEE 1588 DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	- 0.3	0.8	V
Input current	I_{IN}	$0V \le V_{IN} \le OV_{DD}$	—	± 5	μA

8.3.4 IEEE 1588 AC Specifications

The IEEE 1588 AC timing specifications are given in the following table.

Table 27. IEEE 1588 AC Timing Specifications

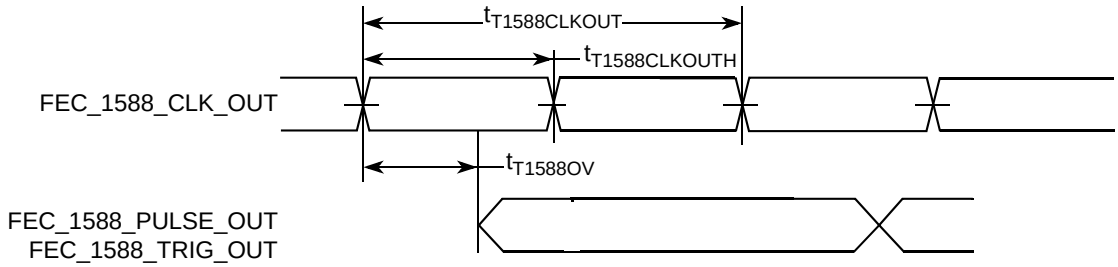
At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
QE_1588_CLK clock period	$t_{T1588CLK}$	2.5	—	$T_{RX\_CLK} \times 9$	ns	1, 3
QE_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	—
QE_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time QE_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time QE_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
QE_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
QE_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
QE_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
QE_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:

1. T_{RX_CLK} is the max clock period of QUICC engine receiving clock selected by TMR_CTRL[CKSEL]. See the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Reference Manual,* for a description of TMR_CTRL registers.
2. It needs to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Reference Manual,* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600 and 280ns, respectively.

The following figure provides the data and command output timing diagram.



Note: The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 18. IEEE1588 Output AC Timing

The following figure provides the data and command input timing diagram.

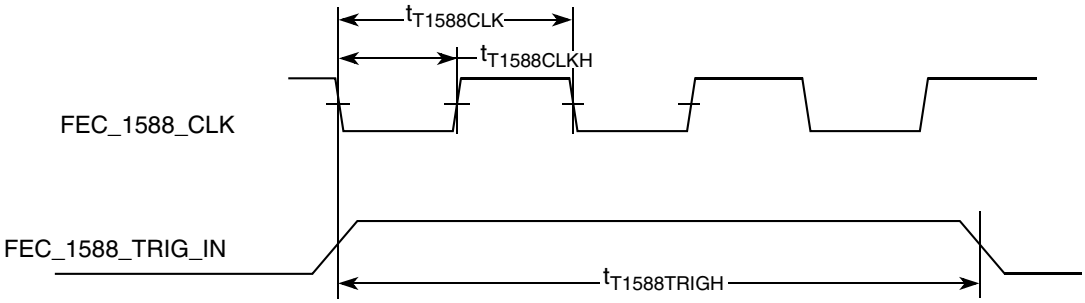


Figure 19. IEEE1588 Input AC Timing

9 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8309.

9.1 TDM/SI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 TDM/SI.

Table 28. TDM/SI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

9.2 TDM/SI AC timing specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 29. TDM/SI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

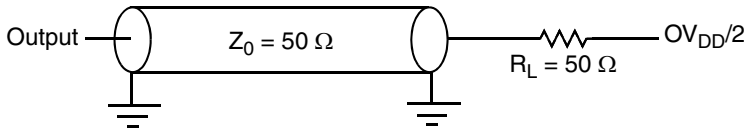
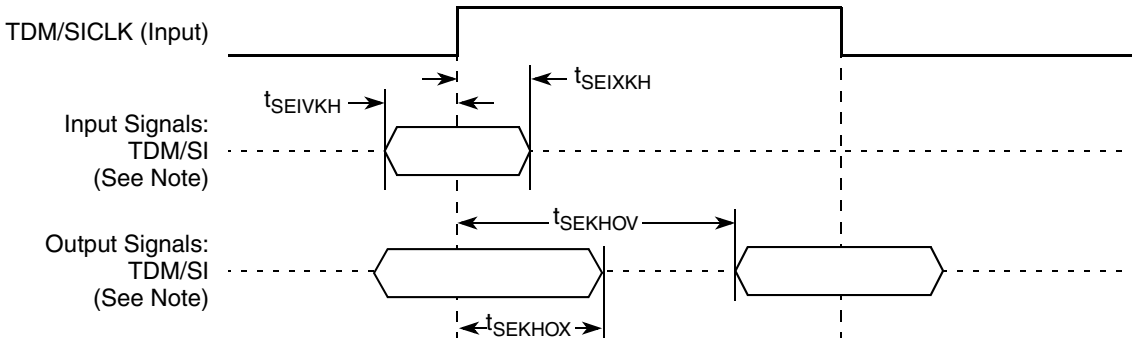


Figure 20. TDM/SI AC test load

The following figure represents the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 21. TDM/SI AC timing (external clock) diagram

10 HDLC

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), of the MPC8309.

10.1 HDLC DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 HDLC protocol.

Table 30. HDLC DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

10.2 HDLC AC timing specifications

The following table provides the input and output AC timing specifications for HDLC protocol.

Table 31. HDLC AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	9	ns
Outputs—External clock delay	t_{HEKHOV}	1	12	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	0	5.5	ns

Table 31. HDLC AC timing specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	9	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load.

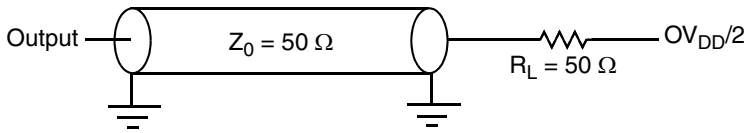
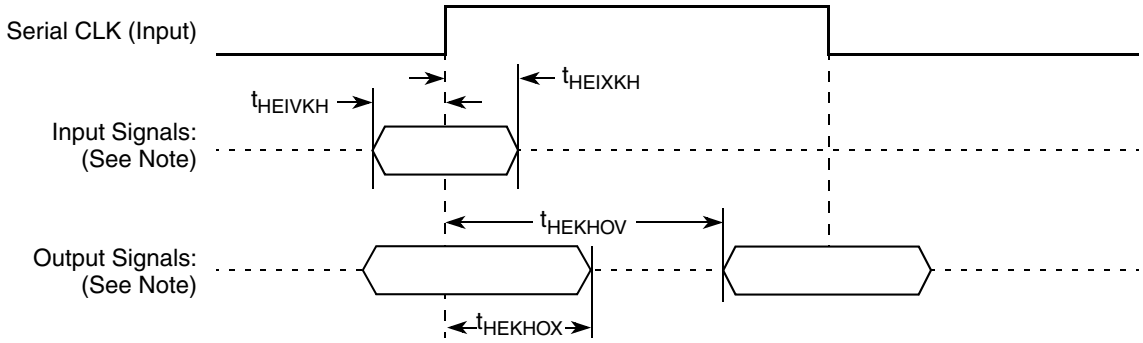


Figure 22. AC test load

Figure 23 and Figure 24 represent the AC timing from Table 31. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

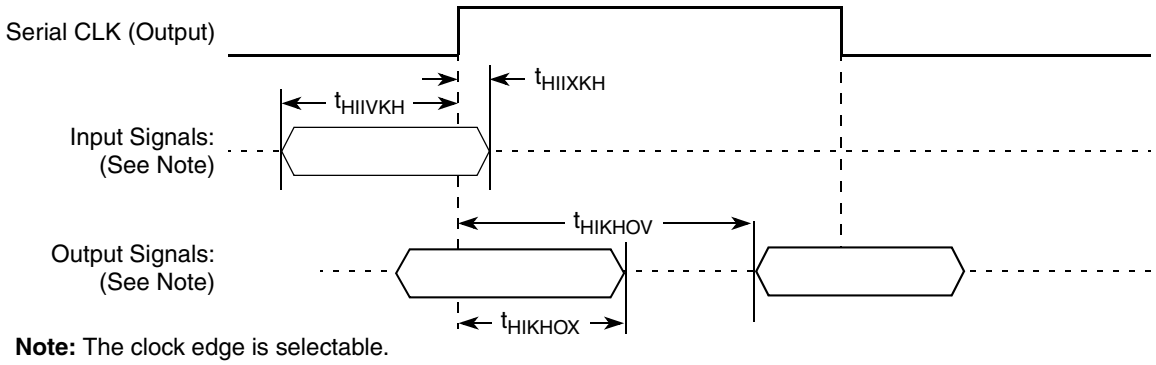
The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 23. AC timing (external clock) diagram

The following figure shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 24. AC timing (internal clock) diagram

11 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8309.

11.1 PCI DC electrical characteristics

Table 32 provides the DC electrical characteristics for the PCI interface of the MPC8309.

Table 32. PCI DC electrical characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	µA

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.
2. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications*.

11.2 PCI AC electrical specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8309. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8309 is configured as a host or agent device. Table 33 shows the PCI AC timing specifications at 66 MHz.

Table 34 shows the PCI AC timing specifications at 33 MHz.

Table 33. PCI AC timing specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Table 34. PCI AC timing specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 25 provides the AC test load for PCI.

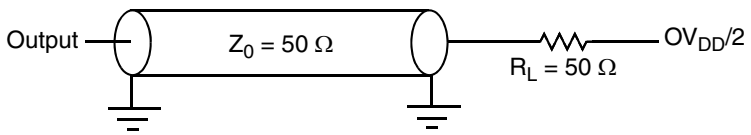


Figure 25. PCI AC test load

Figure 26 shows the PCI input AC timing conditions.

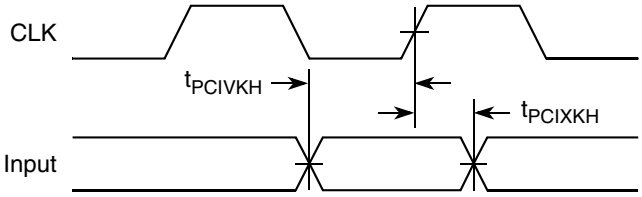


Figure 26. PCI input AC timing measurement conditions

Figure 27 shows the PCI output AC timing conditions.

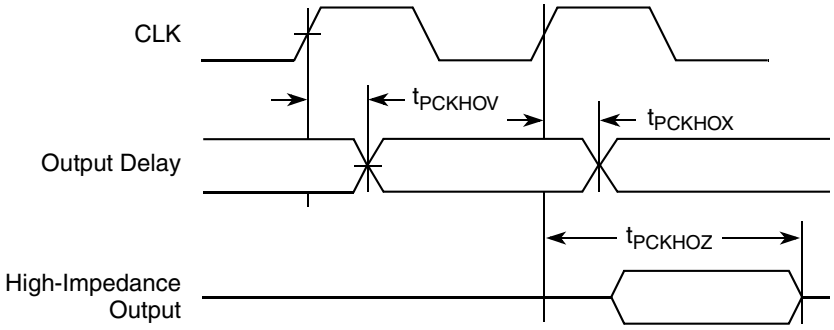


Figure 27. PCI output AC timing measurement condition

12 USB

12.1 USB controller

This section provides the AC and DC electrical specifications for the USB (ULPI) interface.

12.1.1 USB DC electrical characteristics

The following table provides the DC electrical characteristics for the USB interface.

Table 35. USB DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

12.1.2 USB AC electrical specifications

The following table describes the general timing parameters of the USB interface.

Table 36. USB general timing parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	—
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	—
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	—
USB clock to output valid—all outputs (except USBDR_STP_USBDR_STP)	t_{USKHOV}	—	7	ns	—
USB clock to output valid—USBDR_STP	t_{USKHOV}	—	7.5	ns	—
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	—

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following figures provide the AC test load and signals for the USB, respectively.

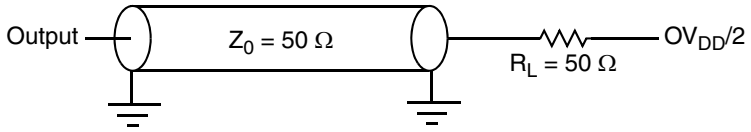


Figure 28. USB AC test load

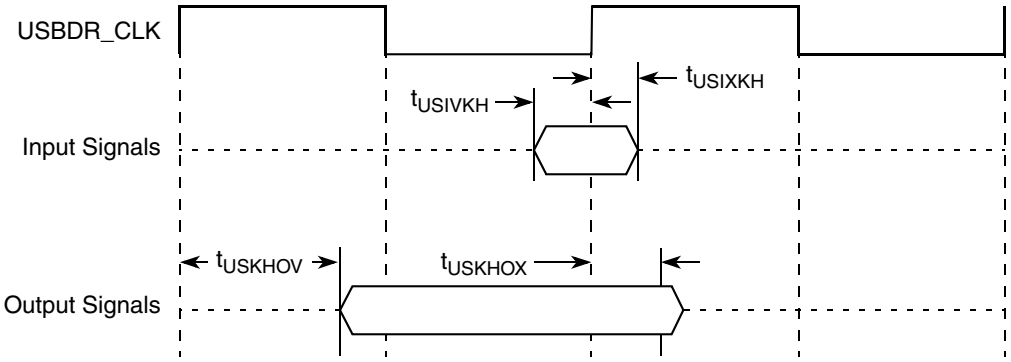


Figure 29. USB signals

13 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8309.

13.1 DUART DC electrical characteristics

The following table provides the DC electrical characteristics for the DUART interface of the MPC8309.

Table 37. DUART DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

13.2 DUART AC electrical specifications

The following table provides the AC timing parameters for the DUART interface of the MPC8309.

Table 38. DUART AC timing specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

14 eSDHC

This section describes the DC and AC electrical specifications for the eSDHC interface of the device.

14.1 eSDHC DC electrical characteristics

The following table provides the DC electrical characteristics for the eSDHC interface.

Table 39. eSDHC Interface DC electrical characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × OV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 μA at OV_{DD} min	0.75 × OV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 μA at OV_{DD} min	—	0.125 × OV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 mA	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	μA	—

Notes:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2..
2. Open drain mode for MMC cards only.

14.2 eSDHC AC timing specifications

The following table provides the eSDHC AC timing specifications as defined in Figure 30 and Figure 31.

Table 40. eSDHC AC timing specifications

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SHSCK}	0	25/33.25 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	4

Table 40. eSDHC AC timing specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–33.25 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

The following figure provides the eSDHC clock input timing diagram.

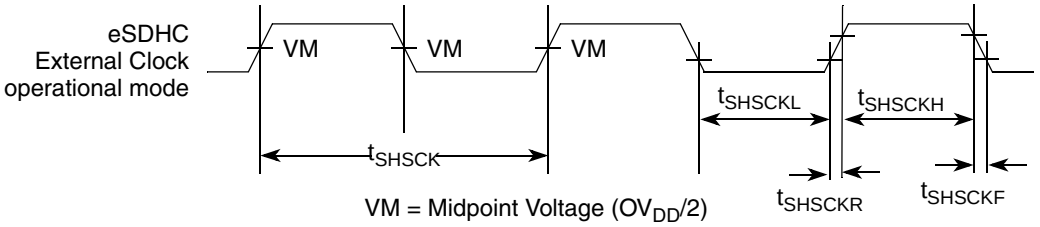


Figure 30. eSDHC clock input timing diagram

The following figure provides the data and command input/output timing diagram.

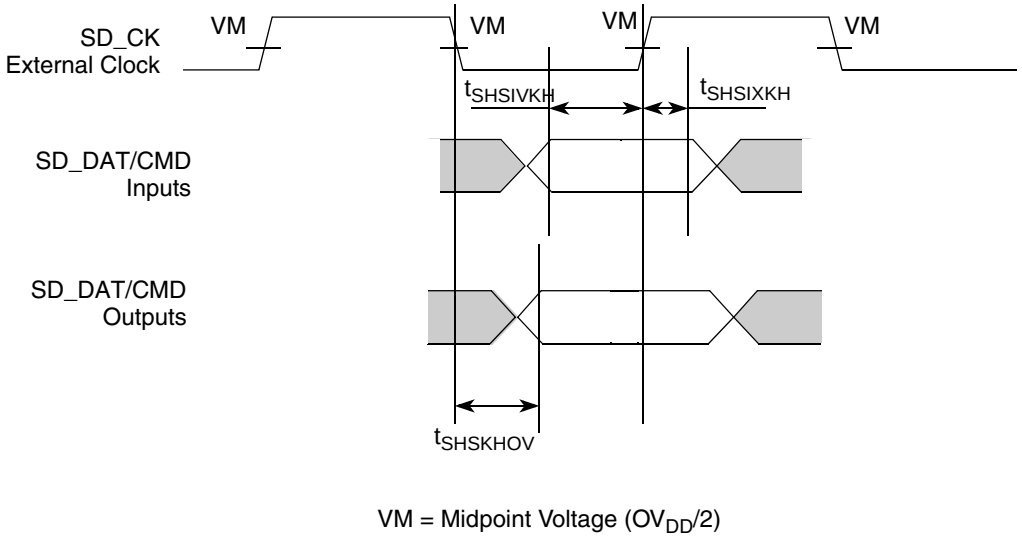


Figure 31. eSDHC data and command input/output timing diagram referenced to clock

15 FlexCAN

This section describes the DC and AC electrical specifications for the FlexCAN interface.

15.1 FlexCAN DC electrical characteristics

The following table provides the DC electrical characteristics for the FlexCAN interface.

Table 41. FlexCAN DC electrical characteristics (3.3V)

For recommended operating conditions, see Table 2

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2.
2. OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

15.2 FlexCAN AC timing specifications

The following table provides the AC timing specifications for the FlexCAN interface.

Table 42. FlexCAN AC timing specifications

For recommended operating conditions, see Table 2

Parameter	Min	Max	Unit	Notes
Baud rate	10	1000	Kbps	—

16 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8309.

16.1 I²C DC electrical characteristics

The following table provides the DC electrical characteristics for the I²C interface of the MPC8309.

Table 43. I²C DC electrical characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

16.2 I²C AC electrical specifications

The following table provides the AC timing parameters for the I²C interface of the MPC8309.

Table 44. I²C AC electrical specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	300	0.9[3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_B$[4]	300	ns

Table 44. I²C AC electrical specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 43).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8309 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

The following figure provides the AC test load for the I²C.

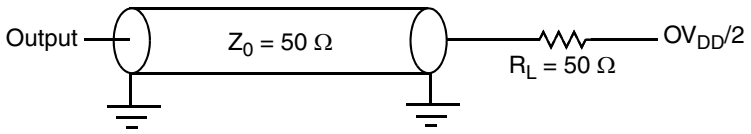


Figure 32. I²C AC test load

The following figure shows the AC timing diagram for the I²C bus.

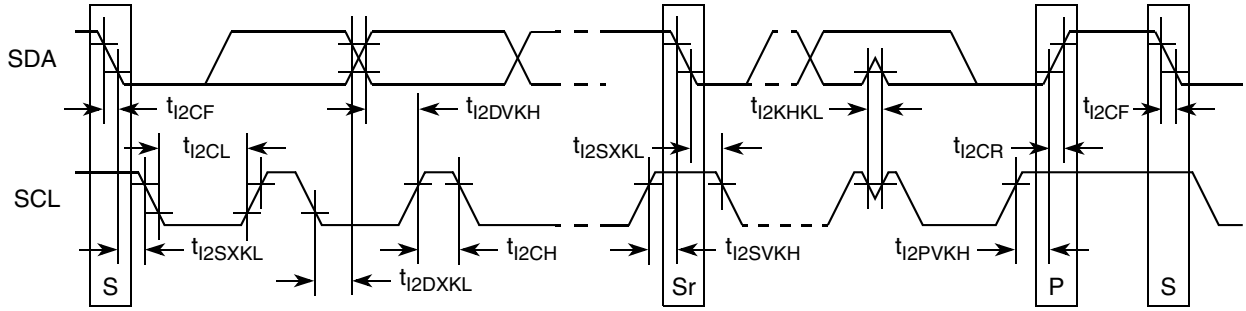


Figure 33. I²C bus AC timing diagram

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8309.

17.1 Timer DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_PIT_CLK.

Table 45. Timer DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

17.2 Timer AC timing specifications

The following table provides the timer input and output AC timing specifications.

Table 46. Timer input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

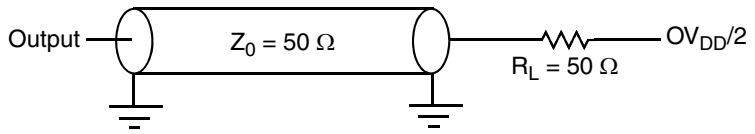


Figure 34. Timers AC test load

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8309.

18.1 GPIO DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 GPIO.

Table 47. GPIO DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

18.2 GPIO AC timing specifications

The following table provides the GPIO input and output AC timing specifications.

Table 48. GPIO input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

The following figure provides the AC test load for the GPIO.

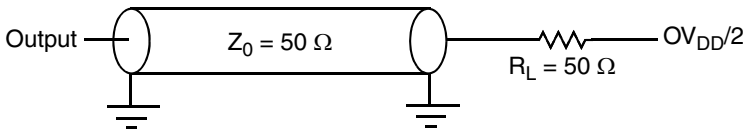


Figure 35. GPIO AC test load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8309.

19.1 IPIC DC electrical characteristics

The following table provides the DC electrical characteristics for the external interrupt pins of the MPC8309.

Table 49. IPIC DC electrical characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output High Voltage	V_{OH}	I_{OL} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$, $\overline{\text{MCP\_OUT}}$, and QE ports Interrupts.
2. $\overline{\text{MCP\_OUT}}$ is open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC timing specifications

The following table provides the IPIC input and output AC timing specifications.

Table 50. IPIC Input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8309.

20.1 SPI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 SPI.

Table 51. SPI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

20.2 SPI AC timing specifications

The following table and provide the SPI input and output AC timing specifications.

Table 52. SPI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. All units of output delay must be enabled for 8309_output_port spimosi_lpgl0(SPI Master mode)
4. Delay units must not be enabled for Slave mode.

The following figure provides the AC test load for the SPI.

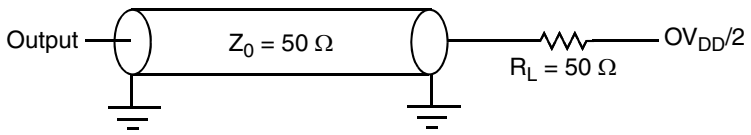
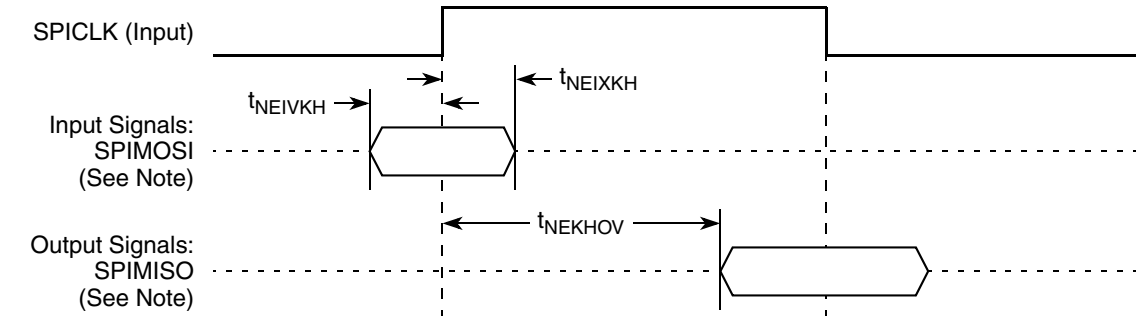


Figure 36. SPI AC test load

Figure 37 and Figure 38 represent the AC timing from Table 52. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

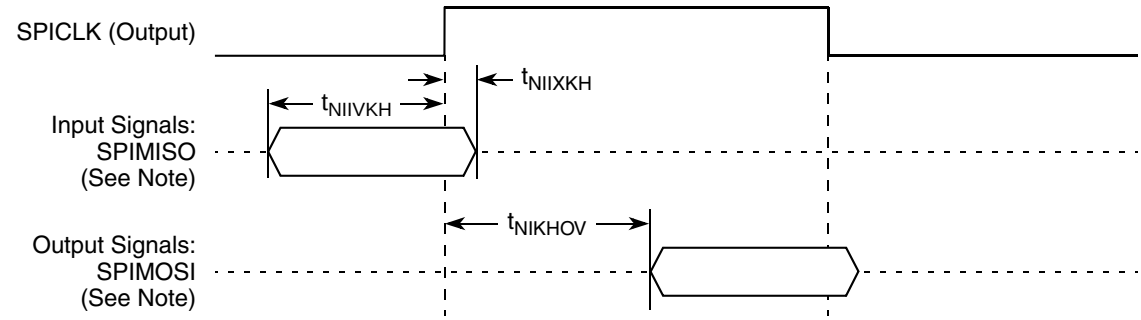
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 37. SPI AC Timing in slave mode (external clock) diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 38. SPI AC timing in master mode (internal clock) diagram

21 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8309.

21.1 JTAG DC electrical characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8309.

Table 53. JTAG interface DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 53. JTAG interface DC electrical characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

21.2 JTAG AC electrical characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8309. The following table provides the JTAG AC timing specifications as defined in Figure 40 through Figure 43.

Table 54. JTAG AC timing specifications (independent of SYS_CLK_IN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 15 15	ns	5

Table 54. JTAG AC timing specifications (independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	2	—		5
TDO	t_{JTKLOX}	2	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 39). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

The following figure provides the AC test load for TDO and the boundary-scan outputs of the MPC8309.

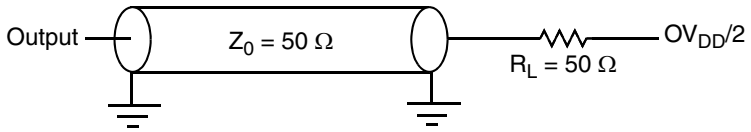


Figure 39. AC test load for the JTAG interface

The following figure provides the JTAG clock input timing diagram.

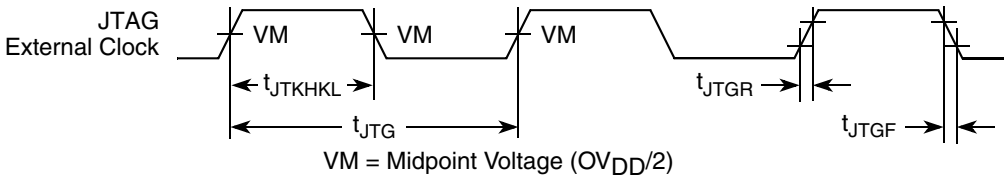


Figure 40. JTAG clock input timing diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

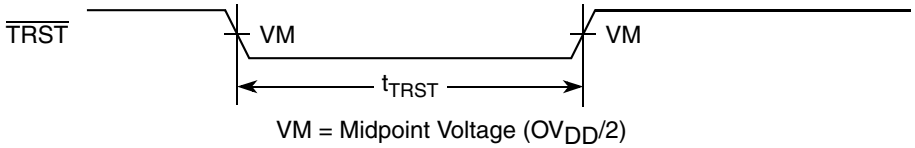


Figure 41. $\overline{\text{TRST}}$ timing diagram

The following figure provides the boundary-scan timing diagram.

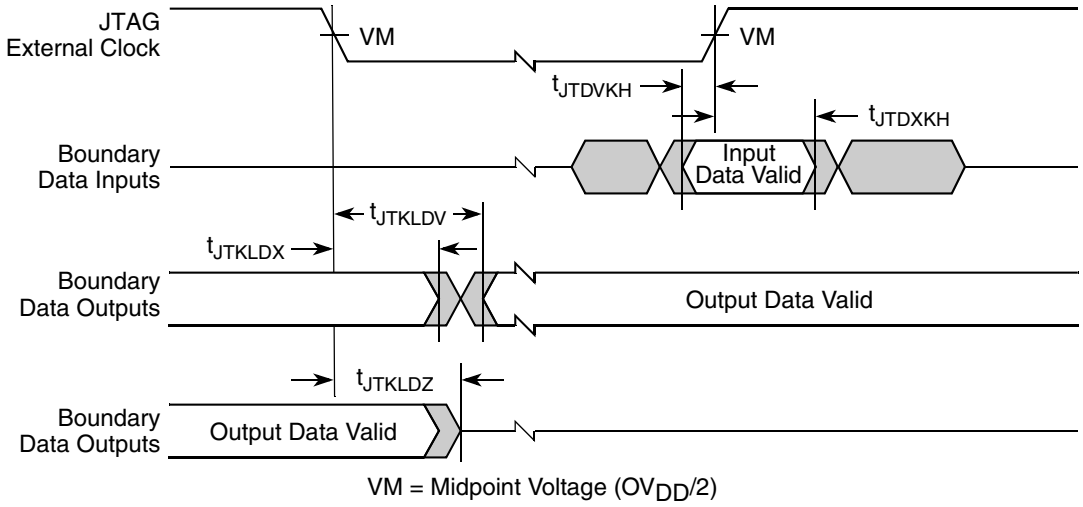


Figure 42. Boundary-Scan timing diagram

The following figure provides the test access port timing diagram.

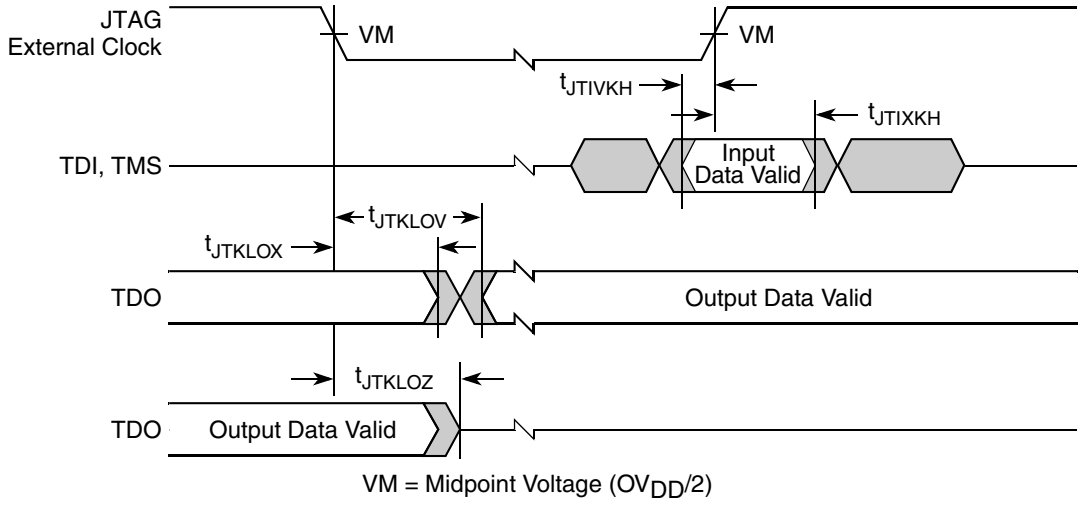


Figure 43. Test access port timing diagram

22 Package and pin listings

This section details package parameters, pin assignments, and dimensions. The MPC8309 is available in a thermally enhanced MAPBGA (mold array process-ball grid array); see Section 22.1, “Package parameters for the MPC8309,” and Section 22.2, “Mechanical dimensions of the MPC8309 MAPBGA,” for information on the MAPBGA.

22.1 Package parameters for the MPC8309

The package parameters are as provided in the following list.

Package outline	19 mm × 19 mm
Package Type	MAPBGA
Interconnects	489
Pitch	0.80 mm
Module height (typical)	1.48 mm; Min = 1.31mm and Max 1.61mm
Solder Balls	96 Sn / 3.5 Ag / 0.5 Cu (VM package)
Ball diameter (typical)	0.40 mm

22.2 Mechanical dimensions of the MPC8309 MAPBGA

The following figure shows the mechanical dimensions and bottom surface nomenclature of the MPC8309, 489-MAPBGA package.

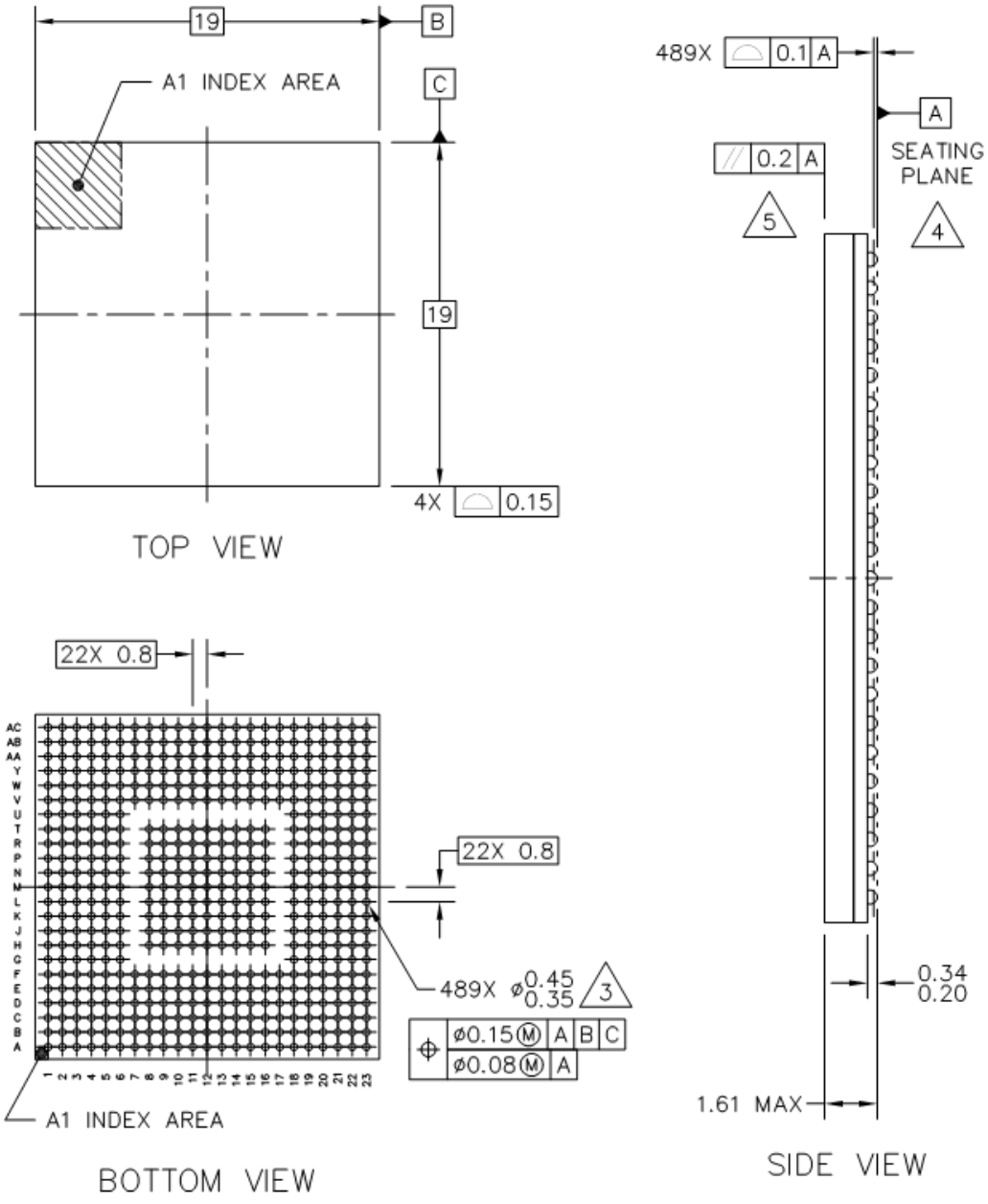


Figure 44. Mechanical dimensions and bottom surface nomenclature of the MPC8309 MAPBGA

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

22.3 Pinout listings

Following table shows the pin list of the MPC8309.

Table 55. MPC8309 pinout listing

Signal	Terminal	Pad Dir	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	U5	IO	GV_{DD}	—
MEMC_MDQ1	AA1	IO	GV_{DD}	—
MEMC_MDQ2	W3	IO	GV_{DD}	—
MEMC_MDQ3	R5	IO	GV_{DD}	—
MEMC_MDQ4	W2	IO	GV_{DD}	—
MEMC_MDQ5	U3	IO	GV_{DD}	—
MEMC_MDQ6	U2	IO	GV_{DD}	—
MEMC_MDQ7	T3	IO	GV_{DD}	—
MEMC_MDQ8	H3	IO	GV_{DD}	—
MEMC_MDQ9	H4	IO	GV_{DD}	—
MEMC_MDQ10	G3	IO	GV_{DD}	—
MEMC_MDQ11	F3	IO	GV_{DD}	—
MEMC_MDQ12	G5	IO	GV_{DD}	—
MEMC_MDQ13	F4	IO	GV_{DD}	—
MEMC_MDQ14	F5	IO	GV_{DD}	—
MEMC_MDQ15	E3	IO	GV_{DD}	—
MEMC_MDQ16	V4	IO	GV_{DD}	—
MEMC_MDQ17	Y2	IO	GV_{DD}	—
MEMC_MDQ18	Y1	IO	GV_{DD}	—
MEMC_MDQ19	U4	IO	GV_{DD}	—
MEMC_MDQ20	V1	IO	GV_{DD}	—
MEMC_MDQ21	R4	IO	GV_{DD}	—
MEMC_MDQ22	U1	IO	GV_{DD}	—
MEMC_MDQ23	T2	IO	GV_{DD}	—
MEMC_MDQ24	J5	IO	GV_{DD}	—
MEMC_MDQ25	G2	IO	GV_{DD}	—
MEMC_MDQ26	G1	IO	GV_{DD}	—
MEMC_MDQ27	F1	IO	GV_{DD}	—
MEMC_MDQ28	E2	IO	GV_{DD}	—

MEMC_MDQ29	D2	IO	GV_{DD}	—
MEMC_MDQ30	C2	IO	GV_{DD}	—
MEMC_MDQ31	C1	IO	GV_{DD}	—
MEMC_MECC0	Y5	IO	GV_{DD}	—
MEMC_MECC1	AA4	IO	GV_{DD}	—
MEMC_MECC2	Y4	IO	GV_{DD}	—
MEMC_MECC3	AA3	IO	GV_{DD}	—
MEMC_MECC4	AC2	IO	GV_{DD}	—
MEMC_MECC5	AB2	IO	GV_{DD}	—
MEMC_MECC6	Y3	IO	GV_{DD}	—
MEMC_MECC7	AB1	IO	GV_{DD}	—
MEMC_MDM0	W1	O	GV_{DD}	—
MEMC_MDM1	E1	O	GV_{DD}	—
MEMC_MDM2	V3	O	GV_{DD}	—
MEMC_MDM3	D1	O	GV_{DD}	—
MEMC_MDM8	W5	O	GV_{DD}	—
MEMC_MDQS0	T5	IO	GV_{DD}	—
MEMC_MDQS1	H5	IO	GV_{DD}	—
MEMC_MDQS2	P5	IO	GV_{DD}	—
MEMC_MDQS3	E5	IO	GV_{DD}	-
MEMC_MDQS8	V5	IO	GV_{DD}	-
MEMC_MBA0	K2	O	GV_{DD}	-
MEMC_MBA1	K3	O	GV_{DD}	-
MEMC_MBA2	N5	O	GV_{DD}	-
MEMC_MA0	L3	O	GV_{DD}	-
MEMC_MA1	L5	O	GV_{DD}	-
MEMC_MA2	L2	O	GV_{DD}	-
MEMC_MA3	L1	O	GV_{DD}	-
MEMC_MA4	M3	O	GV_{DD}	-
MEMC_MA5	M4	O	GV_{DD}	-
MEMC_MA6	M1	O	GV_{DD}	-
MEMC_MA7	N1	O	GV_{DD}	-
MEMC_MA8	N2	O	GV_{DD}	-
MEMC_MA9	N3	O	GV_{DD}	-
MEMC_MA10	L4	O	GV_{DD}	-
MEMC_MA11	P2	O	GV_{DD}	-
MEMC_MA12	N4	O	GV_{DD}	-

MEMC_MA13	P1	O	GV_{DD}	-
MEMC_MWE_B	J1	O	GV_{DD}	-
MEMC_MRAS_B	K1	O	GV_{DD}	-
MEMC_MCAS_B	J3	O	GV_{DD}	-
MEMC_MCS_B0	J4	O	GV_{DD}	-
MEMC_MCS_B1	K5	O	GV_{DD}	-
MEMC_MCKE	P4	O	GV_{DD}	-
MEMC_MCK0	R1	O	GV_{DD}	-
MEMC_MCK1	R3	O	GV_{DD}	-
MEMC_MCK_B0	T1	O	GV_{DD}	-
MEMC_MCK_B1	P3	O	GV_{DD}	-
MEMC_MODT0	H1	O	GV_{DD}	-
MEMC_MODT1	H2	O	GV_{DD}	-
MEMC_MVREF	M6		GV_{DD}	-
Local Bus Controller Interface				
LAD0	B5	IO	OV_{DD}	-
LAD1	A4	IO	OV_{DD}	-
LAD2	C7	IO	OV_{DD}	-
LAD3	D9	IO	OV_{DD}	-
LAD4	A5	IO	OV_{DD}	-
LAD5	E10	IO	OV_{DD}	-
LAD6	A6	IO	OV_{DD}	-
LAD7	C8	IO	OV_{DD}	-
LAD8	D10	IO	OV_{DD}	-
LAD9	A7	IO	OV_{DD}	-
LAD10	B7	IO	OV_{DD}	-
LAD11	C9	IO	OV_{DD}	-
LAD12	E11	IO	OV_{DD}	-
LAD13	B8	IO	OV_{DD}	-
LAD14	A8	IO	OV_{DD}	-
LAD15	C10	IO	OV_{DD}	-
LA16	C11	IO	OV_{DD}	-
LA17	B10	O	OV_{DD}	-
LA18	D12	O	OV_{DD}	-
LA19	A9	O	OV_{DD}	-
LA20	E12	O	OV_{DD}	-
LA21	B11	O	OV_{DD}	-

LA22	A11	O	OV_{DD}	-
LA23	A10	O	OV_{DD}	-
LA24	C12	O	OV_{DD}	-
LA25	A12	O	OV_{DD}	-
LCLK0	E13	O	OV_{DD}	-
LCS_B0	D13	O	OV_{DD}	2
LCS_B1	C13	O	OV_{DD}	2
LCS_B2	A13	O	OV_{DD}	2
LCS_B3	B13	O	OV_{DD}	2
LWE_B0/LFWE_B0/LBS_B0	A14	O	OV_{DD}	-
LWE_B1/LBS_B1	B14	O	OV_{DD}	-
LBCTL	A15	O	OV_{DD}	-
LGPL0/LFCLE	C14	O	OV_{DD}	-
LGPL1/LFALE	C15	O	OV_{DD}	-
LGPL2/LOE_B/LFRE_B	B16	O	OV_{DD}	2
LGPL3/LFWP_B	A16	O	OV_{DD}	-
LGPL4/LGTA_B/LUPWAIT/LFRB_B	E14	IO	OV_{DD}	2
LGPL5	B17	O	OV_{DD}	-
LALE	A17	O	OV_{DD}	-
DUART				
UART1_SOUT1	AB7	O	OV_{DD}	-
UART1_SIN1	AC6	I	OV_{DD}	-
UART1_SOUT2/UART1_RTS_B1	W10	O	OV_{DD}	-
UART1_SIN2/UART1_CTS_B1	Y9	I	OV_{DD}	-
I2C				
IIC_SDA1	A20	IO	OV_{DD}	1
IIC_SCL1	B20	IO	OV_{DD}	1
IIC_SDA2 /CKSTOP_OUT_B	D19	IO	OV_{DD}	1
IIC_SCL2/CKSTOP_IN_B	C20	IO	OV_{DD}	1
Interrupts				
IRQ_B0_MCP_IN_B	A21	IO	OV_{DD}	-
IRQ_B1/MCP_OUT_B	A22	IO	OV_{DD}	-
IRQ_B2/CKSTOP_IN_B	E18	I	OV_{DD}	-
IRQ_B3/CKSTOP_OUT_B/INTA_B	E19	IO	OV_{DD}	-
SPI				
SPIMOSI	B19	IO	OV_{DD}	-

SPIMISO	E16	IO	OV_{DD}	-
SPICLK	E17	IO	OV_{DD}	-
SPISEL	A19	I	OV_{DD}	-
SPISEL_BOOT_B	D18		OV_{DD}	-
JTAG				
TCK	A2	I	OV_{DD}	-
TDI	C5	I	OV_{DD}	2
TDO	A3	O	OV_{DD}	-
TMS	D7	I	OV_{DD}	2
TRST_B	E9	I	OV_{DD}	2
Test Interface				
TEST_MODE	C6	I	OV_{DD}	-
System Control Signals				
HRESET_B	W23	IO	OV_{DD}	1
PORESET_B	W22	I	OV_{DD}	-
Clock Interface				
QE_CLK_IN	R22	I	OV_{DD}	-
SYS_CLK_IN	R23	I	OV_{DD}	-
SYS_XTAL_IN	P23	I	OV_{DD}	-
SYS_XTAL_OUT	P19	O	OV_{DD}	-
PCI_SYNC_IN	T23	I	OV_{DD}	-
PCI_SYNC_OUT	R20	O	OV_{DD}	-
CFG_CLKIN_DIV_B	U23	I	OV_{DD}	-
RTC_PIT_CLOCK	V23	I		
Miscellaneous Signals				
QUIESCE_B	D6	O	OV_{DD}	-
THERM0	E8		OV_{DD}	-
GPIO				
GPIO_0/SD_CLK/MSRCID0 (DDR ID)	E4	IO	OV_{DD}	-
GPIO_1/SD_CMD/MSRCID1 (DDR ID)	E6	IO	OV_{DD}	-
GPIO_2/SD_CD/MSRCID2 (DDR ID)	D3	IO	OV_{DD}	-
GPIO_3/SD_WP/MSRCID3 (DDR ID)	E7	IO	OV_{DD}	-
GPIO_4/SD_DAT0/MSRCID4 (DDR ID)	D4	IO	OV_{DD}	-
GPIO_5/SD_DAT1/MDVAL (DDR ID)	C4	IO	OV_{DD}	-
GPIO_6/SD_DAT2/QE_EXT_REQ_3	B2	IO	OV_{DD}	-
GPIO_7/SD_DAT3/QE_EXT_REQ_1	B3	IO	OV_{DD}	-
GPIO_8/RXCAN1/LSRCID0/LCS_B4	C16	IO	OV_{DD}	-

GPIO_9/TXCAN1/LSRCID1/LCS_B5	C17	IO	OV_{DD}	-
GPIO_10/RXCAN2/LSRCID2/LCS_B6	E15	IO	OV_{DD}	-
GPIO_11/TXCAN2/LSRCID3/LCS_B7	A18	IO	OV_{DD}	-
GPIO_12/RXCAN3/LSRCID4/LCLK1	D15	IO	OV_{DD}	-
GPIO_13/TXCAN3/LDVAL	C18	IO	OV_{DD}	-
GPIO_14/RXCAN4	D16	IO	OV_{DD}	-
GPIO_15/TXCAN4	C19	IO	OV_{DD}	-
USB				
USBDR_PWRFAULT/CE_PIO_1	AA6	I	OV_{DD}	1
USBDR_CLK/UART2_SIN2/UART2_CTS_B1	AC9	I	OV_{DD}	-
USBDR_DIR	AA7	I	OV_{DD}	-
USBDR_NXT/UART2_SIN1/QE_EXT_REQ_4	AC5	I	OV_{DD}	-
USBDR_TXDRXD0/GPIO_32	Y6	IO	OV_{DD}	-
USBDR_TXDRXD1/GPIO_33	W9	IO	OV_{DD}	-
USBDR_TXDRXD2/GPIO_34/QE_BRG_1	AB5	IO	OV_{DD}	-
USBDR_TXDRXD3/GPIO_35/QE_BRG_2	AA5	IO	OV_{DD}	-
USBDR_TXDRXD4/GPIO_36/QE_BRG_3	Y8	IO	OV_{DD}	-
USBDR_TXDRXD5/GPIO_37/QE_BRG_4	AC4	IO	OV_{DD}	-
USBDR_TXDRXD6/GPIO_38/QE_BRG_9	AC3	IO	OV_{DD}	-
USBDR_TXDRXD7/GPIO_39/QE_BRG_11	AB3	IO	OV_{DD}	-
USBDR_PCTL0/UART2_SOUT1/LB_POR_CFG_BOOT_ECC	W8	O	OV_{DD}	-
USBDR_PCTL1/UART2_SOUT2/UART2_RTS_B1/LB_POR_BOOT_ERR	W7	O	OV_{DD}	-
USBDR_STP/QE_EXT_REQ_2	W6	O	OV_{DD}	-
PCI				
PCI_INTA_B	B22	O	OV_{DD}	-
PCI_RESET_OUT_B	F19	O	OV_{DD}	-
PCI_AD0	B23	IO	OV_{DD}	-
PCI_AD1	C21	IO	OV_{DD}	-
PCI_AD2	E20	IO	OV_{DD}	-
PCI_AD3	G19	IO	OV_{DD}	-
PCI_AD4	C23	IO	OV_{DD}	-
PCI_AD5	H19	IO	OV_{DD}	-
PCI_AD6/CE_PIO_0	D21	IO	OV_{DD}	-
PCI_AD7	F20	IO	OV_{DD}	-

PCI_AD8/	E21	IO	OV_{DD}	-
PCI_AD9/	H20	IO	OV_{DD}	-
PCI_AD10/	D22	IO	OV_{DD}	-
PCI_AD11/	D23	IO	OV_{DD}	-
PCI_AD12/	J19	IO	OV_{DD}	-
PCI_AD13/	F21	IO	OV_{DD}	-
PCI_AD14/	G21	IO	OV_{DD}	-
PCI_AD15/	E22	IO	OV_{DD}	-
PCI_AD16/	E23	IO	OV_{DD}	-
PCI_AD17/	J20	IO	OV_{DD}	-
PCI_AD18/	F23	IO	OV_{DD}	-
PCI_AD19/	G23	IO	OV_{DD}	-
PCI_AD20	K19	IO	OV_{DD}	-
PCI_AD21	H21	IO	OV_{DD}	-
PCI_AD22	L19	IO	OV_{DD}	-
PCI_AD23	G22	IO	OV_{DD}	-
PCI_AD24	H23	IO	OV_{DD}	-
PCI_AD25	J21	IO	OV_{DD}	-
PCI_AD26	H22	IO	OV_{DD}	-
PCI_AD27	J23	IO	OV_{DD}	-
PCI_AD28	K18	IO	OV_{DD}	-
PCI_AD29	K21	IO	OV_{DD}	-
PCI_AD30	K22	IO	OV_{DD}	-
PCI_AD31	K23	IO	OV_{DD}	-
PCI_C_BE_B0	L20	IO	OV_{DD}	-
PCI_C_BE_B1	L23	IO	OV_{DD}	-
PCI_C_BE_B2	L22	IO	OV_{DD}	-
PCI_C_BE_B3	L21	IO	OV_{DD}	-
PCI_PAR	M19	IO	OV_{DD}	-
PCI_FRAME_B	M20	IO	OV_{DD}	-
PCI_TRDY_B	M23	IO	OV_{DD}	-
PCI_IRDY_B	M21	IO	OV_{DD}	-
PCI_STOP_B	N23	IO	OV_{DD}	-
PCI_DEVSEL_B	N22	IO	OV_{DD}	-
PCI_IDSEL	N21	IO	OV_{DD}	-
PCI_SERR_B	N19	IO	OV_{DD}	-
PCI_PERR_B	P20	IO	OV_{DD}	-

PCI_REQ_B0	P21	IO	OV_{DD}	-
PCI_REQ_B1/CPCI_HS_ES	P22	IO	OV_{DD}	-
PCI_REQ_B2	T22	IO	OV_{DD}	-
PCI_GNT_B0	T21	IO	OV_{DD}	-
PCI_GNT_B1/CPCI_HS_LED	U22	O	OV_{DD}	-
PCI_GNT_B2/CPCI_HS_ENUM	U21	IO	OV_{DD}	-
M66EN	V21	I	OV_{DD}	-
PCI_CLK0	T19	O	OV_{DD}	-
PCI_CLK1	U19	O	OV_{DD}	-
PCI_CLK2	R19	O	OV_{DD}	-
Ethernet Management				
FEC_MDC	W18	O	OV_{DD}	-
FEC_MDIO	W17	IO	OV_{DD}	-
FEC/GTM/GPIO				
FEC1_COL/GTM1_TIN1/GPIO_16	Y18	IO	OV_{DD}	-
FEC1_CRS/GTM1_TGATE1_B/GPIO_17	AA19	IO	OV_{DD}	-
FEC1_RX_CLK[CLK9]/GPIO_18	W16	IO	OV_{DD}	-
FEC1_RX_DV/GTM1_TIN2/GPIO_19	AC22	IO	OV_{DD}	-
FEC1_RX_ER/GTM1_TGATE2_B/GPIO_20	AA18	IO	OV_{DD}	-
FEC1_RXD0/GPIO_21	AB20	IO	OV_{DD}	-
FEC1_RXD1/GTM1_TIN3/GPIO_22	Y17	IO	OV_{DD}	-
FEC1_RXD2/GTM1_TGATE3_B/GPIO_23	AB19	IO	OV_{DD}	-
FEC1_RXD3/GPIO_24	AC21	IO	OV_{DD}	-
FEC1_TX_CLK[CLK10]/GTM1_TIN4/GPIO_25	W15	IO	OV_{DD}	-
FEC1_TX_EN/GTM1_TGATE4_B/GPIO_26	AC19	IO	OV_{DD}	-
FEC1_TX_ER/GTM1_TOUT4_B/GPIO_27	AC20	IO	OV_{DD}	-
FEC1_TXD0/GTM1_TOUT1_B/GPIO_28/	AA17	IO	OV_{DD}	-
FEC1_TXD1/GTM1_TOUT2_B/GPIO_29	AC18	IO	OV_{DD}	-
FEC1_TXD2/GTM1_TOUT3_B/GPIO_30	AA16	IO	OV_{DD}	-
FEC1_TXD3/GPIO_31	AB17	IO	OV_{DD}	-
FEC2_COL/GTM2_TIN1/GPIO_32	Y15	IO	OV_{DD}	-
FEC2_CRS/GTM2_TGATE1_B/GPIO_33	AC17	IO	OV_{DD}	-

FEC2_RX_CLK[CLK7]/GPIO_34	W14	IO	OV_{DD}	-
FEC2_RX_DV/GTM2_TIN2/GPIO_35	AB16	IO	OV_{DD}	-
FEC2_RX_ER/GTM2_TGATE2_B/GPIO_36	Y14	IO	OV_{DD}	-
FEC2_RXD0/GPIO_37	AA15	IO	OV_{DD}	-
FEC2_RXD1/GTM2_TIN3/GPIO_38	AC15	IO	OV_{DD}	-
FEC2_RXD2/GTM2_TGATE3_B/GPIO_39	AC16	IO	OV_{DD}	-
FEC2_RXD3/GPIO_40	AA14	IO	OV_{DD}	-
FEC2_TX_CLK[CLK8]/GTM2_TIN4/GPIO_41	W13	IO	OV_{DD}	-
FEC2_TX_EN/GTM2_TGATE4_B/GPIO_42	AB14	IO	OV_{DD}	-
FEC2_TX_ER/GTM2_TOUT4_B/GPIO_43	AC14	IO	OV_{DD}	-
FEC2_TXD0/GTM2_TOUT1_B/GPIO_44	Y12	IO	OV_{DD}	-
FEC2_TXD1/GTM2_TOUT2_B/GPIO_45	AA13	IO	OV_{DD}	-
FEC2_TXD2/GTM2_TOUT3_B/GPIO_46	AB13	IO	OV_{DD}	-
FEC2_TXD3/GPIO_47	AC13	IO	OV_{DD}	-
FEC3_COL/GPIO_48	AC12	IO	OV_{DD}	-
FEC3_CRS/GPIO_49	W11	IO	OV_{DD}	-
FEC3_RX_CLK[CLK11]/GPIO_50	W12	IO	OV_{DD}	-
FEC3_RX_DV/FEC1_TMR_TX_ESFD/GPIO_51	AA12	IO	OV_{DD}	-
FEC3_RX_ER/FEC1_TMR_RX_ESFD/GPIO_52	AB11	IO	OV_{DD}	-
FEC3_RXD0/FEC2_TMR_TX_ESFD/GPIO_53	AA11	IO	OV_{DD}	-
FEC3_RXD1/FEC2_TMR_RX_ESFD/GPIO_54	AC11	IO	OV_{DD}	-
FEC3_RXD2/FEC_TMR_TRIG1/GPIO_55	Y11	IO	OV_{DD}	-
FEC3_RXD3/FEC_TMR_TRIG2/GPIO_56	AB10	IO	OV_{DD}	-
FEC3_TX_CLK[CLK12]/FEC_TMR_CLK/GPIO_57	AC10	IO	OV_{DD}	-
FEC3_TX_EN/FEC_TMR_GCLK/GPIO_58	AA10	IO	OV_{DD}	-
FEC3_TX_ER/FEC_TMR_PP1/GPIO_59	AC8	IO	OV_{DD}	-
FEC3_TXD0/FEC_TMR_PP2/GPIO_60	AB8	IO	OV_{DD}	-
FEC3_TXD1/FEC_TMR_PP3/GPIO_61	AA9	IO	OV_{DD}	-
FEC3_TXD2/FEC_TMR_ALARM1/GPIO_62	AA8	IO	OV_{DD}	-
FEC3_TXD3/FEC_TMR_ALARM2/GPIO_63	AC7	IO	OV_{DD}	-

HDLC/TDM/GPIO				
HDLC1_TXCLK[CLK16]/GPIO_0/QE_BRG_5/TDM1_TCK[CLK4]	AA20	IO	OV_{DD}	-
HDLC1_RXCLK[CLK15]/GPIO_1/TDM1_RCK[CLK3]	AA21	IO	OV_{DD}	-
HDLC1_TXD/GPIO_2/TDM1_TD/CFG_RESET_SOURCE[0]	AB22	IO	OV_{DD}	1
HDLC1_RXD/GPIO_3/TDM1_RD	AB23	IO	OV_{DD}	-
HDLC1_CD_B/GPIO_4/TDM1_TFS	W19	IO	OV_{DD}	-
HDLC1_CTS_B/GPIO_5/TDM1_RFS	V19	IO	OV_{DD}	-
HDLC1_RTS_B/GPIO_6/TDM1_STROBE_B/CFG_RESET_SOURCE[1]	AA23	IO	OV_{DD}	-
HDLC2_TXCLK[CLK14]/GPIO_16/QE_BRG_7/TDM2_TCK[CLK6]	Y20	IO	OV_{DD}	-
HDLC2_RXCLK[CLK13]/GPIO_17/TDM2_RCK[CLK5]/QE_BRG_8	Y22	IO	OV_{DD}	-
HDLC2_TXD/GPIO_18/TDM2_TD/CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	1
HDLC2_RXD/GPIO_19/TDM2_RD	W21	IO	OV_{DD}	-
HDLC2_CD_B/GPIO_20/TDM2_TFS	V20	IO	OV_{DD}	-
HDLC2_CTS_B/GPIO_21/TDM2_RFS	Y23	IO	OV_{DD}	-
HDLC2_RTS_B/GPIO_22/TDM2_STROBE_B/CFG_RESET_SOURCE[3]	U20	IO	OV_{DD}	-
Power				
AVDD1	L16	-	-	-
AVDD2	M16	-	-	-
AVDD3	N8	-	-	-
GVDD	F6, G6, H6, J6, K6, L6, N6, P6, R6, T6, U6, V6, V7	-	-	-
NVDD	F7, F8, F9, F10, F11, F12, F13,F14, F15, F16, F17, F18, G18,H18, J18, L18, M18, N18, P18,R18, T18, U18, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	-	-	-

VDD	H8,H9,H10,H11,H12,M8, H13,N16,H14,H15,H16, P16,P8,L8,K16,J16,K8,J 8,R8,T16,R16,T8,T9,T11 ,T10,T12,T13,T14,T15	-	-	-
VSS	A1, C3, F22, J14, K14, M15, L15, N20, R9, Y21, T20, AB21, B1, C22,G4, K15, J15, M2, M22, P9, R10, V2, AA2, AC1, B4,D5, G20, J22, K20, M5, N9, P10, R11, V22, AA22,AC23, B6, D8, J2, K4, M9,L9, N10, P11, R12, W4, AB4, D11, B9, J9, K9, L10,M10, N11, P12, R13, Y7,AB6, B12, D14, J10, K10, L11, M11, P13, N12, R14, Y10,AB9, B15, D17, J11, K11, D20, B18, J12, K12, L13, L12, L14, K13, J13, F2, B21, M14, M13, M12, Y19, Y16, AB15, AB12, Y13, N13, N14, N15, P14, P15, R2, AB18, R15, R21, T4	-	-	-
NC	A23	-	-	-

Notes

1. This pin is an open drain signal. A weak pull-up resistor should be placed on this pin to OV_{DD}

2 This pin has weak pull-up that is always enabled.

4. OVDD here refers to NVDDA, NVDDB,NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.

23 Clocking

The following figure shows the internal distribution of clocks within the MPC8309.

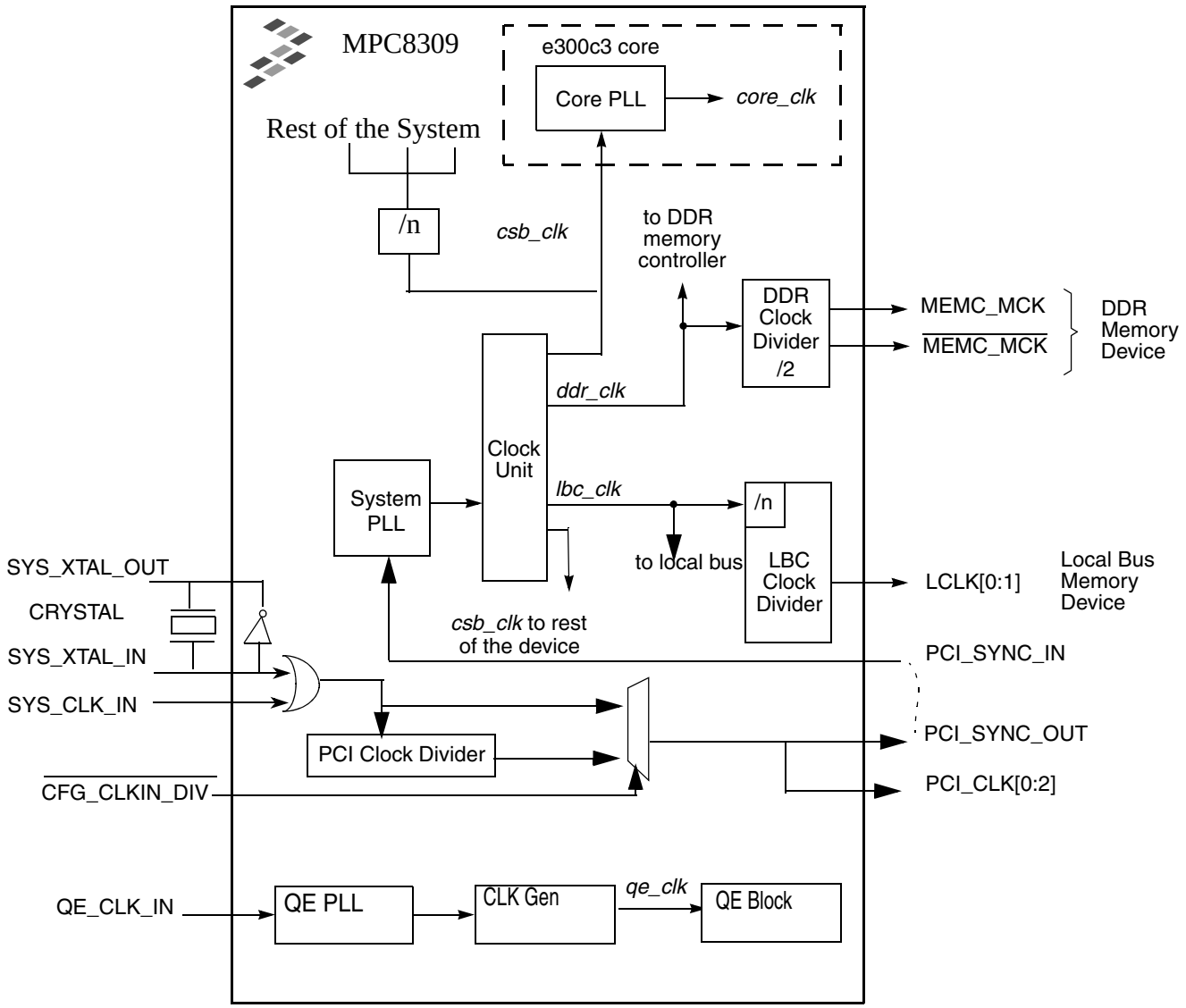


Figure 45. MPC8309 clock subsystem

The primary clock source for the MPC8309 can be one of three inputs,Crystal(SYS_XTAL_IN), SYS_CLK_IN or PCI_SYNC_IN, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

23.1 Clocking in PCI host mode

When the MPC8309 is configured as a PCI host device (RCWH[PCIHOST] = 1), SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK multiplexors. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

23.1.1 PCI clock outputs (PCI_CLK[0:2])

When the MPC8309 is configured as a PCI host, it provides three separate clock output signals, PCI_CLK[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

23.2 Clocking in PCI agent mode

When the MPC8309 is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock. In agent mode, the SYS_CLK_IN signal should be tied to GND, and the clock output signals, PCI_CLK*n* and PCI_SYNC_OUT, are not used.

23.3 System clock domains

As shown in Figure 45, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create four major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*qe_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lbc_clk*)

The *csb_clk* frequency is derived from the following equation:

$$csb\_clk = [\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})] \times \text{SPMF} \qquad \textbf{Eqn. 1}$$

In PCI host mode,

$$PCI\_SYNC\_IN = SYS\_CLK\_IN \div (1 + \sim\overline{CFG\_CLKIN\_DIV}) . \qquad \textbf{Eqn. 2}$$

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset

Configuration chapter in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

The *qe_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF]) and the QUICC Engine PLL division factor (RCWL[CEPDF]) as the following equation:

$$qe\_clk = (QE\_CLK\_IN \times CEPMF) \div (1 + CEPDF) \quad \textbf{Eqn. 3}$$

For more information, see the QUICC Engine PLL Multiplication Factor section and the "QUICC Engine PLL Division Factor" section in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LCLK). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. For more information, see the LBC Bus Clock and Clock Ratios section in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset.

The following table specifies which units have a configurable clock frequency. For detailed description, refer to the "System Clock Control Register (SCCR)" section in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

Table 56. Configurable clock units

Unit	Default Frequency	Options
I2C,SDHC, USB, DMA Complex	*csb_clk*	Off, csb_clk, *csb_clk*/2, *csb_clk*/3

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

The following table provides the maximum operating frequencies for the MPC8309 MAPBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for MAPBGA

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	417	MHz
Coherent system bus frequency (*csb_clk*)	167	MHz
QUICC Engine frequency (*qe_clk*)	233	MHz

Table 57. Operating Frequencies for MAPBGA (continued)

Characteristic[1]	Max Operating Frequency	Unit
DDR2 memory bus frequency (MCLK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting csb_clk, MCLK, LCLK, and core_clk frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR2 data rate is 2× the DDR2 memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the lb_clk frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the csb_clk frequency (depending on RCWL[LBCM]).

23.4 System PLL configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider). The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

Table 58. System PLL multiplication factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 23, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (*SYS_CLK_IN)* and the internal coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

Table 59. CSB frequency options

SPMF	csb_clk : sys_clk_in Ratio	PCI_SYNC_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

23.5 Core PLL configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 60. e300 Core PLL configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷ 2
01	0001	1	1.5:1	÷ 4
10	0001	1	1.5:1	÷ 8
11	0001	1	1.5:1	÷ 8
00	0010	0	2:1	÷ 2
01	0010	0	2:1	÷ 4
10	0010	0	2:1	÷ 8
11	0010	0	2:1	÷ 8
00	0010	1	2.5:1	÷ 2
01	0010	1	2.5:1	÷ 4
10	0010	1	2.5:1	÷ 8
11	0010	1	2.5:1	÷ 8
00	0011	0	3:1	÷ 2

Table 60. e300 Core PLL configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
01	0011	0	3:1	÷ 4
10	0011	0	3:1	÷ 8
11	0011	0	3:1	÷ 8

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

23.6 QUICC Engine PLL configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

Table 61. QUICC Engine PLL multiplication factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in the following table.

Table 62. QUICC Engine PLL VCO divider

RCWL[CEVCOD]	VCO Divider
00	2
01	4
10	8
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

qe_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QUICC Engine VCO Frequency = *qe_clk* × VCO divider × (1 + CEPDF)

23.7 Suggested PLL configurations

To simplify the PLL configurations, the MPC8309 might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs is configured separately.

The following table shows suggested PLL configurations for 33 and 66 MHz input clocks.

Table 63. Suggested PLL configurations

Conf No.	SPMF	Core PLL	CEPMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0111	0	33.33	133.33	266.66	233
2	0010	0000100	0111	1	66.67	133.33	266.66	233
3	0100	0000101	0111	0	33.33	133.33	333.33	233
4	0101	0000101	1001	0	25	125	312.5	225
5	0010	0000101	0111	1	66.67	133.33	333.33	233
6	0100	0000110	0111	0	33.33	133.33	399.96	233
7	0101	0000110	1000	0	25	125	375	225
8	0010	0000110	0011	0	66.67	133.33	399.96	233
9	0101	0000101	0111	0	33.33	166.67	416.67	233

24 Thermal

This section describes the thermal specifications of the MPC8309.

24.1 Thermal characteristics

The following table provides the package thermal characteristics for the 369, 19 × 19 mm MAPBGA of the MPC8309.

Table 64. Package thermal characteristics for MAPBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	40	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	25	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	33	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	22	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	15	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

24.1.1 Thermal management information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

24.1.2 Estimation of junction temperature with junction-to-ambient thermal resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where,

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

24.1.3 Estimation of junction temperature with junction-to-board thermal resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \qquad \text{Eqn. 2}$$

where,

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

24.1.4 Experimental determination of junction temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \text{Eqn. 3}$$

where,

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

24.1.5 Heat sinks and junction-to-case thermal resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance as shown in the following equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

24.2 Heat sink attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint

lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

24.2.1 Experimental determination of the junction temperature with a heat sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface.

From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance using the following equation:

$$T_J = T_C + (R_{\theta JC} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

25 System design information

This section provides electrical and thermal design recommendations for successful application of the MPC8309.

25.1 System clocking

The MPC8309 includes three PLLs.

- The system PLL (AV_{DD2}) generates the system clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the system and SYS_CLK_IN is selected using the system PLL ratio configuration bits as described in Section 23.4, “System PLL configuration.”
- The e300 core PLL (AV_{DD3}) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 23.5, “Core PLL configuration.”
- The QUICC Engine PLL (AV_{DD1}) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

25.2 PLL power supply filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 46, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

The following figure shows the PLL power supply filter circuit.

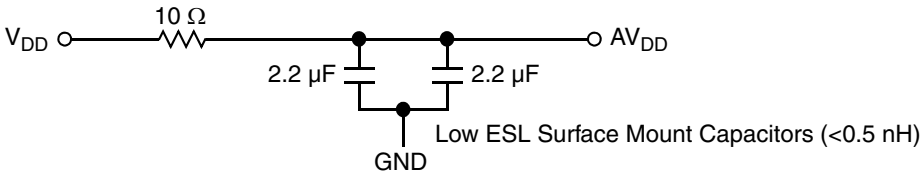


Figure 46. PLL power supply filter circuit

25.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the MPC8309 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8309 system, and MPC8309 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8309. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Output buffer DC impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 47). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

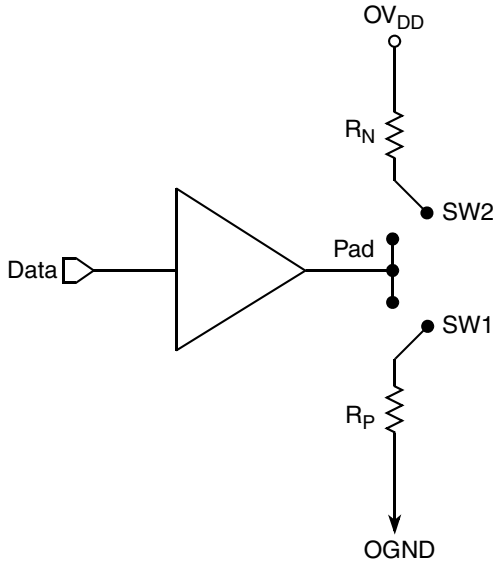


Figure 47. Driver impedance measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 65. Impedance characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration and Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	Ω
R_P	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

25.5 Configuration pin multiplexing

The MPC8309 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the "Reset, Clocking and Initialization" of *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26 Ordering information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 26.1, "Part numbers fully addressed by this document."

26.1 Part numbers fully addressed by this document

The following table provides the Freescale part numbering nomenclature for the MPC8309 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

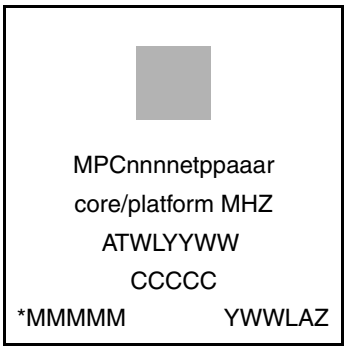
Table 66. Part numbering nomenclature

MPC	*nnnn*	*C*	*VM*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR2 Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8309	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free	AD = 266 MHz AF = 333 MHz AG = 400 MHz AH = 417MHz	D = 266 MHz F = 333 MHz	C = 233 MHz	Contact local Freescale sales office

Notes:
1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 22, "Package and pin listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

26.2 Part marking

Parts are marked as in the example shown in the following figure.



MAPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 48. Freescale part marking for MAPBGA devices

The following table shows the SVR Settings.

Table 67. SVR settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)
MPC8309	MAPBGA	0x8110_0010	0x8110_0011
Note: PVR = 0x8085_0020			

27 Document revision history

The following table provides a revision history for this document.

Table 68. Document revision history

Rev. No.	Date	Substantive Change(s)
3	04/2014	• Re-introduced Section 8.3.3, “IEEE 1588 DC Specifications and Section 8.3.4, “IEEE 1588 AC Specifications
2	09/2012	• In Table 55, swapped CLK13 and CLK14. • In Table 55, removed the following test signals, as there are no corresponding use cases: – ECID_TMODE_IN – BOOT_ROM_ADDR[2] to BOOT_ROM_ADDR[12] – BOOT_ROM_RDATA[0] to BOOT_ROM_RDATA[31] – BOOT_ROM_MOD_EN, BOOT_ROM_RWB, BOOT_ROM_XFR_WAIT, BOOT_ROM_XFR_ERR – UC1_RM, UC2_RM, UC3_RM, UC5_RM, UC7_RM, AND URM_TRIG – TPR_SYS_AAD[0] to TPR_SYS_AAD[15] – TPR_SYS_SYNC, TPR_SYS_DACK – QE_TRB_0, QE_TRB_1 – PLLCZ_CORE_CLKIN – JTAG_BISE, JTAG_PRPGPS, JTAG_BISR_TDO_EN – CLOCK_XLB_CLOCK_OUT – PD_XLB2MG_DDR_CLOCK • In Table 55, changed the following signal names as only QE-Based Fast Ethernet Controller is present in this device: – TSEC_TMR_TRIG1 to FEC_TMR_TRIG1 – TSEC_TMR_TRIG2 to FEC_TMR_TRIG2 – TSEC_TMR_CLK to FEC_TMR_CLK – TSEC_TMR_GCLK to FEC_TMR_GCLK – TSEC_TMR_PP1 to FEC_TMR_PP1 – TSEC_TMR_PP2 to FEC_TMR_PP2 – TSEC_TMR_PP3 to FEC_TMR_PP3 – TSEC_TMR_ALARM1 to FEC_TMR_ALARM1 – TSEC_TMR_ALARM2 to FEC_TMR_ALARM2 – FEC3_TMR_TX_ESFD to FEC2_TMR_TX_ESFD – FEC3_TMR_RX_ESFD to FEC2_TMR_RX_ESFD. • In Table 18, added parameteres $t_{LALEHOV}$,, $t_{LALETOT}$, and t_{LBOTOT} and made the corresponding updates in Figure 8 • In Figure 3, replaced "32 X tSYS_CLK_IN" with "32 X tSYS_CLK_IN/PCI_SYNC_IN.
1	08/2011	• Updated QUICC Engine frequency in Table 5. • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 63. • Updated CEPMF and CEDF as per new QE frequency in Table 63. • Updated QUICC Engine frequency to 233 MHz in Table 66. • Corrected LCCR to LCRR for all instances.
0	03/2011	Initial Release.

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