MC3424, MC3424A
MC3524, MC3524A
MC3324, MC3324A

Advance Information

POWER SUPPLY SUPERVISORY CIRCUIT/DUAL VOLTAGE COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

POWER SUPPLY SUPERVISORY CIRCUIT/ DUAL-VOLTAGE COMPARATOR

The MC3424 series is a dual-channel supervisory circuit, consisting of two uncommitted input comparators, a reference, output comparators, with high current Drive and Indicator outputs for each channel. The input comparators feature programmable hysteresis, high common-mode rejection, and wide common-mode range, capable of comparing at ground potential with single-supply operation. Separate Delay pins are provided to increase noise immunity by delaying activation of the outputs. A 2.5 V bandgap voltage reference is pinned-out for referencing the input comparators, or other external functions. Independent high current Drive and Indicator outputs for each channel can source and sink up to 300 mA and 30 mA respectively. CMOS/TTL compatible digital inputs provide Remote Activation of each channel's outputs. An Input Enable pin allows control of the input comparators.

Although this device is intended for power supply supervision, the pinned-out reference, uncommitted input comparators, and many other features, enable the MC3424 series to be utilized for a wide range of applications.
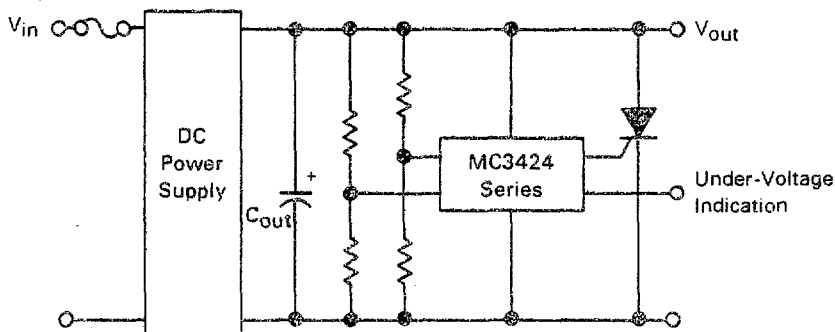
- Pinned-Out 2.5 V Reference
- Wide Common-Mode Range
- Programmable Hysteresis
- Programmable Time Delays
- Two 300 mA Drive Outputs
- Remote Activation Capability
- Wide Supply Range: $4.5 \text{ V} \leqslant V_{CC} \leqslant 40 \text{ V}$

APPLICATIONS
- Dual Over-Voltage "Crowbar" Protection
- Dual Under-Voltage Supervision
- Over/Under Voltage Protection
- Split-Supply Supervision
- Line-Loss Sensing
- Proportional Controller
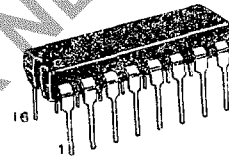- Programmable Frequency Switch
- Battery Charger

P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS

V_{ref} [1]	[16] IE
Enable Select1/C1+ [2]	[15] C2+
C1– [3]	[14] C2–
DLY1 [4]	[13] DLY2
$\overline{RA1}$ [5]	[12] $\overline{RA2}$
IND1 [6]	[11] IND2
Gnd [7]	[10] DRV2
DRV1 [8]	[9] V_{CC}

(Top View)

TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication
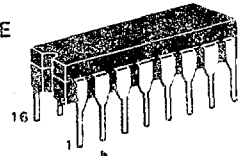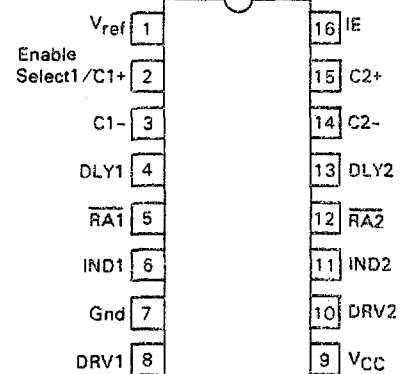
ORDERING INFORMATION

Device	Temperature Range	Package
MC3524L, AL	–55 to +125°C	Ceramic DIP
MC3324L, AL	–40 to +85°C	Ceramic DIP
MC3324P, AP		Plastic DIP
MC3424L, AL	0 to +70°C	Ceramic DIP
MC3424P, AP		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI-594R1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Differential Voltage Range	V_{IDR}	±40	Vdc
Comparator Input Voltage Range	V_{IR}	–0.3 to +40	Vdc
Input Enable Voltage Range	V_{IE}	–0.3 to +40	Vdc
Remote Activation Input Voltage Range	V_{RA}	–0.3 to +40	Vdc
Drive Output Short-Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Reference Short-Circuit Current	$I_{OS(ref)}$	Internally Limited	mA

Power Dissipation and Thermal Characteristics
Ceramic Package
  Maximum Power Dissipation @ T_A = 95°C
  Thermal Resistance Junction to Air
Plastic Package
  Maximum Power Dissipation @ T_A = 70°C
  Thermal Resistance Junction to Air
	
	P_D
	$R_{\theta JA}$
	
	P_D
	$R_{\theta JA}$
		
		1000
		80
		
		1000
		80
			
			mW
			°C/W
			
			mW
			°C/W

Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C
Operating Ambient Temperature Range MC3524, MC3524A MC3324, MC3324A MC3424, MC3424A	T_A	 –55 to +125 –40 to +85 0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +175 –55 to +150	°C

ELECTRICAL CHARACTERISTICS
(4.5 V $\leq V_{CC} \leq$ 40 V; $T_A = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3524A/3424A/3324A			MC3524/3424/3324			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								

Reference Output Voltage
  V_{CC} = 15V; I_L = 0 mA
    T_A = 25°C
    T_{low} to T_{high} (Note 1)
	V_{ref}	
		
		2.475
		2.45
			
			2.5
			2.5
				
				2.525
				2.55
					
					2.4
					2.33
						
						2.5
						2.5
							
							2.6
							2.63
								Vdc

Line Regulation 4.5 V $\leq V_{CC} \leq$ 40 V; I_L = 0 mA; T_J = 25°C	Reg_{line}	—	7.0	15	—	7.0	15	mV

Load Regulation
  0 mA $\leq I_L \leq$ 10 mA; V_{CC} = 15 V;
  T_J = 25°C
	Reg_{load}	—	4.0	12	—	4.0	12	mV

Output Short-Circuit Current (T_A = 25°C)	$I_{OS(ref)}$	—	23	—	—	23	—	mA
Power Supply Voltage Operating Range	V_{CC}	4.5	—	40	4.5	—	40	Vdc

Power Supply Current
  V_{CC} = 40 V; T_A = 25°C; No Output Loads
    V_{C1-}, V_{C2-} = V_{CC};
    V_{C1+}, V_{C2+} = 0 V
	$I_{CC(off)}$	—	12	15	—	12	15	mA

V_{C1+}, V_{C2+} = V_{CC}; V_{C1-}, V_{C2-} = 0 V	$I_{CC(on)}$	—	27	32	—	27	32	mA

NOTES:
(1) T_{low} = –55°C for MC3524, MC3524A T_{high} = +125°C for MC3524, MC3524A
        = –40°C for MC3324, MC3324A   = +85°C for MC3324, MC3324A
        = 0°C for MC3424, MC3424A   = +70°C for MC3424, MC3424A

(2) The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 300 mV. The upper functional limit of the common-mode voltage range is typically V_{CC} –1.4 volts; but either or both inputs can go to 40 volts, independent of V_{CC}, without device destruction.

(3) The $V_{th(ES1)}$ limits are approximately 0.5 times the V_{ref} limits over the applicable temperature range.

(4) The $V_{th(OC)}$ limits are approximately the V_{ref} limits over the applicable temperature range.

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ELECTRICAL CHARACTERISTICS (4.5 V $\leq V_{CC} \leq$ 40 V; $T_A = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	MC3524A/3424A/3324A			MC3524/3424/3324			Unit
		Min	Typ	Max	Min	Typ	Max	
INPUT SECTION								
Input Offset Voltage	V_{IO}							mV
T_A = 25°C		—	±3.0	±8.0		±5.0	±10	
T_{low} to T_{high} (Note 1)		—	±3.0	±12		±5.0	±15	
Input Offset Current	I_{IO}							nA
T_A = 25°C		—	±3.0	±25	—	±3.0	±25	
T_{low} to T_{high} (Note 1)		—	±3.0	±250	—	±3.0	±250	
Input Bias Current	I_{IB}							nA
T_A = 25°C		—	50	250	—	50	250	
T_{low} to T_{high} (Note 1)		—	500	1000	—	500	1000	
Comparator Input Functional Common Mode Range (T_A = 25°C, Note 2)	V_{ICR}	-0.1	V_{CC}-1.4	—	-0.1	V_{CC}-1.4	—	V
Hysteresis Activation Voltage V_{CC} = 15 V; V_{C1+}, V_{C2+} = V_{CC}; T_A = 25°C	$V_{H(act)}$							V
I_H = 10%		—	1.2	—		1.2		
I_H = 90%		—	1.4	—		1.4		
Hysteresis Current V_{CC} = 15 V; V_{C1-}, V_{C2-} = 2.5 V; V_{C1+}, V_{C2+} = V_{CC}; T_A = 25°C	I_H	10	12.5	15	9.0	12.5	16	μA
Common Mode Rejection Ratio	CMRR	60	72	—	60	72	—	dB
Power Supply Rejection Ratio	PSRR	—	95	—	—	95	—	dB
Input Enable Threshold (Pin 16; Note 3)	$V_{th(IE)}$	0.9	1.4	1.9	0.9	1.4	1.9	V
Input Enable Current (Pin 16)								μA
$V_{IL(IE)}$ = 0 V	$I_{IL(IE)}$	—	-0.5	-2.5	—	-0.5	-2.5	
$V_{IH(IE)}$ = 40 V	$I_{IH(IE)}$	—	0.05	1.0	—	0.05	1.0	
Enable Select 1 Threshold Voltage (Pin 2)	$V_{th(ES1)}$	2.2	2.25	2.3	2.1	2.25	2.4	V
Delay Pin Voltage (I_{DLY} = 0 mA)								V
Low State	$V_{OL(DLY)}$	—	0.2	0.5	—	0.2	0.5	
High State	$V_{OH(DLY)}$	V_{CC}-0.5	V_{CC}-0.15	—	V_{CC}-0.5	V_{CC}-0.15	—	
Delay Pin Source Current V_{CC} = 15 V; V_{DLY1}, V_{DLY2} = 0 V	$I_{DLY(source)}$	150	200	250	140	200	260	μA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY1}, V_{DLY2} = 2.5 V	$I_{DLY(sink)}$	1.8	3.0	—	1.8	3.0	—	mA
OUTPUT SECTION								
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	—	200	300	—	mA
Drive Output V (I_{DRV} = 100 mA; T_A = 25°C)	$V_{OH(DRV)}$	V_{CC}-2.5	V_{CC}-2.0	—	V_{CC}-2.5	V_{CC}-2.0	—	V
Drive Output Leakage Current (V_{DRV} = 0 V)	$I_{DRV(leak)}$	—	15	200	—	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	—	2.0	—	A/μS
Drive Output Transient Rejection (T_A = 25°C) V_{CC} = 0 V to 15 V at dV/dt = 200 V/μs; V_{C1-}, V_{C2-} = V_{ref}; V_{C1+}, V_{C2+} = 0 V	$I_{DRV(trans)}$	—	1.0	—	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	—	560	800	—	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	—	25	200	—	25	200	nA
Output Comparator Threshold V (Note 4)	$V_{th(OC)}$	2.46	2.5	2.55	2.33	2.5	2.63	V
Remote Activation Threshold Voltage	$V_{th(RA)}$	1.3	1.4	1.5	1.1	1.4	1.7	V
Remote Activation Current								μA
$V_{IL(RA)}$ = 0 V	$I_{IL(RA)}$	—	-100	-250	—	-100	-250	
$V_{IH(RA)}$ = 40 V	$I_{IH(RA)}$	—	70	250	—	70	250	
Propagation Delay (V_{CC} = 15 V; T_A = 25°C) Input to Drive Output 100 mV Overdrive, C_{DLY} = 0 μF	$t_{PLH(IN/DRV)}$	—	1.0	—	—	1.0	—	μS
Remote Activation to Drive Output 1.4 V Overdrive (2.5 V to 0 V Step)	$t_{PLH(RA/DRV)}$	—	600	—	—	600	—	ns

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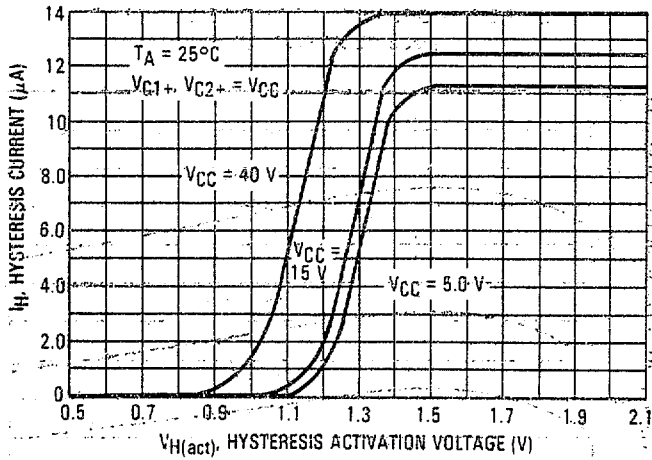**FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE**

FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE
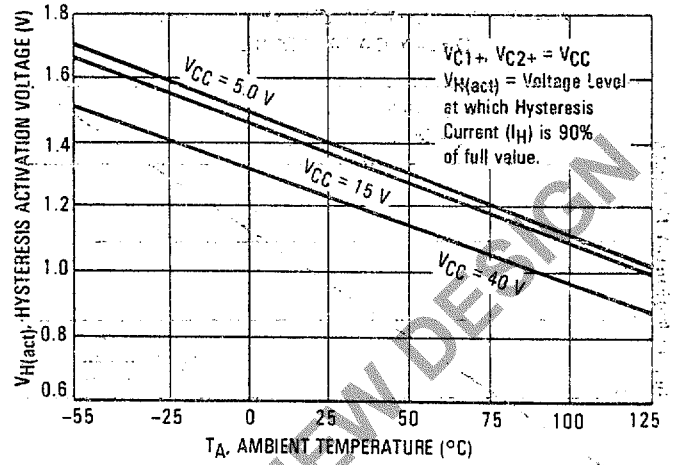

FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE
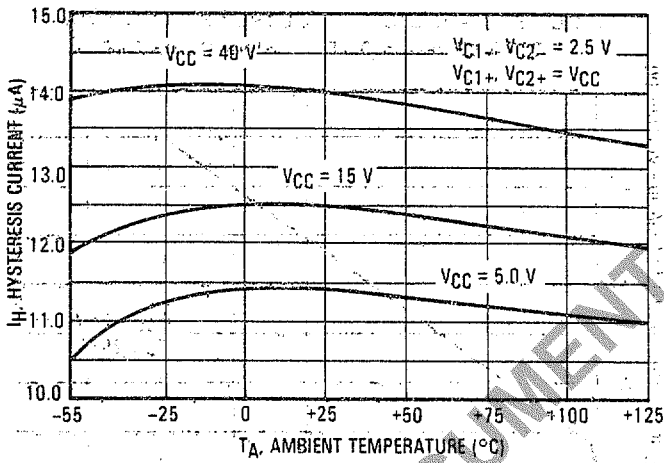

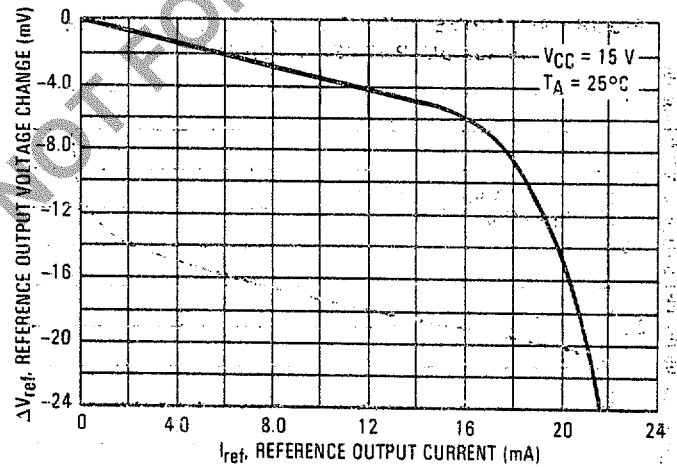**FIGURE 4 — REFERENCE VOLTAGE CHANGE versus OUTPUT CURRENT**

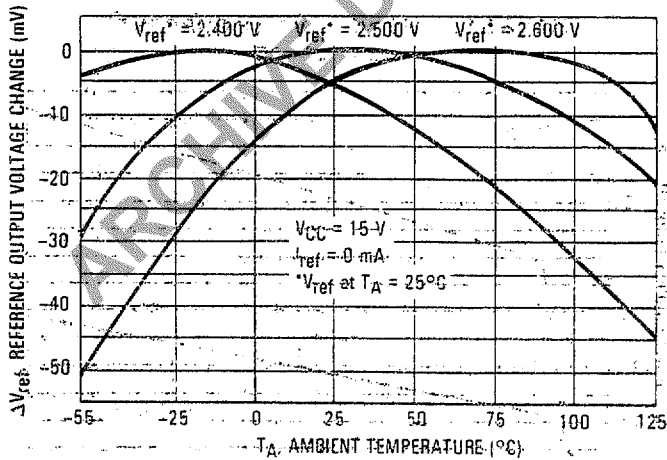**FIGURE 5 — REFERENCE VOLTAGE CHANGE versus TEMPERATURE**

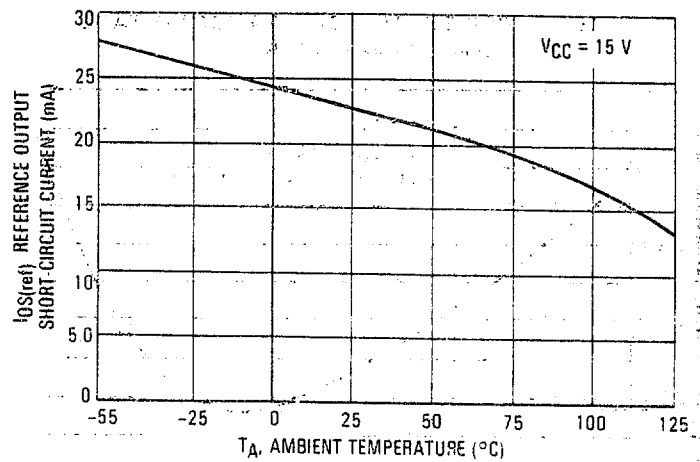**FIGURE 6 — REFERENCE SHORT-CIRCUIT CURRENT versus TEMPERATURE**

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FIGURE 7 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

V_{CC} = 15 V
T_A = 25°C

$$t_{DLY} = \frac{2.5\ C_{DLY}}{200\ \mu A}$$

t_{DLY}, OUTPUT DELAY TIME (mS)

C_{DLY}, DELAY PIN CAPACITANCE (μF)
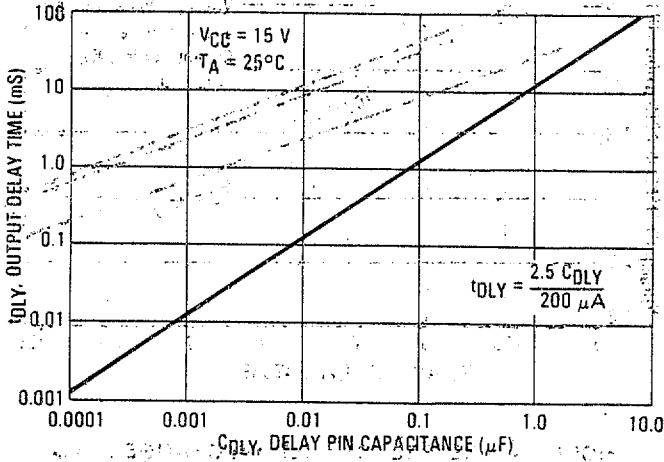
FIGURE 8 — DELAY PIN SOURCE CURRENT versus TEMPERATURE

V_{CC} = 40 V

V_{CC} = 15 V

V_{CC} = 5.0 V

$I_{DLY(source)}$, DELAY PIN SOURCE CURRENT (μA)

T_A, AMBIENT TEMPERATURE (°C)
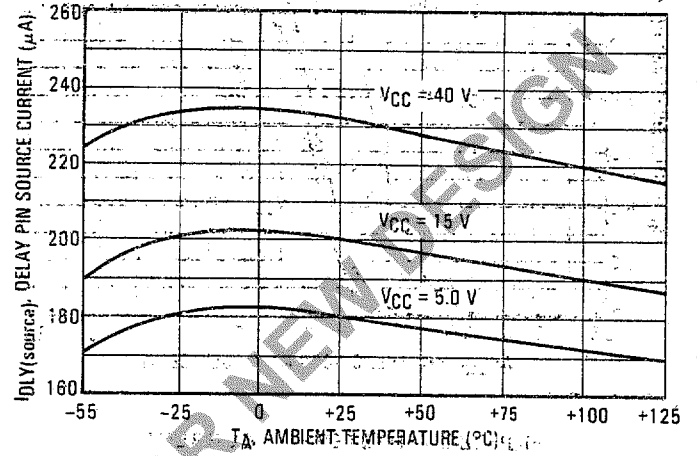
FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT

V_{CC} = 15 V
1.0% Duty Cycle @ 300 Hz
T_A = 25°C

$V_{OH(DRV)}$, DRIVE OUTPUT SATURATION VOLTAGE (V)

$I_{DRV(peak)}$, DRIVE OUTPUT PEAK CURRENT (mA)
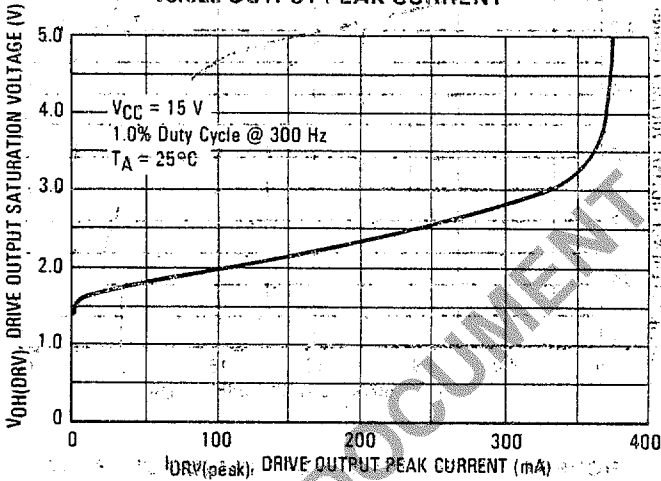
FIGURE 10 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

V_{CC} = 15 V
T_A = 25°C

$V_{IND(sat)}$, INDICATOR OUTPUT SATURATION VOLTAGE (V)

I_{IND}, INDICATOR OUTPUT SINK CURRENT (mA)
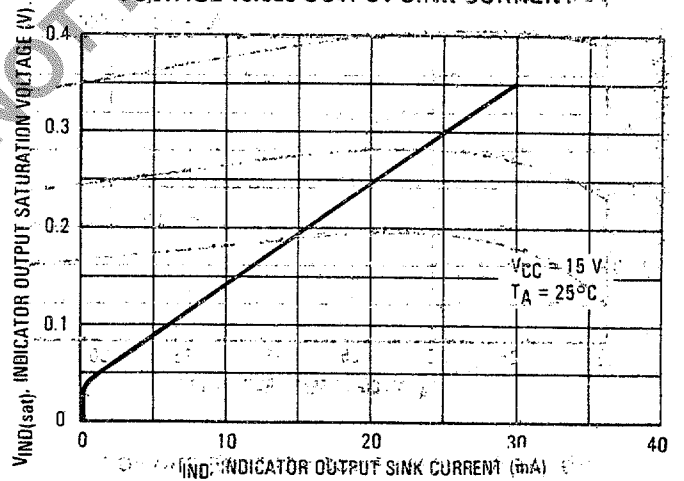
FIGURE 11 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

V_{CC} = 15 V
$I_{DRV(peak)}$ = 200 mA
1.0% Duty Cycle @ 300 Hz

$V_{OH(DRV)}$, DRIVE OUTPUT SATURATION VOLTAGE (V)

T_A, AMBIENT TEMPERATURE (°C)
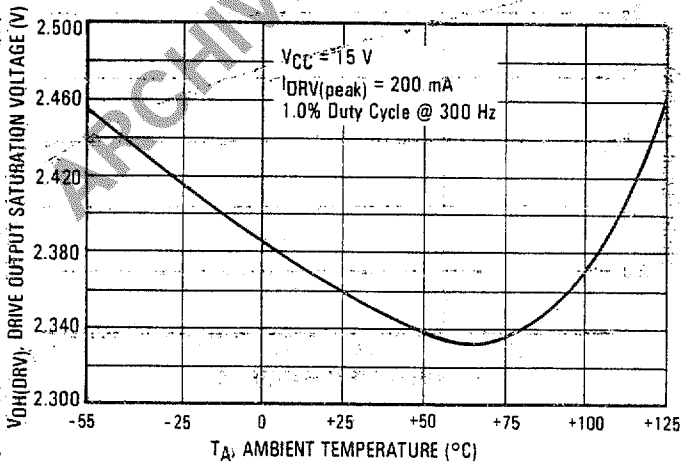
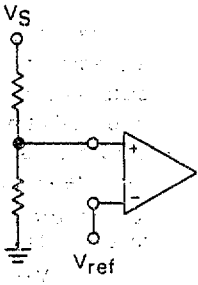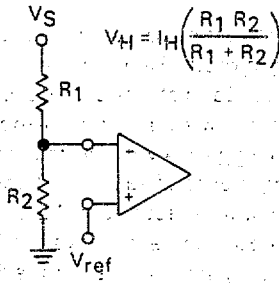## FIGURE 12 — POWER SUPPLY CURRENT versus VOLTAGE

CURVE	$V_{C1}+$, $V_{C2}+$	$V_{C1}-$, $V_{C2}-$
A	V_{CC}	Gnd
B	Gnd	V_{CC}

A

B

T_A = 25°C

I_{CC}, POWER SUPPLY CURRENT (mA)

V_{CC}, POWER SUPPLY VOLTAGE (V)

(M) **MOTOROLA** *Semiconductor Products Inc.*
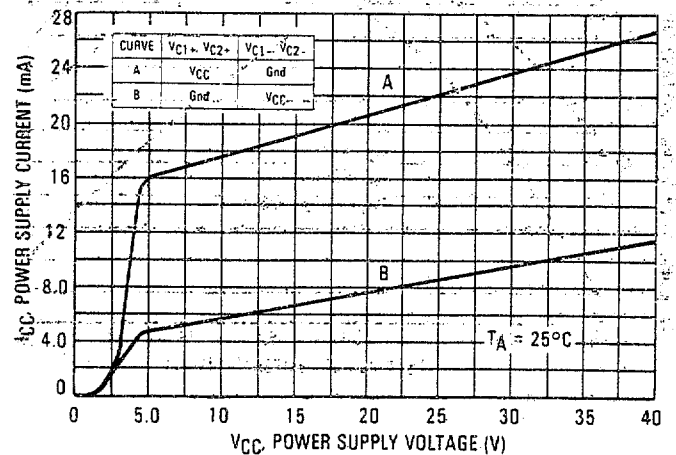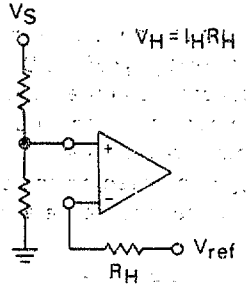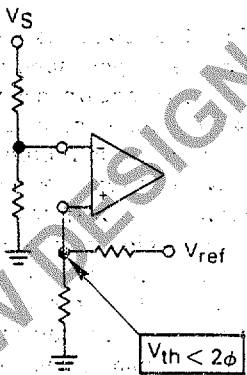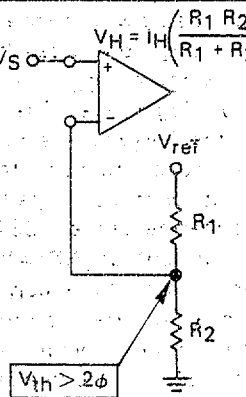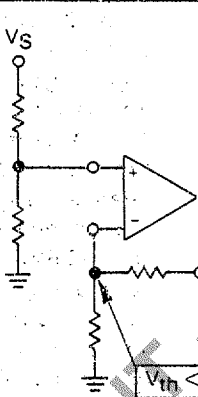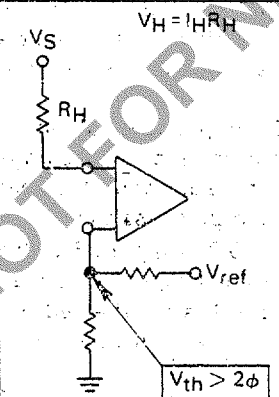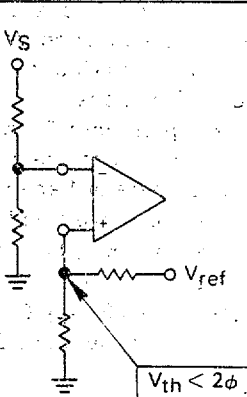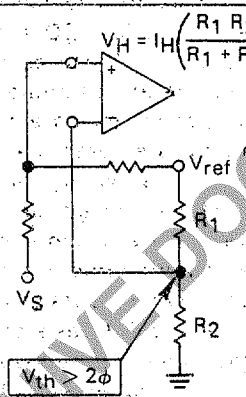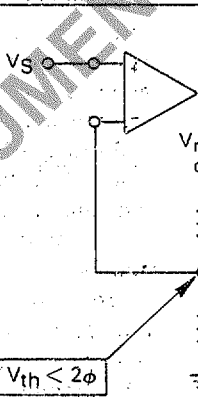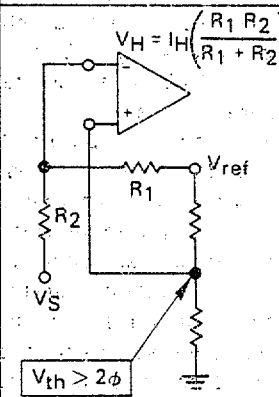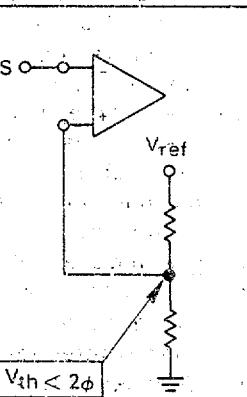
FIGURE 13 — THE COMPLETE VOLTAGE SENSE CAPABILITY OF THE INPUT COMPARATORS, WITH OR WITHOUT PROGRAMMABLE HYSTERESIS.

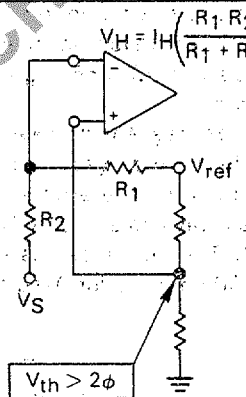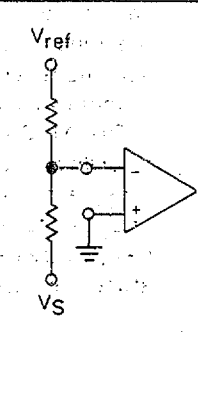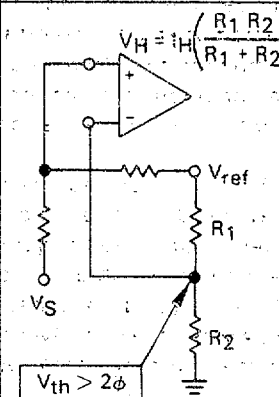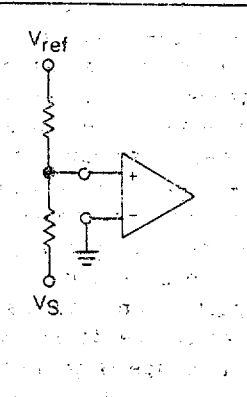| VOLTAGE SENSE (V_S)			
OVER		UNDER	
WITH HYSTERESIS	WITHOUT HYSTERESIS	WITH HYSTERESIS	WITHOUT HYSTERESIS
$V_S > V_{ref}$ — $V_H = I_H R_H$; R_H, V_{ref}	V_S; V_{ref}	V_S; R_1, R_2; $V_H = I_H\left(\dfrac{R_1 R_2}{R_1 + R_2}\right)$; V_{ref}	V_S; V_{ref}; $V_{th} < 2\phi$
$V_S \leqslant V_{ref}$ $V_S \geqslant 2\phi^*$ — $V_H = I_H\left(\dfrac{R_1 R_2}{R_1 + R_2}\right)$; V_{ref}, R_1, R_2; $V_{th} > 2\phi$	V_S; V_{ref}; $V_{th} < 2\phi$	V_S; R_H; $V_H = I_H R_H$; V_{ref}; $V_{th} > 2\phi$	V_S; V_{ref}; $V_{th} < 2\phi$
$V_S < 2\phi^*$ $V_S \geqslant 0\,V$ — $V_H = I_H\left(\dfrac{R_1 R_2}{R_1 + R_2}\right)$; V_{ref}, R_1, R_2, V_S; $V_{th} > 2\phi$	V_S; V_{ref}; R_2; $V_{th} < 2\phi$	$V_H = I_H\left(\dfrac{R_1 R_2}{R_1 + R_2}\right)$; R_1, R_2, V_{ref}, V_S; $V_{th} > 2\phi$	V_S; V_{ref}; $V_{th} < 2\phi$
$V_S < 0\,V$ — $V_H = I_H\left(\dfrac{R_1 R_2}{R_1 + R_2}\right)$; V_{ref}, R_1, R_2, V_S; $V_{th} > 2\phi$	V_{ref}; V_S	$V_H = I_H\left(\dfrac{R_1 R_2}{R_1 + R_2}\right)$; V_{ref}, R_1, R_2, V_S; $V_{th} > 2\phi$	V_{ref}; V_S

*$2\phi \simeq 1.1$ Volts at $T_J = 25°C$

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CIRCUIT DESCRIPTION

The MC3424 series is a high-current output, dual channel power supply supervisory circuit. Basic circuit configuration is shown in Figure 29. Each channel features a true differential input comparator with a common-mode range from ground potential to V_{CC} - 1.4 volts, with single supply operation. The inverting inputs of each input comparator (C1-, C2-) have a feedback activated 12.5 μA current sink for programming input comparator hysteresis. Source resistance of the inverting inputs determines the amount of hysteresis for each input comparator. The hysteresis feature can be defeated by reducing the inverting input voltage of the respective input comparator to less than two diode drops (2 $\phi \cong$ 1.1 volts) above Gnd (See Hysteresis Activation Voltage specification). A complete matrix of various input comparator conditions is shown in Figure 13 on page 6.

The digital Input Enable (IE) pin provides full enable/disable control of one or both of the input comparators. Input Comparator 1 enable control is allowed if the Enable Select 1/Non-Inverting Input (pin 2) is less than 90% of the internal 2.5 volts reference (0.9 $V_{ref} \cong$ 2.25 V). If the Input Enable Select 1/Non-Inverting Input (pin 2) is greater than 0.9 V_{ref}, Comparator 1 is not affected by the logic state of the Input Enable pin and always remains enabled.

The voltage threshold of the Input Enable pin is TTL-compatible. A logic level "1" permits normal operation of input comparators, as stated above. A logic "0" forces the respective Delay pin (DLY1, DLY2) to a low state, independent of the input comparator's state.

The selective enabling feature of Input Comparator 1 is directly applicable when the MC3424 series is used as an over- and under-voltage supervisory circuit, where channel 2 (Input Comparator 2) is monitoring under-voltage conditions, and channel 1 is utilized for over-voltage protection. The ability to keep channel 1 (Input Comparator 1) active, while disabling channel 2, provides immediate over-voltage protection during power supply turn-on, while the under-voltage channel (2) can be disabled during the power supply turn-on rise time to the regulated level, preventing false indication of an under-voltage condition. If it is desired to monitor two independent voltages for an under-voltage condition, both channels can be selectively disabled until the slowest supply reaches its regulated voltage.

Separate Delay pins (DLY1, DLY2) are provided for each channel to independently delay the Drive and Indicator Outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source of typically 200 μA when the non-inverting input voltage is greater than the inverting-input level ($V_{C1+} > V_{C1-}$; $V_{C2+} > V_{C2-}$).

A capacitor (C_{DLY}) tied to these Delay pins will establish a predictable delay time (t_{DLY}) of the Drive and Indicator outputs for the respective channel. The Delay pins are internally tied to the non-inverting input of Output Comparators 1 and 2, which are referenced to 2.5 volts. Therefore, delay time (t_{DLY}) is based on the constant current $I_{DLY(source)}$ charging the external delay capacitor (C_{DLY}) to 2.5 volts or:

$$t_{DLY} = \frac{V_{ref} \, C_{DLY}}{I_{DLY(source)}} = \frac{2.5 \, C_{DLY}}{200 \, \mu A} = 12500 \, C_{DLY}.$$

Figure 7 provides C_{DLY} values for a wide range of time delays.

The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input ($V_{C1+} < V_{C1-}$; $V_{C2+} < V_{C2-}$), or when the Input Enable pin is at a low logic level. The sink current ($\geq$ 1.8 mA) capability of the Delay pins is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

Each independent channel of the MC3424 series has a Drive (DRV) and Indicator output (IND) which respectively source and sink current simultaneously. The Drive outputs are current-limited emitter-followers capable of sourcing 300 mA at a turn-on slew rate of 2.0A/μS, ideal for driving "Crowbar" SCR's. The Indicator outputs are open-collector, NPN transistors, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or regular shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

Separate TTL-compatible Remote Activation inputs ($\overline{RA1}$, $\overline{RA2}$) for each channel will activate the Drive and Indicator outputs of the respective channel, independent of the input comparator state, when a low logic level is applied. The active low for remote activation permits latching of the respective outputs by connecting the Indicator output, via a $\leq$ 5.0 K resistor to the Remote Activation input of the same channel, as shown in Figure 17. Latching will now occur by either of the Remote Activation inputs with a short duration low logic level, or by the input comparators. Unlatching of each channel is accomplished with a short duration, high logic level at the Remote Activation pin.

The MC3424 series has an internal 2.5 V bandgap reference capable of sourcing up to 10 mA of load current for external bias circuits. This reference has an accuracy of ±4.0% for the basic devices and ±1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

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CROWBAR SCR CONSIDERATIONS

Referring to Figure 14, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 14A, the supply's input filter capacitors. This surge current is illustrated in Figure 15, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading.

Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast <1.0 μs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times I_{GT} and < 1.0 μs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 16. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 14 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

14A — SCR ACROSS INPUT OF REGULATOR

14B — SCR ACROSS OUTPUT OF REGULATOR

*Needed if supply not current limited

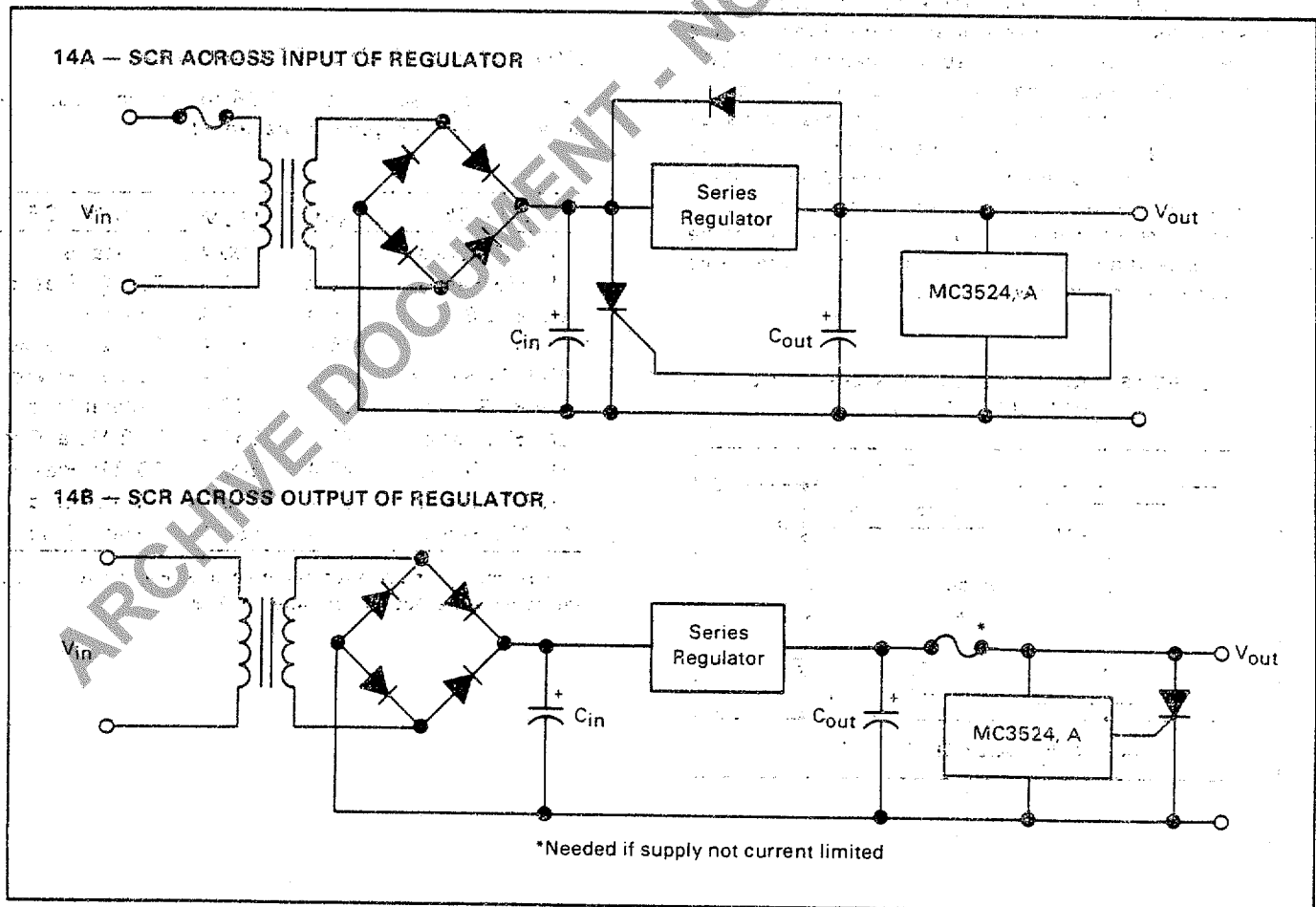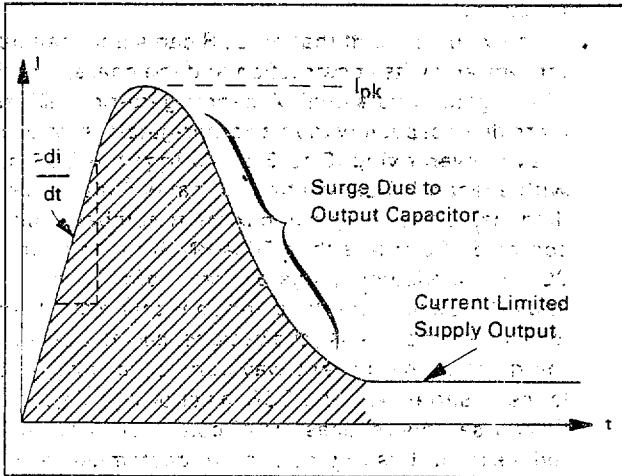**MOTOROLA** *Semiconductor Products Inc.*

FIGURE 15 — CROWBAR SCR SURGE CURRENT WAVEFORM

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 16) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 16 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt

R & L EMPIRICALLY DETERMINED
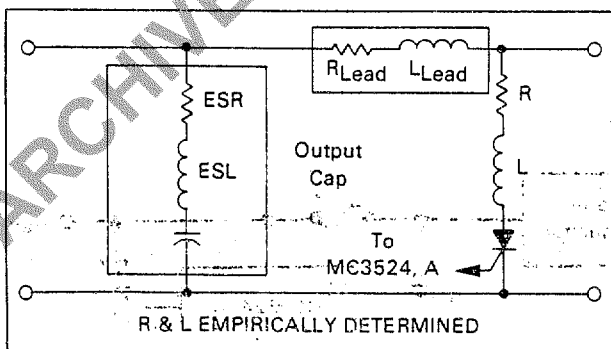
A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 14A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 14B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

APPLICATIONS INFORMATION

FIGURE 17 — OVERVOLTAGE PROTECTION OF SPLIT SUPPLIES WITH DELAY AND LATCHED-FAULT INDICATION.
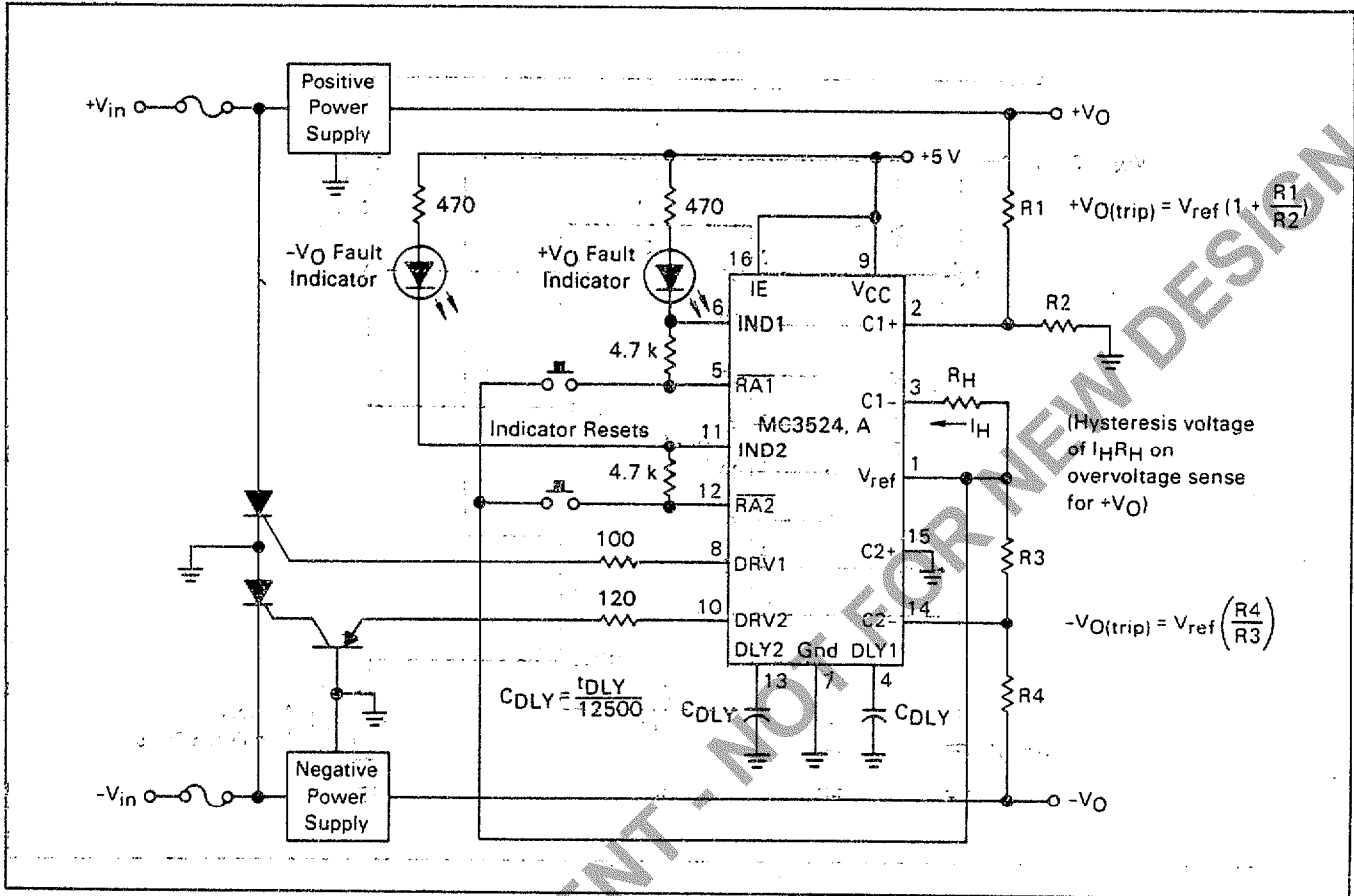

$$+V_{O(trip)} = V_{ref}\left(1 + \frac{R1}{R2}\right)$$

(Hysteresis voltage of $I_H R_H$ on overvoltage sense for $+V_O$)

$$-V_{O(trip)} = V_{ref}\left(\frac{R4}{R3}\right)$$

$$C_{DLY} = \frac{t_{DLY}}{12500}$$

FIGURE 18 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

$V_O = 5.0$ V

$V_{O(trip)} = 6.25$ V

Line Loss Output

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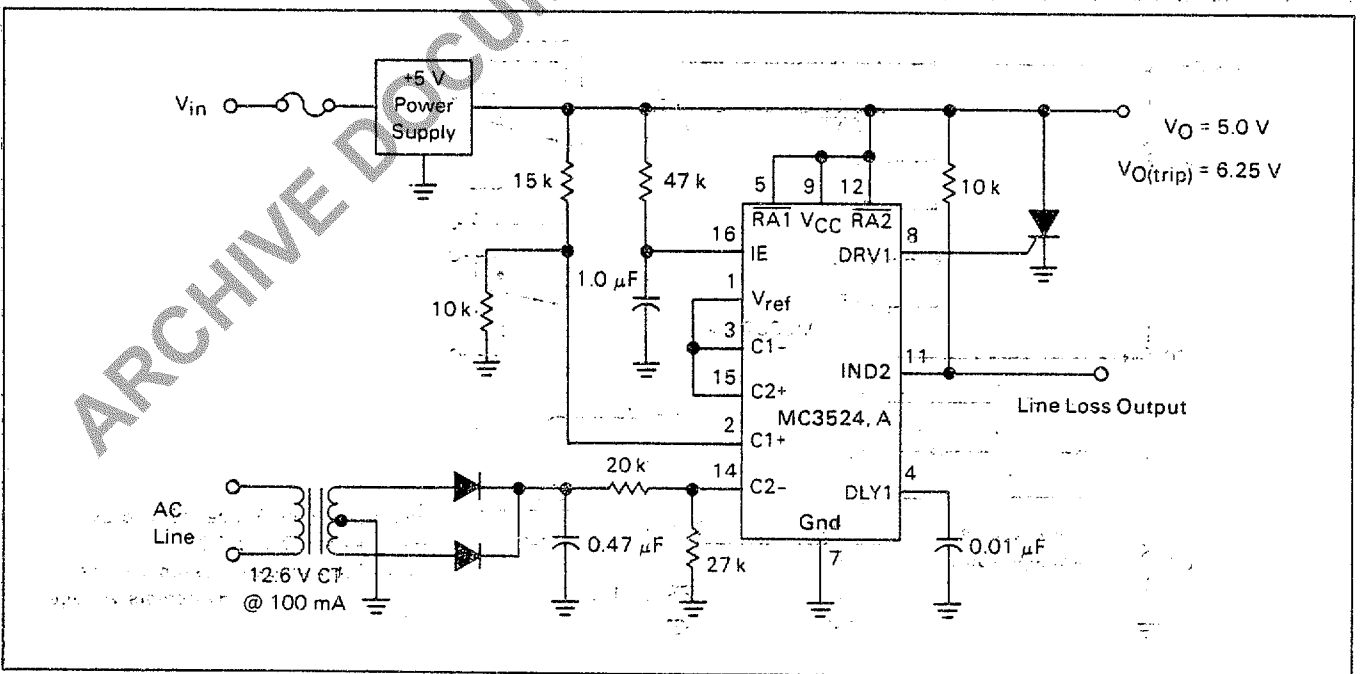
**FIGURE 19 — LATCHING OVERVOLTAGE SENSING CIRCUIT
WITH INTERMITTENT AUDIO ALARM**
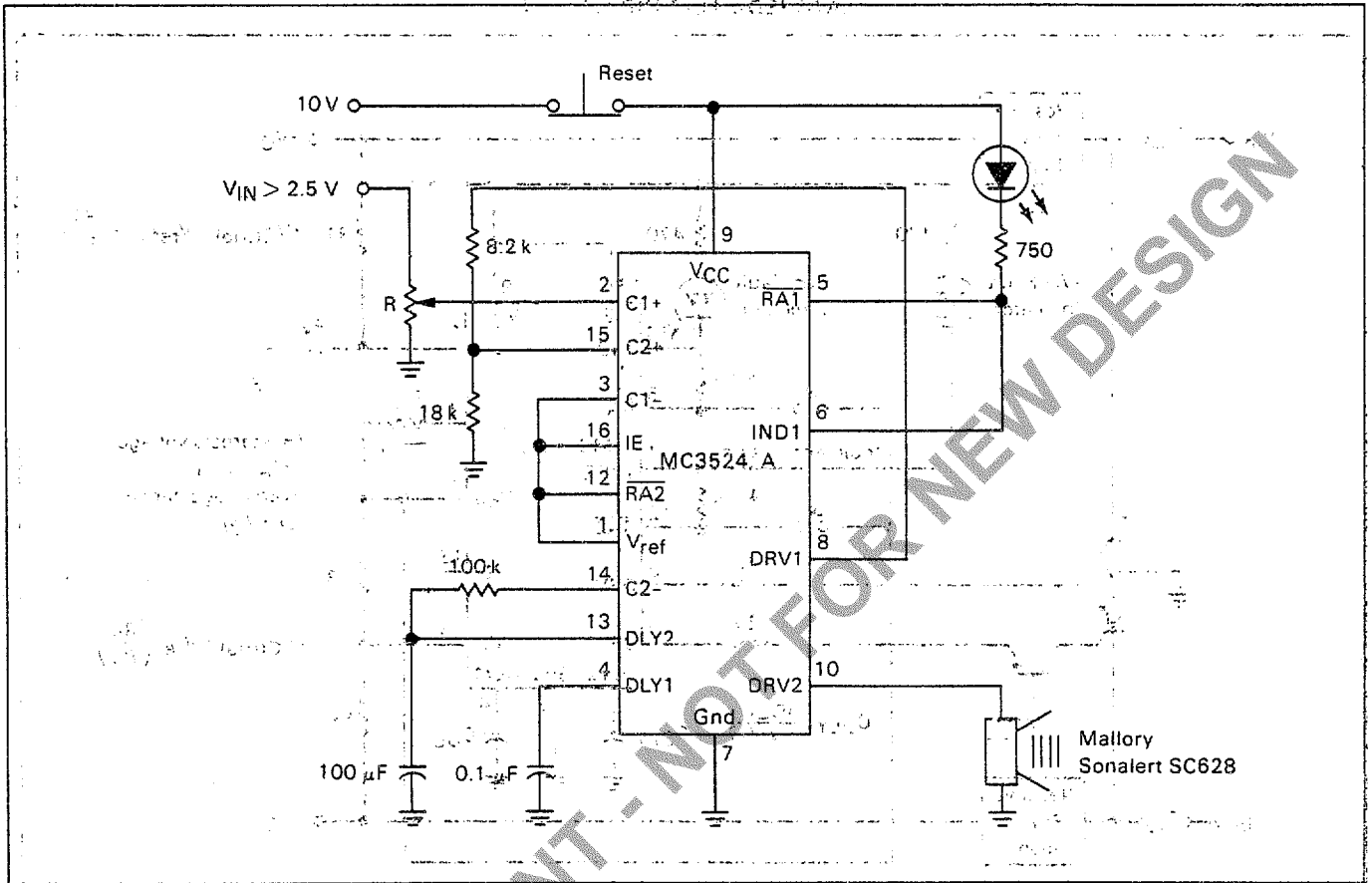
FIGURE 20 — ADJUSTABLE D.C. PICK-UP/DROP-OUT RELAY CIRCUIT

Pick-up Voltage Range: 19 V to 29 V
Hysteresis: 2.0 V to 7.0 V
Drop-Out Voltage = Pick-up Voltage −
                                          Hysteresis Voltage

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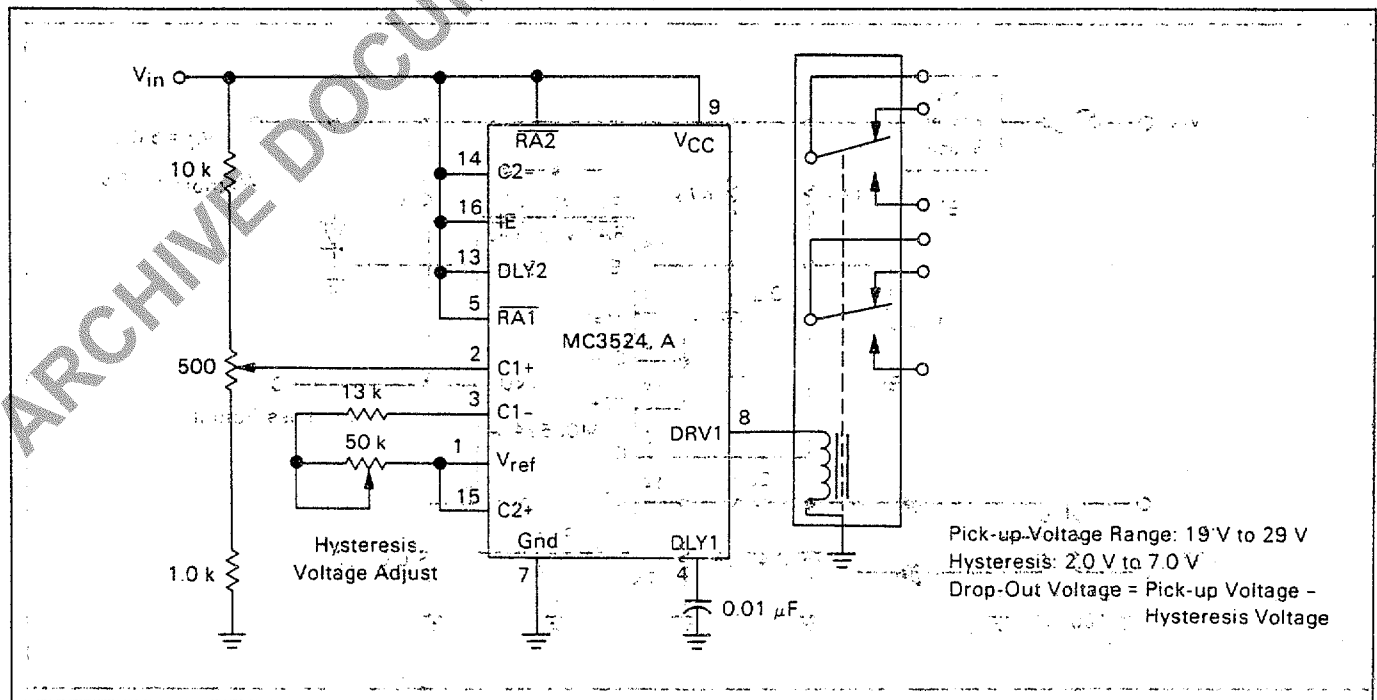
FIGURE 21 — 9.0 V BATTERY CHARGER with ZERO SENSE LOAD CURRENT

The 8.8 volt charge reference is derived from V_{ref} using comparator 2 as an op amp. The $I_H R_H$ product determines the final charge voltage. Resistor R_1 limits the charge current.

$$I_{chg} \simeq \frac{V_{CC} - V_{bat}}{R_1} \simeq \frac{3.0\ V}{R_1}$$

$I_H R_H = 200\ mV$

FIGURE 22 — PROPORTIONAL CONTROL CIRCUIT

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FIGURE 23 — ALTERNATING TWO TONE GENERATOR
(EUROPEAN SIREN)

FIGURE 24 — TONE BURST GENERATOR

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FIGURE 25 — PHOTOFLASH CONVERTER

T1: 30:1 Step up
L_{pin} = 80 μH

T2: Triad PL-10

FIGURE 26 — PROGRAMMABLE FREQUENCY SWITCH

Frequency indicator on when input signal frequency $<$ $f_{(trip)}$

$$f_{(trip)} = \frac{1}{25000\, C_{DLY}\,1}$$

$$C_{DLY}\,2 = 100\, C_{DLY}\,1$$

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1. Battery charge current ≈ 0.6 A. Charger will cycle OFF at 6.6 V, ON at 6.4 V.

2. Lamp is ON with loss of ac and battery voltage ≥ 5.7 V. As battery discharges to < 5.3 V, lamp will turn OFF.

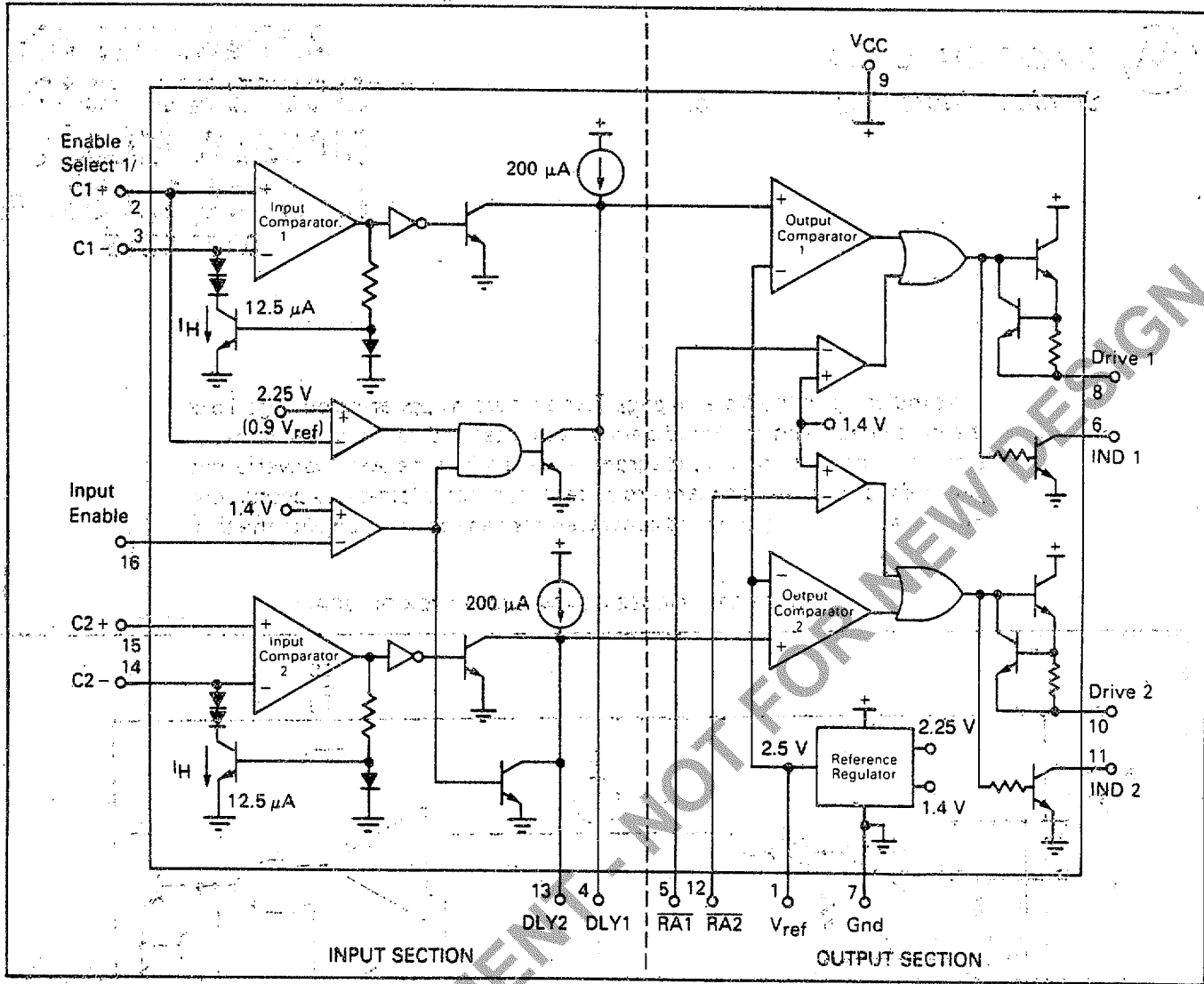**FIGURE 28 — REFERENCE TEMPERATURE COEFFICIENT MODIFICATIONS**

All diodes are 1N4001
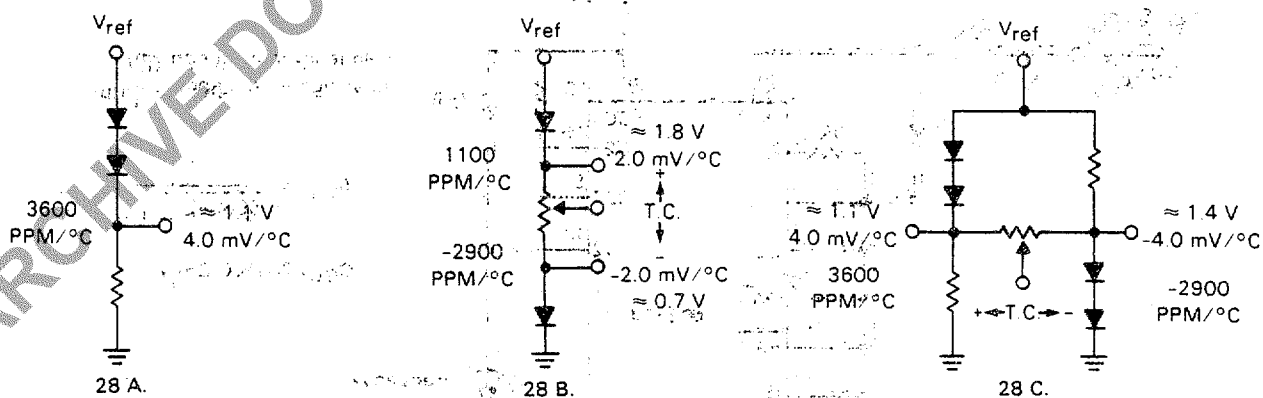
28 A. Fixed positive T.C.
28 B. Variable positive or negative T.C.
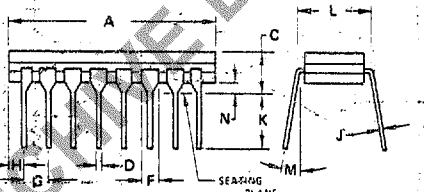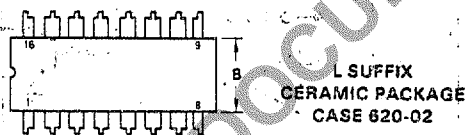28 C. Variable positive or negative T.C. with almost constant voltage.
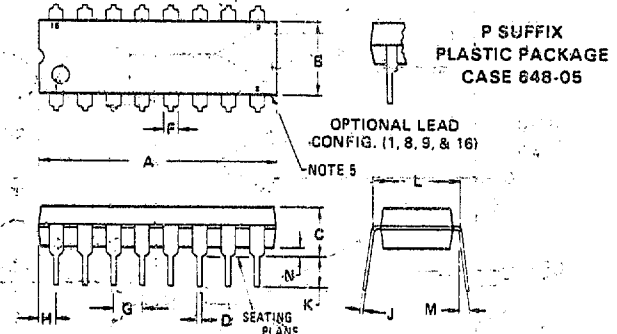
FIGURE 29 — MC3524/3424/3324 BLOCK DIAGRAM

Note: All voltages and currents are nominal.

L SUFFIX CERAMIC PACKAGE CASE 620-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

P SUFFIX PLASTIC PACKAGE CASE 648-05

OPTIONAL LEAD CONFIG. (1, 8, 9, & 16)
NOTE 5

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

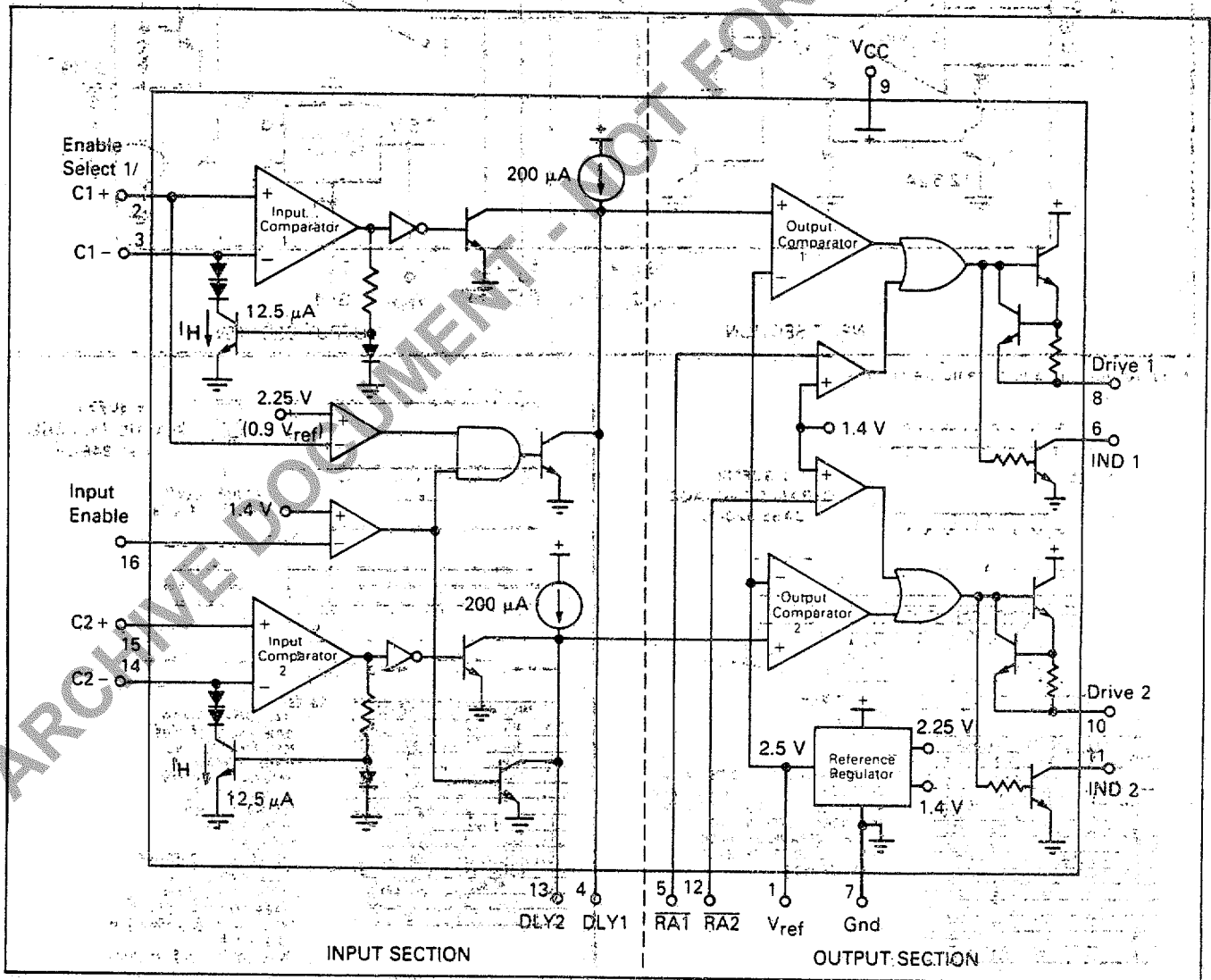## MOTOROLA
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ADDENDUM TO:
MC3424, MC3424A
MC3524, MC3524A
MC3324, MC3324A
DATA SHEET

As indicated in the Note on page 7, the diagram appearing on page 16 of the data sheet, and reprinted below, was intended as a fold-out sheet to simplify consultation of the diagram while reading the text. Inadvertently, page 16 was printed as a standard page rather than a fold-out. Accordingly, this diagram is being supplied separately for easy correlation with the text.

FIGURE 29 — MC3524/3424/3324 BLOCK DIAGRAM

Note: All voltages and currents are nominal.