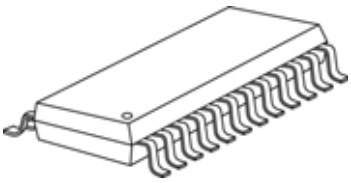
16-Channel Constant Current LED Driver With 16-bit PWM Control and Dot-Correction

Features

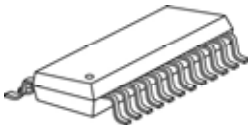
- 16 constant-current output channels
- Constant output current range per channel: 2~60mA
  2~60mA @ 5V supply voltage
  2~45mA @ 3.3V supply voltage
- Excellent output current accuracy,
  - Between channels: <±1.5% (typ.);
  - Between ICs: <±3% (typ.)
- Visual effect control
  - Patented S-PWM technology to improve refresh rate
  - 16-bit or 12-bit gray scale control
  - 8-bit dot-correction
  - 7-bit linear programmable output current gain
- Error detection control
  - In-message error detection:
    on-the-fly, data-in error-out
  - Compulsory individual LED open/short-circuit detection:
    full panel, data independent
    silent error detection in 700ns
  - Configurable short-circuit detection threshold voltage
  - Thermal protection
- Flexible operation modes
  - Auto synchronization mode/manual synchronization mode
  - One-shot mode/continuous mode
  - Disable/enable command
- EMI reduction
  - Staggered delay of output, preventing from current surge
  - Selectable switching speed of output channels (t_{OR}, t_{OF})
- Maximum data clock frequency: 30MHz
- Maximum gray scale clock frequency: 33MHz
- Schmitt trigger input
- Backward compatible with MBI5026 and MBI5030 in package

Small Outline Package



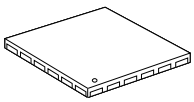
GF: SOP24L-300-1.00

Thin Shrink SOP



GTS: TSSOP24L-173-0.65

QFN



GFN: QFN24L-4*4-0.5

Application

- Full-color LED display

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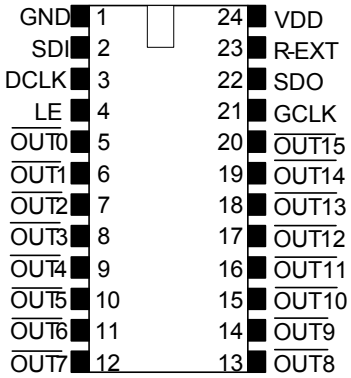
Product Description

MBI5040 is a 16-channel constant current LED driver with selectable 16-/12-bit gray scale control and 8-bit dot correction. MBI5040 provides constant current ranging from 2mA to 60mA for each output channel. The output current can be set by an external resistor. MBI5040 adopts **Share-I-O™** technology to be backward compatible with MBI5026 and MBI5030 in package and to extend the functionality, such as in-message error detection, compulsory error detection, thermal protection, and current gain control in LED display systems.

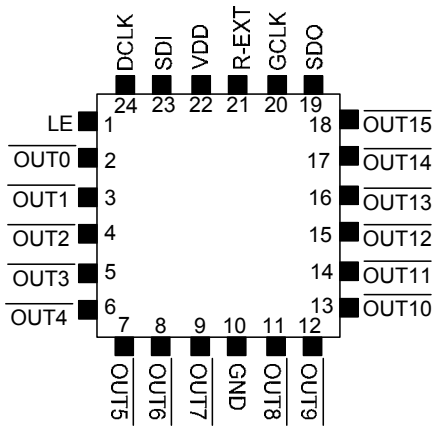
With Scrambled-PWM (S-PWM) technology, MBI5040 enhances pulse width modulation by scrambling the “on” time into several “on” periods, so that MBI5040 is able to increase visual refresh rate and reduce flickers. In addition, MBI5040 provides 16-bit gray scale control to enrich the color of image, allowing to present video images with 65,536 gray scales. MBI5040 also provides 8-bit dot correction to individually calibrate the deviated brightness and color of LEDs. Moreover, the preset current of MBI5040 can be further adjusted by 128 steps for LED global brightness adjustment.

With in-message error detection, MBI5040 can detect individual LED for both open- and short-circuit errors on-the-fly without extra components. Additionally, to enhance the system reliability, MBI5040 is built with thermal protection functions.

Pin Configuration



MBI5040GF/GP/GTS

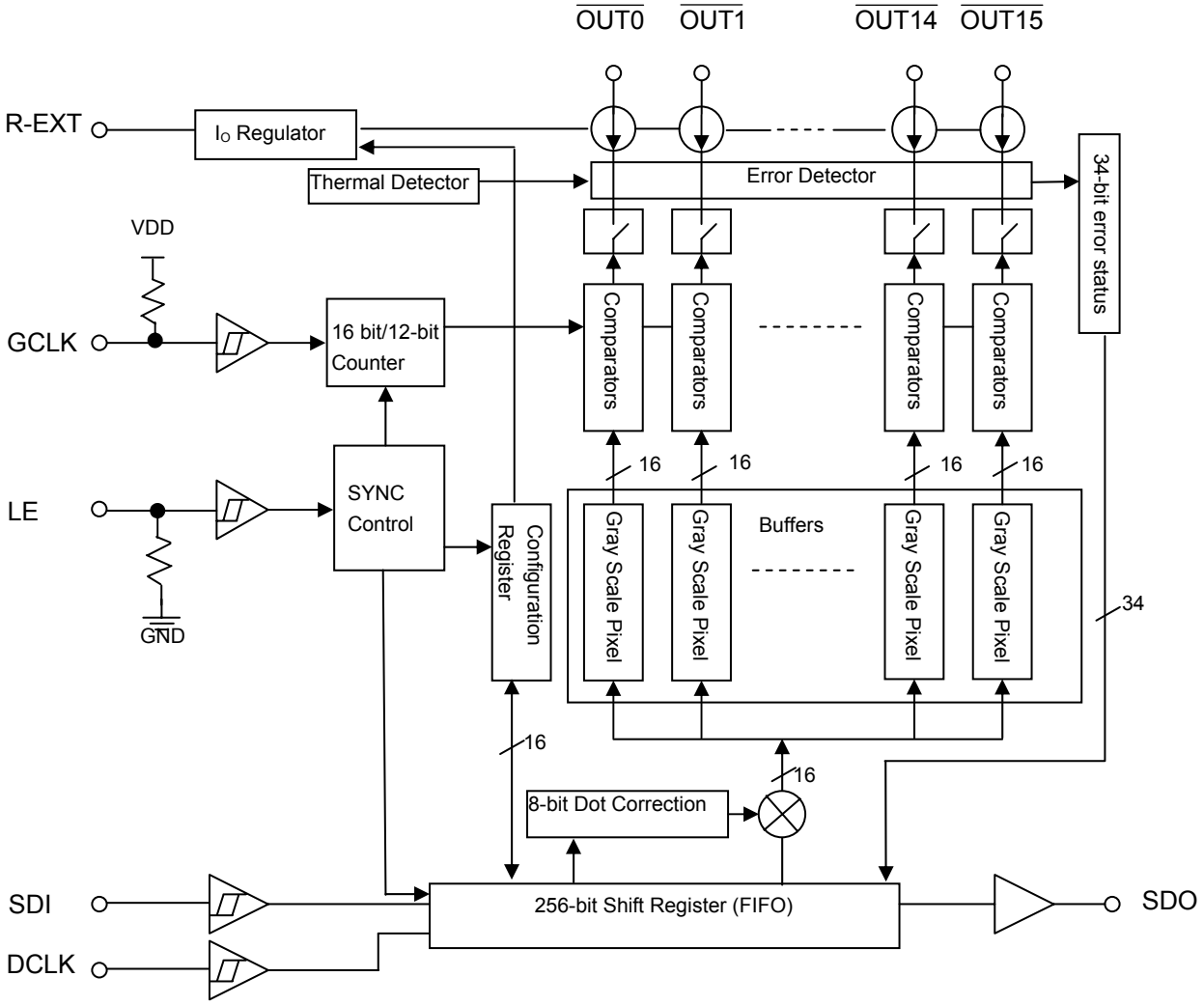


MBI5040GFN

Terminal Description

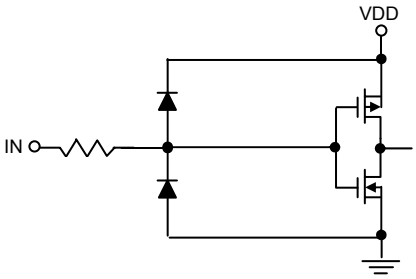
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Block Diagram

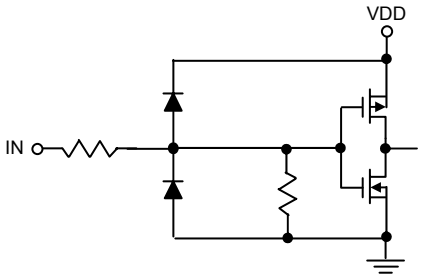


Equivalent Circuits of Inputs and Outputs

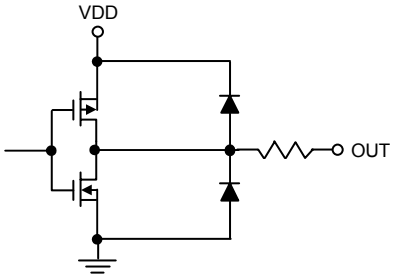
GCLK, DCLK, SDI terminal



LE terminal



SDO terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Input Pin Voltage (SDI, DCLK, LE, GCLK, R-EXT)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+80	mA
Sustaining Voltage at OUT Port		V_{DS}	-0.5~17	V
GND Terminal Current		I_{GND}	+1280	mA
Power Dissipation (On PCB, Ta=25°C)	GF Type	P_D	2.52	W
	GTS Type		3.53	
	GFN Type		3.13	
Thermal Resistance (On PCB, Ta=25°C)	GF Type	$R_{th(j-a)}$	49.69	°C/W
	GTS Type		35.45	
	GFN Type		40.01	
Empirical Thermal Resistance (Ta=25°C)	GF Type		78.83	
	GTS Type		89.11	
	GFN Type		94.25	
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.7)	HBM	Class 3 (≧4000V)	-
	Machine Mode (JEDEC EIA/JESD22-A115,)	MM	Class M4 (≧400V)	-

Electrical Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	60	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Output Leakage Current		I_{OUT}	V_{DS}=17.0V		-	-	0.5	μA
Current Skew (Channel)		dI_{OUT}	I_{OUT}=25.8mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
			I_{OUT}=45mA V_{DS}=1.0V	R_{ext}=310Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25.8mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
			I_{OUT}=45mA V_{DS}=1.0V	R_{ext}=310Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=560Ω@25.8mA		-	±0.1	±0.5	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±0.5	±1.0	% / V
Input Voltage of SDI, DCLK, LE, GCLK	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
LED Open Error Detection Threshold		$V_{DS,TH}$	-		-	0.30	0.35	V
Pull-down Resistor of LE		R_{IN}(down)	-		250	450	800	KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	2.4	5	mA
		I_{DD}(off) 2	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	6.5	10	
		I_{DD}(off) 3	R_{ext}=310Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	8.8	12	
	"On"	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	6.6	11	
		I_{DD}(on) 2	R_{ext}=310Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	9.9	13	
Supply Current (DCLK=GCLK =30MHz, SDI=15MHz switching)	"On"	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	23.0	-	
		I_{DD}(on) 2	R_{ext}=310Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	23.7	-	
Thermal Flag Temperature 1 **		T_{TF1}	Junction Temperature		-	140	-	°C
Thermal Flag Temperature 2 **		T_{TF2}	Junction Temperature		-	160	-	°C

*One channel on.
**Thermal flag 1 is over-temperature alarm, and thermal flag 2 is thermal shutdown.

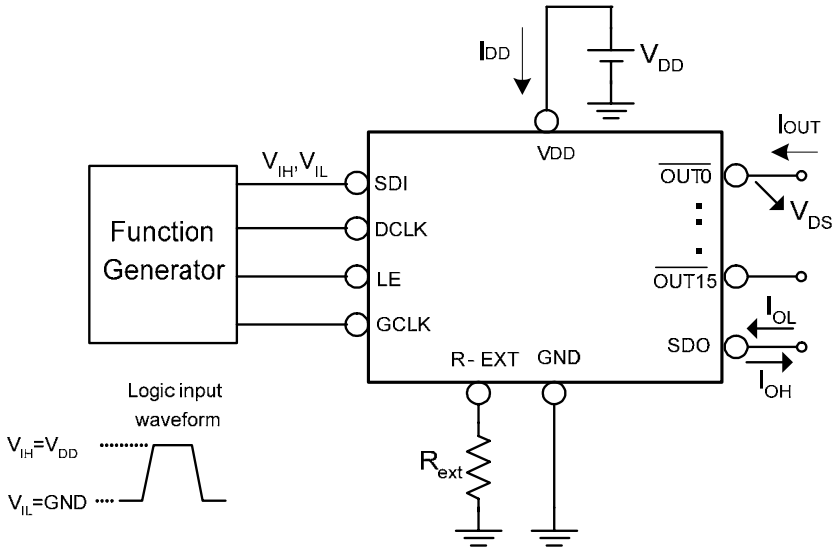
Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		2	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Output Leakage Current		I_{OUT}	V_{DS}=17.0V		-	-	0.5	μA
Current Skew (Channel)		dI_{OUT}	I_{OUT}=25.8mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
		dI_{OUT}	I_{OUT}=45mA V_{DS}=1.0V	R_{ext}=310Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25.8mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
		dI_{OUT2}	I_{OUT}=45mA V_{DS}=1.0V	R_{ext}=310Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=560Ω@25.8mA		-	±0.1	±0.5	% / V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 3.0V and 3.6V		-	±0.5	±1.5	% / V
Input Voltage of SDI, DCLK, LE, GCLK	"H" level	V_{IH}	Ta=-40~85ºC		$0.7xV_{DD}$	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	$0.3xV_{DD}$	V
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
LED Open Error Detection Threshold		$V_{DS,TH}$	-		-	0.30	0.35	V
Pull-down Resistor of LE		R_{IN}(down)	-		250	450	800	KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	1.9	4.5	mA
		I_{DD}(off) 2	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	6.1	9.5	
		I_{DD}(off) 3	R_{ext}=310Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	8.3	11.5	
	"On"	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	6.1	11	
		I_{DD}(on) 2	R_{ext}=310Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	9.4	13	
Supply Current (DCLK=GCLK=30 MHz, SDI=15Mhz switching)	"On"	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	16.2	-	
		I_{DD}(on) 2	R_{ext}=310Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	16.7	-	
Thermal Flag Temperature 1 **		T_{TF1}	Junction Temperature		-	140	-	°C
Thermal Flag Temperature 2 **		T_{TF2}	Junction Temperature		-	160	-	°C

*One channel on.

**Thermal flag 1 is over-temperature alarm, and thermal flag 2 is thermal shutdown.

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}=5.0V; Ta=25°C)

Characteristics			Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time		SDI–DCLK↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω V_{DS}=1V R_L=150Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	1	-	-	ns
		LE↑–DCLK↑	t_{SU1}		1	-	-	ns
		LE↓–DCLK↑	t_{SU2}		5	-	-	ns
Hold Time		DCLK↑–SDI	t_{H0}		3	-	-	ns
		DCLK↑–LE↓	t_{H1}		7	-	-	ns
		DCLK↓–LE↓	t_{H2}		10	-	-	ns
Propagation Delay Time		DCLK–SDO	t_{PD0}		-	25	33	ns
		GCLK – $\overline{OUT4n}$ *	t_{PD1}		-	50	-	ns
		LE–SDO**	t_{PD2}		-	30	40	ns
Staggered Delay of Output		$\overline{OUT4n+1}$*	t_{DL1}		-	5	-	ns
		$\overline{OUT4n+2}$*	t_{DL2}		-	10	-	ns
		$\overline{OUT4n+3}$*	t_{DL3}		-	15	-	ns
Pulse Width		LE	$t_{w(L)}$		5	-	-	ns
In-message Error Detection Duration (Count by GCLK)			t_{EDD}		-	-	10	GCLK
Compulsory Error Detection Operation Time***			t_{ERR-C}		-	-	700	ns
Data Clock Frequency			F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency****			F_{GCLK}		-	-	33	MHz
Switching Speed of Output Channels	High-Speed	Rise Time	t_{OR}	GCLK=2MHz (All channels turn on)	-	11	-	ns
		Fall Time	t_{OF}		-	20	-	ns
	Low-Speed	Rise Time	t_{OR}		-	19	-	ns
		Fall Time	t_{OF}		-	25	-	ns

* Refer to the Timing Waveform in P.12, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Users have to leave more time than the maximum error detection time for the error detection.

****With uniform output current.

Switching Characteristics (V_{DD}=3.3V; Ta=25°C)

Characteristics			Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time		SDI–DCLK↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω V_{DS}=1V R_L=150Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	1	-	-	ns
		LE↑–DCLK↑	t_{SU1}		1	-	-	ns
		LE↓–DCLK↑	t_{SU2}		5	-	-	ns
Hold Time		DCLK↑–SDI	t_{H0}		3	-	-	ns
		DCLK↑–LE↓	t_{H1}		7	-	-	ns
		DCLK↓–LE↓	t_{H2}		10	-	-	ns
Propagation Delay Time		DCLK–SDO	t_{PD0}		-	30	40	ns
		GCLK–$\overline{OUT4n}$ *	t_{PD1}		-	60	-	ns
		LE–SDO	t_{PD2}**		-	40	50	ns
Staggered Delay of Output		$\overline{OUT4n+1}$*	t_{DL1}		-	5	-	ns
		$\overline{OUT4n+2}$*	t_{DL2}		-	10	-	ns
		$\overline{OUT4n+3}$*	t_{DL3}		-	15	-	ns
Pulse Width		LE	$t_{w(L)}$		5	-	-	ns
In-message Error Detection Duration (Count by GCLK)			t_{EDD}			-	10	GCLK
Compulsory Error Detection Operation Time***			t_{ERR-C}		-	-	700	ns
Data Clock Frequency			F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency****			F_{GCLK}		-	-	20	MHz
Switching Speed of Output Channels	High-Speed	Rise Time	t_{OR}	GCLK=2MHz (All channels turn on)	-	17	-	ns
		Fall Time	t_{OF}		-	25	-	ns
	Low-Speed	Rise Time	t_{OR}		-	28	-	ns
		Fall Time	t_{OF}		-	48	-	ns

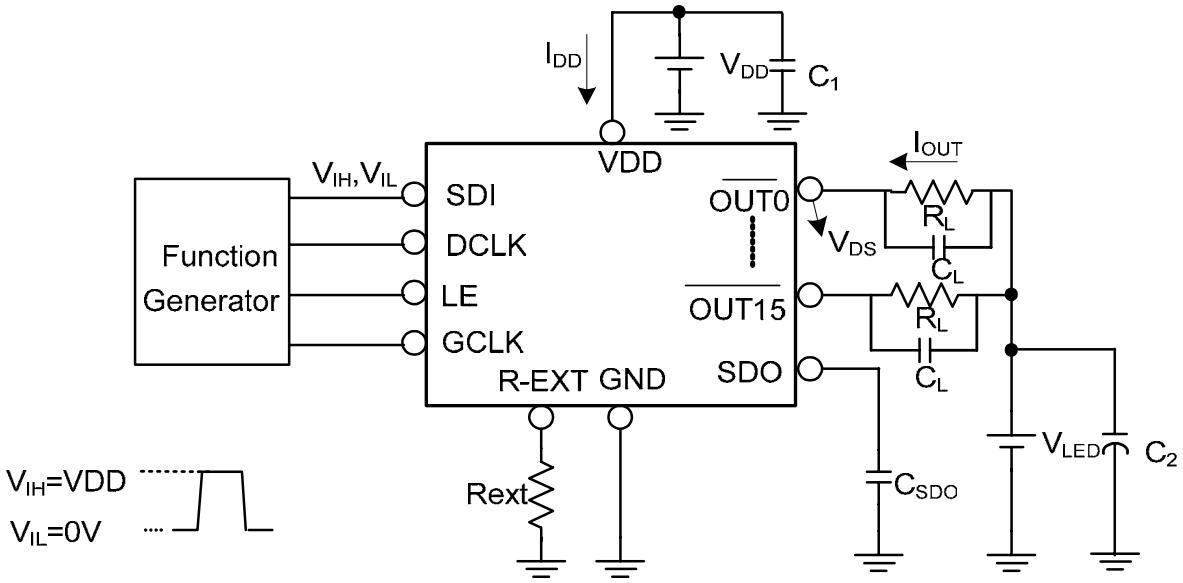
* Refer to the Timing Waveform in P.12, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Users have to leave more time than the maximum error detection time for the error detection.

****With uniform output current.

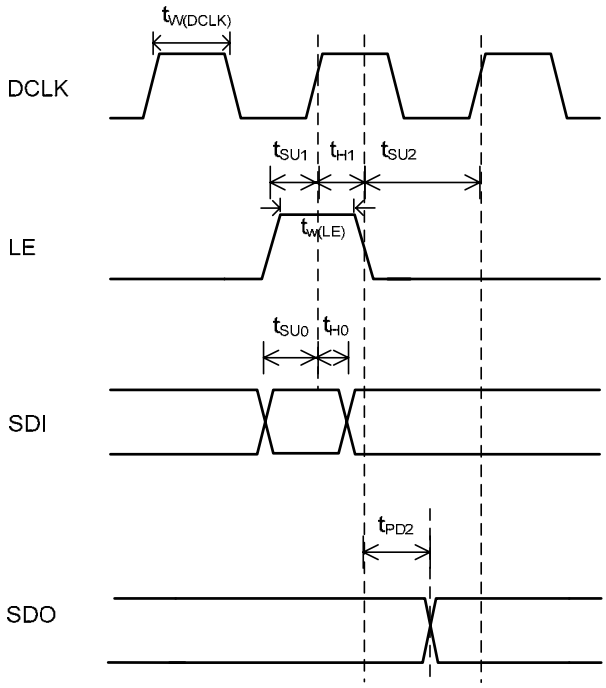
Test Circuit for Switching Characteristics



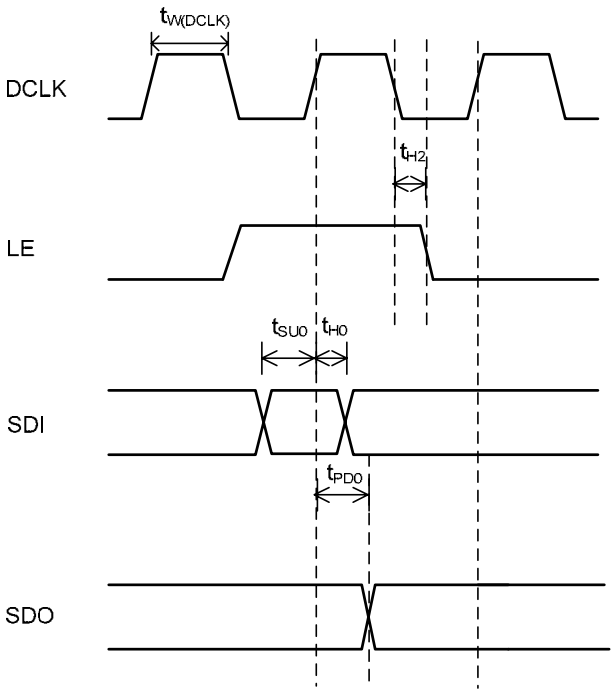
Timing Waveform

(1)

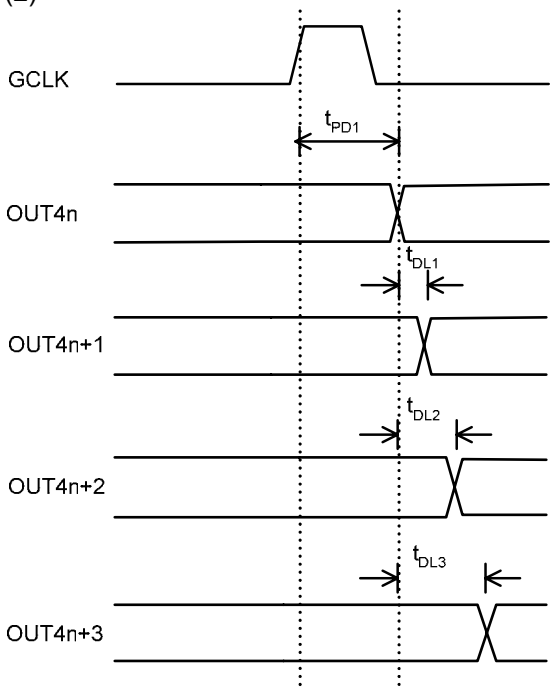
Timing Waveform for Read Configuration



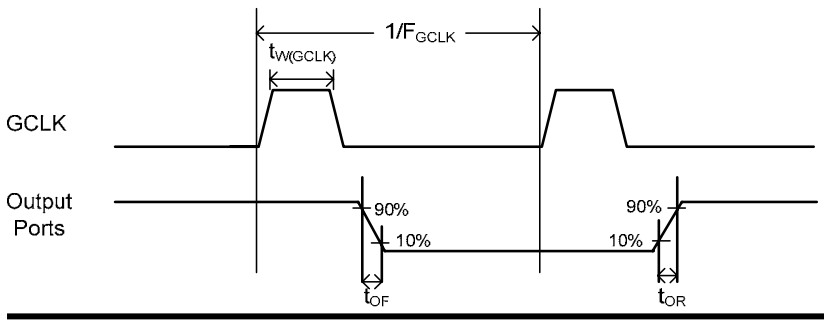
Timing Waveform for Global Latch



(2)



(3)



Principle of Operation

Users should set the operation modes in the configuration register through the “write configuration” command before sending gray scale data. The control command and configuration register are summarized in the following two tables.

Control Command

Command Name	Signals Combination		Description
	LE	Number of DCLK Rising Edge When LE is Asserted	The Action After a Falling Edge of LE
Latch data or stop compulsory error detection	High	0	Latch the serial data to the register for gray scale or dot correction or configuration register or stop compulsory error detection.
Dot correction	High	1	Enter the dot correction mode; the shift register is set to be 128 bits
Enable output	High	3	Enable output channels and activate the PWM counter
Compulsory error detection	High	4	Start compulsory error detection
Write configuration	High	5	Write 16-bit configuration register
Read configuration	High	6	Read the configuration register value
Disable output	High	7	Disable output channels and reset the PWM counter
12-bit gray scale setting	High	192(12x16)	Set the 12-bit gray scale mode
16-bit gray scale setting	High	256(16x16)	Set the 16-bit gray scale mode

Note: Please do **NOT** use the number of DCLK which are not specified in the table. Otherwise, it might cause malfunction on the LED drivers.

Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1

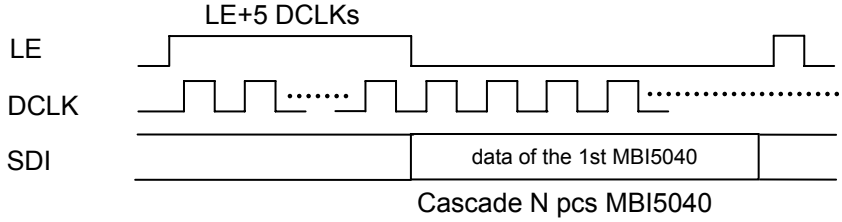
Bit	Attribute	Definition	Value	Function
F	Read/Write	PWM gray scale mode	0	12 bits
			1 (Default)	16 bits
E	Read/Write	PWM algorithm	0	Conventional PWM
			1 (Default)	S-PWM, divide the duty into 64 parts
D	Read/Write	PWM data synchronization	0	Manual synchronization
			1 (Default)	Auto synchronization
C	Read/Write	PWM counting mode	0 (Default)	Continuous counting mode
			1	One-shot counting mode
B	Read/Write	Thermal shutdown	0	Disable thermal shutdown
			1 (Default)	Enable thermal shutdown
A	Read/Write	Error detection	0	Disable both in-message and compulsory error detections
			1 (Default)	Enable both in-message and compulsory error detections
9~8	Read/Write	Threshold voltage of short-circuit detection	00 (Default) 01 10 11	2'b00: Disable short-circuit detection 2'b01: $0.4xV_{DD}\pm0.1$(V) 2'b10: $0.5xV_{DD}\pm0.1$(V) 2'b11: $0.73xV_{DD}\pm0.1$(V)
7	Read/Write	Switching speed of output channels	0 (Default)	Low switching speed
			1	High switching speed
6~0	Read/Write	Output current gain adjustment	1111111 (Default)	Output current; $I=I_0$xCurrent Gain[6:0]/127; $I_0=(V_{R-EXT}/R_{ext})x23$

Shift Register

The effective length of the shift register in MBI5040 is auto-adjusted among 256 / 192 / 128 / 16 bits according to different modes of input data.

Write Configuration Register

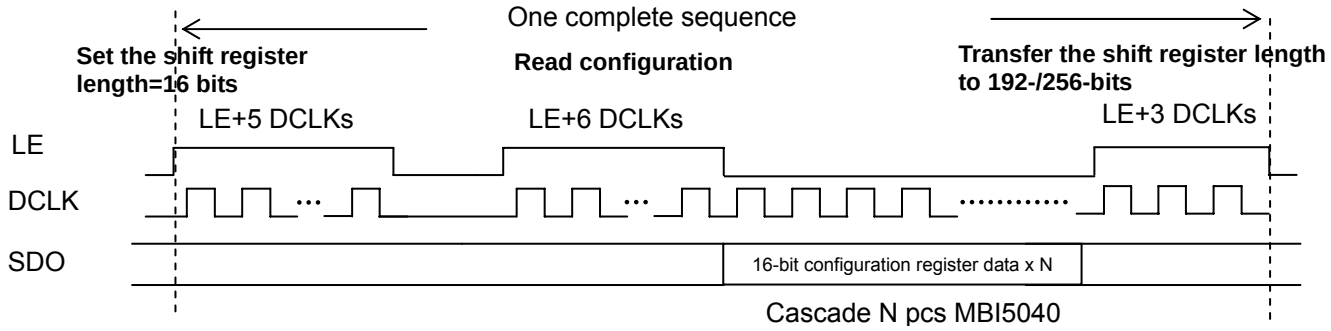
MBI5040 can write the configuration register when receiving one LE pulse containing 5 DCLKs, and then send 16-bit configuration setting to each LED driver. The following waveform shows the input signal waveform when cascading N pieces of MBI5040:



Cascade N pcs MBI5040

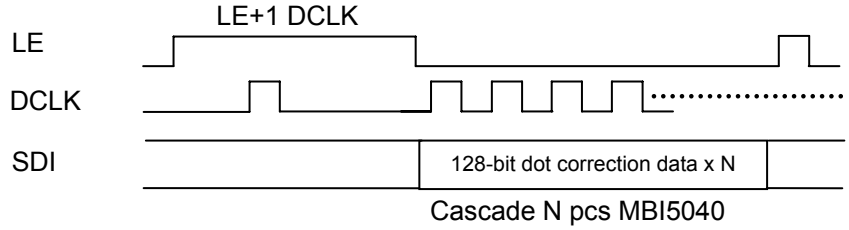
Read Configuration Register

MBI5040 can read the configuration register when receiving one LE pulse containing 5 DCLKs in order to set the shift register length to 16 bits, and then send one LE pulse containing 6 DCLKs to read the configuration setting. After the command, 16-bit configuration of each MBI5040 will be shifted out sequentially from the Nth MBI5040 to the 1st MBI5040. The following waveform shows the output signal waveform when cascading N pieces of MBI5040:



Input the Dot Correction Data

MBI5040 can input the dot correction data when receiving one LE pulse containing one DCLK, and then send 128-bit dot correction data to each LED driver. The following waveform shows the input signal waveform when cascading N pieces of MBI5040:



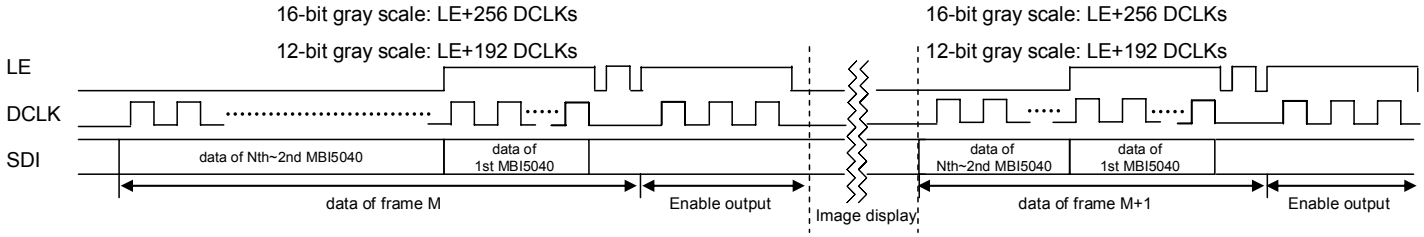
Enable and Disable Output

MBI5040 can disable output channels when receiving one LE pulse containing 7 DCLKs. The output channels will be enabled again when receiving one LE pulse containing 3 DCLKs. This “enable” command can also reactivate the IC from thermal shutdown when the junction temperature decreases.

Set the PWM Gray Scale Mode

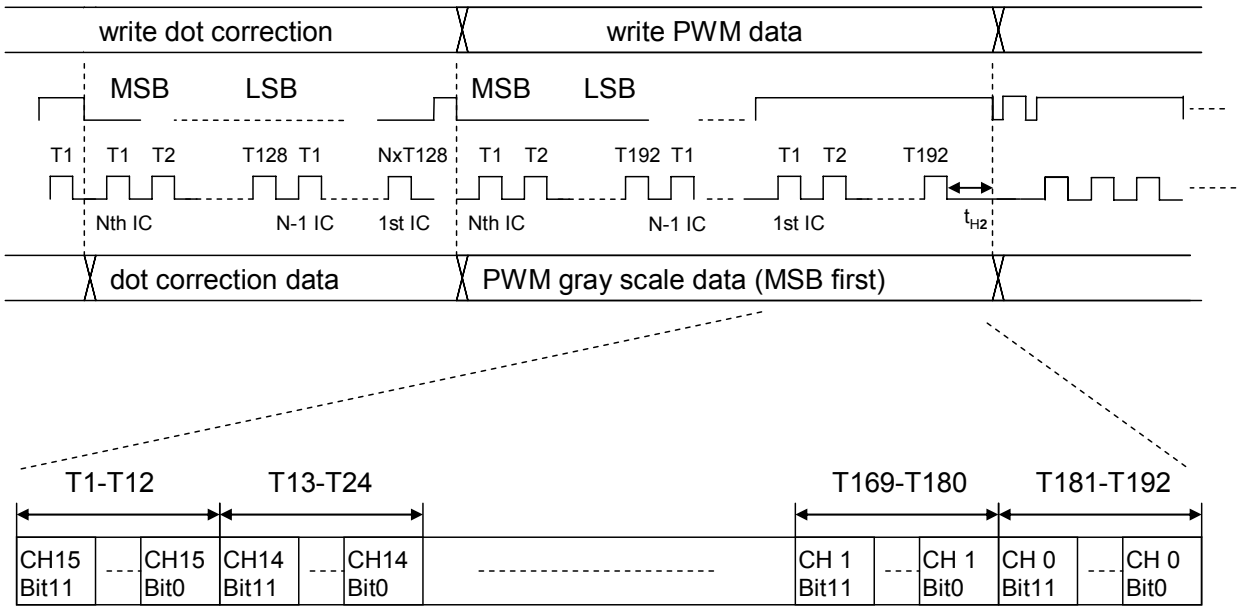
MBI5040 provides a selectable 16-bit or 12-bit gray scale mode by setting bit “F” of the configuration register. For 16-bit gray scale mode, the bit “F” is set to “1” (default), and for 12-bit gray scale mode, the bit “F” is set to “0”.

Users need to set the gray scale mode before sending the data, and then send the data from Nth MBI5040 to the 1st MBI5040. MBI5040 will enter 16-bit or 12-bit gray scale mode when receiving one LE pulse containing 256 DCLKs or 192 DCLKs respectively. To latch the data, the command of one LE pulse containing 0 DCLK should be sent after the gray scale mode. Then MBI5040 will enable the output when receiving one LE pulse containing 3 DCLKs. The following waveform shows the input signal waveform when cascading N pieces of MBI5040:



Gray Scale Data Format

The data input sequence of both 16-bit and 12-bit gray scale data are the same, and the following waveform illustrates the sequence:



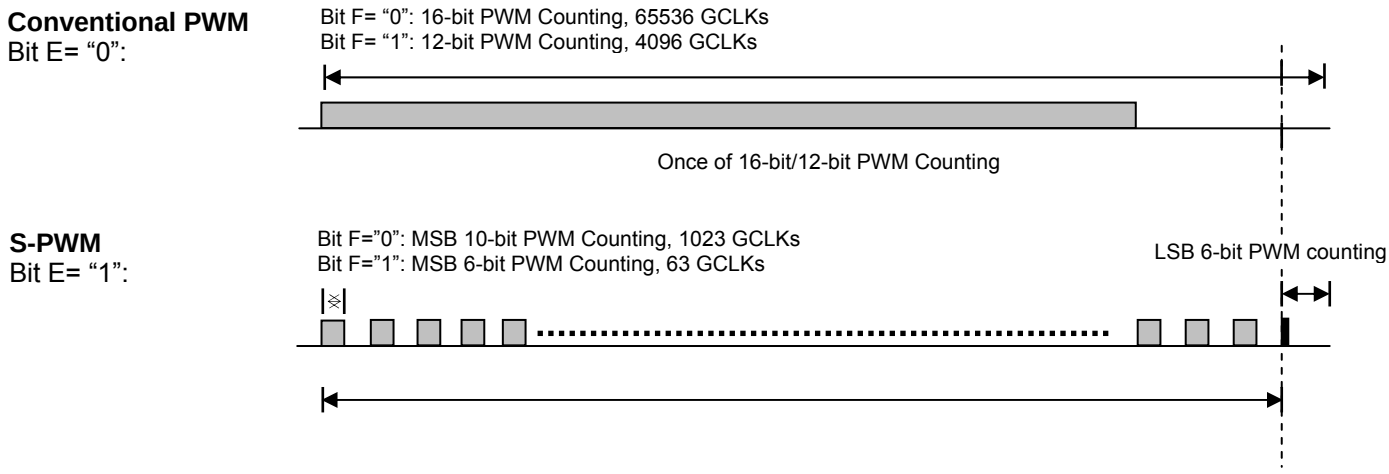
t_{H2}: In the end of gray scale mode, DCLK↓–LE↓ should be no less than 10ns.

Set the PWM Counting Mode

PWM Algorithm

MBI5040 defines the different counting algorithms that support scrambled PWM technology, S-PWM. With S-PWM, the total PWM cycles can be broken down into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles, and the MSB information can be dithered across 63 refresh cycles.

MBI5040 is flexible for either the conventional PWM algorithm or S-PWM algorithm by setting bit "E" of the configuration register. For S-PWM algorithm, the bit "E" is set to "1" (default), and for conventional PWM algorithm, the bit "E" is set to "0":



: Output ports are turned "on".

Synchronization of PWM Cycle

MBI5040 is also flexible for either manual synchronization or auto synchronization by setting bit "D" of the configuration register.

For auto synchronization, the bit "D" is set to "1" (default). MBI5040 will automatically process the synchronization of previous data and next data for PWM counting. The next image data will be updated to output buffers and start PWM counting when the previous data finishes one internal PWM cycle. This prevents the lost count of image data resolution and guarantees the data accuracy.

For manual synchronization, the bit "D" is set to "0". Once the next input data is correctly recognized, MBI5040 will stop the present PWM cycle and restart a new PWM cycle to show the new data immediately.

PWM Counting Mode

Users can set either continuous counting mode or one-shot counting mode by setting bit “C” of the configuration register.

For the continuous counting mode, the bit “C” is set to “0” (default). In the continuous counting mode, MBI5040 will continuously repeat the PWM cycles and turn on the output channels according to the image data until the next image data is correctly recognized.

For the one-shot counting mode, the bit “C” is set to “1”. In the one-shot counting mode, MBI5040 will run the PWM cycle for each image data one time, and then stop the output channels until the next image data is correctly recognized.

Error Detection Principle

MBI5040 provides two error detection functions: in-message error detection and compulsory error detection. Users can read the open-/short-circuit error reports, and thermal flag from SDO. For all the detection functions, “0” indicates error or abnormal state and “1” indicates normal state.

In-message Error Detection

Users can set the in-message error detection by bit “A” of configuration register. To enable the in-message error detection, the bit “A” is set to “1” (default). To disable the in-message error detection, the bit “A” is set to “0”.

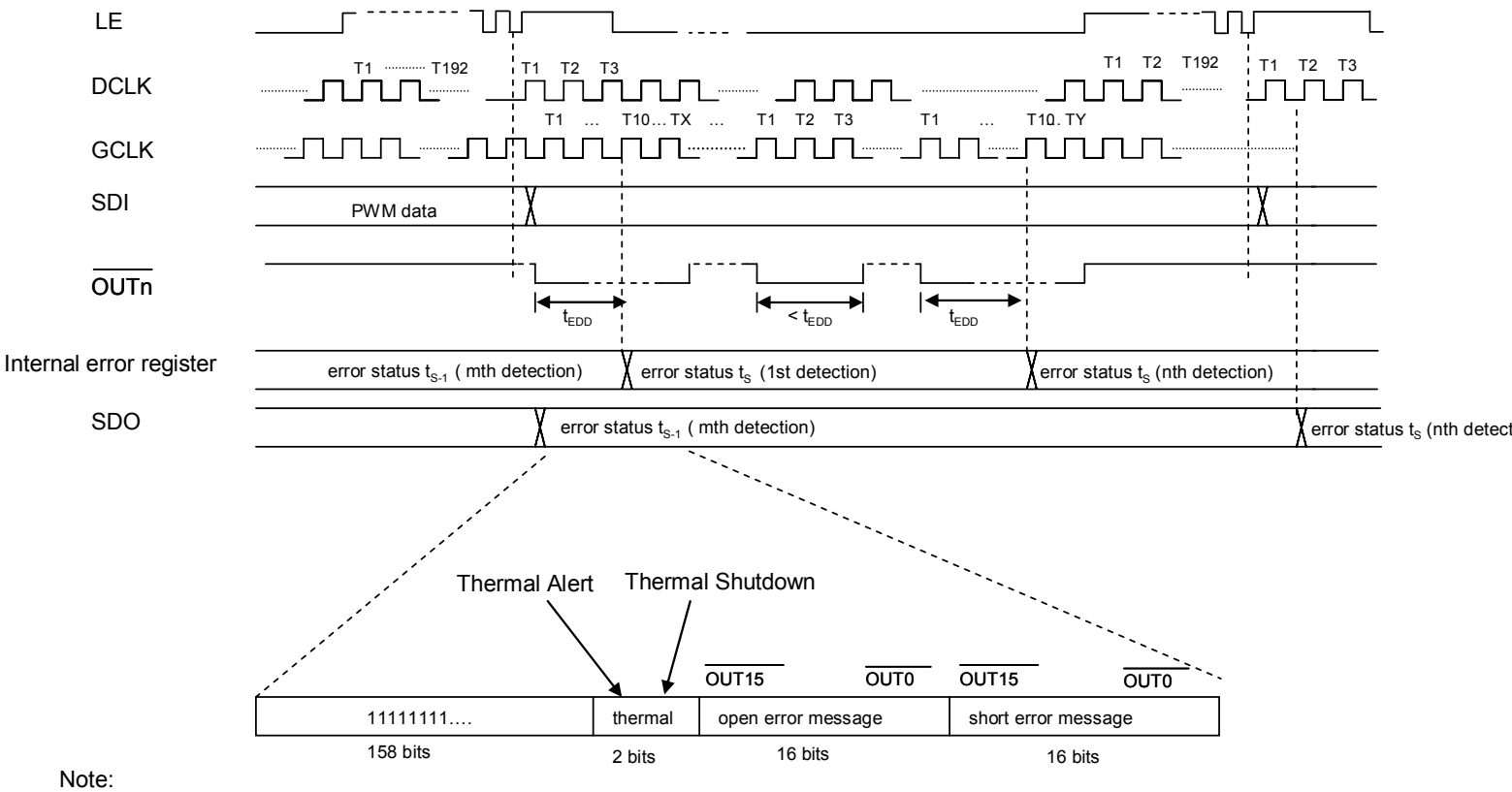
The open-/short-circuit error will be reported only when output channels are turned on in 10 GCLKs, and the error reports will be put into the shift register after the gray scale data is latched.

Since the PWM output duty cycle of MBI5040 is the product of gray scale data and dot correction data. If the S-PWM algorithm is selected, the open-/short-circuit in-message error detection will be performed while the product of gray scale data and dot correction data is from 640 to 65,535 in the 16-bit gray scale mode or from 640 to 4,095 in the 12-bit gray scale mode. If the conventional PWM algorithm is selected, the open-/short-circuit error will be reported when the product of gray scale data and dot correction data is larger than 10.

MBI5040 will judge if the turn-on time is enough or not to deliver the error report. If the turned-on time is too short, MBI5040 will report normal state coded as “1”.

Error data (N)=error data(N-1) presents detection result.
It will be reset to 1 until the error data is read out.

Please see the example of the following diagram of 12-bit gray scale mode for the control sequence and data output format of all error reports.



Note:

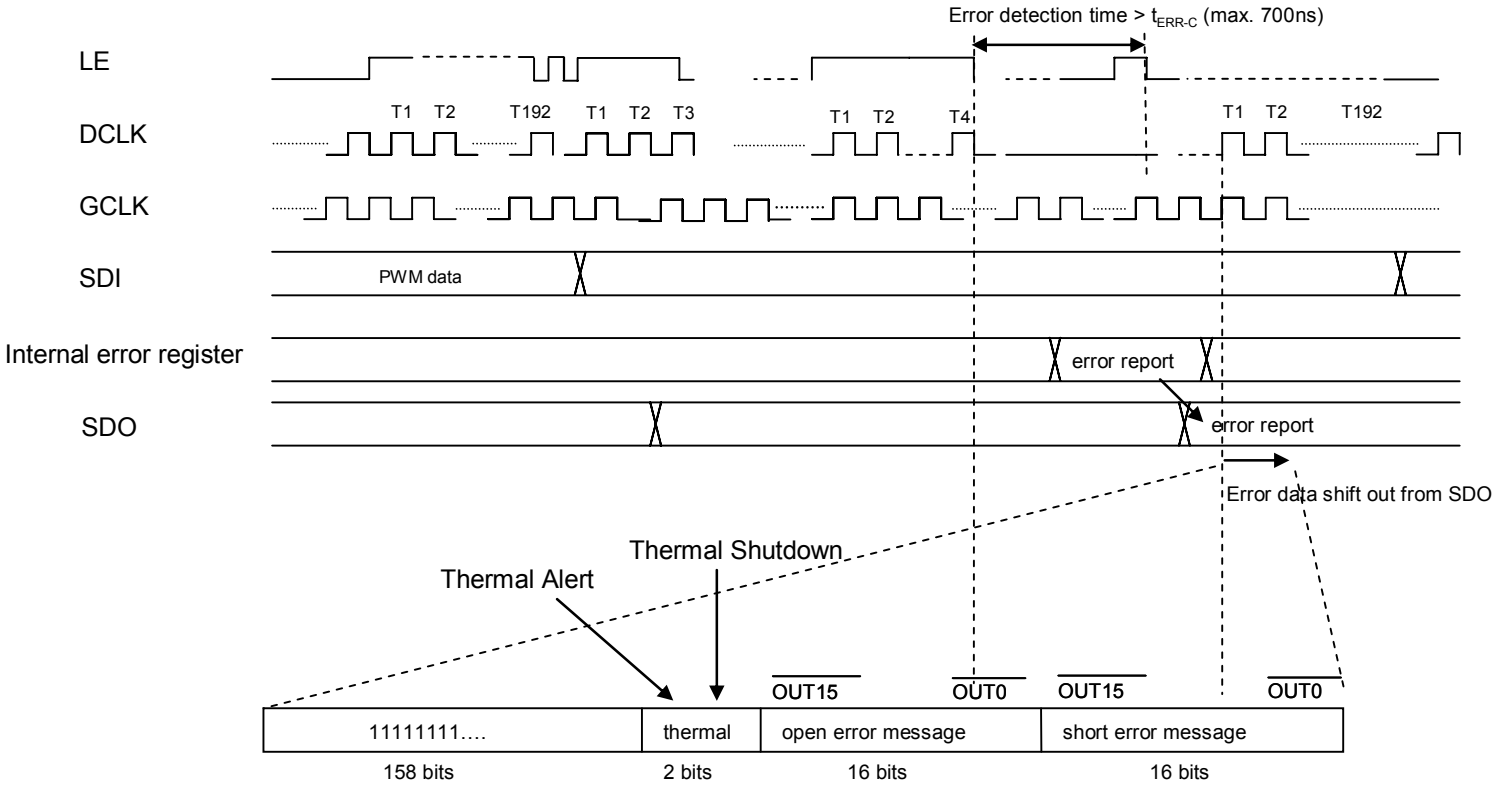
t_S: the Sth frame

t_{S-1}: the (S-1)th frame

t_{EDD}=10 GCLKs

Compulsory Error Detection

MBI5040 can also perform the compulsory error detection when receiving one LE pulse containing 4 DCLKs and stop the compulsory error detection when receiving one LE pulse containing 0 DCLK. The output channels will be forced to turned on within 700ns (between the LE falling edges) to perform the compulsory error detection. The error report will be pushed out after compulsory error detection operation time (700ns). MBI5040 will shift out both open and short error reports from SDO simultaneously. The following is an illustration of the timing sequence of compulsory error detection of 12-bit gray scale mode.



Setting the Threshold Voltage for Compulsory Short-Circuit Detection

Users can set the threshold voltage ($V_{SD.TH}$) for compulsory short-circuit detection by bit [9:8] of configuration register as summarized below:

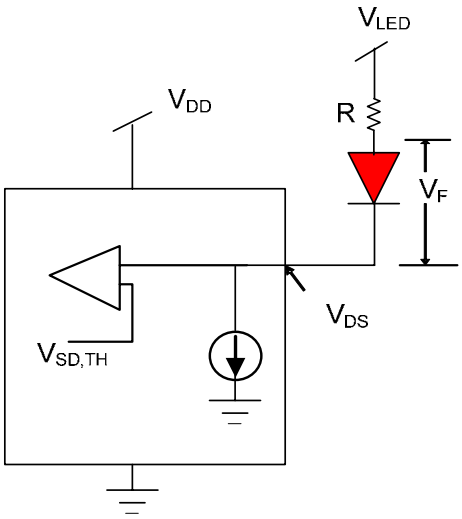
2'b00: Disable the short-circuit detection (default)

2'b01: $0.4xV_{DD}\pm0.1(V)$

2'b10: $0.5xV_{DD}\pm0.1(V)$

2'b11: $0.73xV_{DD}\pm0.1(V)$

MBI5040 provides settable $V_{SD,TH}$ for different LED configuration. If the detected voltage is larger than $V_{SD.TH}$, the MBI5040 identifies the LED as short-circuit. For example, if each output channel of MBI5040 drives one red LED, the $V_{SD,TH}$ should be set smaller. If each output channel of MBI5040 drives several white LEDs, the $V_{SD,TH}$ should be set larger. The system should consider the accumulated V_F of the LEDs to set a suitable $V_{SD,TH}$.



Thermal Protection

Users can set the thermal protection by bit "B" of configuration register. To enable the thermal shutdown function, the bit "B" is set to "1" (default). To disable the thermal shutdown function, the bit "B" is set to "0".

MBI5040 provides two thermal flags:

Thermal flag 1 is over-temperature alarm, and thermal flag 2 is thermal shutdown. When the IC junction temperature is over 140°C, thermal flag 1 will report "0". When the IC junction temperature is under 120°C, thermal flag 1 will recover to "1".

When the IC junction temperature is over 160°C, the thermal flag 2 will become "0" and MBI5040 will turn off the output current of all channels automatically. MBI5040 will turn on the output channels when receiving one LE pulse containing 3 DCLKs.

Adjust the Switching Speed of the Output Channels

Users can select the switching speed of output channels by bit “7” of configuration register. For low switching speed, the bit “7” is set to “0” (default). For high switching speed, the bit “7” is set to “1”.

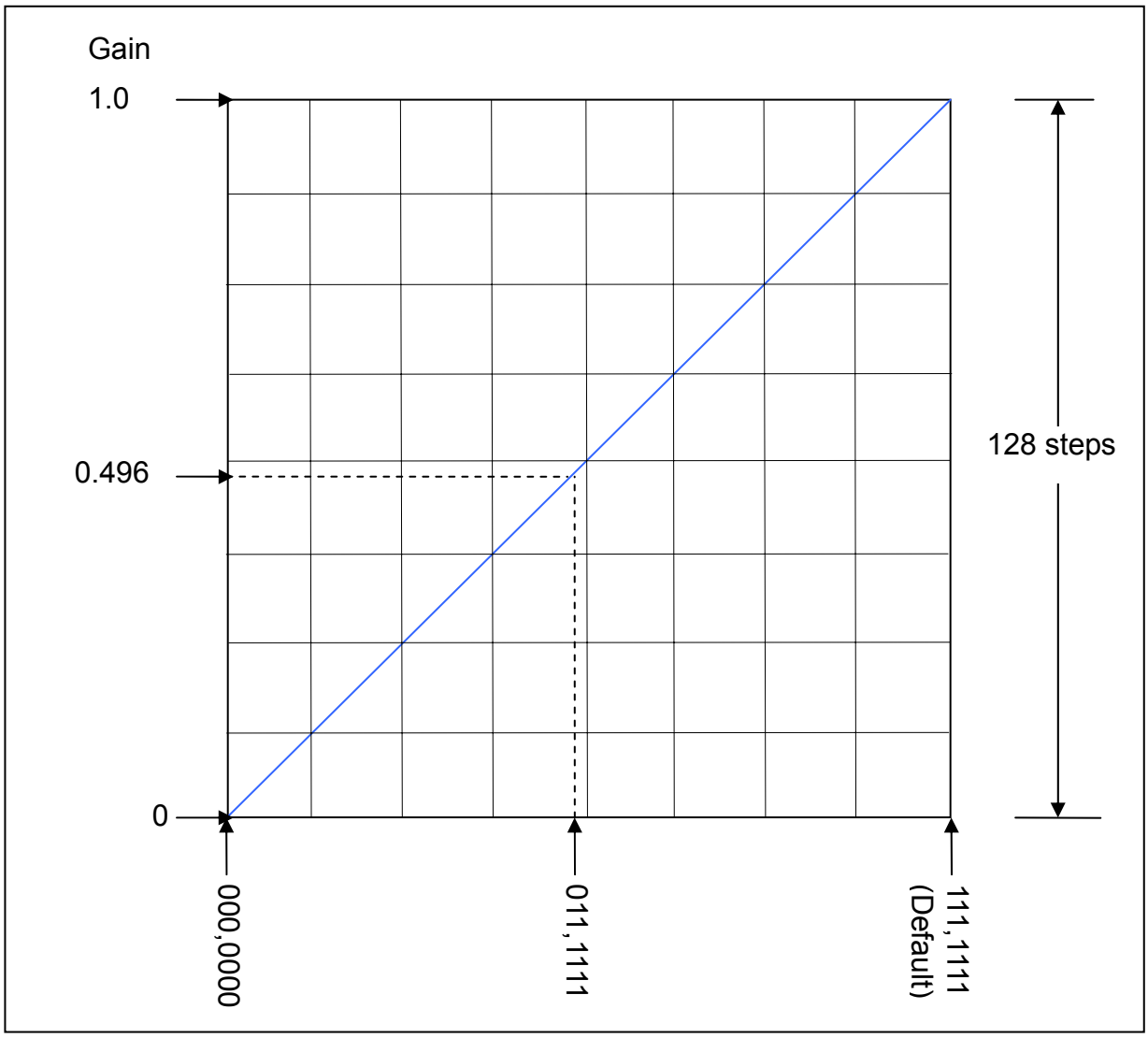
Low switching speed helps to reduce the EMI and overshoot of the output channels. On the other hand, high switching speed is suitable for high GCLK frequency and high refresh rate applications.

Adjust the Output Current Gain

Users can adjust output current gain by bit [6:0] of configuration register. The default current gain value is 7b’1111111.

The output current; $I=I_0$xCurrent Gain [6:0]/127, where $I_0=(V_{R\text{-}EXT}/R_{ext})$x23

The current gain value is proportional to the output current. In other words, current gain value versus output current is linear. This function helps users to tune the output current by software in stead of by hardware for daily operation.



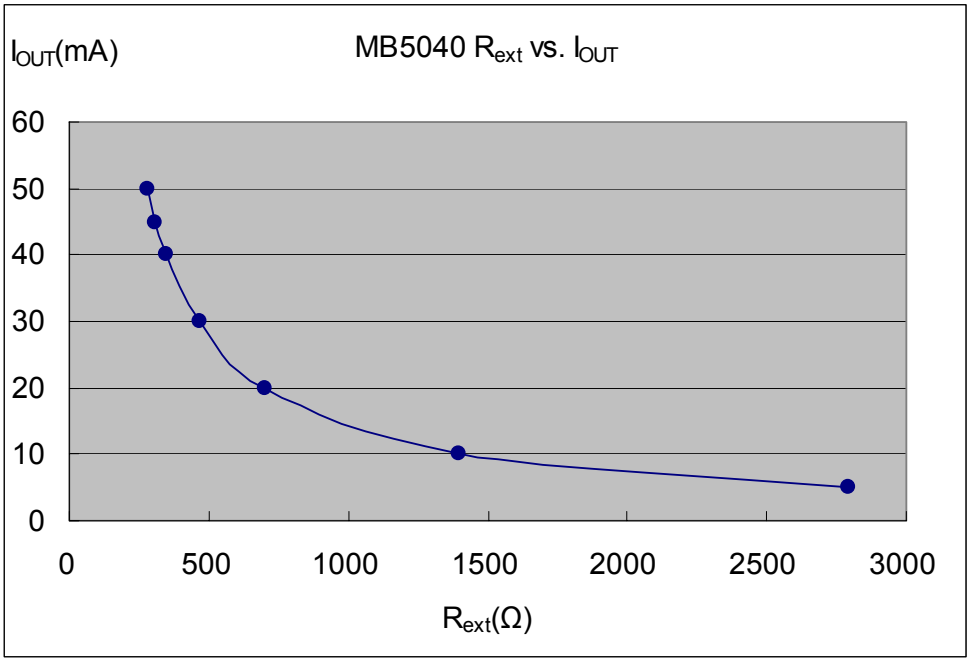
Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

Also, the output current can be calculated from the equation:

V_{R-EXT}=0.61; I_{OUT}=(V_{R-EXT}/R_{ext})x23xG/127

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and V_{R-EXT} is its voltage. G is the digital current gain, which is set by the bit[6:0] of the configuration register. The default value of G is 127. For your information, the output current is about 25mA when R_{ext}=560Ω and 45mA when R_{ext}=310Ω if G is set to default value 127. The formula and setting for G are described in further section.

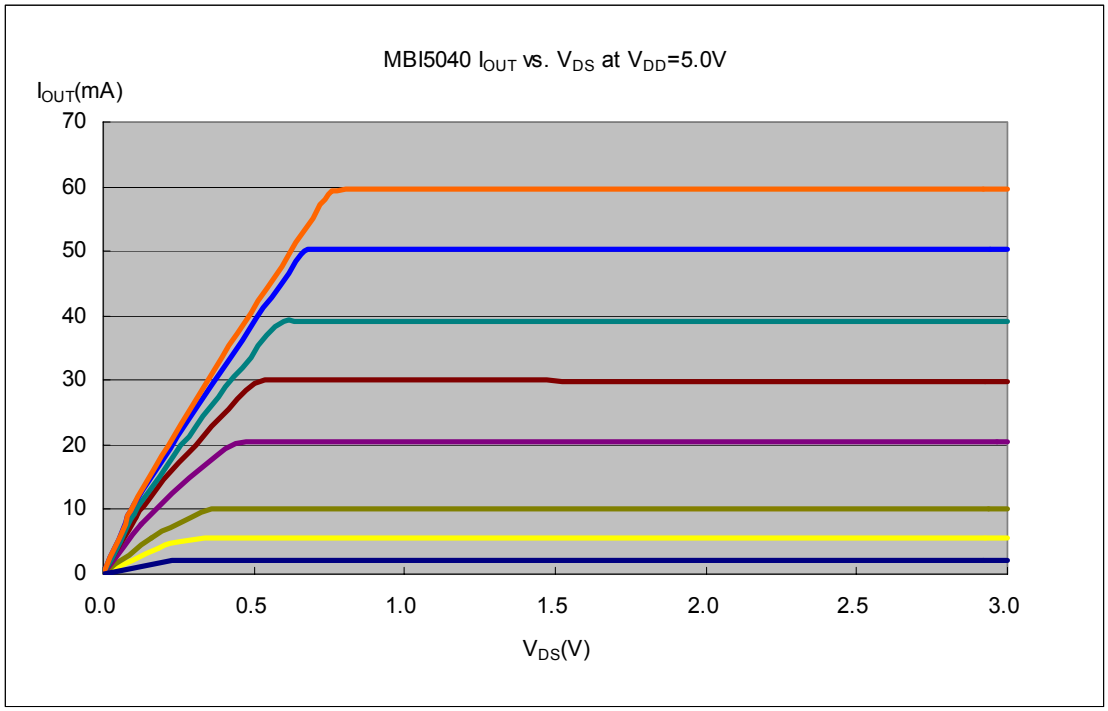


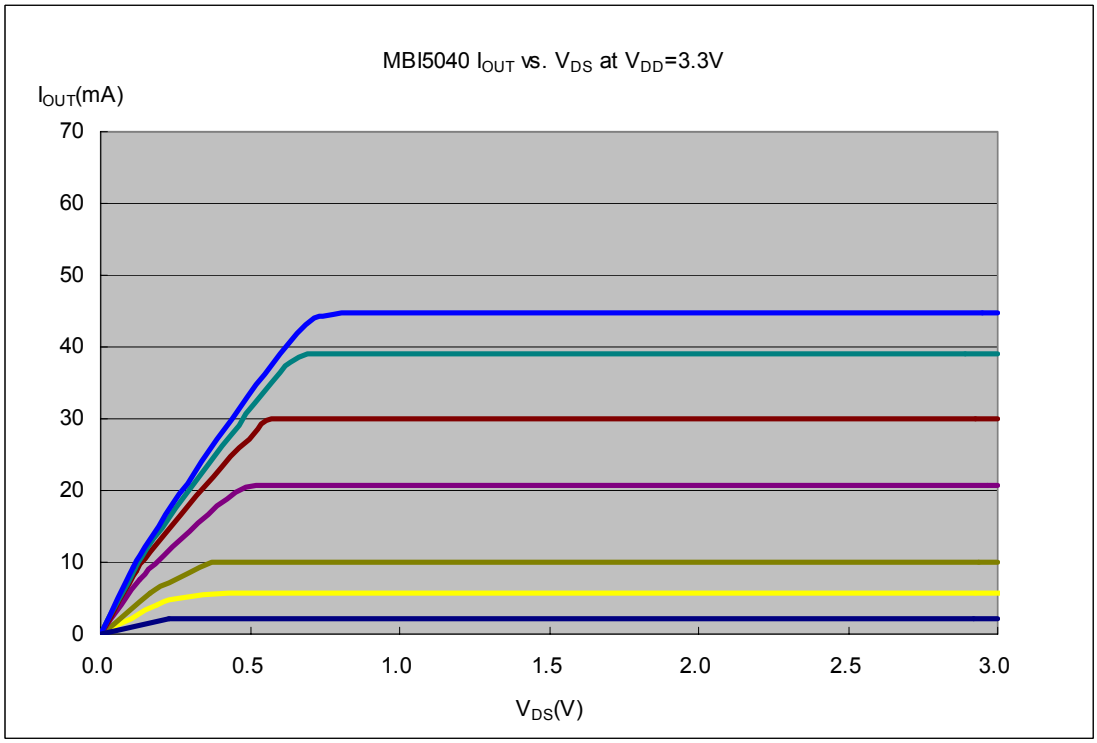
Constant Current

In LED display application, MBI5040 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than 1.5%, and that between ICs is less than ±3%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





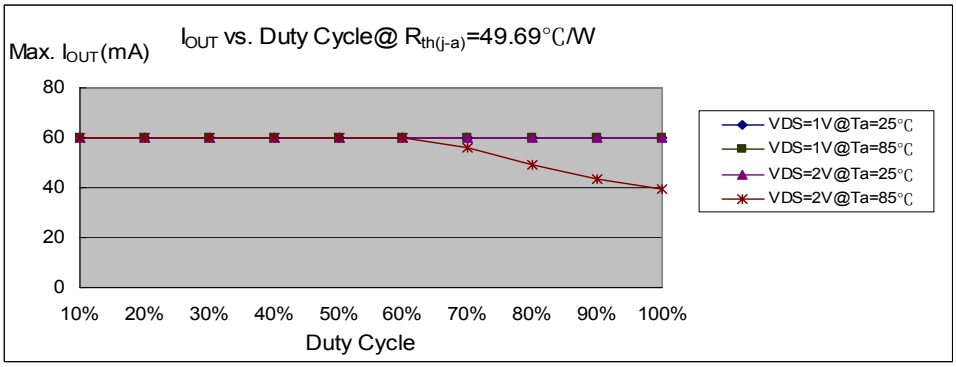
Staggered Delay of Output

MBI5040 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 5ns delay time among $\overline{OUT4n}$, $\overline{OUT4n+1}$, $\overline{OUT4n+2}$, and $\overline{OUT4n+3}$, by which the output ports will be divided to four groups at a different time so that the instant current from the power line will be lowered.

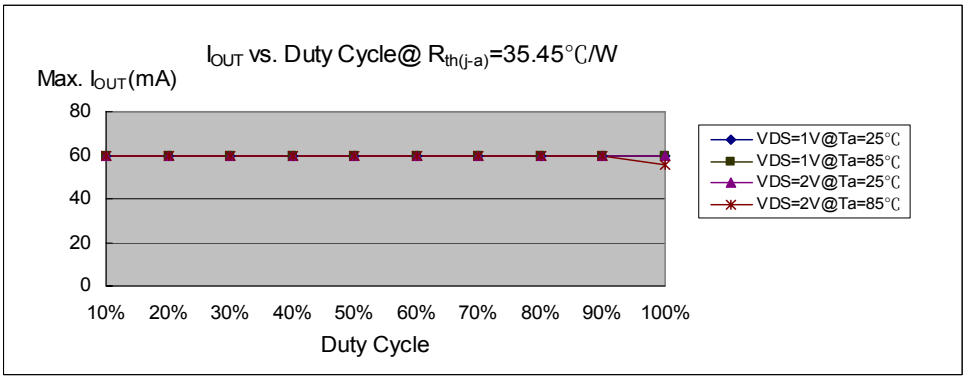
Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

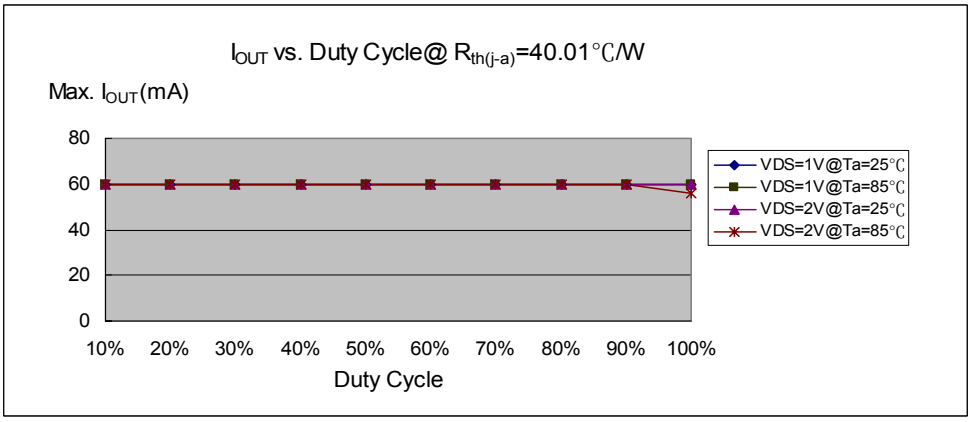
$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.



MBI5040GF



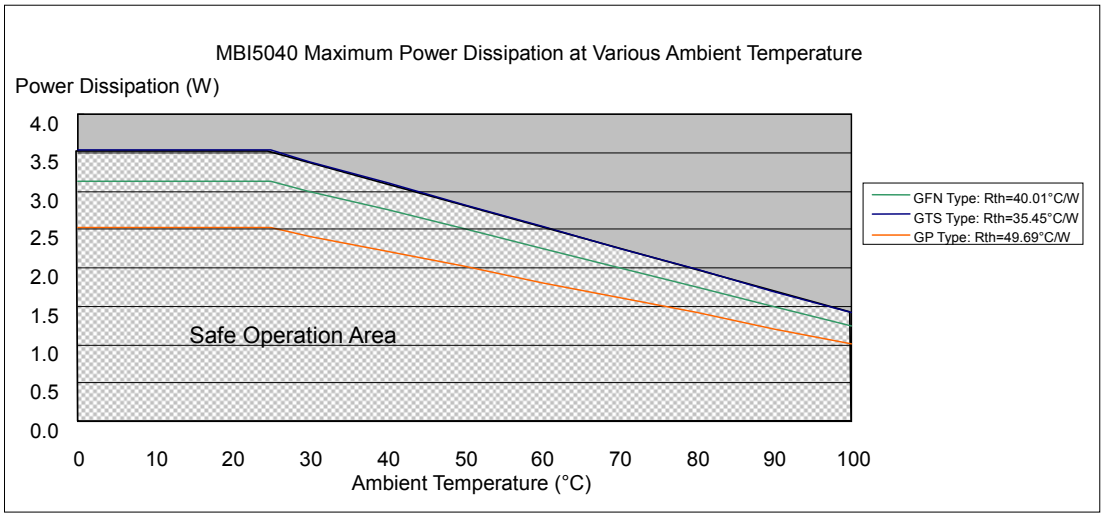
MBI5040GTS



MBI5040GFN

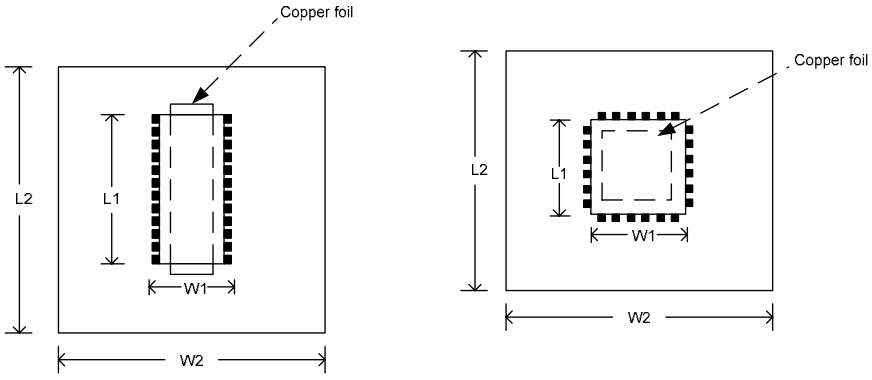
Device Type	$R_{th(j-a)}$ (°C/W)
GF	49.69
GTS	35.45
GFN	40.01

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



Usage of Thermal Pad

The PCB area (L2xW2) is 4 times of the IC's area (L1xW1).The thickness of the PCB is 1.6mm, copper foil 1 Oz.
The thermal pad on the IC's bottom has to be mounted on the copper foil.

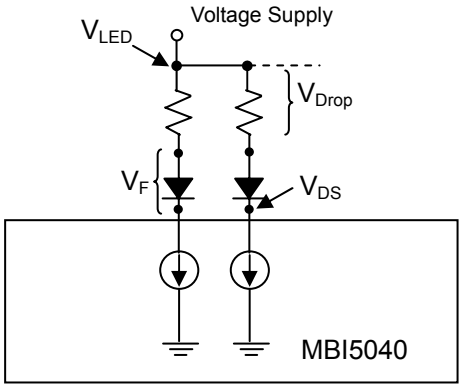


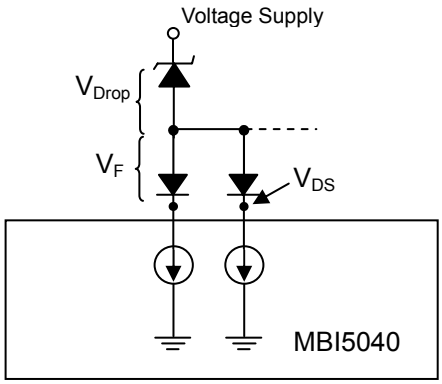
LED Supply Voltage (V_{LED})

MBI5040 are designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=2~60mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.



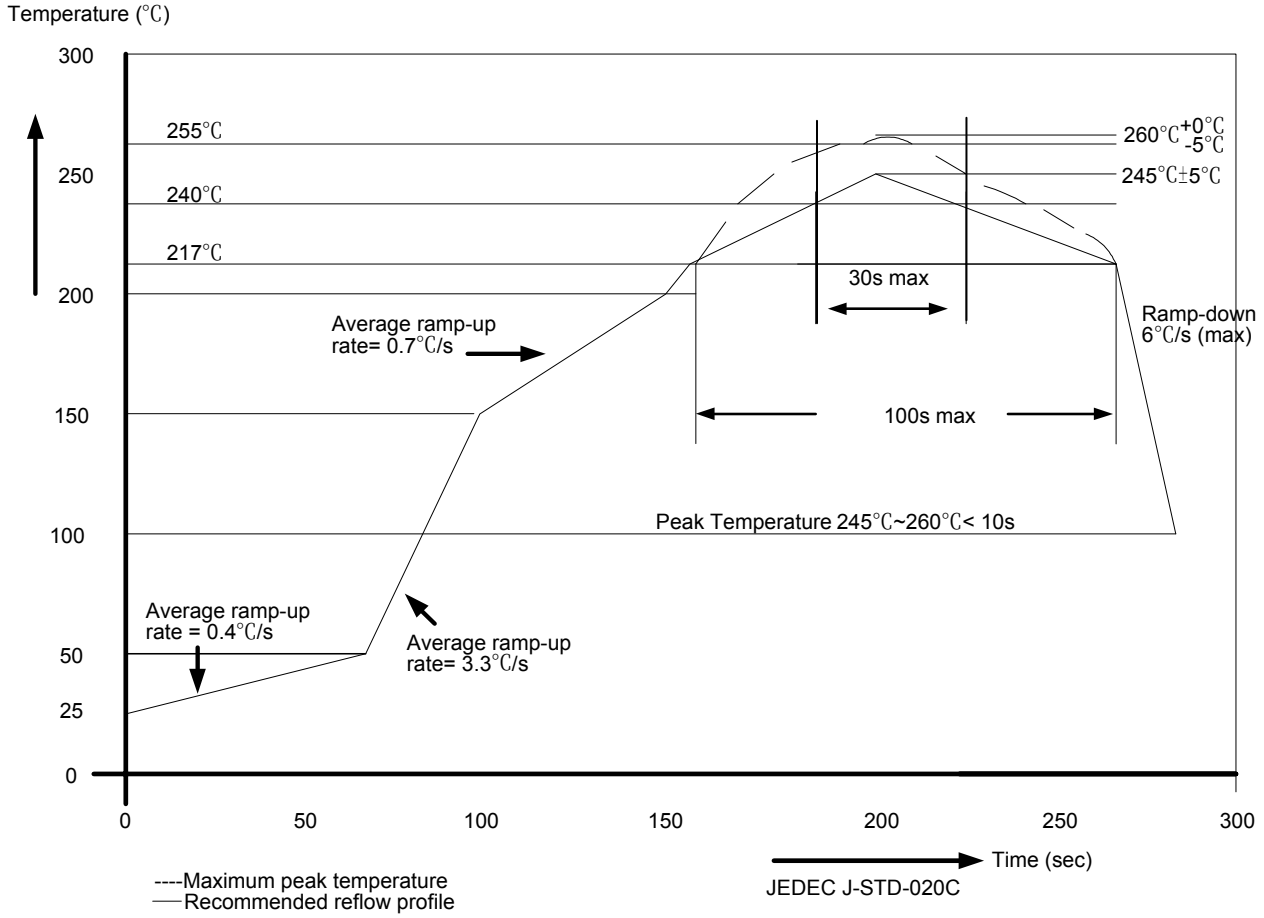


Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers-Overshoot”.

Soldering Process of "Pb-free" Package Plating*

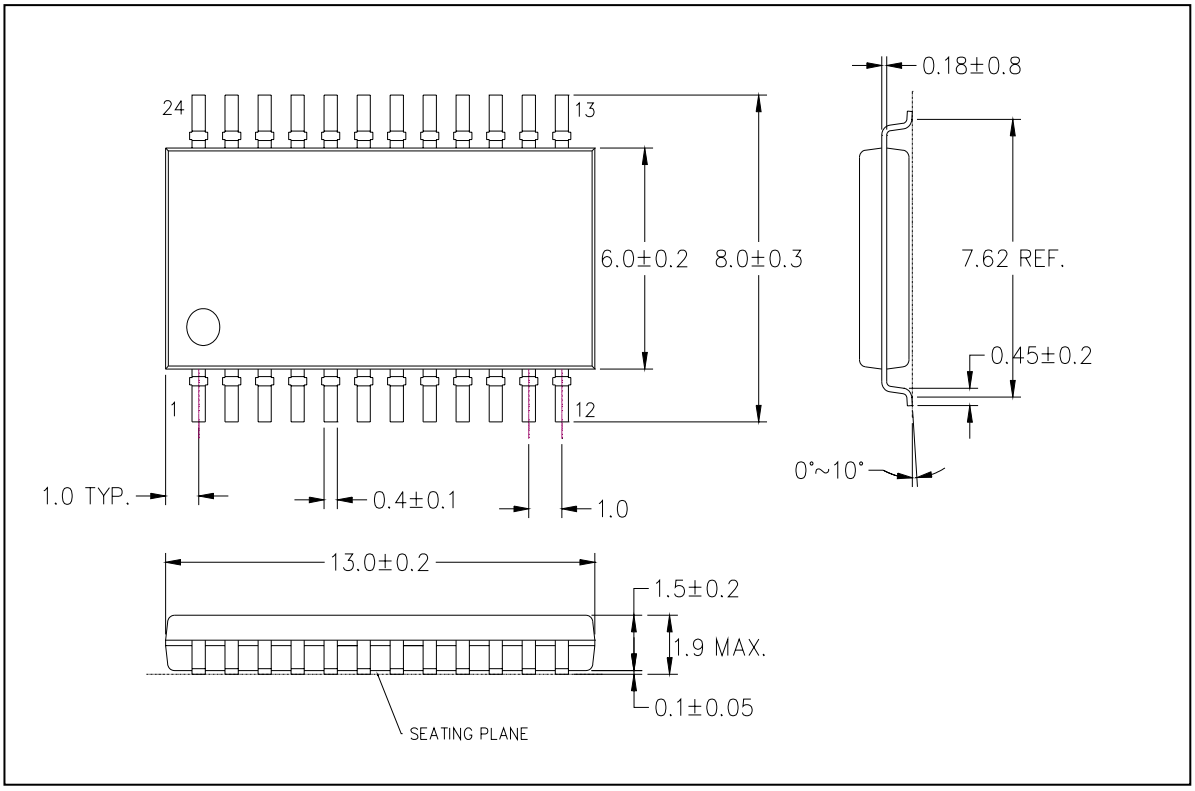
Macroblock has defined "Pb-Free" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to reflow processes which adopt tin/lead (SnPb) solder paste. Please refer to JEDEC J-STD-020C for temperature setting. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

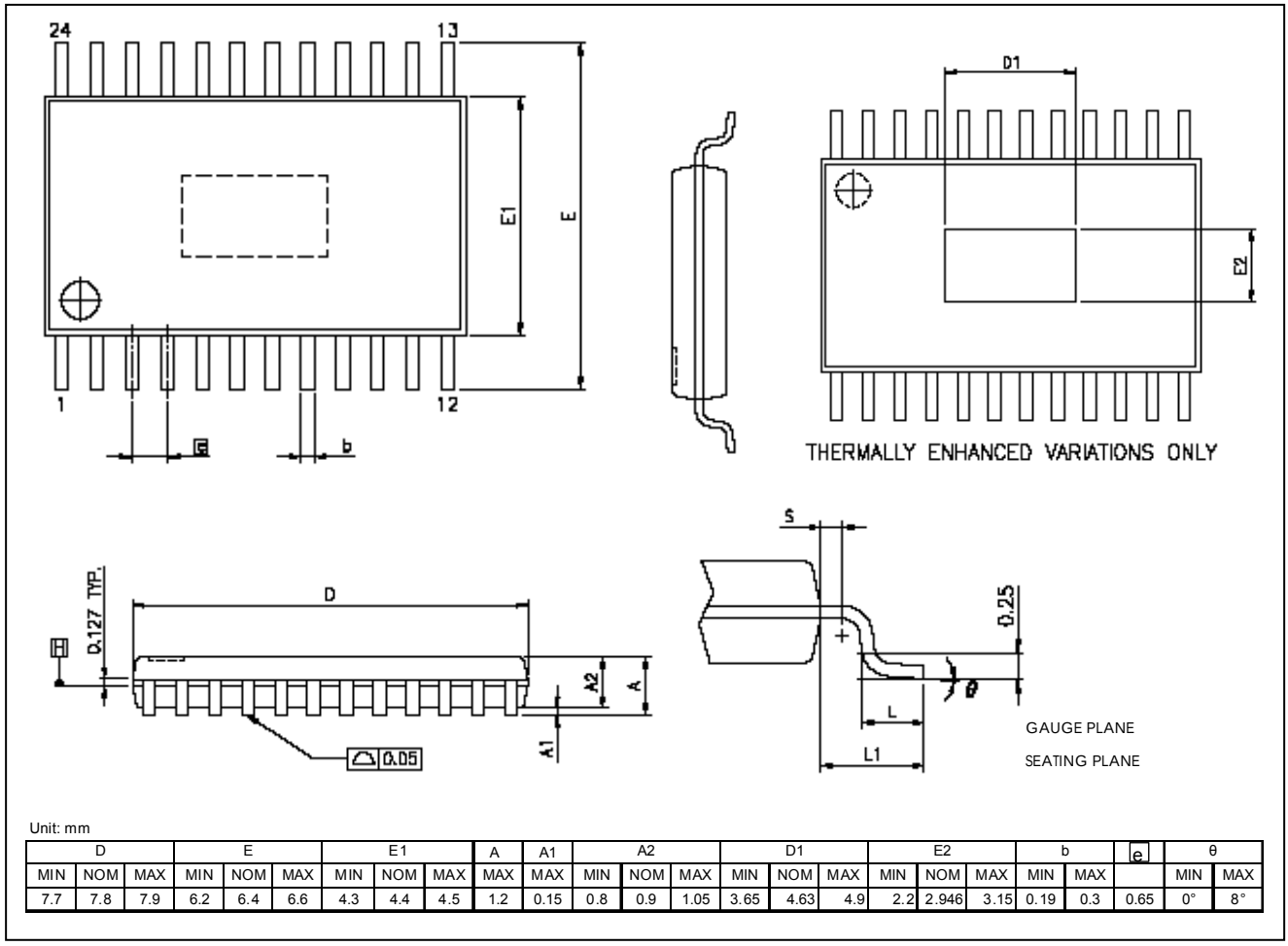
*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



MBI5040GF Outline Drawing

Note: The unit for the outline drawing is mm.



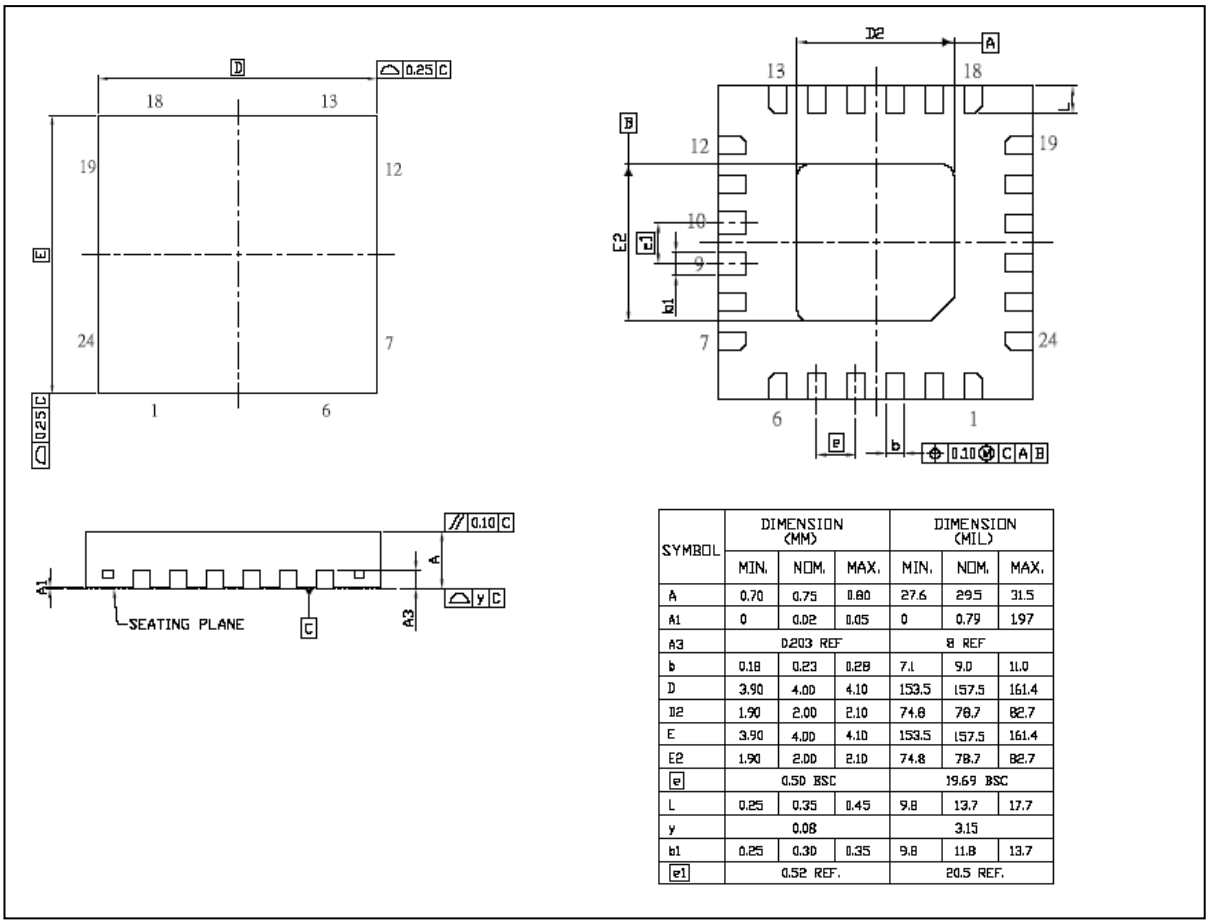
Unit: mm

D			E			E1			A	A1	A2			D1			E2			b		e	θ	
MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MAX	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	MAX		MIN	MAX
7.7	7.8	7.9	6.2	6.4	6.6	4.3	4.4	4.5	1.2	0.15	0.8	0.9	1.05	3.65	4.63	4.9	2.2	2.946	3.15	0.19	0.3	0.65	0°	8°

MBI5040 GTS Outline Drawing

Remark: The thermal pad size may exist a tolerance due to the manufacturing process, please use the maximum dimensions-D1(max.) x E2(max.) for the thermal pad layout. In addition, to avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.

Note: The unit for the outline drawing is mm.



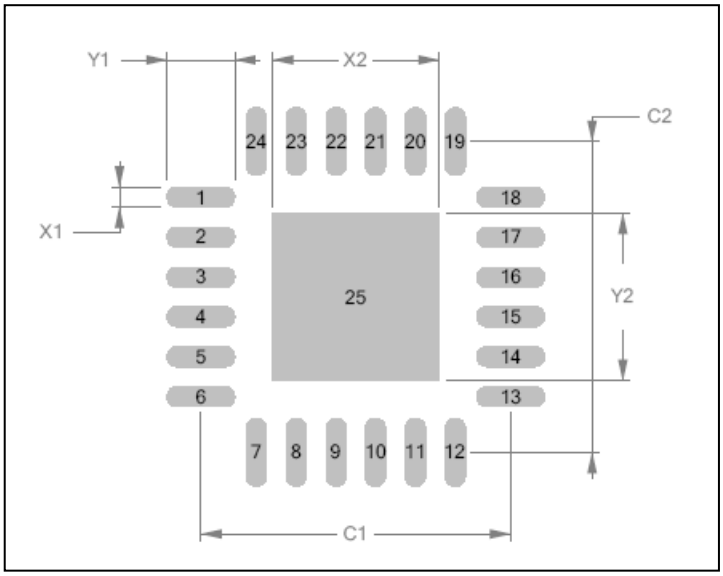
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.23	0.28	7.1	9.0	11.0
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	1.90	2.00	2.10	74.8	78.7	82.7
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	1.90	2.00	2.10	74.8	78.7	82.7
e	0.50 BSC			19.69 BSC		
L	0.25	0.35	0.45	9.8	13.7	17.7
y	0.08			3.15		
b1	0.25	0.30	0.35	9.8	11.8	13.7
e1	0.52 REF.			20.5 REF.		

MBI5040 GFN Outline Drawing

Remark: The thermal pad size may exist a tolerance due to the manufacturing process, please use the maximum dimensions-D2(max.) x E2(max.) for the thermal pad layout. In addition, to avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.

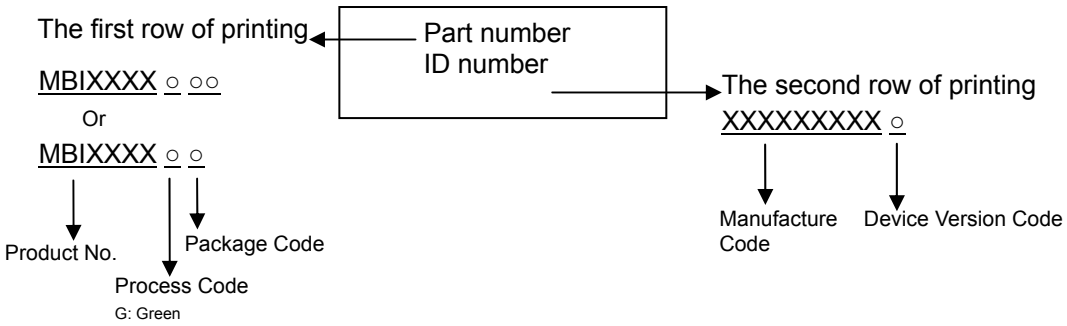
Land Pattern for GFN Package

C1-3.90mm
Y1-0.85mm
X1-0.25mm
C2-3.90mm
Y2-2.10mm
X2-2.10mm

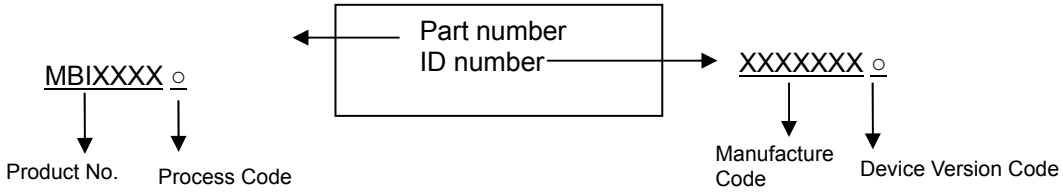


Product Top Mark Information

GF, GTS



GFN



Product Revision History

Datasheet version	Device Version Code
VA.00	A

Product Ordering Information

Part Number	RoHS Compliant Package Type	Weight (g)
MBI5040GF	SOP24L-300-1.00	0.282
MBI5040GTS	TSSOP24L-173 -0.65	0.0967
MBI5040GFN	QFN24L-4*4- 0.5	0.0379

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