

GSC2117

750mA CMOS Positive Voltage Regulator

Description

The GSC2117 of positive, linear regulators feature low quiescent current (45µA typ.) with low dropout voltage, making them ideal for battery applications.

Output voltages are set at the factory and trimmed to 1.5% accuracy.

These rugged devices have both Thermal Shutdown, and Current Fold-back to prevent device failure under the "Worst" of operating conditions.

The GSC2117 is stable with an output capacitance of 4.7µF or greater.

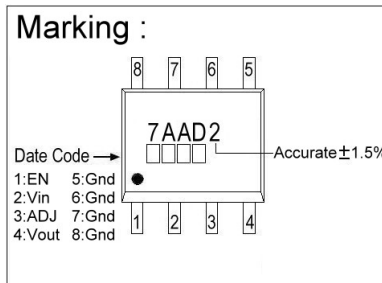
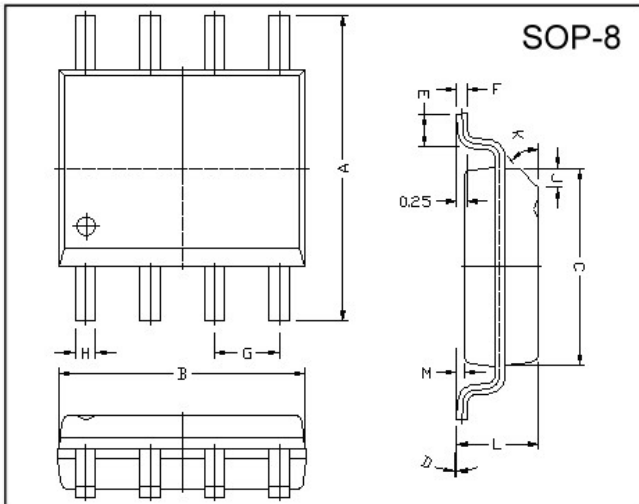
Features

- Very Low Dropout Voltage
- Guaranteed 750mA output
- Over-Temperature Shutdown
- Current Limiting
- Short Circuit Current Fold-back
- Low Temperature Coefficient
- Noise Reduction Bypass Capacitor
- Power-saving Shutdown Mode
- Adjustable Version

Applications

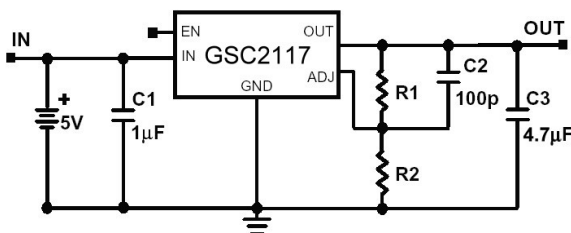
- Battery Powered Widgets
- Instrumentation
- Wireless Devices
- PC Peripherals
- Portable Electronics

Package Dimensions

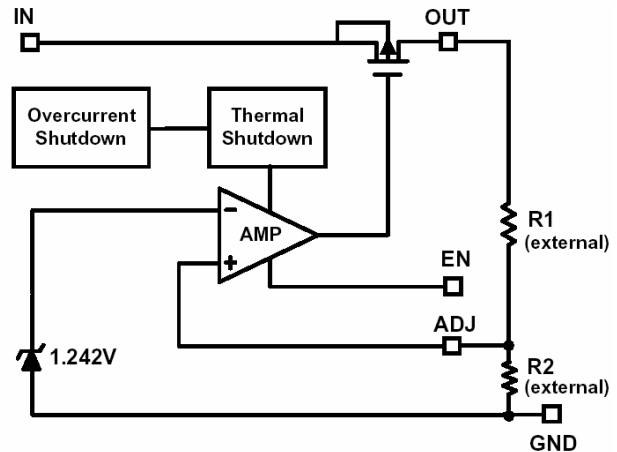


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input Max Voltage	V _{IN}	8	V
Output Current	I _{OUT}	P _D /(V _{IN} - V _O)	mA
Output Voltage	V _{OUT}	Gnd-0.3 to V _{IN} +0.3	V
Operating Ambient Temperature	T _{opr}	-40 ~ +85	°C
Junction Temperature	T _j	-40 ~ +125	°C
Maximum Junction Temperature	T _{j Max}	150	°C
Internal Power Dissipation(ΔT=100°C)	P _D	810	mW
EDS Classification		B	

Electrical Characteristics TA=25°C unless otherwise noted(V_{IN}=V_{OUT}(T) + 2V, V_{EN}=V_{IN}, C_{IN}=1μF, C_{OUT}=4.7μF)

Parameter	Symbol	Condition	Min	TYP	Max	Unit	
Output Voltage	V _{OUT} (E) (Note1)	I _O =1mA, V _{IN} =V _{OUT} (T)+2V	-1.5	V _{OUT} (T) (Note2)	1.5	%	
Output Current	I _O	V _O >1.2V	750	-	-	mA	
Current Limit	I _{LIM}	V _O >1.2V	750	-	-	mA	
Short Circuit Current	I _{SC}	V _{IN} =V _{OUT} (T)+1V, V _O < 0.4V	-	750	-	mA	
Load Regulation	REG _{LOAD}	V _{IN} =V _{OUT} (T)+2V, I _O =1mA to 750mA	-1	0.2	1	%	
Dropout Voltage	V _{DROPOUT}	I _O =750mA V _O =V _{OUT} (E)-2%	V _{OUT} (T)=1.5V	-	-	1000	mV
			V _{OUT} (T)=1.8V	-	-	650	
			V _{OUT} (T)≥2.0V	-	-	500	
Quiescent Current	I _Q	V _{IN} =V _{OUT} (T)+2V, I _O =0mA	-	45	70	μA	
Ground Pin Current	I _{GN} D	V _{IN} =V _{OUT} (T)+2V, I _O =1mA to 750mA	-	45	-	μA	
Line Regulation	REG _{LINE}	I _O =1mA V _{IN} =V _{OUT} (T)+1 to V _{OUT} (T)+2	V _{OUT} (T)<2.0V	-0.15	-	0.15	%
			2.0V≤V _{OUT} (T)<4.0V	-0.1	0.02	0.1	
			4.0V≤V _{OUT} (T)	-0.4	-	0.4	
Input Voltage	V _{IN}		Note3	-	7	V	
Over Temperature Shutdown	OTS		-	150	-	°C	
Over Temperature Hysteresis	OTH		-	30	-	°C	
Output Voltage Temperature Coefficient	TC		-	30	-	ppm/°C	
ADJ Input Bias Current	I _{ADJ}		-	1	-	μA	
Minimum Load Current	I _{Load}	V _{IN} =2.5V	-	-	70	μA	
ADJ Reference Voltage	V _{REF}		1.221	1.240	1.26	V	
Power Supply Rejection	PSRR	I _O =100mA C _O =4.7μF (ceramic)	f=1kHz	-	75	-	dB
			f=10kHz	-	55	-	
			f=100kHz	-	30	-	
Output Voltage Noise	e _N	f=10Hz~100kHz, I _O =10mA, C _O =4.7μF	-	30	-	μVrms	
EN Input Threshold	V _{EH}	V _{IN} =2.7V to 7V	2.0	-	V _{IN}	V	
	V _{EL}	V _{IN} =2.7V to 7V	0	-	0.4	V	
EN Input Bias Current	I _{EH}	V _{EN} =V _{IN} , V _{IN} =2.7V to 7V	-	-	1	μA	
	I _{EL}	V _{EN} = 0V, V _{IN} =2.7V to 7V	-	-	1	μA	
Shutdown Supply Current	I _{SD}	V _{IN} =5V, V _O =0V, V _{EN} <V _{EL}	-	0.5	2	μA	

Note 1: V_{OUT}(E) =Effective Output Voltage (i.e. the output voltage when "V_{OUT}(T) + 2.0V" is provided at the V_{IN} pin while maintaining a certain I_{OUT} value).

2: V_{OUT}(T) =Specified Output Voltage

3: V_{IN}(MIN) =V_{OUT}+V_{DROPOUT}

Ordering Information (contd.)

Part Number	Marking	Output Voltage	Part Number	Marking	Output Voltage
GSC2117-AD	7AAD2 XXXX	Adjustable			

Detailed Description

The GSC2117 of COMS regulator contains a PMOS pass transistor, voltage reference, error amplifier, over-current protection, and thermal shutdown.

The P-channel pass transistor receives data from the error amplifier, over-current shutdown, and thermal protection circuits. During normal operation, the error amplifier compares the output voltage to a precision reference. Over-current and Thermal shutdown circuits become active when the junction temperature exceeds 140°C, or the current exceeds 2.2A. During thermal shutdown, the output voltage remains low. Normal operation is restored when the junction temperature drops below 120°C.

The GSC2117 behaves like a current source when the load reaches 2.2A. However, if the load impedance drops below 0.3ohms, the current drops back to 600mA to prevent excessive power dissipation. Normal operation is restored when the load resistance exceeds 0.75ohms.

External Capacitors

The GSC2117 is stable with an output capacitance to ground of 4.7µF or greater. Ceramic capacitors have the lowest ESR, and will offer the best AC performance. Conversely, Aluminum Electrolytic capacitors exhibit the highest ESR, resulting in the poorest AC response. Unfortunately, large value ceramic capacitors are comparatively expensive. One option is to parallel a 0.1µF ceramic capacitor with a 10uF Aluminum Electrolytic. The benefit is low ESR, high capacitance, and low overall cost.

A second capacitor is recommended between the input and ground to stabilize VIN. The input capacitor should be at least 0.1µF to have a beneficial effect.

All capacitors should be placed in close proximity to the pins. A "Quiet" ground termination is desirable. This can be achieved with a "Star" connection.

Enable

When EN pin is pulled low, the PMOS pass transistor shuts off, and all internal circuits are powered down. In this state, the quiescent current is less than 2µA. This pin behaves much like an electronic switch.

100KΩ resistor is necessary between VEN source and EN pin when VEN is high than VIN.

(Note: There is no internal pull-up for EN pin. It can not be floating.)

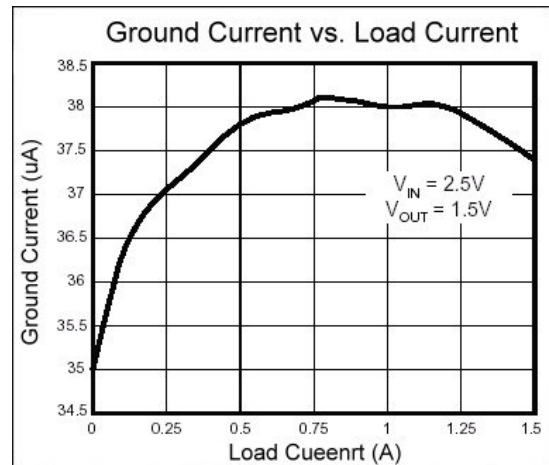
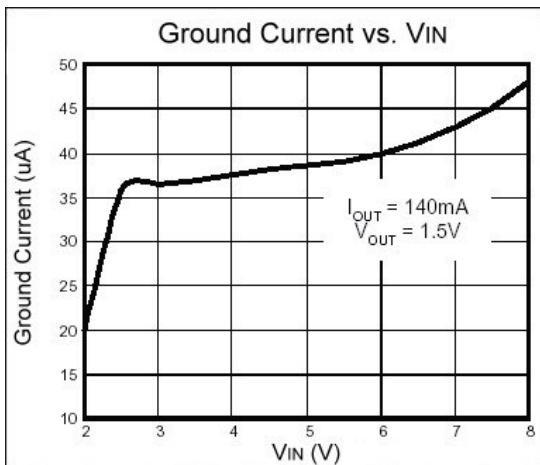
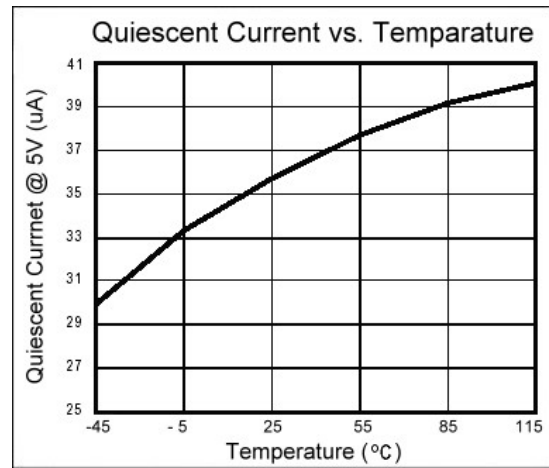
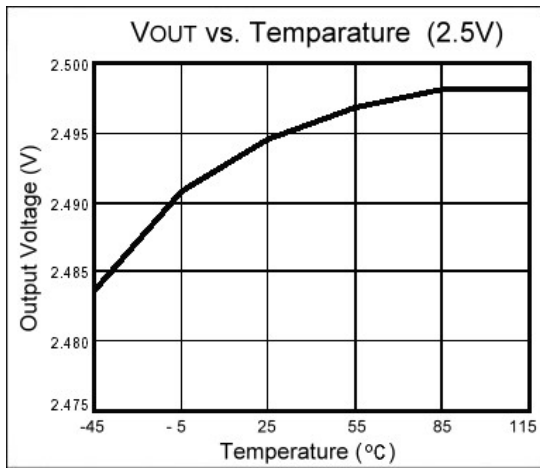
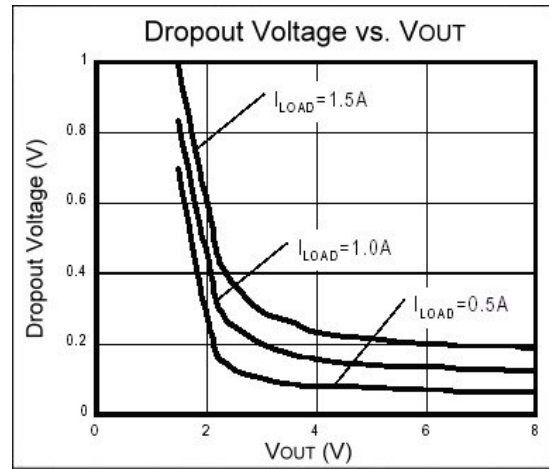
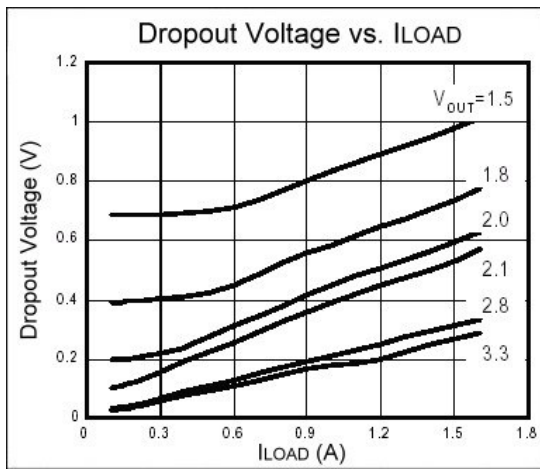
Adjustable Version

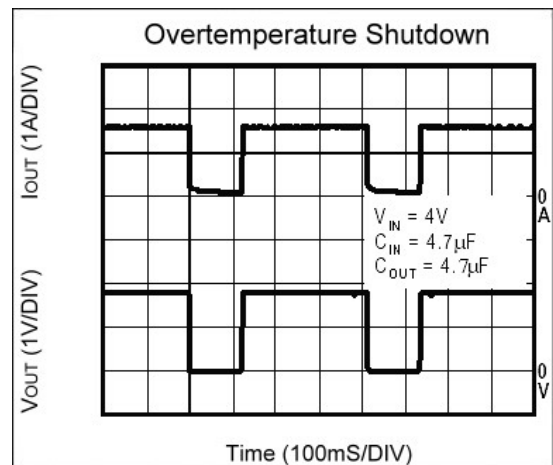
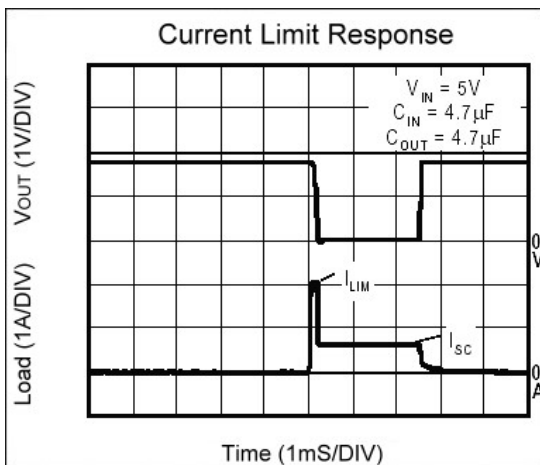
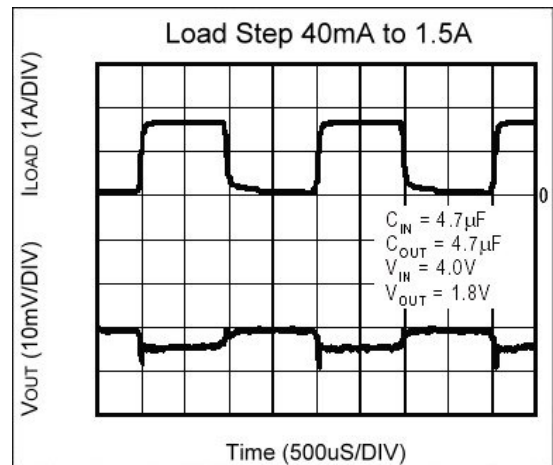
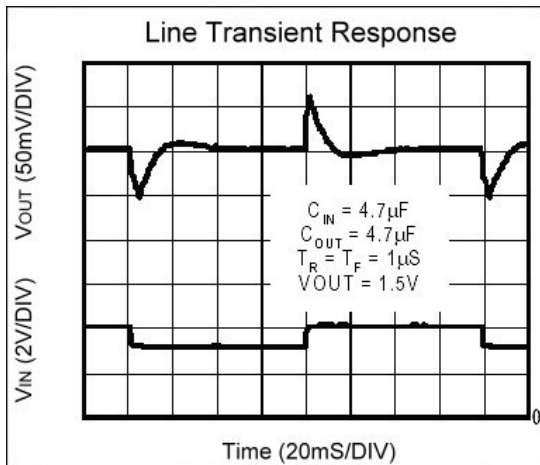
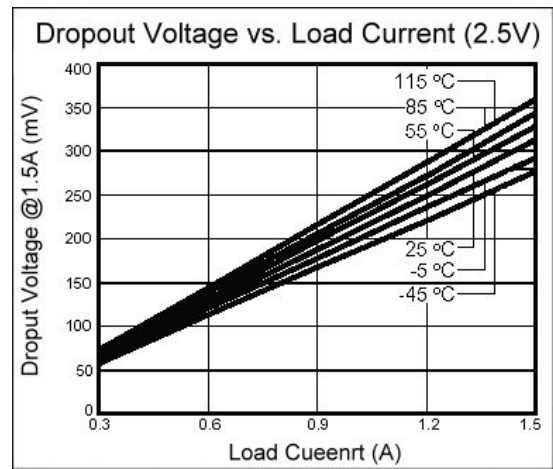
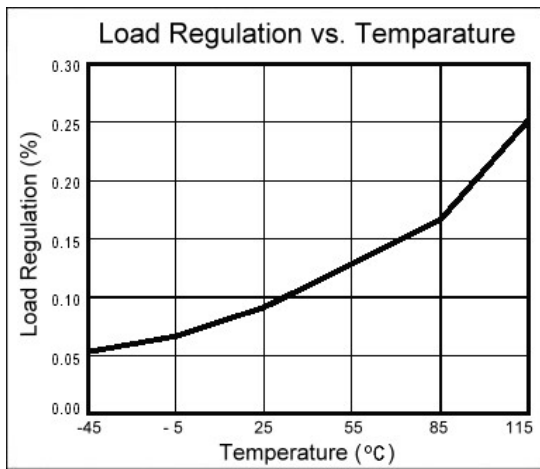
The adjustable version uses external feedback resistors to generate an output voltage anywhere from 1.5V to 5.0V. Vadj is trimmed to 1.24V and Vout is given by the equation:

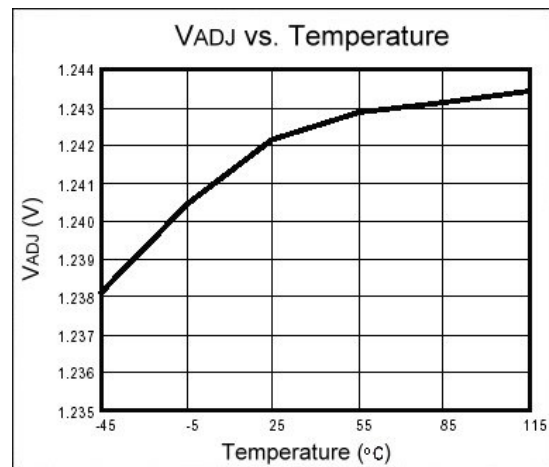
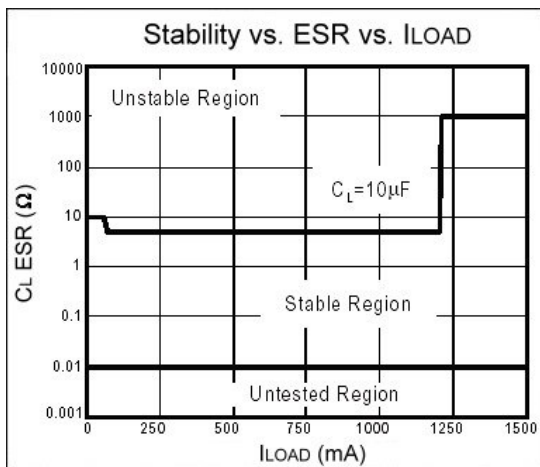
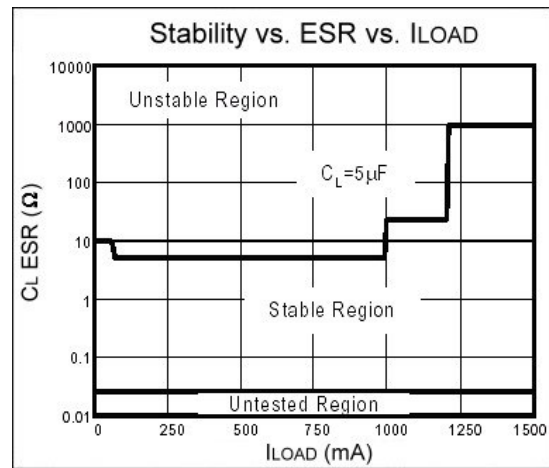
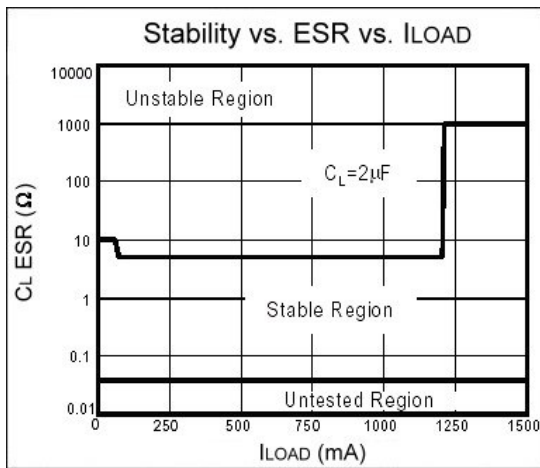
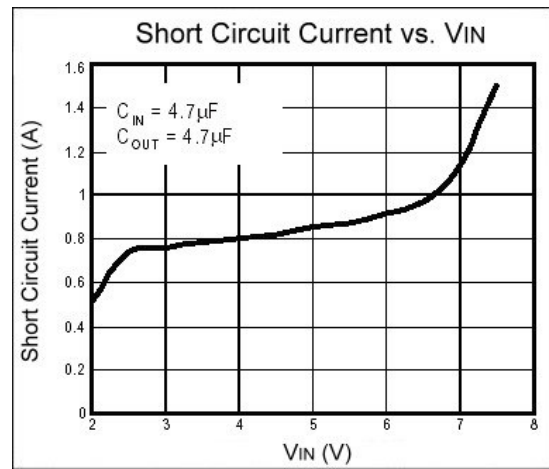
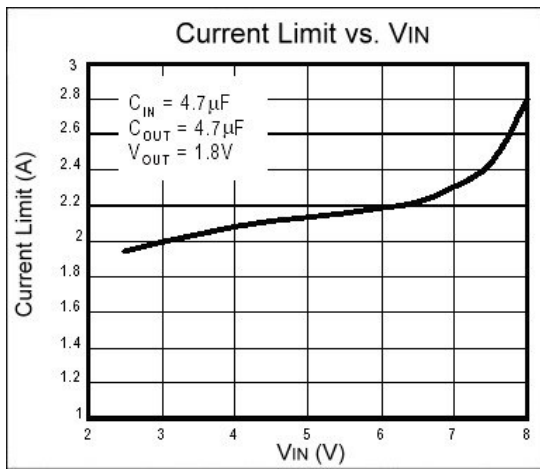
$$V_{OUT}=V_{adj} * (1+R1/R2)$$

Feedback resistors R1 and R2 should be high enough to keep quiescent current low, but increasing R1+R2 will reduce stability. In general, R1 and R2 in the 10's of kΩ will produce adequate stability, given reasonable layout precautions. To improve stability characteristics, keep parasitic on the ADJ pin to minimum, and lower R1 and R2 values.

Characteristics Curve







External Resistor Divider Table

R1(kΩ)	1	2	5	10	20
VOUT	$R2(k\Omega)=(1.24*R1(k\Omega))/(VOUT-1.24)$				
1.30	20.67	41.33	103.33	206.67	413.33
1.35	11.27	22.55	56.36	112.73	225.45
1.40	7.75	15.50	38.75	77.50	155.00
1.45	5.90	11.81	29.52	59.05	118.10
1.50	4.77	9.54	23.85	47.69	95.38
1.55	4.00	8.00	20.00	40.00	80.00
1.60	3.44	6.89	17.22	34.44	68.89
1.65	3.02	6.05	15.12	30.24	60.49
1.70	2.7	5.39	13.48	26.96	53.91
1.75	2.43	4.86	12.16	24.31	48.63
1.80	2.21	4.43	11.07	22.14	44.29
1.85	2.03	4.07	10.16	20.33	40.66
1.90	1.88	3.76	9.39	18.79	37.58
1.95	1.75	3.49	8.73	17.46	34.93
2.00	1.63	3.26	8.16	16.32	32.63
2.05	1.53	3.06	7.65	15.31	30.62
2.10	1.44	2.88	7.21	14.42	28.84
2.15	1.36	2.73	6.81	13.63	27.25
2.20	1.29	2.58	6.46	12.92	25.83
2.25	1.23	2.46	6.14	12.28	24.55
2.30	1.17	2.34	5.85	11.70	23.40
2.35	1.12	2.23	5.59	11.17	23.34
2.40	1.07	2.14	5.34	10.69	21.38
2.45	1.02	2.05	5.12	10.25	20.50
2.50	0.98	1.97	4.92	9.84	19.68
2.55	0.95	1.89	4.73	9.47	18.93
2.60	0.91	1.82	4.56	9.12	18.24
2.65	0.88	1.76	4.40	8.79	17.59
2.70	0.85	1.70	4.25	8.49	16.99
2.75	0.82	1.64	4.11	8.21	16.42
2.80	0.79	1.59	3.97	7.95	15.90
2.85	0.77	1.54	3.85	7.70	15.40
2.90	0.75	1.49	3.73	7.47	14.94
2.95	0.73	1.45	3.63	7.25	14.50
3.00	0.70	1.41	3.52	7.05	14.09
3.05	0.69	1.37	3.43	6.85	13.70
3.10	0.67	1.33	3.33	6.67	13.33
3.15	0.65	1.30	3.25	6.49	12.98

R1(kΩ)	1	2	5	10	20
VOUT	$R2(k\Omega)=(1.242*R1(k\Omega))/(VOUT-1.242)$				
3.20	0.63	1.27	3.16	6.33	12.65
3.25	0.62	1.23	3.08	6.17	12.34
3.30	0.60	1.20	3.01	6.02	12.04
3.35	0.59	1.18	2.94	5.88	11.75
3.40	0.57	1.15	2.87	5.74	11.48
3.45	0.56	1.12	2.81	5.61	11.22
3.50	0.55	1.10	2.74	5.49	10.97
3.55	0.54	1.07	2.68	5.37	10.74
3.60	0.53	1.05	2.63	5.25	10.51
3.65	0.51	1.03	2.57	5.15	10.29
3.70	0.50	1.01	2.52	5.04	10.08
3.75	0.49	0.99	2.47	4.94	9.88
3.80	0.48	0.97	2.42	4.84	9.69
3.85	0.48	0.95	2.38	4.75	9.50
3.90	0.47	0.93	2.33	4.66	9.32
3.95	0.46	0.92	2.29	4.58	9.15
4.00	0.45	0.90	2.25	4.49	8.99
4.05	0.44	0.88	2.21	4.41	8.83
4.10	0.43	0.87	2.17	4.34	8.67
4.15	0.43	0.85	2.13	4.26	8.52
4.20	0.42	0.84	2.09	4.19	8.38
4.25	0.41	0.82	2.06	4.12	8.24
4.30	0.41	0.81	2.03	4.05	8.10
4.35	0.40	0.80	1.99	3.99	7.97
4.40	0.39	0.78	1.96	3.92	7.85
4.45	0.39	0.77	1.93	3.86	7.73
4.50	0.38	0.76	1.90	3.80	7.61
4.55	0.37	0.75	1.87	3.75	7.49
4.60	0.37	0.74	1.85	3.69	7.38
4.65	0.36	0.73	1.82	3.64	7.27
4.70	0.36	0.72	1.79	3.58	7.17
4.75	0.35	0.71	1.77	3.53	7.07
4.80	0.35	0.70	1.74	3.48	6.97
4.85	0.34	0.69	1.72	3.43	6.87
4.90	0.34	0.68	1.69	3.39	6.78
4.95	0.33	0.67	1.67	3.34	6.68
5.00	0.33	0.66	1.65	3.30	6.60

Note: Small load (greater than 2mA) is necessary as R1 or R2 is larger than 50kΩ. Otherwise, output voltage probably can not be pulled down to 0V on disable mode.

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