64Kx18 Monolithic High Speed Synchronous Static RAM

ADVANCE INFORMATION

The EDI20180C is a high performance, 1 megabit Synchronous Static RAM organized as 64Kx18, available in six versions.

Inputs are registered or latched on the rising edge of CLK (K), depending on version. The output can be self-timed, registered, or latched, also depending on version.

Address, Data, and Control need to be held valid for a small percentage of cycle time and output timing can be matched to very tight system constraints.

These options allow the designer tremendous flexibility in the design of very high speed computer systems.

Features

64Kx18 bit Synchronous Static Random Access Memory

- Fast Access Times 15, 20 and 25ns
- Works with System Clocks to 65Mhz
- 18 Common Data Input/Output Lines

Surface Mount Package (Proposed)

- 52 Pad PLCC, No. 26

Single +5V (±10%) Supply Operation

Part No.	Input	Output	#CLK
EDI20180C	Latched	Latched	1
EDI20181C	Registered	Registered	1
EDI20182C	Latched	Asynchronous	1
EDI20183C	Registered	Asynchronous	1
EDI20184C	Latched	Registered	2
EDI20185C	Registered	Registered	2

Pin Names

AØ-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G1}$-$\overline{G2}$	Output Enables
K1-K2	Clock
DQØ-DQ17	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Pinout

To be determined

Functional Block Diagram