9 Electrical and Physical Specifications

This chapter describes the CL480's electrical and mechanical characteristics.

9.1 Operating Conditions

Tables 9-1 through 9-3 specify the CL480's electrical characteristics.

Table 9-1 Operating Conditions

Parameters		Commercial Min	Commercial Max	Unit
V_{DD3}	Supply Voltage	2.7[1]	3.6	V
V_{DDMAX}	VDDMAX pin (max input voltage)	V_{DD3}	5.25	V

1. Silicon revision A3 is 3.0V.

Table 9-2 Absolute Maximum Ratings[1]

Parameter	Value
Supply voltage (V_{DD3})	-0.3 to 4.5 V
Input voltage[2]	-0.3 to V_{DDMAX} + 0.25V
Output voltage	-0.3 to (V_{DD3} +0.5)
Storage temperature range	-55°C to 150°C
Operating temperature range (ambient)	-10°C to 70°C
Reflow soldering temperature	240°C for 5 Seconds Maximum

1. Exposure to stresses beyond those listed in this table may result in device unreliability, permanent damage, or both.
2. 5.5V is the maximum for all input voltages except XTL IN (pin 19), which should be 4.0V.

Table 9-3 DC Characteristics

Parameters		Test Conditions	Commercial			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage [1]	V_{DD} = MAX	2.4			V
V_{IL}	Low-level input voltage [1]	V_{DD} = MIN			0.8	V
$V_{IH\ (OSC)}$ [2]	High-level OSC input V.	V_{DD3} = MAX	$0.8V_{DD3}$		V_{DD3}+ 0.2V	V
$V_{IL\ (OSC)}$ [2]	Low-level OSC input V.		0		$0.2V_{DD3}$	V
V_{OH27}	High-level output voltage	V_{DD} = 2.7V, I_{OH} = -2 mA	2.1			V
V_{OH30}	High-level output voltage	V_{DD} = 3.0V, I_{OH} = -2 mA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} = MIN, I_{OL} = 2 mA			0.5	V
I_{IH}	High-level input current	V_{DD} = MAX, HostV_{DD} = MAX DRAMV_{DD} = MAX			10	µA
I_{IL}	Low-level input current	V_{DD} = MAX, V_{IN} = 0 V	-10			µA
I_{OZ}	Output leakage current	Hi-Z output driven to 0V and 5.25 V	-10		+10	µA
I_{DD27}	Supply Current [3] @ V_{DD3} = 2.7V	GCK = 40MHz V_{IN} = 0 or 2.7V, C_L=50pF, Ta=70°C		150	200	mA
I_{DD33}	Supply Current @ V_{DD3} = 3.3V	GCK = 40MHz V_{IN} = 0 or 3.3V, C_L=50pF, Ta=70°C		180	240	mA
I_{DD36}	Supply Current @ V_{DD3} = 3.6V	GCK = 40MHz V_{IN} = 0 or 3.6V, C_L=50pF, Ta=70°C		200	270	mA
C_{IN}	Input Capacitance [1]			10		pF
C_{OUT}	Output Capacitance [1]			12		pF
CI/O	Output Capacitance [1]			12		pF

1. Not 100% tested, guaranteed by design characterization
2. This value refers to XTL IN, pin 19.
3. Supply current is a few percent lower at -10°C than 70°C.

9.1.1 Duty Cycle

The CL480 was designed for GCK and VCK duty cycles of 55/45.

9.1.2 Power Pin Supply Voltages

Pins 7, 21, 22, 29, 49, 65, 77, 81, 98, 110, and 112 should be connected to 2.7 to 3.6 volts. The maximum voltage output by the CL480 is the voltage on these pins. Pins 43 and 123 should be connected to the maximum voltage that any of the inputs or I/Os will receive. For example, if a 5-volt DRAM and a 3-volt host are being used, connect both these pins to 5 volts.

9.1.3 Power-Up and Power-Down Constraints

During power-up and power-down, the 5-volt supply voltage (VDDMAX) should always be at a higher voltage than the 3.3-volt supply. The 5-volt supply is connected to the N-well of the P-channel output transistor in the I/O pads. The source terminal of this transistor is connected to 3.3 volts. If the 3.3-volt supply is more than about .6 volts above the 5-volt supply, the diode between the P-diffusion and the N-well conducts current, which could latch up the chip or destroy the bond wires for the 5-volt supply.

9.2 AC Timing Characteristics

This section describes the AC timing characteristics of the CL480. The timing characteristics are divided into related groups.

- GCK, $\overline{\text{RESET}}$ and CFLEVEL Timing:
  - Figure 9-1, Timing Diagram - GCK (XTLIN)
  - Figure 9-2, Timing Diagram - $\overline{\text{RESET}}$
  - Figure 9-3, Timing Diagram - CFLEVEL
  - Table 9-4, Timing Characteristics, GCK, $\overline{\text{RESET}}$ and CFLEVEL
- Host Bus Interface Timing:
  - Figure 9-4, Host Interface Local Register, Write Operation
  - Table 9-5, Timing Characteristics, Local Register Write
  - Figure 9-4, Host Interface Local Register, Read Operation
  - Table 9-6, Timing Characteristics - Local Register Read
- DRAM/ROM Bus Timing:
  - Figure 9-6, Local DRAM Bus Timing
  - Figure 9-7, Local DRAM $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh
  - Table 9-7, Timing Characteristics - Local DRAM Bus
- CD Interface Timing:
  - Figure 9-8, CD Input: Data Latch Timing High
  - Figure 9-9, CD Input: Data Latch Timing Low
  - Table 9-8, CD Input Timing
- CD Subcode (CD+G) Interface Timing:
  - Figure 9-10, Clocking CD Subcode Data
  - Figure 9-11, Separate CD Subcode Control Signals
  - Figure 9-12, Composite CD Subcode Control Signals
  - Table 9-9, Timing Characteristics: CD+G (Preliminary)
- Video Bus Timing
  - Figure 9-13, VCK (In and Out)
  - Table 9-10, Timing Characteristics: VCK

- Figure 9-14, $\overline{\text{VOE}}$ and VD
- Table 9-11, Timing Characteristics: $\overline{\text{VOE}}$ and VD
- Figure 9-15, VCK and VD (pixel data)
- Table 9-12, Timing Characteristics: VCK and VD
- Figure 9-16, $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ Out
- Figure 9-17, $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ In
- Figure 9-18, VCK Out to $\overline{\text{HSYNC}}$ Out
- Figure 9-19, $\overline{\text{HSYNC}}$ In to VCK In
- Figure 9-20, VCK In to $\overline{\text{HSYNC}}$ Out
- Figure 9-21, $\overline{\text{HSYNC}}$ In to VCK Out
- Table 9-13, Timing Characteristics: VCK and $\overline{\text{HSYNC}}$
- Figure 9-22, VCK Out to CSYNC/$\overline{\text{VSYNC}}$ Out
- Figure 9-23, VCK In to CSYNC/$\overline{\text{VSYNC}}$ Out
- Table 9-14, Timing Characteristics: VCK and CSYNC/$\overline{\text{VSYNC}}$

- Audio Bus Timing
  - Figure 9-24, Audio Interface Timing Modes
  - Table 9-15, Timing Characteristics: Audio

9.2.1 GCK (XTLIN), $\overline{\text{RESET}}$ and CFLEVEL Timing

This section describes CL480 GCK, $\overline{\text{RESET}}$ and CFLEVEL timing.

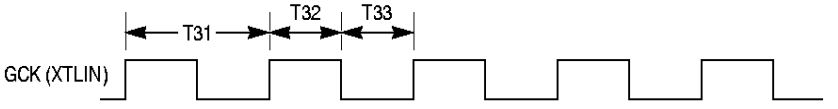


Figure 9-1 Timing Diagram - GCK (XTLIN)

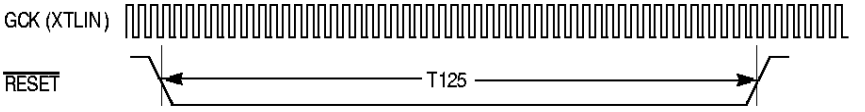


Figure 9-2 Timing Diagram - $\overline{\text{RESET}}$

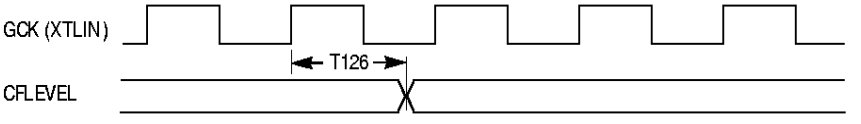


Figure 9-3 Timing Diagram - CFLEVEL

Table 9-4 Timing Characteristics - GCK, $\overline{\text{RESET}}$, and CFLEVEL

Time	Description	Min	Max	Units
T31	GCK (XTLIN) period	24.5	25.6	ns
T32	GCK (XTLIN) HIGH pulse width	10		ns
T33	GCK (XTLIN) LOW pulse width	10		ns
T125	$\overline{\text{RESET}}$ pulse width	10 (T31)		
T126	CFLEVEL access time from GCK HIGH	38		ns

9.2.2 Host Bus Interface Timing

This section describes the host-related AC timing of the CL480.

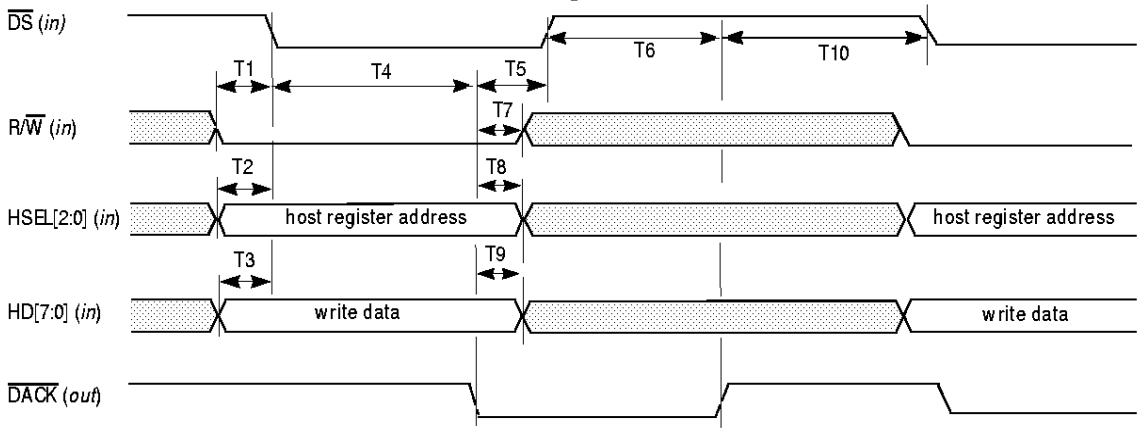


Figure 9-4 Host Interface Local Register, Write Operation

Table 9-5 Timing Characteristics - Local Register Write

Time	Description	Min	Max	Units
T1	R/$\overline{\text{W}}$ valid to $\overline{\text{DS}}$ LOW	0		ns
T2	HSEL[2:0] valid to $\overline{\text{DS}}$ LOW	0		ns
T3	HD[7:0] valid to $\overline{\text{DS}}$ LOW	0		ns
T4	$\overline{\text{DS}}$ LOW to $\overline{\text{DACK}}$ LOW	(note)[1]	(note)[2]	
T5	$\overline{\text{DACK}}$ LOW to $\overline{\text{DS}}$ HIGH	3		ns
T6	$\overline{\text{DS}}$ HIGH to $\overline{\text{DACK}}$ HIGH	1 GCK	2 GCK	
T7	R/$\overline{\text{W}}$ holds after $\overline{\text{DACK}}$ LOW	0		ns
T8	HSEL[2:0] holds after $\overline{\text{DACK}}$ LOW	0		ns
T9	HD[7:0] holds after $\overline{\text{DACK}}$ LOW	0		ns
T10	$\overline{\text{DACK}}$ HIGH to $\overline{\text{DS}}$ LOW (next operation)	5		ns

1. (GCK * 2) when A_MSB, A_MB, A_LSB and D_LSB write operation; (GCK * 21) when CFIFO D_MSB write; (GCK * 6) when D_MSB write.
2. (GCK * 3) when A_MSB, A_MB, A_LSB and D_LSB write operation; (GCK * 22) when CFIFO D_MSB write; (GCK * 6 + GBUS waiting time) when D_MSB write. Note: GBUS waiting time can be from 0 to over 500 GCKs.

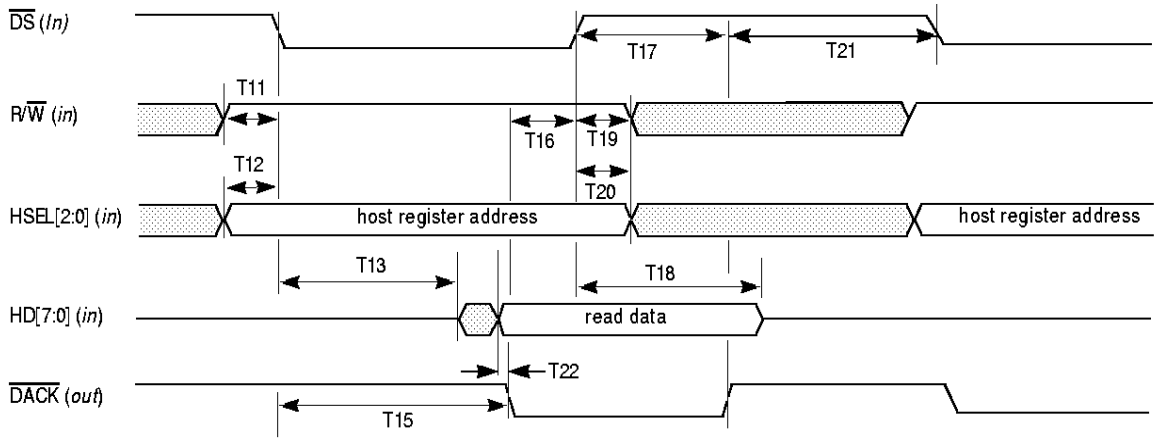


Figure 9-5 Host Interface Local Register, Read Operation

Table 9-6 Timing Characteristics - Local Register Read

Time[1]	Description	Min	Max	Units
T11	R/$\overline{W}$ valid to $\overline{DS}$ LOW	0		ns
T12	HSEL[2:0] valid to $\overline{DS}$ LOW	0		ns
T13	$\overline{DS}$ LOW to HD[7:0] (non-tristate)	20		ns
T15	$\overline{DS}$ LOW to $\overline{DACK}$ LOW	Note[2]	Note[3]	ns
T16	$\overline{DACK}$ LOW to $\overline{DS}$ HIGH	3		ns
T17	$\overline{DS}$ HIGH to $\overline{DACK}$ HIGH	1 GCK	3 GCK	
T18	$\overline{DS}$ HIGH to HD[7:0] tristate	1 GCK	3 GCK	
T19	R/$\overline{W}$ hold after $\overline{DS}$ HIGH	0		
T20	HSEL[2:0] hold after $\overline{DS}$ HIGH	0		
T21	$\overline{DACK}$ HIGH to $\overline{DS}$ LOW (next operation)	5		ns
T22	HD[7:0] setup to $\overline{DACK}$ LOW	10[4]		ns

1. Not 100% tested, guaranteed by design.
2. (GCK * 2) when A_MSB and D_LSB read; (GCK * 6) when D_MSB read
3. GCK * 3) when A_MSB and D_LSB read; (GCK * 6) + GBUS waiting time when D_MSB read
4. Note: A3 silicon is -10 ns.

9.2.3 DRAM/ROM Bus Timing

Local DRAM/ROM Bus Timing is shown next.

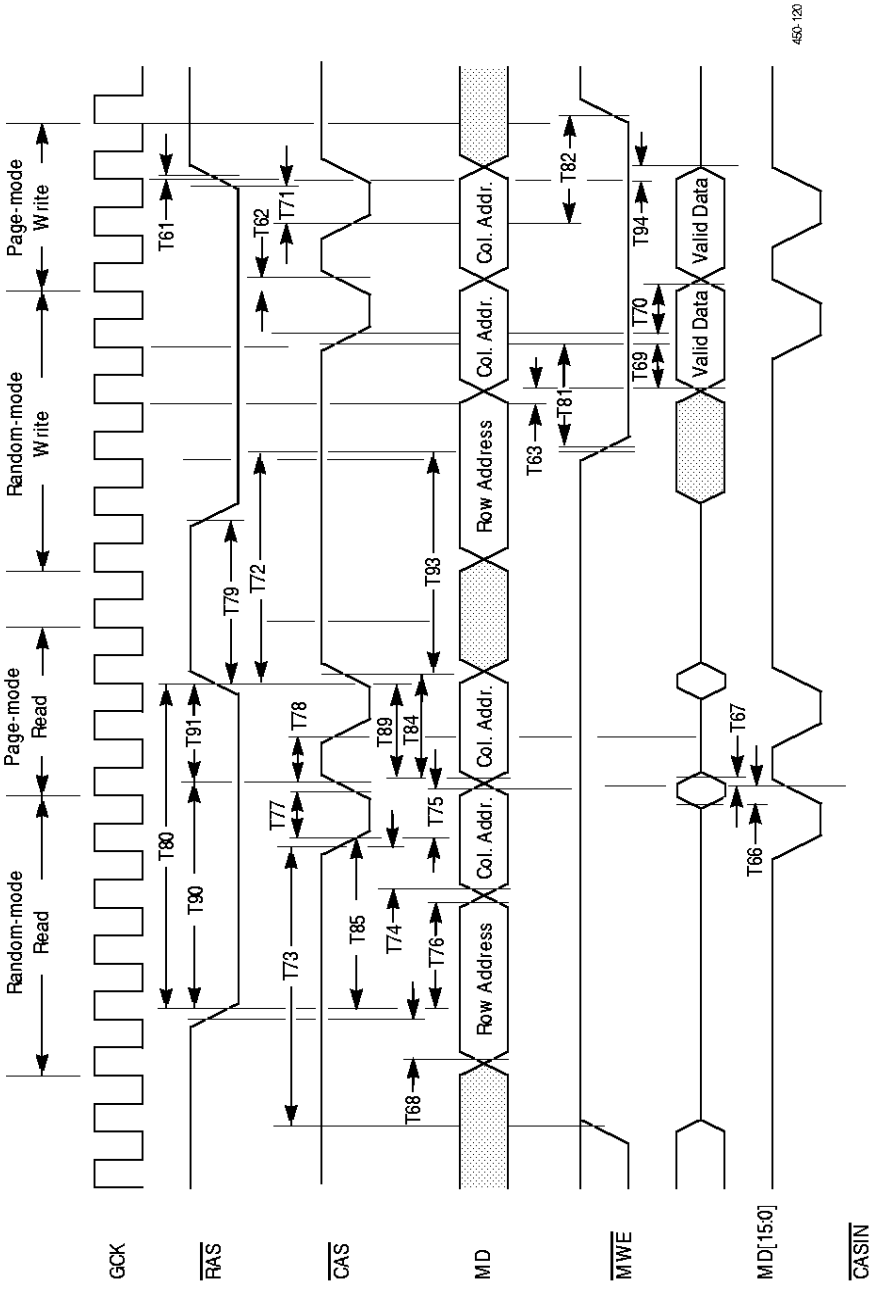


Figure 9-6 Local DRAM Bus Timing

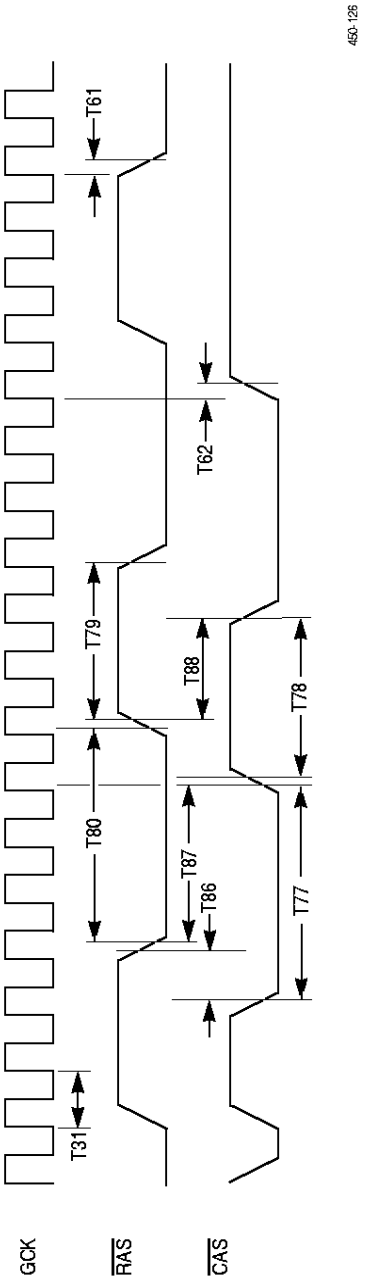


Figure 9-7 Local DRAM CAS-before-RAS Refresh

Table 9-7 Timing Characteristics - Local DRAM Bus[1, 2]

Time	Description	Parameter	Min	Max	Units
T66	Read Data Setup Time before $\overline{CASIN}$ HIGH		5		ns
T67	Read Data Hold Time after $\overline{CASIN}$ HIGH		5		ns
T68	Row Address Setup Time [2]	t_{ASR}	5		ns
T69	Write Data Setup Time before $\overline{CAS}$ LOW [2]	t_{DS}	5		ns
T70	Write Data Hold Time after $\overline{CAS}$ LOW [2]	t_{DH}	15		ns
T71	$\overline{RAS}$ Hold Time after $\overline{CAS}$ LOW [2]	t_{RSH}	20		ns
T72	Read Command Hold Time from $\overline{RAS}$ [2]	t_{RRH}	2		ns
T73	Read Command Setup Time to $\overline{CAS}$ LOW [2]	t_{RCS}	15		ns
T74	Column Address Setup Time to $\overline{CAS}$ LOW [2]	t_{ASC}	5		ns
T75	Column Address Hold Time from $\overline{CAS}$ LOW [2]	t_{CAH}	15		ns
T76	Row Address Hold Time from $\overline{RAS}$ LOW [2]	t_{RAH}	10		ns
T77	$\overline{CAS}$ LOW Time [2]	t_{CAS}	21		ns
T78	$\overline{CAS}$ HIGH Time [2]	t_{CP}	10		ns
T79	$\overline{RAS}$ HIGH Time [2]	t_{RP}	62		ns
T80	$\overline{RAS}$ LOW Time [2]	t_{RAS}	80	5000	ns
T81	Write Setup time to $\overline{CAS}$		10		ns
T82	Write Command Hold Time from $\overline{CAS}$ LOW [2]	t_{WCH}	15		ns
T84	Column Address to $\overline{CAS}$ HIGH [2]	t_{AA} + T66	45		ns
T85	$\overline{RAS}$ to $\overline{CAS}$ delay [2]	t_{RCD}	50		ns
T86	$\overline{CAS}$ Setup Time to $\overline{RAS}$ (Memory Refresh Cycle) [2]	t_{CSR}	10		ns
T87	$\overline{CAS}$ Hold Time from $\overline{RAS}$ (Memory Refresh Cycle) [2]	t_{CHR}	15		ns
T88	$\overline{RAS}$ HIGH to $\overline{CAS}$ LOW delay (Memory Refresh Cycle) [2]	t_{RPC}	0		ns
T89	Column Address to $\overline{RAS}$ HIGH [2]	t_{RAL}	40		ns
T90	$\overline{RAS}$ LOW to $\overline{CAS}$ HIGH [2]	t_{RAC} + T66	85		ns
T91	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge [2]	t_{RHCP}	47		ns
T93	Read Command Hold Time from $\overline{CAS}$	t_{RRH},t_{RCH}	0		ns
T94	GCK to MD three-state (write)		15	40	ns

1. Inputs switch between 0.0V and 3.5V at 1V/ns and measurements are made at 0.8V and 2.4V. Output load capacitance = 50 pF.
2. Not 100% tested, guaranteed by design.

9.2.4 CD Interface Timing

Figures 9-8 and 9-9 and Table 9-8 show the timing for each of the six different CD signal input formats.

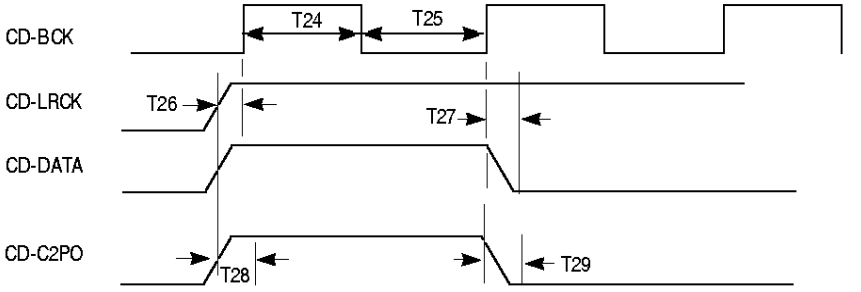


Figure 9-8 CD Input: Data Latch Timing High

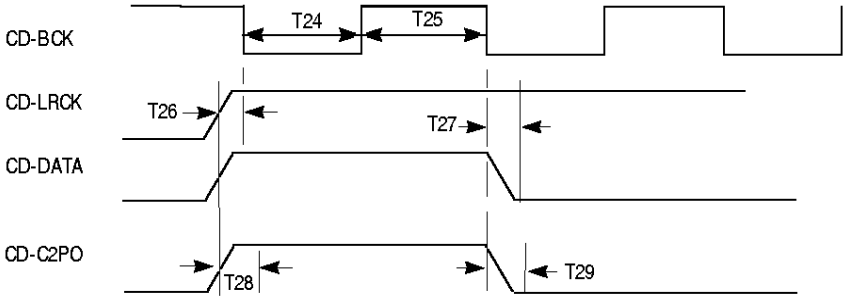


Figure 9-9 CD Input: Data Latch Timing Low

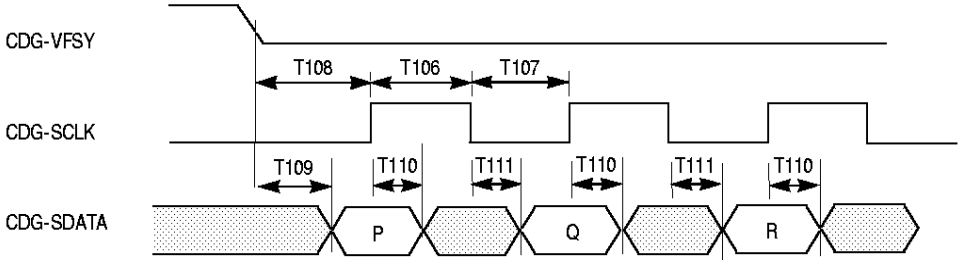
Table 9-8 CD Input Timing[1]

Time	Description	Min	Max	Units
T24	CD-BCK High Pulse Width	(3 GCKs)		
T25	CD-BCK Low Pulse Width	(3 GCKs)		
T26	CD-DATA, CD-LRCK setup	10		ns
T27	CD-DATA, CD-LRCK hold	10		ns
T28	CD-C2PO setup	10		ns
T29	CD-C2PO hold	10		ns

1. Not 100% tested, guaranteed by design.

9.2.5 CD Subcode (CD+G) Interface Timing

Timing for the four CD+G signal pins is shown in Figures 9-10 to 9-12 and Table 9-9. CD+G functions are available only in Silicon Revision C and later silicon. In all cases, new bits of subcode are clocked in on each rising edge of CDG-SCLK as Figure 9-10 shows.



Note: CDG-SCLK must remain LOW between clocking in the "W" subcode bit and the next falling CDG-VFSY edge.

Figure 9-10 Clocking CD Subcode Data

The CL480 supports two different subcode control signal formats. One format uses separate block and frame synchronization signals (see Figure 9-11), and the other format uses a composite frame/block signal as Figure 9-12 shows.

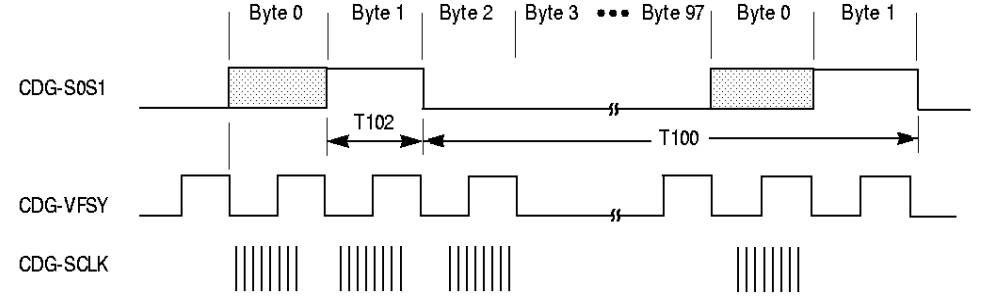


Figure 9-11 Separate CD Subcode Control Signals

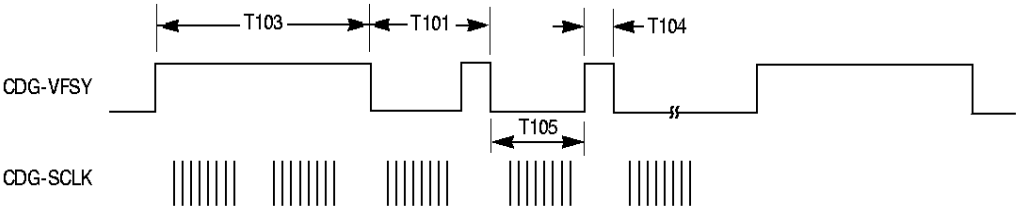


Figure 9-12 Composite CD Subcode Control Signals

Table 9-9 Timing Characteristics: CD+G (Preliminary)

Time[1]	Description	Min	Max	Units
T100	Block period	12.0	14.7	ms
T101	Frame period	122	150	µs
T102	CDG-S0S1 HIGH pulse width	122	800	µs
T103	Composite VFSY HIGH pulse width at start of block	244	800	µs
T104	CDG-VFSY HIGH pulse width	4		µs
T105	CDG-VFSY LOW pulse width	1.5		µs
T106	CDG-SCLK (input) HIGH pulse width	2	6	µs
T107	CDG-SCLK (input) LOW pulse width	2	6	µs
T108	Delay time from CDG-VFSY LOW to CDG-SCLK HIGH edge for "P" subcode bit (CDG-SCLK input)	10	30	µs
T109	Subcode "P" bit access time from CDG-VFSY LOW edge		10	µs
T110	CDG-SDATA hold time from CDG-SCLK HIGH	0		ns
T111	CDG-SDATA access time from CDG-SCLK LOW		80	ns

1. Not 100% tested, guaranteed by design.

9.2.6 Video Bus Timing

Timing diagrams for video output are shown in the following pages.

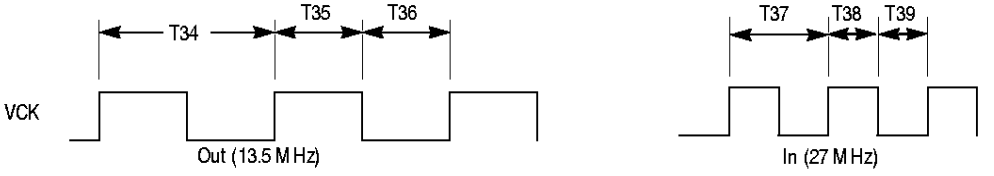


Figure 9-13 Timing - VCK (In and Out)

Table 9-10 Timing Characteristics: VCK

Time[1]	Description	Min	Max	Units
T34	VCK (Out) Frequency (13.5 MHz)	3 GCK	3 GCK	
T35	VCK (Out) HIGH	33	42	ns
T36	VCK (Out) LOW	33	42	ns
T37	VCK (In) Frequency (27 MHz)	26.8 GCK	27.2 GCK	MHz
T38	VCK (In) HIGH	16		ns
T39	VCK (In) LOW	16		ns

1. Not 100% tested, guaranteed by design.

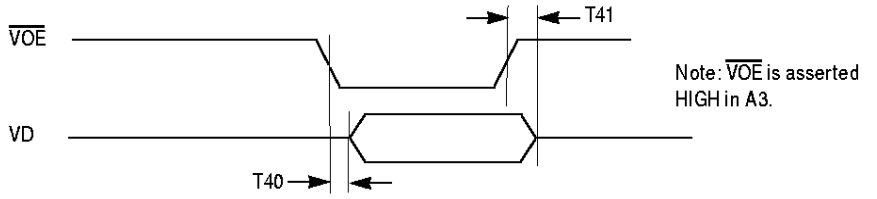


Figure 9-14 Timing - $\overline{VOE}$ and VD

Table 9-11 Timing Characteristics: $\overline{VOE}$ and VD

Time[1]	Description	Min	Max	Units
T40	$\overline{VOE}$ LOW to VD non-tristate	3	25	ns
T41	$\overline{VOE}$ HIGH to VD tristate	3	25	ns

1. Not 100% tested, guaranteed by design.

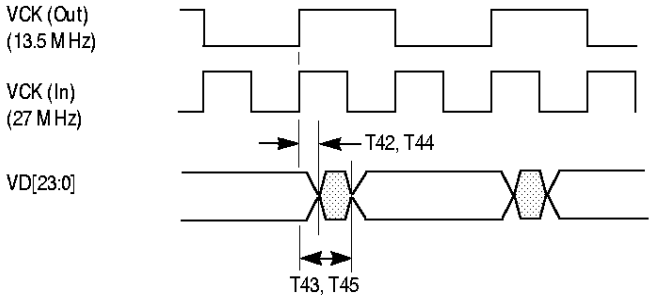


Figure 9-15 Timing - VCK and VD (pixel data)

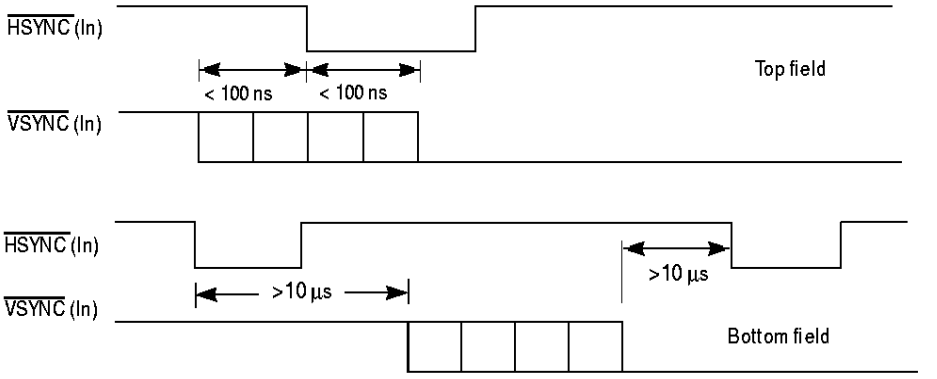
Table 9-12 Timing Characteristics: VCK and VD

Time[1]	Description	Min	Max	Units
T42	601: VCK (In) HIGH to VD invalid (VD hold after VCK)	3		ns
T43	601: VCK (In) HIGH to VD valid	7	32	ns
T44	601: VCK (Out) HIGH to VD invalid (VD hold after VCK)	-10		ns
T45	601: VCK (Out) HIGH to VD valid	-5	15	ns

1. Not 100% tested, guaranteed by design.

Figure 9-16 VSYNC and HSYNC Out

Note: When HSYNC and VSYNC are outputs (Figure 9-16), the position of the VSYNC edges in the HSYNC period is completely programmable by writing to DRAM locations.



Note: *Top field* means the field that starts with the first line from the top of the screen, while *bottom field* begins with the second line from the top of the screen.

Figure 9-17 VSYNC and HSYNC In

Note: HSYNC must always be synchronous to VCK in HSYNC in mode and is produced synchronously for HSYNC out.

For VSYNC/HSYNC In, the minimum HSYNC LOW time is one VCK, and the minimum VSYNC LOW time is two VCKs.

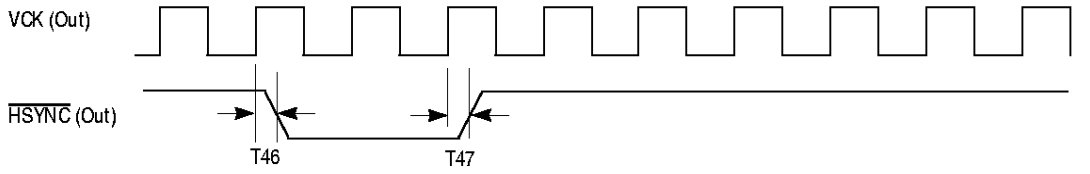


Figure 9-18 VCK Out to HSYNC Out

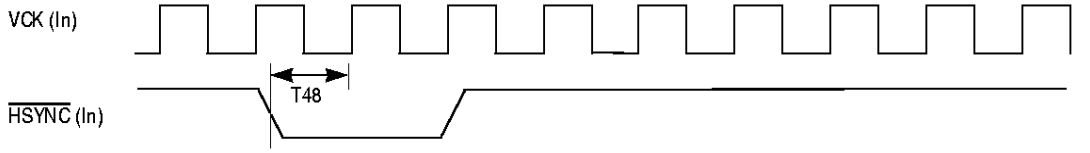


Figure 9-19 HSYNC In to VCK In

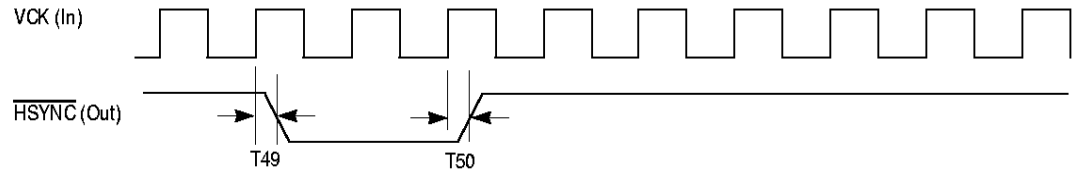


Figure 9-20 VCK In to HSYNC Out

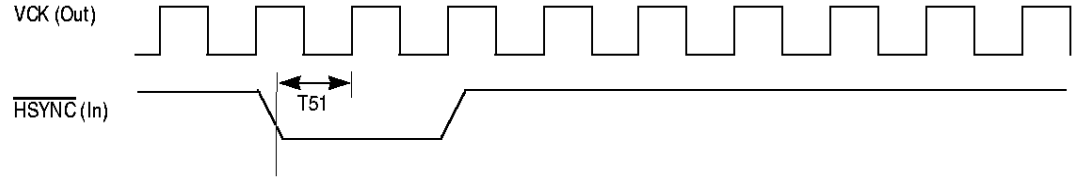


Figure 9-21 HSYNC In to VCK Out

Table 9-13 Timing Characteristics: VCK and $\overline{\text{HSYNC}}$

Time[1]	Description	Min	Max	Units
T46	VCK (Out) HIGH to $\overline{\text{HSYNC}}$ (Out) LOW	-5	10	ns
T47	VCK (Out) HIGH to $\overline{\text{HSYNC}}$ (Out) HIGH	-5	10	ns
T48	$\overline{\text{HSYNC}}$ (In) LOW to VCK (In) HIGH	15		ns
T49	VCK (In) HIGH to $\overline{\text{HSYNC}}$ (Out) LOW	3	30	ns
T50	VCK (In) HIGH to $\overline{\text{HSYNC}}$ (Out) HIGH	3	30	ns
T51	$\overline{\text{HSYNC}}$ (In) LOW to VCK (Out) HIGH	22		ns

1. Not 100% tested, guaranteed by design.

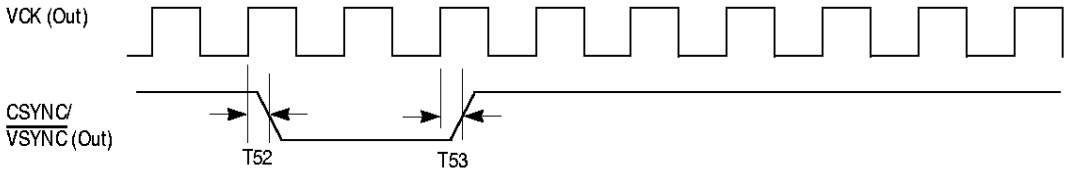


Figure 9-22 VCK Out to CSYNC/$\overline{\text{VSYNC}}$ Out

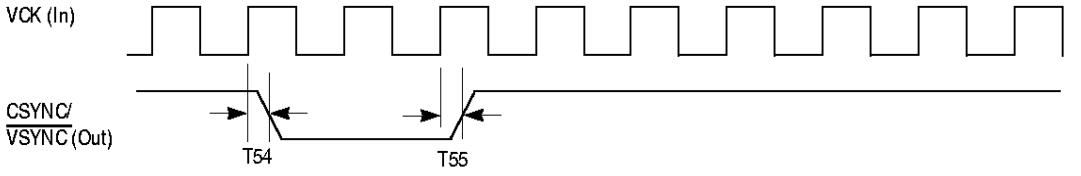


Figure 9-23 VCK In to CSYNC/$\overline{\text{VSYNC}}$ Out

Table 9-14 Timing Characteristics: VCK and CSYNC/$\overline{\text{VSYNC}}$

Time[1]	Description	Min	Max	Units
T52	VCK (Out) HIGH to CSYNC/$\overline{\text{VSYNC}}$ (Out) LOW	-5	10	ns
T53	VCK (Out) HIGH to CSYNC/$\overline{\text{VSYNC}}$ (Out) HIGH	-5	10	ns
T54	VCK (In) HIGH to CSYNC/$\overline{\text{VSYNC}}$ (Out) LOW	3	30	ns
T55	VCK (In) HIGH to CSYNC/$\overline{\text{VSYNC}}$ (Out) HIGH	3	30	ns

1. Not 100% tested, guaranteed by design.

9.2.7 Audio Bus Timing

Figure 9-24 shows the timing for the audio interface of the CL480.

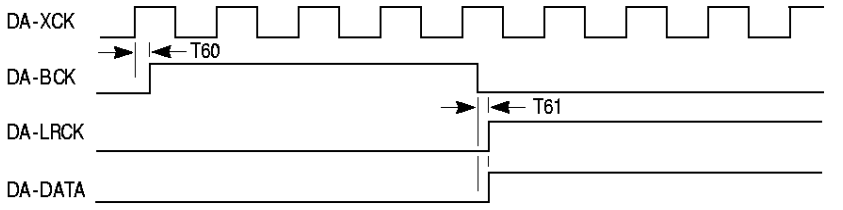


Figure 9-24 Audio Interface Timing Modes

The DA-BCK output pin of the audio bus is synchronized to the rising edge of the input signal DA-XCK, and it has a delay of T60 as Table 9-15 shows. The DA-LRCK and DA-DATA output pins are synchronized to the falling edge of the DA-BCK output signal and have a delay of T61, which is also shown in Table 9-15. The signal DA-XCK is independent of GCK, so it does not have a specified set and hold time.

Table 9-15 Timing Characteristics: Audio

Time[1]	Description	Min.	Max	Units
T60	Delay from DA-XCK to DA-BCK,	3	30	ns
T61	Delay from DA-BCK to DA-LRCK and DA-DATA	3	30	ns

1. Not 100% tested, guaranteed by design.

Note: DA-DATA is driven out of the CL480 on the falling edge of DA-BCK and is typically latched in the audio DAC with the rising edge DA-BCK.

9.3 Package Specifications

The CL480 is packaged in a 128-pin, small outline plastic, quad flat pack (PQFP). This section includes information on the following:

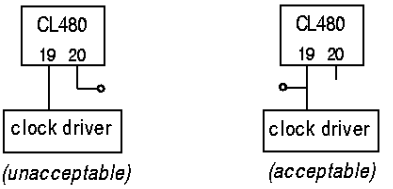
- The CL480 Pinout Diagram
- Tables of CL480 Pin Connections
  - Host Bus Interface Pins
  - CD Interface Pins
  - Global Interface Pins
  - DRAM/ROM Bus Interface Pins
  - Audio Bus Interface Pins
  - Video Bus Interface Pins
  - Power and Miscellaneous Pins
- Package Physical Dimensions

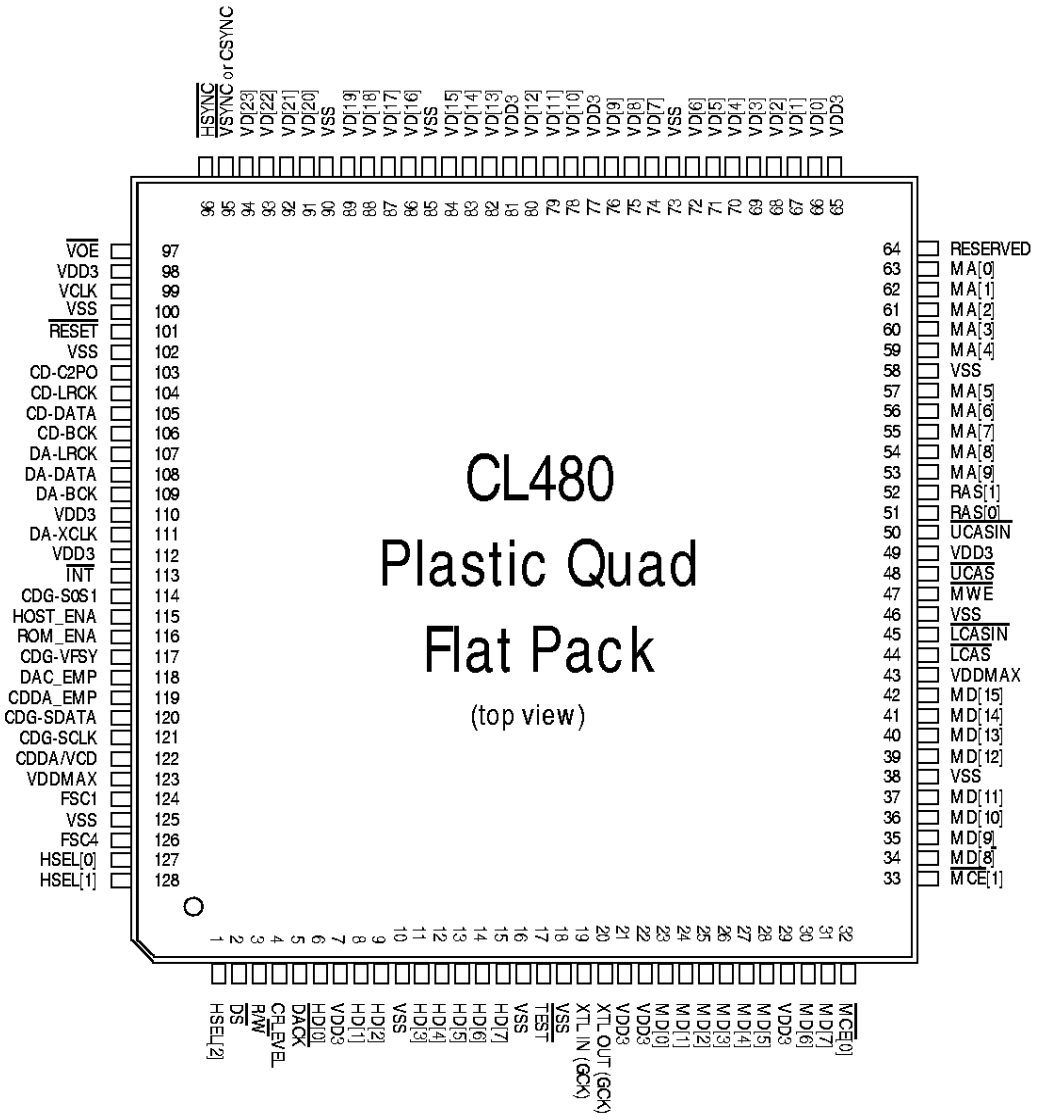
The CL480 is shipped in a drypack with desiccant and a humidity monitor. Do not use the parts if the humidity indicator indicates that the humidity is more than 30 percent at the initial opening of the drypack. To avoid cracking the plastic during soldering, the parts should be soldered within three days after breaking the drypack seal.

Note: "RESERVED" pins are reserved for future use. They should be pulled either HIGH or LOW.

The 40-MHz (or 40.5-MHz, if VCK is an output of the CL480) clock can be derived from either a crystal connected across XTL IN (pin 19) and XTL OUT (pin 20), or from a clock driver connected to XTL IN (pin 19).

If a clock driver is used, the signal amplitude at pin 19 must be in the range 0.8(V_{DD3}) to V_{DD3} + 0.2V, and pin 20 should not be connected. That is, pin 20 should be connected to a pad on the board, but there should be no extra traces coming from that pad. If a test point is desired, it should come from XTL IN (pin 19) as shown in the diagram below:





Note: All VDD3 pins should be 2.7 volts to 3.6 volts.

Note: If an oscillator is used, it should be connected to pin 19 (XTLIN) with a minimum amplitude of $0.8V_{DD3}$ and a maximum amplitude of $V_{DD3} + 0.2V$.

Figure 9-25 CL480 PQFP Pinout Diagram

9.3.1 Pin List

Table 9-16 Host Bus Interface Pins

Function	Group	I/O	Pin #	Function	Group	I/O	Pin #
HSEL2	Host	I	1	HD[3]	Host	I/O	11
HSEL1	Host	I	128	HD[2]	Host	I/O	9
HSEL0	Host	I	127	HD[1]	Host	I/O	8
CRLEVEL[1]	Host	O	4	HD[0]	Host	I/O	6
$\overline{DS}$	Host	I	2	R/$\overline{W}$[2]	Host	I	3
HD[7]	Host	I/O	15	$\overline{DACK}$[1]	Host	O	5
HD[6]	Host	I/O	14	$\overline{INT}$[1]	Host	I/O	113
HD[5]	Host	I/O	13	HOST_ENA	Host	I	115
HD[4]	Host	I/O	12				

1. Open-drain output, requires a pullup resistor of 1.5K ohms.
2. Note: The signal is asserted $\overline{R/W}$ in Silicon A3.

Table 9-17 CD Interface Pins

Function	Group	I/O	Pin #	Function	Group	I/O	Pin #
CD-LRCK	CD	I	104	CD-BCK	CD	I	106
CD-DATA	CD	I	105	CD-C2PO	CD	I	103
CDDA/VCD	CD	O	122	CDG-SDATA	CD	I	120
CDG-S0S1	CD	I	114	CDG-SCLK	CD	I/O	121
CDG-VFSY	CD	I	117				

Table 9-18 Global Interface Pins

Function	Group	I/O	Pin #	Function	Group	I/O	Pin #
XTL IN (GCK)	Global	I	19	XTL OUT (GCK)	Global	O	20
$\overline{RESET}$	Global	I	101	$\overline{TEST}$[1]	Global	I	17

1. Requires a pullup resistor of 1.5K ohms.

Table 9-19 DRAM/ROM Bus Interface Pins

Function	Group	I/O	Pin #	Function	Group	I/O	Pin #
MA9	DR/RM	O	53	MD8	DR/RM	I/O	34
MA8	DR/RM	O	54	MD7	DR/RM	I/O	31
MA7	DR/RM	O	55	MD6	DR/RM	I/O	30
MA6	DR/RM	O	56	MD5	DR/RM	I/O	28
MA5	DR/RM	O	57	MD4	DR/RM	I/O	27
MA4	DR/RM	O	59	MD3	DR/RM	I/O	26
MA3	DR/RM	O	60	MD2	DR/RM	I/O	25
MA2	DR/RM	O	61	MD1	DR/RM	I/O	24
MA1	DR/RM	O	62	MD0	DR/RM	I/O	23
MA0	DR/RM	O	63	$\overline{RAS}$[0]	DR/RM	O	51
MD15	DR/RM	I/O	42	$\overline{RAS}$[1]	DR/RM	O	52
MD14	DR/RM	I/O	41	$\overline{LCAS}$	DR/RM	O	44
MD13	DR/RM	I/O	40	$\overline{UCAS}$	DR/RM	O	48
MD12	DR/RM	I/O	39	$\overline{LCASIN}$	DR/RM	I	45
MD11	DR/RM	I/O	37	$\overline{UCASIN}$	DR/RM	I	50
MD10	DR/RM	I/O	36	$\overline{MWE}$	DRAM	O	47
MD9	DR/RM	I/O	35	$\overline{MCE}$[1]	ROM	O	33
$\overline{MCE}$[0]	ROM	O	32	RESERVED	ROM	O	64
ROM_ENA	ROM	I	116				

Table 9-20 Audio Bus Interface Pins

Function	Group	I/O	Pin #	Function	Group	I/O	Pin #
DA-LRCK	Audio	O	107	DA-BCK	Audio	O	109
DA-DATA	Audio	O	108	DA-XCK	Audio	I	111
DAC_EMP	Audio	O	118	CDDA_EMP	Audio	I	119

Table 9-21 Video Bus Interface Pins

Function	Group	I/O	Pin #	Function	Group	I/O	Pin #
VD23	Video	O	94	VD9	Video	O	76
VD22	Video	O	93	VD8	Video	O	75
VD21	Video	O	92	VD7	Video	O	74
VD20	Video	O	91	VD6	Video	O	72
VD19	Video	O	89	VD5	Video	O	71
VD18	Video	O	88	VD4	Video	O	70
VD17	Video	O	87	VD3	Video	O	69
VD16	Video	O	86	VD2	Video	O	68
VD15	Video	O	84	VD1	Video	O	67
VD14	Video	O	83	VD0	Video	O	66
VD13	Video	O	82	$\overline{\text{HSYNC}}$	Video	I/O	96
VD12	Video	O	80	$\overline{\text{VOE}}$[1]	Video	I	97
VD11	Video	O	79	VCK	Video	I/O	99
VD10	Video	O	78	$\overline{\text{VSYNC}}$/ CSYNC	Video	I/O	95
FSC1	Color	O	124	FSC4	Color	I	126

1. Note: In Silicon A3, this signal is asserted HIGH (i.e., VOE, not $\overline{\text{VOE}}$).

Table 9-22 Power and Miscellaneous Pins

Function	Group	I/O	Pin #	Function	Group	I/O	Pin #
VDD3	Power	PWR	7	VSS	Power	GND	10
VDD3	Power	PWR	29	VSS	Power	GND	16
VDDMAX[1]	Power	PWR	43	VSS	Power	GND	18
VDD3	Power	PWR	49	VSS	Power	GND	38
VDD3	Power	PWR	65	VSS	Power	GND	46
VDD3	Power	PWR	77	VSS	Power	GND	58
VDD3	Power	PWR	81	VSS	Power	GND	73
VDD3	Power	PWR	98	VSS	Power	GND	85
VDD3	Power	PWR	110	VSS	Power	GND	90
VDD3	Power	PWR	112	VSS	Power	GND	100
VDDMAX[1]	Power	PWR	123	VSS	Power	GND	102
VDD3	Power	PWR	21	VSS	Power	GND	125
VDD3	Power	PWR	22	XTL OUT	Global	O	20
XTL IN[2]	Global	I	19				

1. VDDMAX is the maximum of the DRAM and host interface input voltages.
2. The maximum input voltage for XTL IN is 4.0 V. This signal has a minimum amplitude of 0.8VDD3 and a maximum amplitude of VDD3 + 0.2V.

9.3.2 Package Drawings

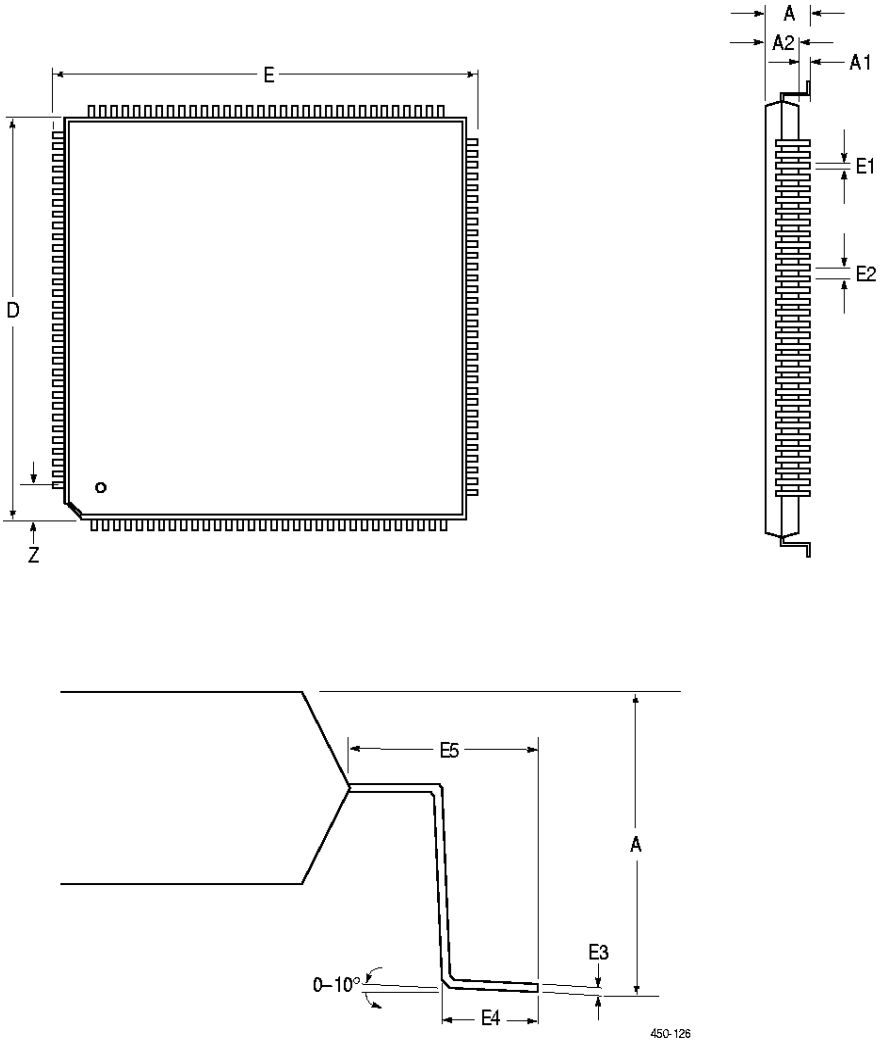


Figure 9-26 Plastic Quad Flat Pack Physical Dimensions

Table 9-23 Plastic Quad Flat Pack Physical Dimensions

SYMBOL	DIMENSIONS MM
A	3.7 MAX.[1]
A1	0 MIN.
A2	3.5 MAX.[2]
D	18.0 ±0.20
E	20.0 ±0.20
E1	0.2 TYP.
E2	0.5 TYP.
E3	0.15 TYP.
E4	0.50 ±0.20
E5	1.0 ±0.20
Z	1.25 TYP.

1. With the new, thinner package design, this parameter has been reduced to 1.7 mm.
2. With the new, thinner package design, this parameter has been reduced to 1.4 mm.