Digital DC/DC PMBus 6A Power Module

ZL9006M

The ZL9006M is a 6A variable output, step-down PMBus-compliant digital power supply. Included in the module is a high-performance digital PWM controller, power MOSFETs, an inductor, and all the passive components required for a highly integrated DC/DC power solution. This power module has built-in auto-compensation algorithms, which eliminates the need for manual compensation design work. The ZL9006M operates over a wide input voltage range and supports an output voltage range of 0.6V to 3.6V, which can be set by external resistors or via PMBus. Only bulk input and output capacitors are needed to finish the design. The output voltage can be precisely regulated to as low as 0.6V with ±1% output voltage regulation over line, load, and temperature variations.

The ZL9006M functions as a switch mode power supply with added benefits of auto compensation, programmable power management features, parametric monitoring, and status reporting capabilities.

The ZL9006M is packaged in a thermally enhanced, compact (17.2mmx11.45mm) and low profile (2.5mm) over-molded High-Density Array (HDA) package module suitable for automated assembly by standard surface mount equipment. The ZL9006M is Pb-free and RoHS compliant.

Figure 1 represents a typical implementation of the ZL9006M. For PMBus operation, it is recommended to tie the Enable pin (EN) to SGND.

Features

- Complete digital switch mode power supply
- Auto compensating PID filter
- ±1% Output Voltage Accuracy
- External synchronization
- Output voltage tracking
- Current sharing and phase interleaving
- Programmable sequencing (delay and ramp time)
- *Snapshot™* parametric capture
- PMBus compliant

Applications

- Server, telecom, and datacom
- Industrial and medical equipment
- General purpose point of load

Related Literature

- See AN2033, “Zilker Labs PMBus Command Set - DDC Products”
- See AN2034, “Configuring Current Sharing on the ZL2004 and ZL2006”

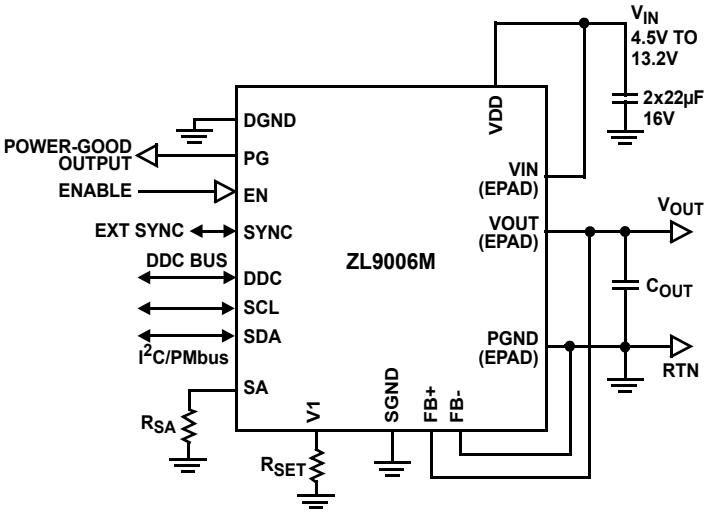
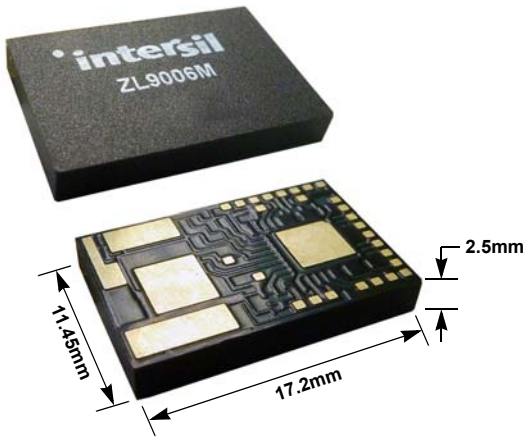


FIGURE 1. TYPICAL APPLICATION CIRCUIT



*Patent pending package

FIGURE 2. SMALL FOOTPRINT PACKAGE WITH LOW PROFILE AT 2.5mm

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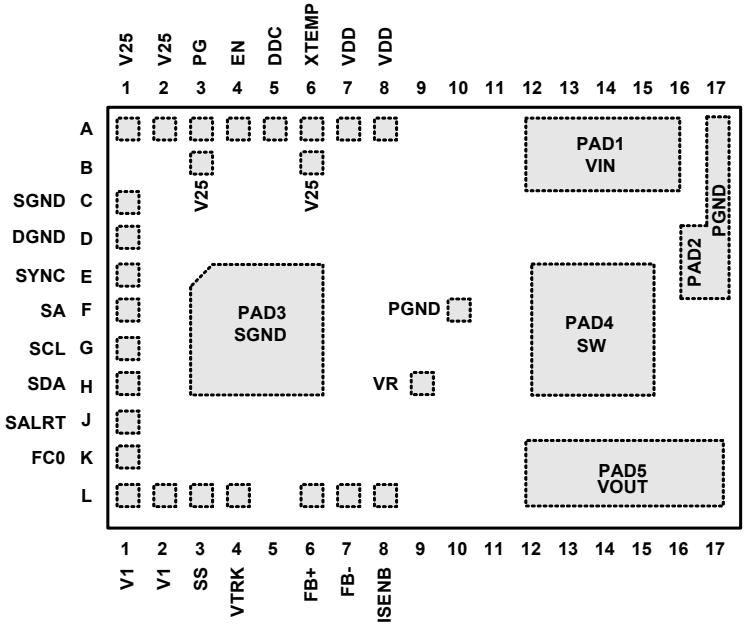
Pin Configuration

ZL9006M
(32 LD HDA)
TOP VIEW



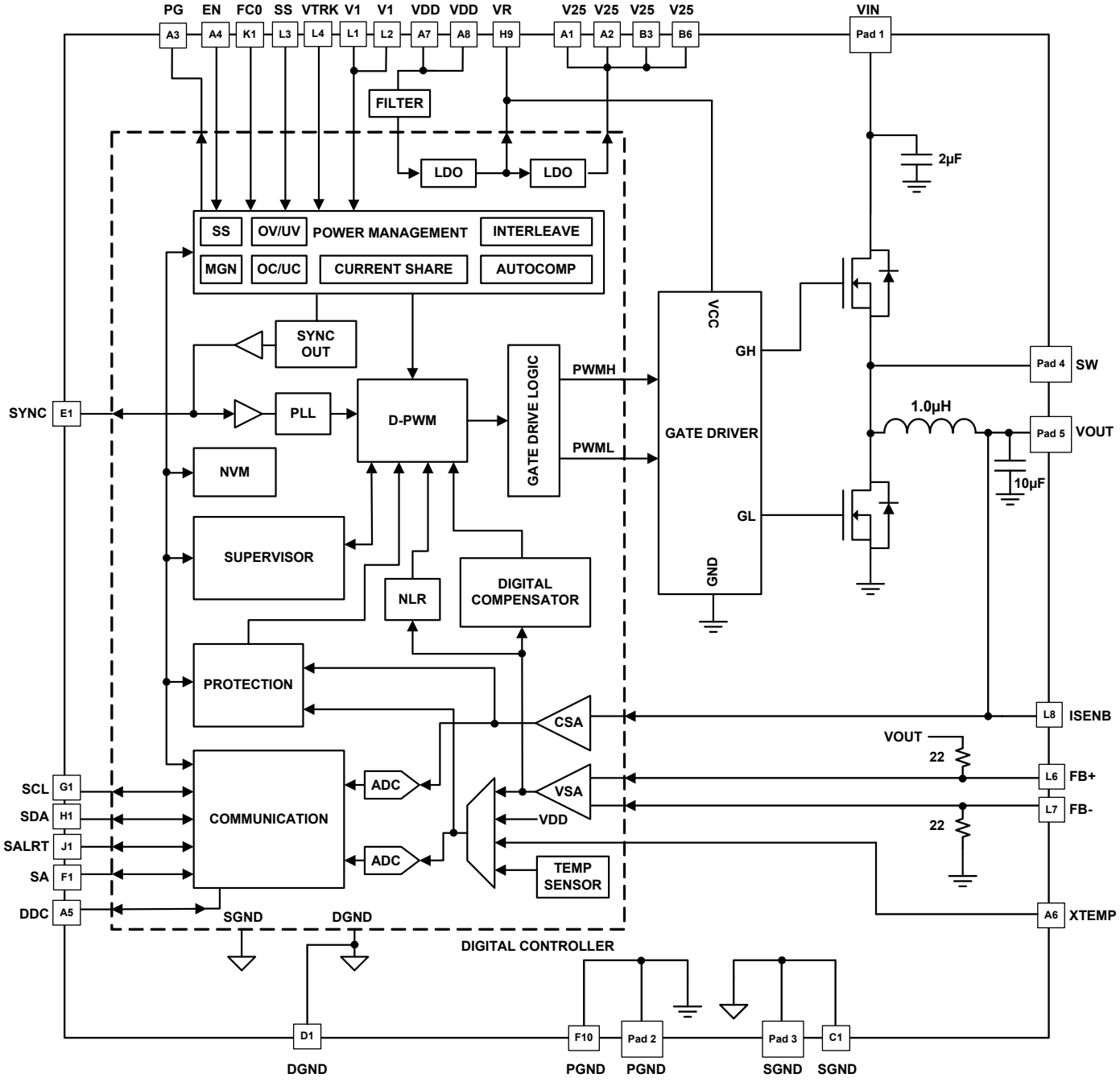
Pin Descriptions

PIN	LABEL	TYPE	DESCRIPTION
A1, A2, B3, B6	V25	PWR	**Internal 2.5V reference.** It is used to power internal circuitry.
A3	PG	O	**Power-good output**. Provide open-drain power-good signal. By default, the PG pin asserts if the output is within +15/-10% of the target voltage. These limits and the polarity of the pin may be changed via the I^2C/PMbus interface.
A4	EN	I	**Enable input.** This pin is factory set as active high. Pull-up to enable the module switching and pull-down to disable switching. If the module is controlled through PMbus command, tie a 10kΩ resistor from this pin to SGND to avoid this pin floating.
A5	DDC	I/O	**Digital-DC bus** (open drain). The DDC pin on all Digital modules in one application should be connected together. This dedicated bus provides the communication channel between modules for features such as sequencing, fault spreading, and current sharing.
A6	XTEMP	I	**External temperature sensor input.** Connect to an external 2N3904 transistor with a diode configuration (see Figure 25 on page 24).
A7, A8	VDD	PWR	**Controller input voltage.** Tie to VIN directly.
C1	SGND	PWR	**Signal ground.** Connect to low impedance ground plane.
D1	DGND	PWR	**Digital ground.** Common return for digital signals. Connect to low impedance ground plane.
E1	SYNC	I/O	**Clock synchronization.** Used for synchronization to external frequency reference.
F1	SA	I	**Serial address select pin.** Used to assign unique PMbus address to each module and phase spreading.
F10	PGND	PWR	**Power ground.** Connect to low impedance ground plane.
G1	SCL	I/O	**Serial clock**. I^2C/PMbus interface pin.
H1	SDA	I/O	**Serial data**. I^2C/PMbus interface pin.
H9	VR	PWR	**Internal 5V reference.** Used to power internal drivers. The current limit for the VR pin is 10mA. Please consider this when using the VR pin for driving external circuitry.
J1	SALRT	O	**Serial alert**. I^2C/PMbus interface pin.
K1	FC0	I	**Mode Setting.** Used to set the single-phase/current sharing mode, auto-compensation, and SYNC configuration (see Table 9 on page 19).

Pin Descriptions (Continued)

PIN	LABEL	TYPE	DESCRIPTION
L1, L2	V1	I	**Output voltage selection pin.** Used to program the output voltage through pin-strap setting or connecting a resistor from the V1 pin to SGND (see Table 4 on page 15). The set voltage on this pin is the maximum allowed output voltage in I^2C/PMbus programming.
L3	SS	I	**Soft-start pin.** Set SS pin by pin-strapping or connecting a resistor to SGND using the appropriate resistor. The pin can program the delay from when EN is asserted until the output voltage starts to ramp, the output voltage ramp time during turn on/off, and input undervoltage lockout (UVLO) level (see Table 6 on page 17). This pin can also set tracking ratio and upper track limit (see Table 10 on page 21).
L4	VTRK	I	**Tracking sense input.** Used to track an external voltage source.
L6	FB+	I	**Output voltage positive feedback.** Positive inputs of differential remote sense for the regulator. Connect to the output rail or the regulation point of load/processor.
L7	FB-	I	**Output voltage negative feedback.** Negative input of the differential remote sense for the regulator. Connect to the negative rail or ground of the load/processor.
L8	ISENB	I	**Test pin.** For factory test use. Solder down the pin for mechanical strength, but do not connect the pin.
PAD1	VIN	PWR	**Power inputs.** Input voltage range: 4.5V to 13.2V. Tie directly to the input rail. When the input is between 4.5V to 5.5V, VIN should be tied directly to VCC.
PAD2	PGND	PWR	**Power ground.** Power ground pins for both input and output returns.
PAD3	SGND	PWR	**Signal ground.** Connect to low impedance ground plane (see Figure 26 on page 25).
PAD4	SW	PWR	**Switch node.** Use for monitoring switching frequency. SW pad should be floating or used for snubber connections. To achieve better thermal performance, the SW planes can also be used for heat removal with thermal vias connected to large inner layers (see Figure 26 on page 25).
PAD5	VOUT	PWR	**Power Output.** Apply output load between these pins and PGND pins. Output voltage range: 0.6V to 3.6V.

Pinout Internal Circuit



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ZL9006MIRZ	ZL9006M	-40 to +85	32 Ld 17.2x11.45 HDA	Y32.17.2x11.45

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ZL9006M. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings (Note 4)

DC Supply Voltage for VDD Pin . . . . . -0.3V to 17V
Input Voltage for VIN Pin . . . . . -0.3V to 17V
MOSFET Drive Reference for VR Pin . . . . . -0.3V to 6.5V
2.5V Logic Reference for V25 Pin. . . . . -0.3V to 3V
Logic I/O Voltage for PG, EN, DDC, SYNC,
PG, SCL, SDA, SALRT, FCO, V1, SS Pins . . . . . -0.3V to 6V
Analog Input Voltages XTEMP, VTRK,
FB+, FB-, ISENB Pins . . . . . -0.3V to 6V
Switch Node for SW Pin
Continuous . . . . . (PGND - 0.3V) to 30V
Transient (<100ns). . . . . (PGND - 5V) to 30V
Ground Voltage Differential (DGND - SGND, PGND - SGND)
for DGND, SGND and PGND Pins . . . . . -0.3V to +0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F). 2000V
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per JESD22-C110D) 750V
Latch Up (Tested per JESD78C; Class 2, Level A). 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld HDA Package (Notes 7, 8)	17	1

Storage Temperature . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Supply Voltage Range, V_{IN} . . . . . 4.5V to 13.2V
Input Supply for Controller, V_{DD} (Note 5). . . . . 4.5V to 13.2V
Driver Supply Voltage, VR . . . . . 4.5V to 5.5V
Output Voltage Range, V_{OUT} (Note 6) . . . . . 0.54V to 3.6V
Output Current Range, $I_{OUT(DC)}$ (Note 18) . . . . . 0A to 6A
Operating Junction Temperature Range, T_J. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Voltage measured with respect to SGND.
5. V_{IN} supplies the power FETs. V_{DD} supplies the controller. V_{IN} can be tied to V_{DD}. For $V_{DD} \leq 5.5V$, V_{DD} should be tied to VR.
6. Includes ±10% margin limits.
7. θ_{JA} is simulated in free air with device mounted on a four-layer FR-4 test board (76.2 x 114.3 x 1.6mm) with 80% coverage, 2oz Cu on top and bottom layers, plus two, buried, one-ounce Cu layers with coverage across the entire test board area. Multiple vias were used, with via diameter = 0.3mm on 1.2mm pitch.
8. For θ_{JC}, the "case" temperature is measured at the center of the package underside.

Electrical Specifications

$V_{IN} = V_{DD} = 12V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNIT
INPUT AND SUPPLY CHARACTERISTICS					
Input Bias Supply Current, I_{DD}	$V_{IN} = VDD = 13.2V$, $f_{SW} = 400kHz$, No load	–	35	**45**	mA
Input Bias Shutdown Current, I_{DDS}	EN = 0V, No I^2C/PMbus activity	–	15.5	**20**	mA
Input Supply Current, I_{VIN}	$V_{IN} = 12V$, $I_{OUT} = 6A$, $V_{OUT} = 1.2V$, $f_{SW} = 400kHz$	–	0.74	–	A
VR Reference Output Voltage (Note 11)	$V_{DD} > 6V$	**4.5**	5.2	**5.7**	V
V25 Reference Output Voltage (Note 11)	$V_R > 3V$	**2.25**	2.5	**2.75**	V
OUTPUT CHARACTERISTICS					
Output Voltage Adjustment Range (Note 11)	$V_{IN} > V_{OUT}$. Does not include margin limits	**0.6**	–	**3.3**	V
Output Voltage Set-point Resolution	Set using resistors. (See Table 1)	–	50 - 200	–	mV
	Set using I^2C/PMbus with temperature compensation applied	–	±0.025	–	% FS
Output Voltage Accuracy (Notes 11, 12)	Includes line, load, temperature	**-1**	–	**1**	%
VSEN Input Bias Current (Note 11)	VSEN = 5.5V	–	110	**200**	µA
Output Load Current (Note 19)	$V_{IN} = 12V$, $V_{OUT} = 1.2V$	–	6	–	A
Peak-to-peak Output Ripple Voltage, ΔV_{OUT} (Note 12)	$I_{OUT} = 6A$, $V_{OUT} = 1.2V$, $C_{OUT} = 1000µF$	–	20	–	mV
Soft-start Delay Duration Range (Notes 11, 13)	Set using SS pin or resistor	**5**	–	**20**	ms
	Set using I^2C/PMbus	**0.005**	–	**500**	s

Electrical Specifications $V_{IN} = V_{DD} = 12V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNIT
Soft-start Delay Duration Accuracy (Notes 11, 13)	Turn-on delay (Note 15)	-	-0.25/+4	-	ms
	Turn-off delay (Note 15)	-	-0.25/+4	-	ms
Soft-start Ramp Duration Range (Notes 11, 13)	Set using SS pin or resistor	**2**	–	**20**	ms
	Set using I^2C	**0**	–	**200**	ms
Soft-start Ramp Duration Accuracy (Note 11)		–	100	–	µs
DYNAMIC CHARACTERISTICS					
Voltage Change for Positive Load Step	I_{OUT} = 1.2A to 6A, slew rate = 1.6A/µs, V_{OUT} = 1.2V (see Figure 19)	–	4	–	%
Voltage Change for Negative Load Step	I_{OUT} = 6A to 1.2A, slew rate = 1.6A/µs, V_{OUT} = 1.2V (see Figure 19)	–	4	–	%
OSCILLATOR AND SWITCHING CHARACTERISTICS (Note 11)					
Switching Frequency Range		**300**	–	**1000**	kHz
Switching Frequency Set-point Accuracy	Predefined settings (See Table 1)	**-5**	–	**5**	%
Maximum PWM Duty Cycle	Factory setting (Note 18)	-	–	**95**	%
Minimum SYNC Pulse Width		**150**	–	–	ns
Input Clock Frequency Drift Tolerance	External clock source	**-13**	–	**13**	%
LOGIC INPUT/OUTPUT CHARACTERISTICS (Note 11)					
PMbus Speed		–	100	–	kHz
Logic Input Bias Current	EN, PG, SCL, SDA pins	**-10**	–	**10**	µA
Logic Input Low, V_{IL}		–	–	**0.8**	V
Logic Input High, V_{IH}		**2.0**	–	–	V
Logic Output Low, V_{OL}	$I_{OL} \leq$ 4mA (Note 17)	–	–	**0.4**	V
Logic Output High, V_{OH}	$I_{OH} \geq$ -2mA (Note 17)	**2.25**	–	–	V
TRACKING (Note 11)					
VTRK Input Bias Current	VTRK = 5.5V	–	110	**200**	µA
VTRK Tracking Ramp Accuracy	100% Tracking, V_{OUT} -VTRK, no prebias	**-100**	–	**+ 100**	mV
VTRK Regulation Accuracy	100% Tracking, V_{OUT} -VTRK	**-1**	–	**1**	%
FAULT PROTECTION CHARACTERISTICS (Note 11)					
UVLO Threshold Range	Configurable via I^2C/PMbus	**2.85**	–	**16**	V
UVLO Set-point Accuracy		**-150**	–	**150**	mV
UVLO Hysteresis	Factory setting	–	3	–	%
	Configurable via I^2C/PMbus	**0**	–	**100**	%
UVLO Delay		–	–	**2.5**	µs
Power-Good V_{OUT} Threshold	Factory setting	–	90	–	% V_{OUT}
Power-Good V_{OUT} Hysteresis	Factory setting	–	5	–	%
Power-Good Delay (Note 16)	Configurable via I^2C/PMbus	**0**	–	**500**	s
VSEN Undervoltage Threshold	Factory setting	–	85	–	% V_{OUT}
	Configurable via I^2C/PMbus	**0**	–	**110**	% V_{OUT}

Electrical Specifications $V_{IN} = V_{DD} = 12V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNIT
VSEN Overvoltage Threshold	Factory setting	–	115	–	% V_{OUT}
	Configurable via I^2C/PMbus	**0**	–	**115**	% V_{OUT}
VSEN Undervoltage Hysteresis		–	5	–	% V_{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory setting	–	16	–	µs
	Configurable via I^2C/PMbus	**5**	–	**60**	µs
Thermal Protection Threshold (Controller Junction Temperature)	Factory setting	–	125	–	°C
	Configurable via I^2C/PMbus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		–	15	–	°C

NOTES:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
10. Parameters with TYP limits are not production tested unless otherwise specified.
11. Parameters are 100% tested for internal controller prior to module assembly.
12. V_{OUT} measured at the termination of the FB+ and FB- sense points.
13. The device requires a delay period following an enable signal and prior to ramping its output.
14. Precise ramp timing mode is only valid when using the EN pin to enable the device rather than PMBus enable.
15. The devices may require up to a 4ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.
16. Factory setting for Power-Good delay is set to the same value as the soft-start ramp time.
17. Nominal capacitance of logic pins is 5pF.
18. Maximum duty cycle is limited by the equation MAX_DUTY(%) = $[1 - (150 \times 10^{-9} \times f_{SW})] \times 100$ and not to exceed 95%.
19. The load current is related to the thermal derating curves. The maximum allowed current is derated while the output voltage goes higher than 2.5V.

Typical Performance Curves

Operating conditions: T_A = +25°C, No air flow, C_{OUT} = 3 x 100µF + 1 x 330µF. Typical values are used unless otherwise noted.

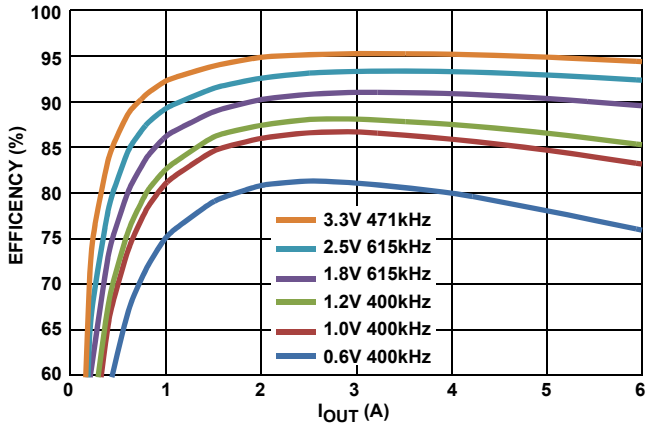


FIGURE 3. ZL9006M EFFICIENCY, V_{IN} = 5V

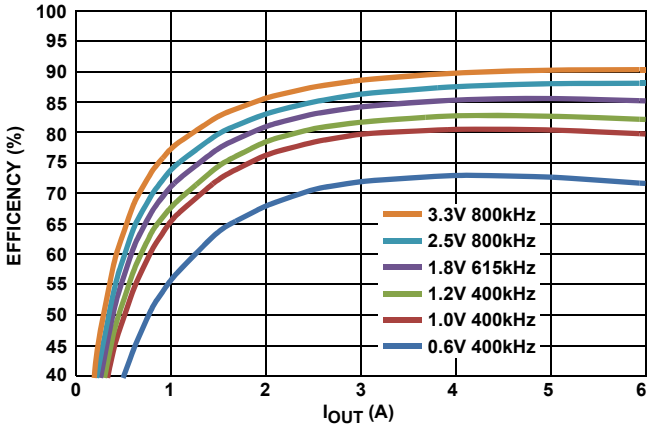


FIGURE 4. ZL9006M EFFICIENCY, V_{IN} = 12V

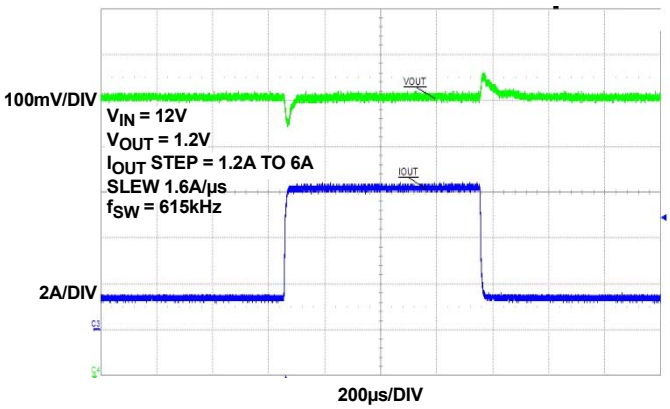


FIGURE 5. V_{OUT} = 1.2V TRANSIENT RESPONSE

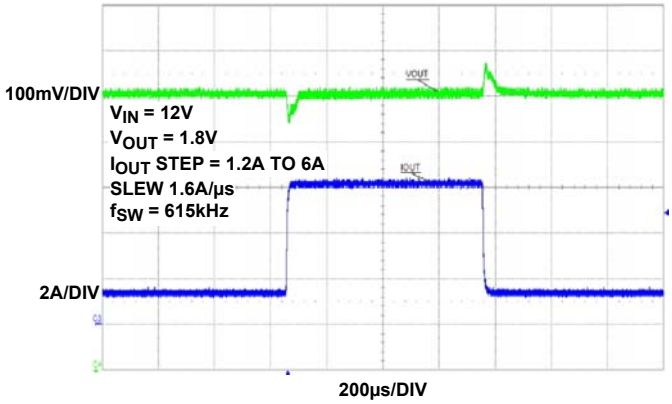


FIGURE 6. V_{OUT} = 1.8V TRANSIENT RESPONSE

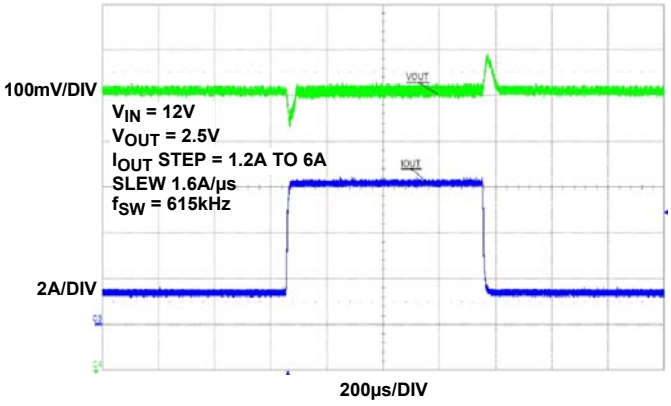


FIGURE 7. V_{OUT} = 2.5V TRANSIENT RESPONSE

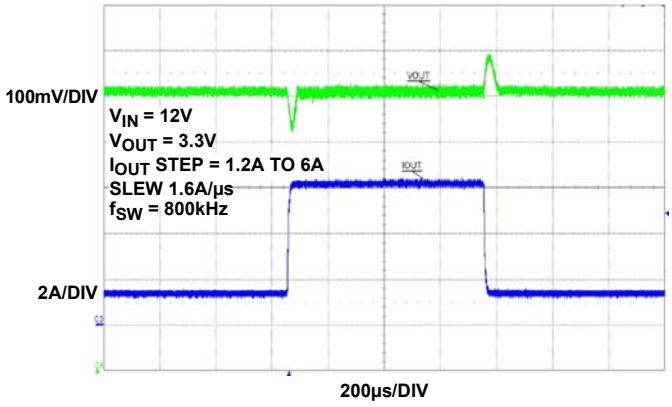


FIGURE 8. V_{OUT} = 3.3V TRANSIENT RESPONSE

Typical Performance Curves

Operating conditions: T_A = +25°C, No air flow, C_{OUT} = 3 x 100µF + 1 x 330µF. Typical values are used unless otherwise noted. **(Continued)**

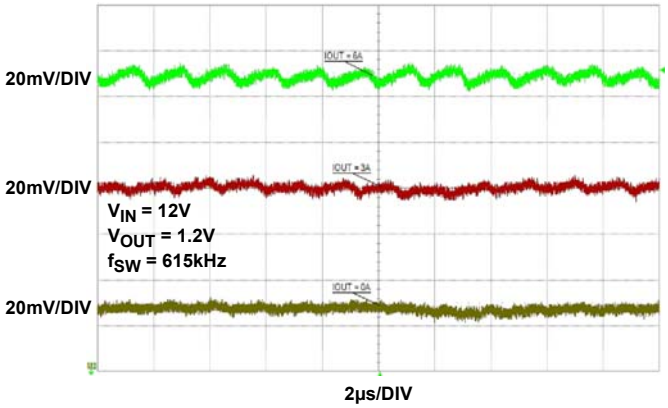


FIGURE 9. V_{OUT} = 1.2V OUTPUT VOLTAGE RIPPLE

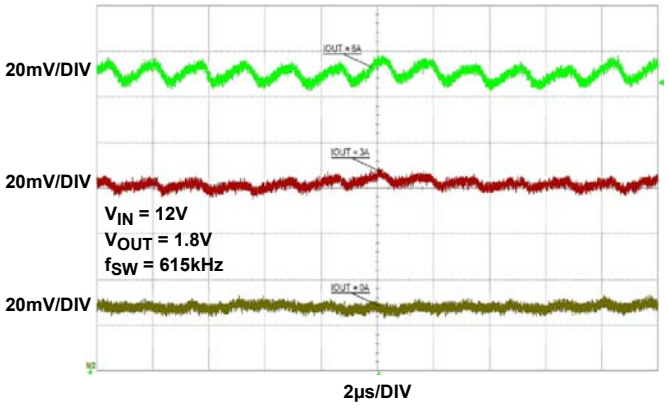


FIGURE 10. V_{OUT} = 1.8V OUTPUT VOLTAGE RIPPLE

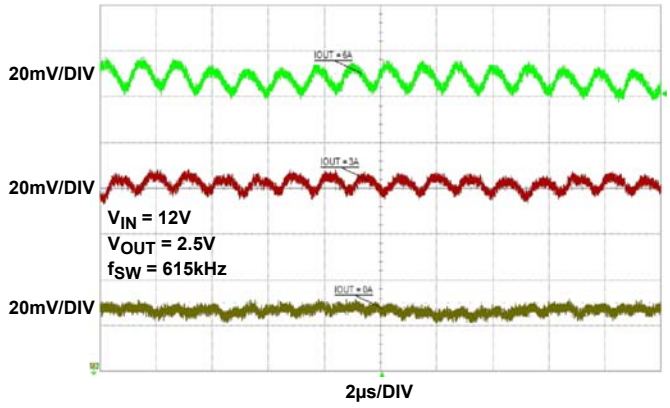


FIGURE 11. V_{OUT} = 2.5V OUTPUT VOLTAGE RIPPLE

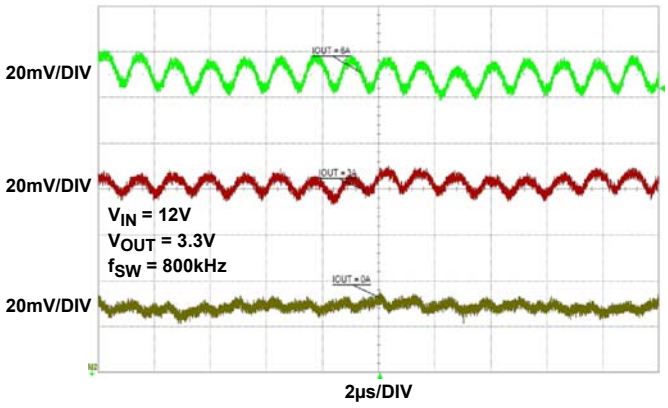


FIGURE 12. V_{OUT} = 3.3V OUTPUT VOLTAGE RIPPLE

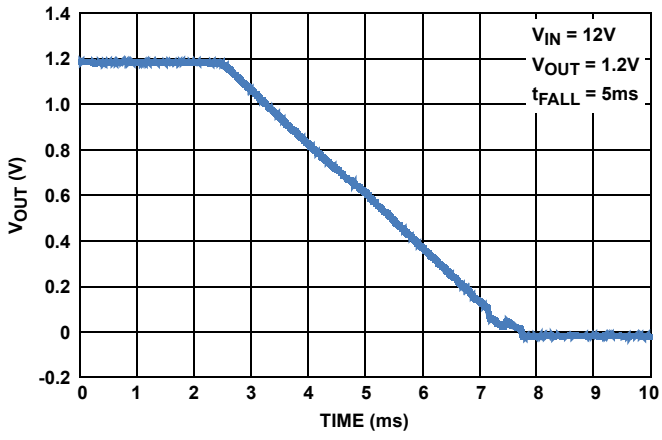


FIGURE 13. SOFT-STOP RAMP-DOWN

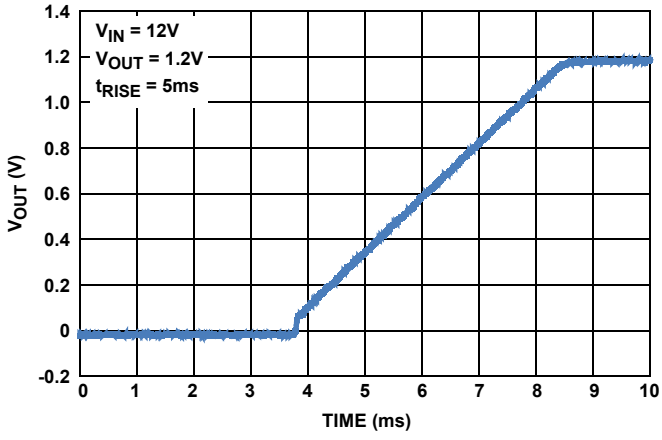


FIGURE 14. SOFT-START RAMP-UP

Derating Curves

Operating conditions: T_A = +25°C, No air flow. f_{SW} corresponds to those used in Efficiency curves. C_{OUT} = 3 x 100µF + 1 x 330µF. Typical values are used unless otherwise noted.

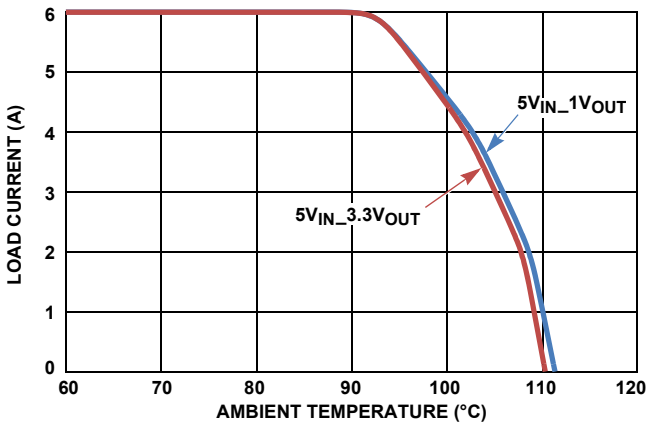


FIGURE 15. DERATING CURVE, $5V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES, NO AIR FLOW

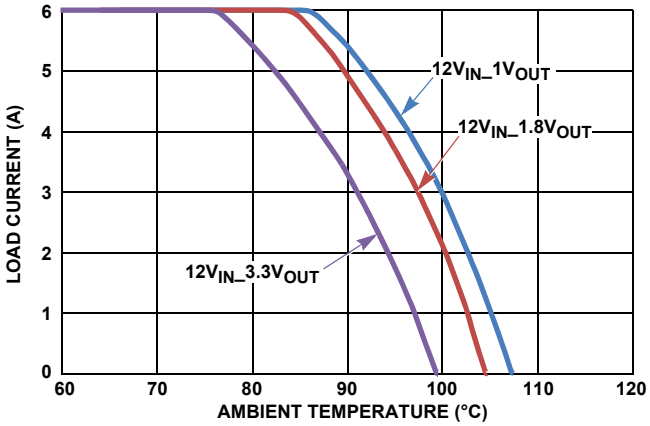


FIGURE 16. DERATING CURVE, $12V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES, NO AIR FLOW

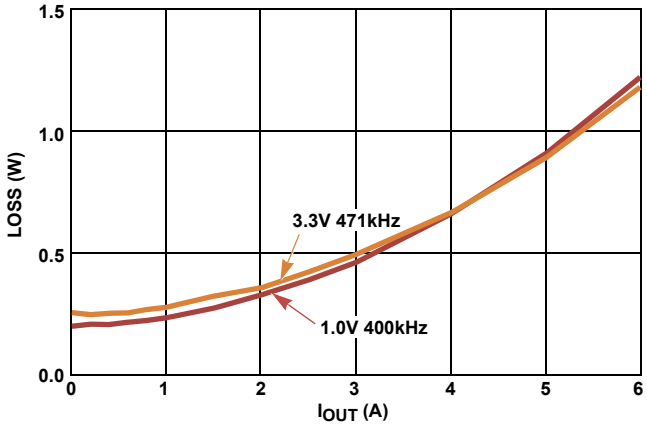


FIGURE 17. POWER LOSS CURVE, $5V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES

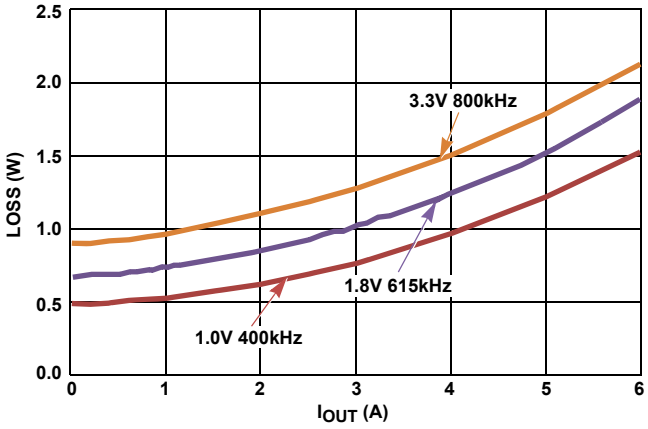


FIGURE 18. POWER LOSS CURVE, $12V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES

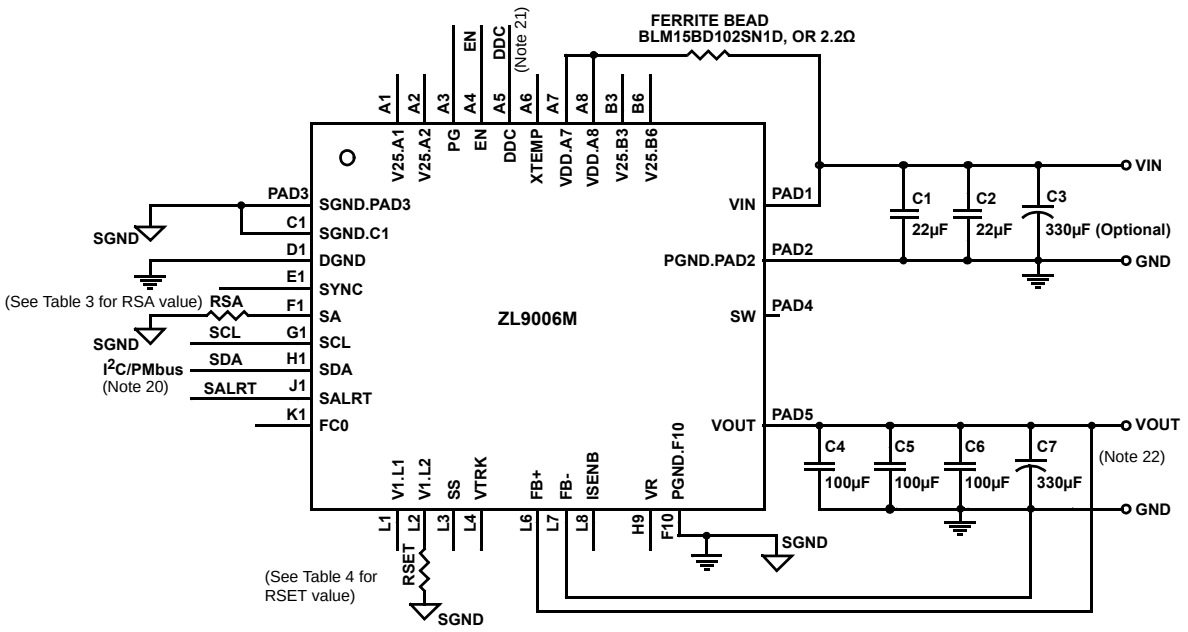


FIGURE 19. TEST CIRCUIT FOR ALL PERFORMANCE AND DERATING CURVES

NOTES:

20. The I^2C/PMbus requires pull-up resistors. Please refer to the I^2C/PMbus specifications for more details.
21. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus (and on the number of devices connected). The 10kΩ default value, assuming a maximum of 100pF per device, provides the necessary 1µs pull-up rise time. Please refer to "Digital-DC Bus" on page 23 for more details.
22. Additional capacitance may be required to meet specific transient response targets.

Application Information

Internal Bias and Input Voltage Considerations

Beside VIN supplying the main power conversion, the ZL9006M employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry allowing it to operate from a single input supply. The internal bias regulators are as indicated in the following:

VR - The VR LDO provides a regulated 5V bias supply for the MOSFET driver circuits. It is powered from the VDD pin.

V25 - The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node.

When the input supply (VDD) is higher than 5.5V, the VR pin should not be connected to any other pin. Due to the dropout voltage associated with the VR bias regulator, the VDD pin can be connected to the VR pin for designs operating from a supply below 5.5V. The internal bias regulators are not designed to be outputs for powering other circuitry, so keep current into the VDD pin below 80mA.

Typically, VDD is connected directly to VIN. In the case that VDD is powered separately from VIN, the recommended power sequence is to keep EN low, power VDD, and then VIN. When the voltage is applied to VIN, VDD should also be applied to avoid unintentional turn-on of the internal high-side MOSFET. If the VDD voltage is different from VIN, Pre-Bias start-up and Auto-compensation may not work correctly as the VDD voltage is used to measure input voltage as part of the Pre-Bias and Auto-compensation calculation.

Pre-programming Configuration

The Intersil digital power module allows pre-programming before the main power rail is supplied to the VIN pins of the module. If the system bias (i.e., 3.3V bias) is available, the power module can be programmed to load the configuration file or change the settings without main power being on. See Figure 20 for an example with 3.3V bias voltage and 12V input voltage for the main power rail. To pre-program the module without applying power to the VIN pin, the bias voltage 3.3V is applied to pin VR through a Schottky diode such that 3.0 $\leq$ VR and < VDD when VIN is applied. The body diode of the PMOS will be reverse biased, preventing back feeding to the VIN rail. When the main power rail 12V VIN is ON, the PMOS is ON to supply the power to the module. In this case, only a small voltage is dropped on the PMOS, so the controller can still detect the input voltage accurately. If there are more Intersil digital modules on the board, only one PMOS (as shown in Figure 20) is required to drive the VIN voltages of all modules.

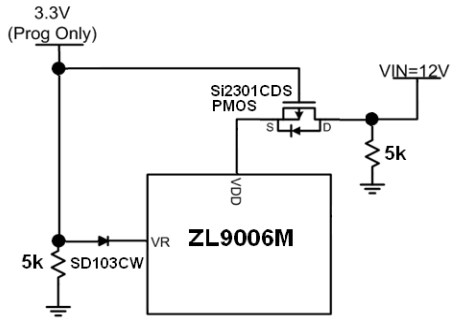


FIGURE 20. PRE-PROGRAMMING CONFIGURATION

Design Trade-offs with Switching Frequency

For design of the buck power stage, there is a trade-off when choosing switching frequency to achieve higher power supply efficiency, output ripple, and transient response. For output voltages below 2.0V, a lower switching frequency results in higher efficiency. A lower output ripple and faster transient response is achieved with higher switching frequencies, and thereby can reduce the required amount of output capacitance. Also, given an input to output voltage relation, there is a limitation on the allowable switching frequency due to normal part operation. See "Switching Frequency and PLL" on page 18 for more considerations.

To start the design with a goal of high efficiency, select a frequency based on Table 1. To achieve good transient response, a minimum switching frequency of 615kHz is recommended.

TABLE 1. OPTIMAL SWITCHING FREQUENCY FOR EFFICIENCY

V_O-VIN	3.3V (kHz)	5.0V (kHz)	12.0V (kHz)
0.6 - 1.5	300	400	400
1.5 - 2.5	300	615	615
2.5 - 3.6	300	471	800

Completing a Power Supply Design

To achieve a power supply design with digital capabilities using the ZL9006M, only input and output capacitors and two resistors are needed. The two resistors are installed on the SA and V1 pins for setting the I^2C address and output voltage, respectively.

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, but consideration should be taken for the higher surge current during power-up. The ZL9006M provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by Equation 1:

$$C_{IN(MIN)} = I_O \bullet \frac{D \bullet (1-D)}{V_{P\text{-}P(MAX)} \bullet F_S} \quad \text{(EQ. 1)}$$

Where:

$C_{IN(MIN)}$ is the minimum input capacitance (µF) required
I_O is the output current (A)
D is the duty cycle (V_O/V_{IN})
$V_{P\text{-}P(MAX)}$ is the maximum peak-to-peak voltage (V)
F_S is the switching frequency (Hz)

In addition to the bulk capacitance, some low Equivalent Series Resistance (ESR) ceramic capacitance should be placed as close as possible to decouple between the drain terminal of the high side MOSFET (VIN PAD1) and the source terminal of the low side MOSFET (PGND PAD2). This is used to reduce voltage ringing created by the switching current across parasitic circuit elements. This ripple's (I_{CINrms}) impact should be considered, and can be determined from Equation 2:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1-D)} \quad \text{(EQ. 2)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated in Equation 2 to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure.

Selection of the Output Capacitors

The ZL9006M is designed for low output voltage ripple. The output voltage ripple and transient requirements can be met with bulk output capacitors (C_{OUT}) with low ESR; the recommended minimum ESR is <6MΩ. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor.

The typical output capacitance range is from 200µF to 1200µF, and decoupling ceramic output capacitors are used per phase. The optimized output capacitance is 700µF with an ESR of 5mΩ. The maximum recommended product of output capacitance and equivalent ESR value is given by [C_{OUT} x ESR] < 3600 (µF x mΩ) .

With a step load faster than 0.2A/µs, the recommended amount of output capacitor is 100µF per ampere of step load. Additional output filtering may be needed if further reduction of output ripple or dynamic transient spikes are required.

Functional Description

Multi-mode Pins

In order to simplify circuit design, the ZL9006M family incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device without programming. Most power management features can be configured using these pins. The multi-mode pins can respond to two types of configurations summarized in Table 2: pin strapping and resistor programming. These pins are sampled when power is applied or by issuing a PMBus Restore command (see Application Note AN2033).

With pin strapping, parameters can be set by strapping the pins in one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to SGND for logic LOW as this pin provides a voltage lower than 0.8V. For logic OPEN, they have no connection. These pins can be connected to the V25 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2V when power is applied to the VDD pin.

Resistor programming allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth standard resistor value is used so the device can reliably recognize the value of resistance

connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

TABLE 2. MULTI-MODE PIN CONFIGURATION

PIN TIED TO	VALUE
LOW (Logic LOW)	$<0.8V_{DC}$
OPEN (N/C)	No connection
HIGH (Logic HIGH)	$>2.0V_{DC}$
Resistor to SGND	Set by resistor value

There are five multi-mode pins in ZL9006M: FC0, SA, SYNC, SS, V1. The multi-mode pin configuration can set ZL9006M power management features and mode of operation to both single-phase and current-sharing without any programming. SA and V1 are the only two pins that must be set for a general single-phase operation, which use the default settings associated with the other three pins, or overriding other parameters via the I^2C/PMbus.

SA sets the I^2C address, phase spreading, and Reference/Member assignment in current sharing mode. The effective phase spreading depends on the mode of operation. The Reference/Member is pre-assigned in current sharing mode, and up to 8 two-phase with 5 three-phase current-shared group is possible.

FC0 is used to distinguish between the two modes of operation, and is used in combination with SA in current sharing mode. FC0 pin strapping and resistor programming in the range of 10kΩ-42.2kΩ set the operation to single-phase mode, while the range of 46.4kΩ-178kΩ is for current sharing mode. FC0 also sets the Autcomp and Sync configuration.

SYNC sets the switching frequency, and is only effective in single-phase mode, as SYNC pins are connected together in current-sharing mode.

SS sets the ramp timing, UVLO, and tracking. V1 sets the output voltage. SS and V1 are the same purpose in single-phase and current-share modes.

I^2C/PMbus Communications

The ZL9006M provides an I^2C/PMbus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ZL9006M can be used with any I^2C host device. In addition, the module is compatible with PMbus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the I^2C/PMbus as specified in the PMbus 2.0 specification. The ZL9006M accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin be tied to SGND.

The PMbus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I^2C/PMbus. The device address is set using the SA pin. VOUT_MAX is determined as 10% greater than the voltage set by the V1 pin.

ZL9006M supports 100kHz and 400kHz I^2C clock speed with communication interval of 20ms between STORE and RESTORE commands, and ~2ms for other general commands.

I^2C/PMbus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. Table 3 lists the available module addresses.

TABLE 3. PMbus ADDRESS VALUES

R_{SA} (kΩ)	PMbus ADDRESS
LOW	0x23
OPEN	0x24
HIGH	0x25
10	0x50
11	0x51
12.1	0x52
13.3	0x53
14.7	0x54
16.2	0x55
17.8	0x56
19.6	0x57
21.5	0x58
23.7	0x59
26.1	0x5A
28.7	0x5B
31.6	0x5C
34.8	0x5D
38.3	0x5E
42.2	0x5F
46.4	0x60
51.1	0x61
56.2	0x62
61.9	0x63
68.1	0x64
75	0x65
82.5	0x66
90.9	0x67
100	0x68
110	0x69
121	0x6A
133	0x6B
147	0x6C
162	0x6D
178	0x6E

Phase Spreading for a Single-Phase Mode of Operation

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable spreading, all converters must be synchronized to the same switching clock. The FC0 pin is used to set the configuration of the SYNC pin for each device as described in “Switching Frequency and PLL” on page 18.

Selecting the phase offset for the device in a standalone mode of operation is accomplished by selecting a device address according to the following equation:

Phase offset = device address x 45°

For example:

- A device address of 0x50 or 0x60 would configure no phase offset
- A device address of 0x51 or 0x61 would configure 45° of phase offset
- A device address of 0x52 or 0x62 would configure 90° of phase offset

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments via the I^2C/PMbus interface. Refer to Application Note AN2033 for further details.

Output Voltage Selection

The output voltage may be set to a voltage between 0.6V and 3.6V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification.

The V1 pins are used to set the output voltage using a single resistor, R_{SET} between the V1 pins and SGND. Table 4 lists the available output voltage settings with a single resistor.

TABLE 4. SINGLE RESISTOR V_{OUT} SETTING

R_{SET} (kΩ)	V_{OUT}
LOW	1.20
OPEN	1.50
HIGH	3.30
10	0.60
11	0.65
12.1	0.70
13.3	0.75
14.7	0.80

TABLE 4. SINGLE RESISTOR V_{OUT} SETTING (Continued)

R_{SET} (kΩ)	V_{OUT}
16.2	0.85
17.8	0.90
19.6	0.95
21.5	1.00
23.7	1.05
26.1	1.10
28.7	1.15
31.6	1.20
34.8	1.25
38.3	1.30
42.2	1.40
46.4	1.50
51.1	1.60
56.2	1.70
61.9	1.80
68.1	1.90
75	2.00
82.5	2.10
90.9	2.20
100	2.30
110	2.50
121	2.80
133	3.00
147	3.30
162	3.60

The output voltage may also be set to any value between 0.6V and 3.6V using a PMBus command over the I^2C/PMbus interface. See Application Note AN2033 for details.

The R_{SET} resistors program places an upper limit in output voltage setting through PMBUS programming to 10% above the value set by the resistors.

Start-up Procedure

The ZL9006M follows a specific internal start-up procedure after power is applied to the VDD pin. Table 5 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5ms to 6ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/PMbus interface and the device is ready to be enabled. Once enabled, the device requires a minimum delay period following an enable signal and prior to ramping its output, as described in "Soft-start Delay and Ramp Times" on page 17. If a soft-start delay period less than the minimum has been configured (using PMBus commands), the device will default to the minimum delay period. If a delay period greater than the minimum is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin. It should be noted that if the EN pin is tied to VDD, the device will still require approximately 5ms to 6ms before the output can begin its ramp-up as described in Table 5.

TABLE 5. ZL9006M START-UP SEQUENCE

STEP #	STEP NAME	DESCRIPTION	TIME DURATION
1	Power Applied	Input voltage is applied to the ZL9006M's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approximately 5ms to 6ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	-
5	Pre-ramp Delay	The device requires a minimum delay period following an enable signal and prior to ramping its output, as described in "Soft-start Delay and Ramp Times" on page 17.	-

Soft-start Delay and Ramp Times

It may be necessary to set a delay when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL9006M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin.

The soft-start delay and ramp times can be set to a custom value by pin-strapping or connecting a resistor from the SS pin to SGND using the appropriate resistor value from Table 6. See “Input Undervoltage Lockout” on page 19 for further explanation of UVLO setting using SS pin. The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL9006M.

TABLE 6. SOFT-START PIN-STRAP/RESISTOR SETTINGS

R_{SS} (kΩ)	DELAY TIME (ms)	RAMP TIME (ms)	UVLO (V)
LOW	5	2	4.5
OPEN	5	5	
HIGH	10	10	
10	5	2	3
11	5	5	
12.1	10		
13.3	20		
14.7	5	10	
16.2	10		
17.8	20		
19.6	5	2	4.5
21.5	10		
23.7	5	5	
26.1	10		
28.7	20		
31.6	5	10	
34.8	10		
38.3	20		
42.2	5	2	10.8
46.4	10		
51.1	5	5	
56.2	10		
61.9	20		
68.1	5	10	
75	10		
82.5	20		

With the SS pin OPEN, the default value for delay time and ramp time is 5ms. The soft-start delay and ramp times are set to custom values via the I^2C/PMbus interface. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

The ZL9006M has a minimum t_{ON_DELAY} requirement that is a function of the operating mode. Table 7 shows the different mode configurations and the minimum t_{ON_DELAY} required for each mode. Current sharing is configured with the ISHARE_CONFIG PMBus command, Auto compensation is configured with the AUTO_COMP_CONFIG command, and Standby Mode is configured as Low Power with the USER_CONFIG command. See Application Note AN2033 for details. Resistor programming on the SS pin with a delay time of 20ms can be used to satisfied the minimum t_{ON_DELAY} of 15ms.

TABLE 7. MINIMUM t_{ON_DELAY} vs OPERATING MODE

CURRENT SHARING	AUTOCOMP	LOW-POWER STANDBY	MIN. t_{ON_DELAY} (ms)
X	Disabled	False	5
Disabled	Enabled	False	5
Disabled	X	True	10
Enabled	Disabled	True	15
Enabled	Enabled	X	15

Power-Good

The ZL9006M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within +15/-10% of the target voltage. These limits and the polarity of the pin may be changed via the I^2C/PMbus interface. See Application Note AN2033 for details.

A PG delay period is defined as the time when all conditions within the ZL9006M for asserting PG are met, to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic.

By default, the ZL9006M PG delay is set to 1ms, and may be changed using the I^2C/PMbus as described in Application Note AN2033.

By default, the ZL9006M PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 6ms, the PG delay is set to 6ms. The PG delay may be set independently of the soft-start ramp using the I^2C/PMbus as described in Application Note AN2033.

If Auto Comp is enabled, the PG timing is further controlled by the PG Assert parameter, as described in “Loop Compensation” on page 18.

Switching Frequency and PLL

The ZL9006M incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices. With the FC0 pin,the SYNC pin can be configured as input, Auto detect, and Output. Pinstrap resistor setting to “input” mode is applicable for member devices used in current sharing mode only.

When multiple modules are used together, connecting the SYNC pins together will force all devices to synchronize with each other. One device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as Auto Detect.

SYNC AUTO DETECT

In Auto Detect mode, the module will check for a clock signal on the SYNC pin immediately after power-up. In this case, the incoming clock signal must be in the range of 300kHz to 1.0MHz and must be stable within 10µs after V25 rises above 2.25V. If the device is in Low Power Mode, it will check for a clock signal on the SYNC pin immediately after EN goes true. In this case, the incoming clock signal must be in range and stable before EN goes true. If a clock signal is present, the ZL9006M's oscillator will then synchronize with the rising edge of the external clock.

If no incoming clock signal is present, the ZL9006M will configure the switching frequency according to an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 8, given that FC0 used pin-strap or has a resistor R_{FC0} in the range of 10-13.3kΩ. When FC0 is OPEN, or used with resistor settings in the range, the switching frequency of the ZL9006M is set to a default of 615kHz. The module will only read the SYNC pin connection during the first start-up sequence; changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on. Frequency modifications without restarting the V_{DD} power can disable the SYNC auto detect function.

SYNC OUTPUT

When the SYNC pin is configured as an output via I^2C, the device will run from its internal oscillator and will drive the resulting internal oscillator signal onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

When FC0 is used with resistor settings in the range of 14.7-31.6kΩ, the ZL9006M drives the SYNC pin with frequency as described in Table 9, and will ignore any resistor settings on the SYNC pin. Similarly, when FC0 is used with a selected value of resistors in the range of 46.4-178kΩ, the ZL9006M operates in current sharing mode with the SYNC pin providing clock out.

When FC0 is used with resistor settings in the range of 34.8 to 42.2kΩ, ZL9006M will first read the SYNC pin connection, and drives the SYNC pin with the frequency described in Table 8. In this mode, the SYNC pin should not be pin strapped to LOW or HIGH (voltage source). It is recommended to connect a buffer with high impedance, as seen by the SYNC pin of the module providing the clock out, to subsequently drive the SYNC pin of other devices.

SYNC SETTING VIA I^2C CONSIDERATION

The switching frequency can be set to any value between 300kHz and 1.0MHz using the I^2C/PMbus interface. The available frequencies below 1.0MHz are defined by f_{SW} = 8MHz/N, where the whole number N is $8 \leq N \leq 27$. See Application Note AN2033 for details.

If a value other than f_{SW} = 8MHz/N is entered using a PMBus command, the internal circuitry will select the valid switching frequency value that is closest to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N = 10).

TABLE 8. SWITCHING FREQUENCY PIN-STRAP/RESISTOR SETTINGS

SYNC PIN/ R_{SYNC} (kΩ)	f_{SW} (kHz)	SYNC PIN/ R_{SYNC} (kΩ)	f_{SW} (kHz)
LOW	400	23.7	471
OPEN	615	26.1	533
HIGH	800	28.7	571
14.7	296	31.6	615
16.2	320	34.8	727
17.8	364	38.3	800
19.6	400	46.4	889
21.5	421	51.1	1000

Loop Compensation

The ZL9006M operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. The module is internally compensated via the I^2C/PMbus interface. The auto compensation feature measures the characteristics of the power train and calculates the proper tap coefficients, and can be configured according to an external resistor, R_{FC0}, connected between FC0 and SGND in Table 9.

If the device is configured to store auto comp values, the calculated compensation values will be saved in the Auto Comp Store and may be read back through the PID_TAPS command. If repeat mode is enabled, the first Auto Comp results after the first ramp will be stored; the values calculated periodically are not stored in the Auto Comp Store. When compensation values are saved in the Auto Comp Store, the device will use those compensation values on subsequent ramps. In repeat mode, the latest Auto Comp results will always be used during operation. Stored Auto Comp results can only be cleared by disabling Auto Comp Store, which is not permitted while the output is enabled. However, sending the AUTOCOMP_CONTROL command while enabled in Store mode will cause the next results to be stored, overwriting previously stored values. If auto compensation is disabled, the device will use the compensation parameters that are stored in the DEFAULT_STORE or USER_STORE.

If the PG Assert parameter is set to "Use PG Delay," PG will be asserted according to the POWER_GOOD_DELAY command, after which Auto Comp will begin. When Auto Comp is enabled, the user must not program a Power-Good Delay that will expire before the ramp is finished. If PG Assert is set to "After Auto Comp," PG will be asserted immediately after the first Auto Comp cycle completes (POWER_GOOD_DELAY will be ignored).

The routine can be set via the I^2C/PMbus interface to execute one time after ramp or periodically while regulating, and have

either PG Assert behavior described earlier. Note that the Auto Compensation feature requires a minimum t_{ON_DELAY} as described in "Soft-start Delay and Ramp Times" on page 17.

The Auto Comp Gain control scales the Auto Comp results to allow a trade-off between transient response and steady-state duty cycle jitter. A setting of 100% will provide the fastest transient response while a setting of 10% will produce the lowest jitter.

With resistor settings, auto compensation can only be set to execute one time after ramp with option to store auto comp values. With auto compensation disabled, PG is asserted according to POWER_GOOD_DELAY. With auto compensation executed once and auto comp values not stored, PG is asserted after auto compensation is complete at every start-up event. With auto compensation executed once and auto comp values stored, PG is asserted after auto compensation is complete at the first start-up event, and is asserted according to POWER_GOOD_DELAY for subsequent start-up event along with using the stored auto comp values from the first start-up. By default with FCO OPEN, auto compensation is configured to execute one time after ramp with 70% Auto Comp Gain, PG asserted immediately after the first Auto Comp cycle completes, and auto comp values not stored.

Note that if Auto Comp is enabled, for best results V_{IN} must be stable before Auto Comp begins, as shown in Equation 3.

$$\frac{\Delta Vin}{Vin_{Nom}}(in\%) \leq \frac{100\%}{1+\frac{256 \bullet Vout}{Vin_{Nom}}} \quad \text{(EQ. 3)}$$

The auto compensation function can also be configured via the AUTO_COMP_CONFIG command and controlled using the AUTO_COMP_CONTROL command over the I^2C/PMbus interface. Please refer to Application Note AN2033 for further details.

TABLE 9. FCO PIN-STRAP/RESISTOR SETTINGS

FCO PIN/ R_{FCO} (kΩ)	AUTOCOMP CONFIG			SYNC PIN CONFIG	SYNC OVERRIDE
	AC SINGLE/ DISABLE	AC GAIN	STORE VALUES		
LOW	Auto Comp Disabled			Auto Detect	
OPEN	Single	70	Not Stored		
HIGH			Store in Flash		
10	Single	50	Not Stored	Auto Detect	
11			Store in Flash		
12.1		90	Not Stored		
13.3			Store in Flash		

TABLE 9. FCO PIN-STRAP/RESISTOR SETTINGS (Continued)

FCO PIN/ R_{FCO} (kΩ)	AUTOCOMP CONFIG			SYNC PIN CONFIG	SYNC OVERRIDE
	AC SINGLE/ DISABLE	AC GAIN	STORE VALUES		
14.7	Auto Comp Disabled			Output	400kHz
16.2	Single	70	Not Stored		
17.8			Store in Flash		
19.6	Auto Comp Disabled				615kHz
21.5	Single	70	Not Stored		
23.7			Store in Flash		
26.1	Auto Comp Disabled				800kHz
28.7	Single	70	Not Stored		
31.6			Store in Flash		
34.8	Auto Comp Disabled				Depend on RSYNC
38.3	Single	70	Not Stored		
42.2			Store in Flash		

Adaptive Diode Emulation

Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

Note: the overall bandwidth of the device may be reduced when in diode emulation mode. Disabling the diode emulation prior to applying significant load steps is recommended.

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL9006M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range.

The UVLO threshold (V_{UVLO}) can be set between 2.85V and 16V using the I^2C/PMbus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways, as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device remains in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault is cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the module. The controller continuously checks for the presence of the fault condition. If the fault condition is no longer present, the ZL9006M is re-enabled.

Please refer to Application Note AN2033 for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I^2C/PMbus interface.

Output Overvoltage Protection

The ZL9006M offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the FB+ pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the FB+ voltage exceeds this threshold, the PG pin de-asserts, and the controller can then respond in a number of ways, as follows:

1. Initiate an immediate shutdown until the fault is cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side and turn on the low-side MOSFETs until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. The controller continuously checks for the presence of the fault condition, and when the fault condition no longer exists, the device is re-enabled.

For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown.

Please refer to Application Note AN2033 for details on how to select specific overvoltage fault response options via I^2C/PMbus.

Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a pre-bias condition exists at the output. The ZL9006M provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage, and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the pre-bias voltage to the target voltage varies, depending on the pre-bias voltage, but the total time elapsed from when the delay period expires and when the output reaches its target value will match the pre-configured ramp time (see Figure 21).

If a pre-bias voltage higher than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage, and both drivers are enabled with a PWM duty cycle that would ideally create the pre-bias voltage.

Once the pre-configured soft-start ramp period has expired, the PG pin is asserted (assuming the pre-bias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage, and the output ramps down to the preconfigured output voltage.

If a pre-bias voltage higher than the overvoltage limit exists, the device does not initiate a turn-on sequence and declares an overvoltage fault condition to exist. In this case, the device responds based on the output overvoltage fault response method that has been selected. See "Output Overvoltage Protection" on page 20 for response options due to an overvoltage condition.

Note that pre-bias protection is not offered for current sharing groups that also have tracking enabled. V_{DD} must be the same voltage as V_{IN} for proper prebias start-up in single module operation.

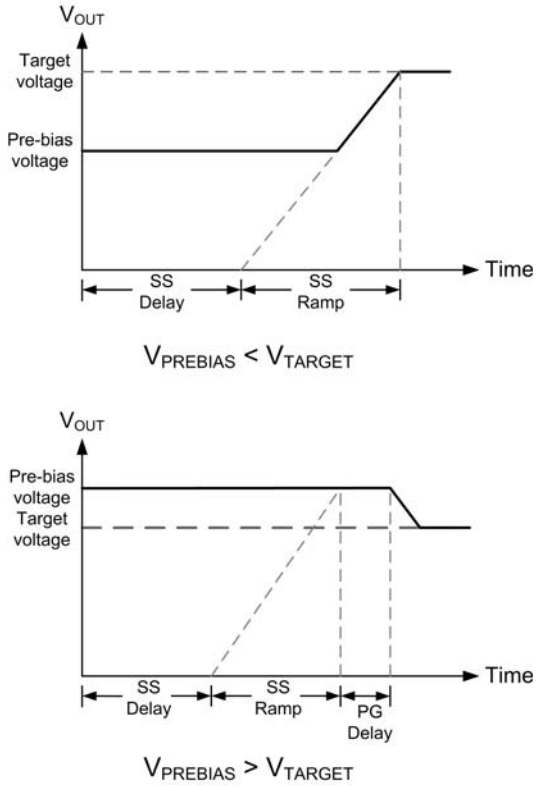


FIGURE 21. OUTPUT RESPONSES TO PRE-BIAS VOLTAGES

Output Overcurrent Protection

The ZL9006M can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the controller. The controller continuously checks for the presence of the fault condition, and if the fault condition no longer exists, the device is re-enabled.

Please refer to Application Note AN2033 for details on how to select specific overcurrent fault response options via I^2C/PMbus.

Thermal Overload Protection

The ZL9006M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +125°C in the factory, but the user may set the limit to a different value if desired. See Application Note AN2033 for details. Note that setting a higher thermal limit via the I^2C/PMbus interface may result in permanent damage to the controller. Once the module has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the module to restart, the controller waits the preset delay period (if configured to do so) and then checks the module temperature. If the temperature has dropped below a threshold that is approximately +15°C lower than the selected temperature fault limit, the controller attempts to re-start. If the temperature still exceeds the fault limit, the controller waits the preset delay period and retries again.

The default response from a temperature fault is an immediate shutdown of the module. The controller continuously checks for the fault condition, and once the fault has cleared, the ZL9006M is re-enabled.

Please refer to Application Note AN2033 for details on how to select specific temperature fault response options via I^2C/PMbus.

Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications. Voltage tracking protects these sensitive ICs by limiting the differential voltage between multiple power supplies during the power-up and power down sequence.

The ZL9006M integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device's output regulation. Figure 22 illustrates the typical connection of two tracking modules.

The ZL9006M offers two modes of tracking as follows, and can be configured according to an external resistor, R_{SS}, connected between SS and SGND in Table 10 or via I^2C/PMbus. The T_{ON_DELAY} time is set to 5ms, and t_{OFF_DELAY} time is set to 35ms. The RAMP time is set to 2ms, but can track to a slower RAMP time, i.e., >2ms.

TABLE 10. TRACKING RESISTOR SETTINGS

R_{SS} (kΩ)	TRACK RATIO (%)	UPPER TRACK LIMIT	RAMP-UP/DOWN BEHAVIOR
90.9	100	Limited by target	Output does not decrease before PG
100			Output always follows VTRK
110		Limited by VTRK	Output does not decrease before PG
121			Output always follows VTRK
133	50	Limited by target	Output does not decrease before PG
147			Output always follows VTRK
162		Limited by VTRK	Output does not decrease before PG
178			Output always follows VTRK

1. **Coincident**. This mode configures the module to ramp its output voltage at the same rate as the voltage applied to the VTRK pin. Two options are available for this mode:
   - Track at 100% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches its target voltage (Figure 23A).
   - Track at 100% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin (Figure 23B).
2. **Ratiometric**. This mode configures the module to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string may be used to configure a different tracking ratio:
   - Track at 50% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches 50% of the target voltage (Figure 24A).
   - Track at 50% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin until the member rail reaches 50% of the reference rail voltage, or if the member is configured to less than 50% of the reference the member will achieve its configured target (Figure 24B).

The master module device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. A delay of at least 6ms must be configured into the master device, and the user may also configure a specific ramp rate. Any device that is configured for tracking mode will ignore its soft-start delay and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. All of the ENABLE pins in the tracking group must be connected together and driven by a single logic source. Tracking is configured via the I^2C/PMbus interface by using the TRACK_CONFIG PMBus command. Please refer to Application Note AN2033 for further details on configuring tracking mode using PMBus.

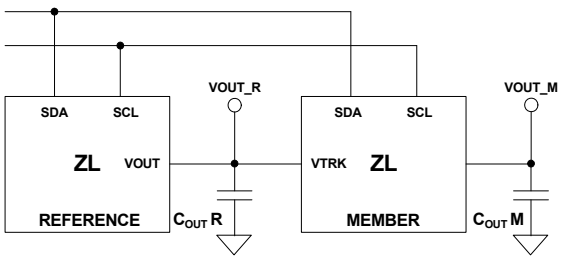


FIGURE 22. PMBus TRACKING CONFIGURATION

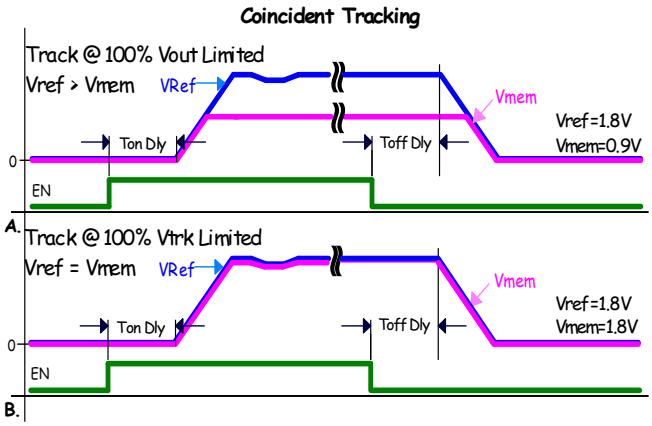


FIGURE 23. COINCIDENT TRACKING

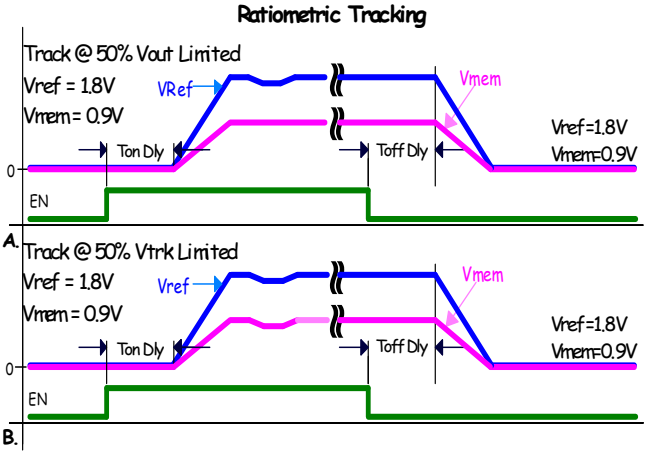


FIGURE 24. RATIOMETRIC TRACKING

When the ZL9006M is configured to the voltage tracking mode, the voltage applied to the VTRK pin acts as a reference for the member device(s) output regulation. When the Auto Compensation algorithm is used the soft-start values (Rise/Fall times) are used to calculate the loop gain used during the turn-on/turn-off ramps. If current sharing is used, constrain the rise/fall time between 5 and 20ms to ensure current sharing while ramping.

Tracking Groups

In a tracking group, the device configured to the highest voltage within the group is defined as the reference device. The device(s) that track the reference is called member device(s). The reference device will control the ramp delay and ramp rate of all tracking devices and is not placed in the tracking mode. The reference device is configured to the highest output voltage for the group and all other device(s)' output voltages are meant to track and never exceed the reference device output voltage. The reference device must be configured to have a minimum Time-On Delay and Time-On Rise as shown in Equation 4:

$$t_{ON\_DLY}(REF) \geq t_{ON\_DLY}(MEM) + t_{ON\_RISE}(REF) + 5ms \geq t_{ON\_DLY}(MEM) + 6ms \quad \text{(EQ. 4)}$$

This delay allows the member device(s) to prepare their control loops for tracking following the assertion of ENABLE.

The member device Time-Off Delay has been redefined to describe the time that the VTRK pin will follow the reference voltage after enable is de-asserted. The delay setting sets the timeout for the member's output voltage to turn off in the event that the reference output voltage does not achieve zero volts.

The member device(s) must have a minimum Time-Off Delay of as shown in Equation 5:

$$t_{OFF\_DLY}(MEM) \geq t_{OFF\_DLY}(REF) + t_{OFF\_FALL}(REF) + 5ms \quad \text{(EQ. 5)}$$

All of the ENABLE pins must be connected together and driven by a single logic source or a PMBus Broadcast Enable command may be used.

The configuration settings for Figures 23 and 24 are shown below in Tables 11 through 14. In each case the reference and member rise times are set to the same value.

TABLE 11. TRACKING CONFIGURATION FIGURE 23A

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	0.9	5	5	15	5	100% V_{OUT} Limited

TABLE 12. TRACKING CONFIGURATION FIGURE 23B

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	1.8	5	5	15	5	100% V_{TRK} Limited

TABLE 13. TRACKING CONFIGURATION FIGURE 24A

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	0.9	5	5	15	5	50% V_{OUT} Limited

TABLE 14. TRACKING CONFIGURATION FIGURE 24B

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	1.8	5	5	15	5	50% V_{TRK} Limited

Voltage Margining

The ZL9006M offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. The MGN command is set through the I^2C/PMbus interface.

The module's output will be forced higher than its nominal set point when the MGN command is set HIGH, and the output will be forced lower than its nominal set point when the MGN command is set LOW. Default margin limits of V_{NOM} ±5% are pre-loaded in the factory, but the margin limits can be modified through the I^2C/PMbus interface to as high as V_{NOM} + 10% or as low as 0V, where V_{NOM} is the nominal output voltage set point determined by the V1 pin.

The margin limits and the MGN command can both be set individually through the I^2C/PMbus interface. Additionally, the transition rate between the nominal output voltage and either margin limit can be configured through the I^2C interface. Please refer to Application Note AN2033 for further instructions on modifying the margining configurations.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Zilker Labs Digital-DC modules and devices. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as shown in Equation 6:

$$\text{Rise Time} = R_{PU} * C_{LOAD} \approx 1\mu s \quad \text{(EQ. 6)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As a rule of thumb, each device connected to the DDC bus presents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that ensures a logic 0 (typically 0.8V at the device monitoring point), given the pull-up voltage and the pull-down current capability of the ZL9006M (nominally 4mA).

Output Sequencing

A group of Digital-DC modules or devices may be configured to power-up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up. Multi-device sequencing can be achieved by configuring each device through the I^2C/PMbus interface.

Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that follows in the sequencing chain.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Refer to Application Note AN2033 for details on sequencing via the I^2C/PMbus interface.

Fault Spreading

Digital DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shut down together, if configured to do so, and attempt to re-start in their prescribed order, if configured to do so.

Monitoring Via I^2C/PMbus

A system controller can monitor a wide variety of different ZL9006M system parameters through the I^2C/PMbus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be pulled low when any number of pre-configured fault conditions occur.

The module can be monitored continuously for any number of power conversion parameters including the following:

- Input voltage
- Output voltage
- Output current
- Internal temperature
- External temperature
- Switching frequency
- Duty cycle

The PMBus host should respond to SALRT as follows:

1. ZL device pulls SALRT low.
2. PMBus host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. PMBus host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the system designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to Application Note AN2033 for details on how to monitor specific parameters via the I^2C/PMbus interface.

Temperature Monitoring Using the XTEMP Pin

The ZL9006M supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA or ASIC, or using a discrete diode-connected 2N3904 NPN transistor. Figure 25 illustrates the typical connections required.

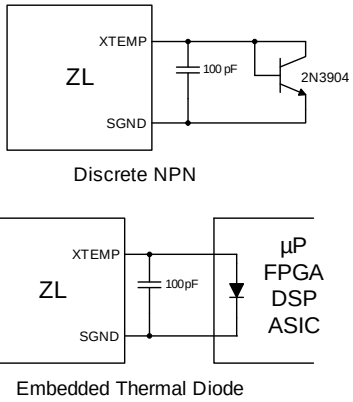


FIGURE 25. EXTERNAL TEMPERATURE MONITORING

SnapShot Parameter Capture

The ZL9006M offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The SnapShot functionality is enabled by setting bit 1 of MISC_CONFIG to 1.

See AN2033 for details on using SnapShot in addition to the parameters supported. The SnapShot feature enables the user to read parameters via a block read transfer through the PMbus. This can be done during normal operation, although it should be noted that reading the 22 bytes occupies the PMbus for some time.

The SNAPSHOT_CONTROL command enables the user to store the SnapShot parameters to Flash memory in response to a pending fault, as well as to read the stored data from Flash memory after a fault has occurred. Table 15 describes the usage of this command. Automatic writes to Flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to Flash memory is not allowed if the device is configured to re-try following the specific fault condition).

It should also be noted that the module's V_{DD} voltage must be maintained during the time when the controller is writing the data to Flash memory; a process that requires between 700µs to 1400µs depending on whether the data is set up for a block write. Undesirable results may be observed if the device's V_{DD} supply drops below 3.0V during this process.

TABLE 15. SNAPSHOT_CONTROL COMMAND

DATA VALUE	DESCRIPTION
1	Copies current SNAPSHOT values from Flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to Flash memory. Only available when device is disabled.

If the module experiences a fault and power is lost, the user can extract the last SnapShot parameters stored during the fault by writing a 1 to SNAPSHOT_CONTROL (transfers data from Flash memory to RAM) and then issuing a SNAPSHOT command (reads data from RAM via PMbus).

Non-Volatile Memory and Device Security Features

The ZL9006M has internal non-volatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the module to a level that has been made available to them.

During the initialization process, the ZL9006M checks for stored values contained in its internal non-volatile memory. The ZL9006M offers two internal memory storage units that are accessible by the user as follows:

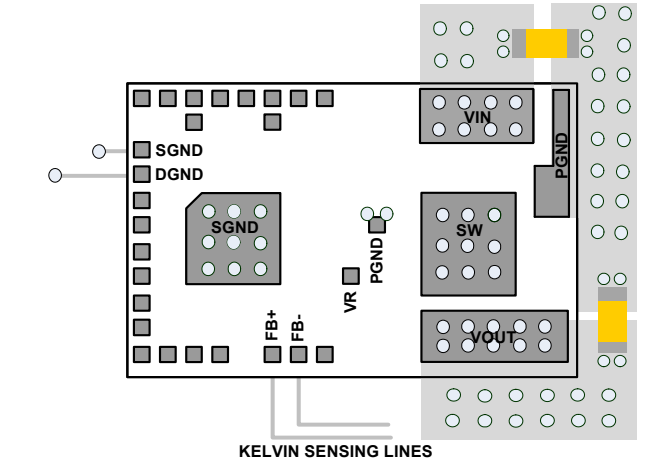
1. Default Store: The ZL9006M has a default configuration that is stored in the default store in the controller. The module can be restored to its default settings by issuing a RESTORE_DEFAULT_ALL command over the PMbus.
2. User Store: The user can modify certain power supply settings as described in this data sheet. The user stores their configuration in the user store.

Please refer to Application Note AN2033 for details on how to set specific security measures via the I^2C/PMbus interface.

Layout Guide

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary (Figure 26).

- Establish a continuous ground plane connecting the DGND pin and PGND pin F10 with via directly to the ground plane.
- Establish SGND island connecting (pad 3, pin C1) and the return path of analog signals and resistor programming pin signals.
- Establish PGND island connecting PGND (pad 2, 5, pin F10).
- Make a single point connection between SGND and PGND islands.
- Place a high frequency ceramic capacitor between (1) VIN and PGND (pad 2) (2) VOUT and PGND (pad 5) as close to the module as possible to minimize high frequency noise. High frequency ceramic capacitors close to the module between VOUT and PGND will help to minimize noise at the output ripple.
- Use large copper areas for power path (VIN, PGND, VOUT, SW) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Connect remote sensed traces FB+ and FB- to the regulation point to achieve a tight output voltage regulation, and keep them in parallel. Route a trace from FB- to a location near the load ground, and a trace from FB+ to the point-of-load where the tight output voltage is desired.
- Avoid routing any sensitive signal traces, such as the VOUT, FB+, FB- sensing point near the SW pad.



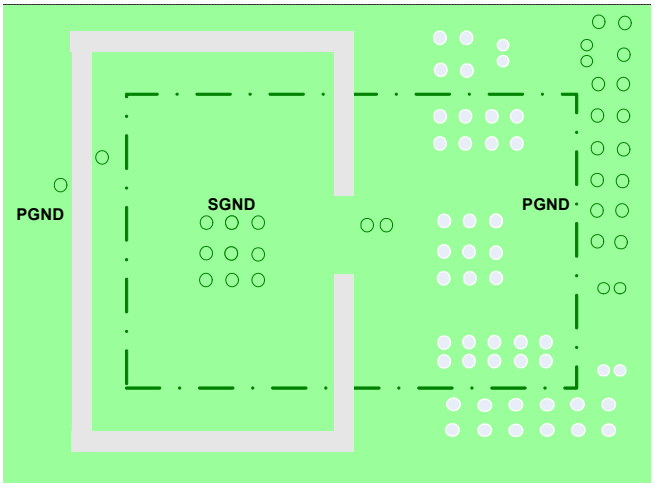


FIGURE 26. RECOMMENDED LAYOUT

Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margin should be considered.

Package Description

The structure of ZL9006M belongs to the High Density Array (HDA) package. This kind of package has advantages, such as good thermal and electrical conductivity, low weight and small size. The HDA package is applicable for surface mounting technology. The ZL9006M contains several types of devices, including resistors, capacitors, inductors and control ICs. The ZL9006M is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the package outline drawing Y32.17.2x11.45 on page 27. The module has a small size of 17.2mm x 11.45mm x 2.5mm. Figure 27 shows typical reflow profile parameters. These guidelines are general design rules. Users could modify parameters according to their application.

PCB Layout Pattern Design

The bottom of the ZL9006M is a lead-frame footprint, which is attached to the PCB by surface mounting process. The PCB layout pattern is shown in the Package Outline Drawing Y32.17.2x11.45 on page 27. The PCB layout pattern is essentially 1:1 with the HDA exposed pad and I/O termination dimensions. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the Package Outline Drawing Y32.17.2x11.45 on page 27. The gap width pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

Reflow Parameters

Due to the low mount height of the HDA, "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 27 is provided as a guideline, to be customized for varying manufacturing practices and applications.

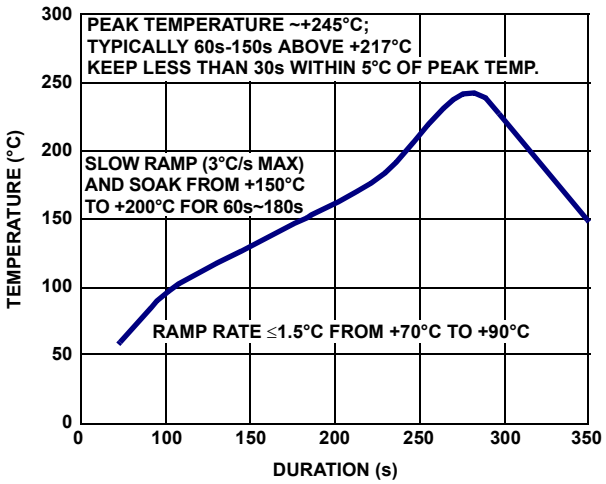


FIGURE 27. TYPICAL REFLOW PROFILE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 5, 2013	FN7959.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ZL9006M

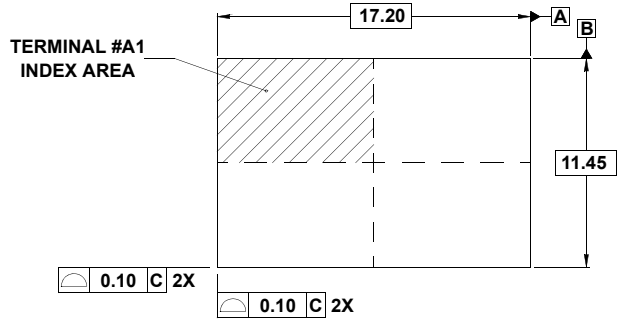
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

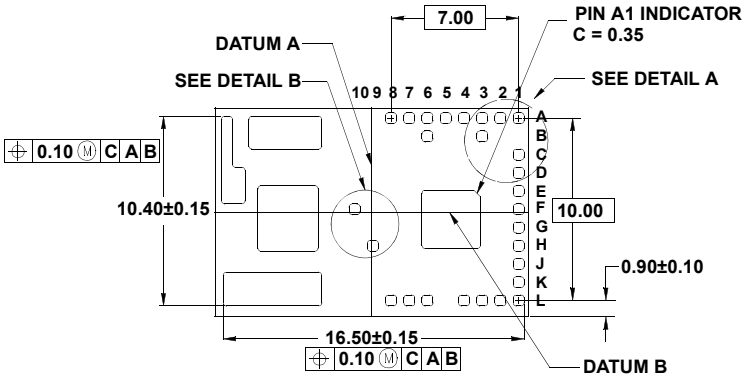
Package Outline Drawing
Y32.17.2x11.45

32 I/O 17.2mm x 11.45mm x 2.5mm HDA MODULE

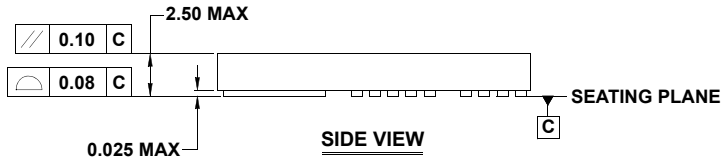
Rev 1, 11/12



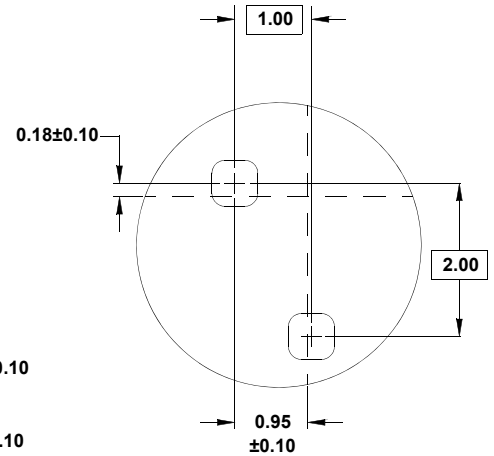
TOP VIEW



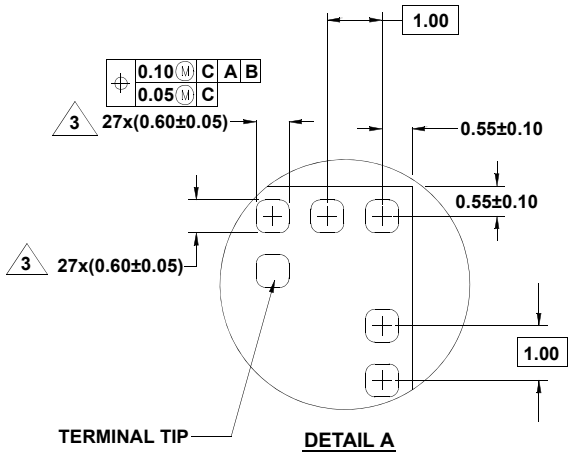
BOTTOM VIEW



SIDE VIEW



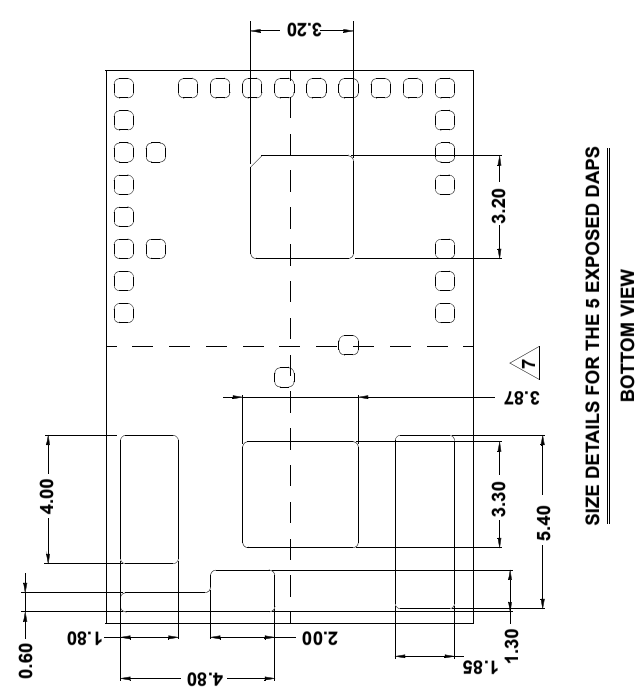
DETAIL B



DETAIL A

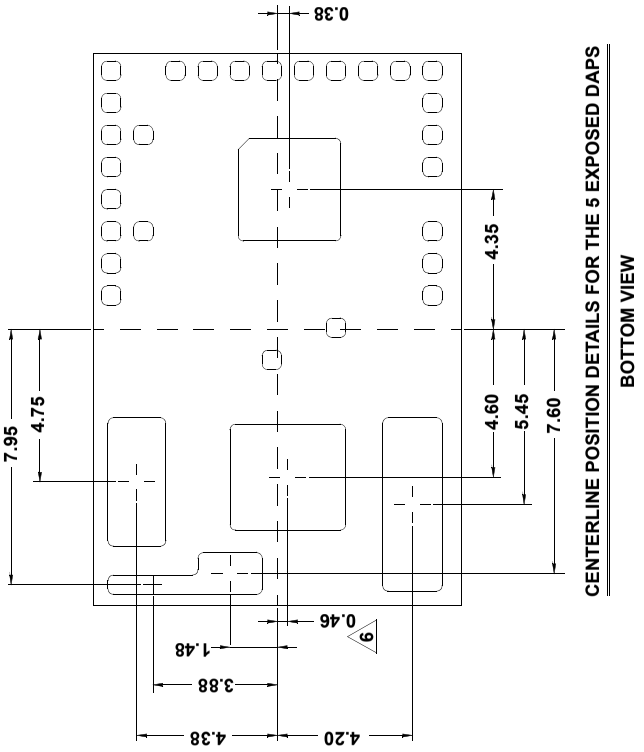
NOTES:

1. All dimensions are in millimeters.
2. 1.0mmx1.0mm represents the basic land grid pitch.
3. "27" is the total number of I/O (excluding large pads). All 27 I/O's are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Tolerance for exposed DAP edge location dimension on page 2 is ±0.1mm.



SIZE DETAILS FOR THE 5 EXPOSED DAPS

BOTTOM VIEW

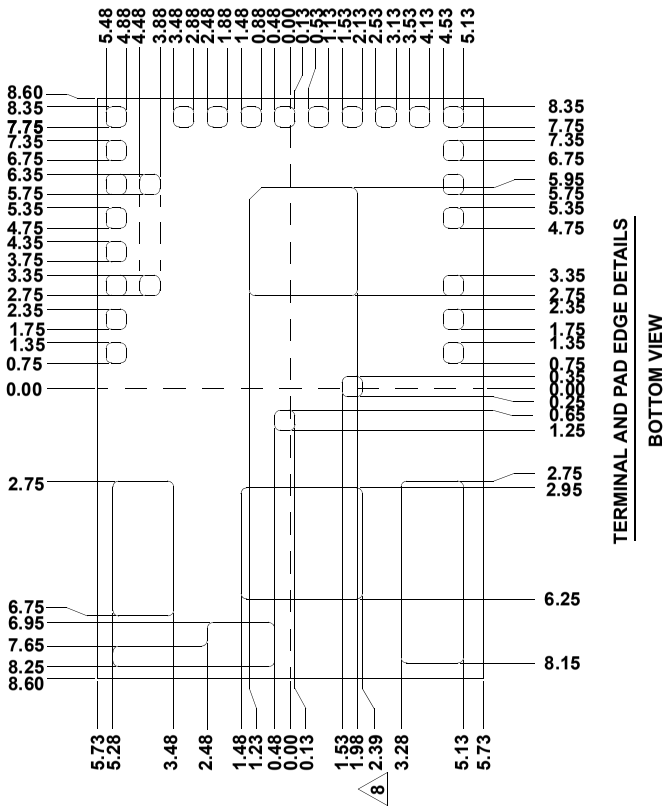


CENTERLINE POSITION DETAILS FOR THE 5 EXPOSED DAPS

BOTTOM VIEW

NOTES:

6. Shown centerline measurement of 0.46mm applies to ZL9006M module. For the ZL9010M module, this measurement is 0.33mm. All other measures identical for both the ZL9006M and ZL9010M modules.
7. Shown pad edge measurement of 3.87mm applies to ZL9006M module. For the ZL9010M module, this measurement is 3.60mm. All other measurements are identical for both the ZL9006M and ZL9010M modules.

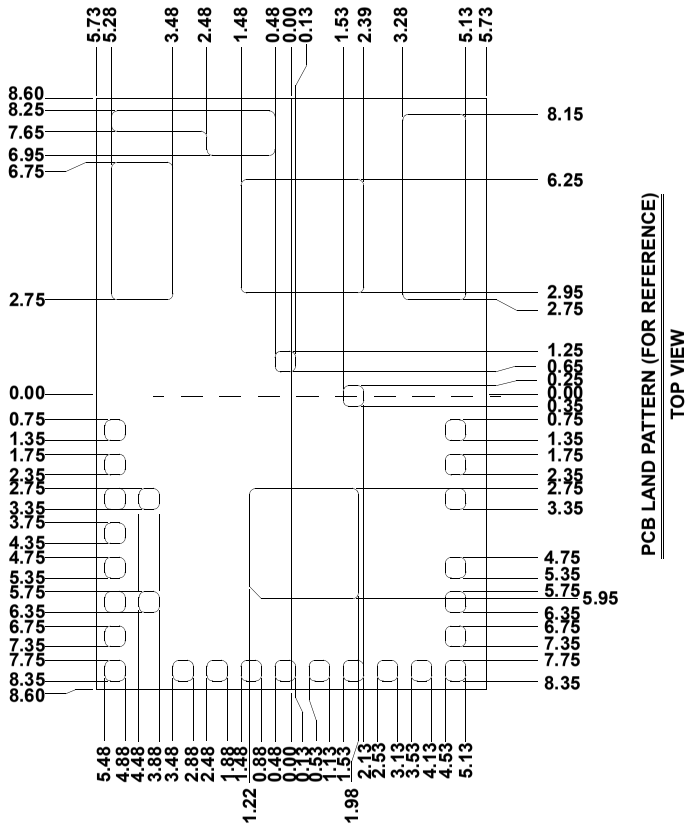


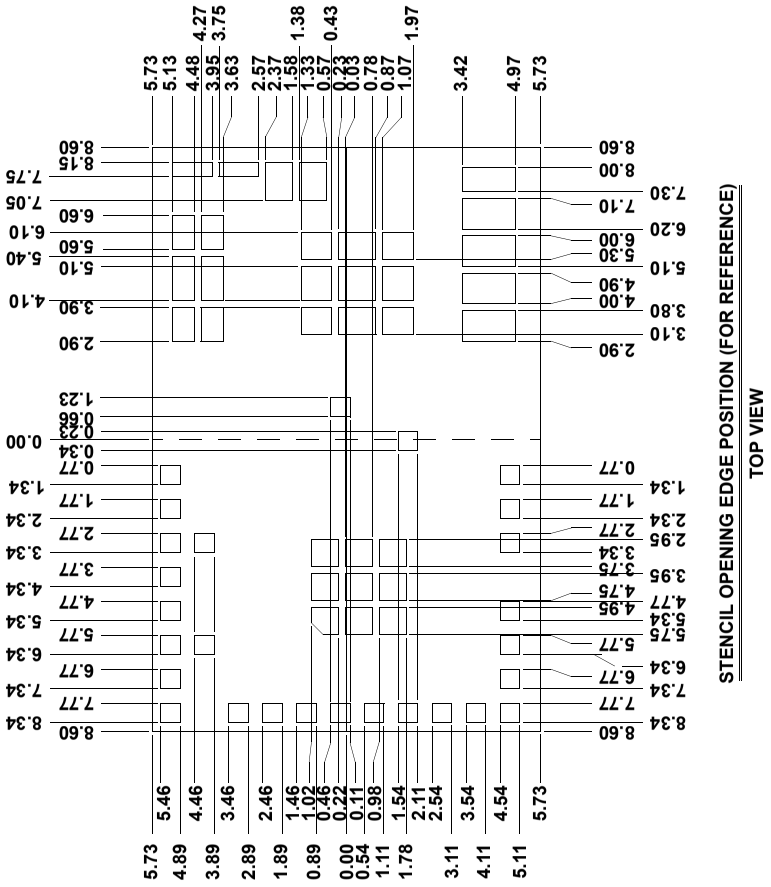
TERMINAL AND PAD EDGE DETAILS

BOTTOM VIEW

NOTES:

8. Shown edge pad measurement of 2.39mm applies to ZL9006M module. For the ZL9010M module, this measurement is 2.13mm. All other measurements are identical for both the ZL9006M & ZL9010M modules.


PCB LAND PATTERN (FOR REFERENCE)
TOP VIEW


STENCIL OPENING EDGE POSITION (FOR REFERENCE)
TOP VIEW