W567BXXX Data Sheet

4-CHANNEL SPEECH+MELODY PROCESSOR (BandDirector™ Series)

Table of Contents-

1. GENERAL DESCRIPTION

The W567Bxxx is a powerful microcontroller (uC) dedicated to speech and melody synthesis applications. With the help of the embedded 8-bit microprocessor & dedicated H/W, the W567Bxxx can synthesize 4-channel speech+melody simultaneously.

The two channels of synthesized speech can be in different kinds of format, for example ADPCM and MDPCM. The W567Bxxx can provide 4-channel high-quality ***WinMelody***^{TM} , which can emulate the characteristics of musical instruments, such as piano and violin. The output of speech/melody channels are mixed together through the on-chip digital mixer to produce colorful effects. With these hardware resources, the W567Sxxx is very suitable for high-quality and sophisticated scenario applications.

The W567Bxxx is also capable of transmitting infrared (IR) signals with on-chip carrier generator. As a result, toys can be designed to interact with each other for more play values. A serial interface can be supported as external memory for memory expansion or content-updateable applications.

The W567Bxxx family contains several items with different playback duration as shown below: (@5-bit MDPCM algorithm, 6KHz sampling rate)

Item	**W567B010**	**W567B015**	**W567B020**	**W567B030**	**W567B040**
*Duration	14 sec.	18 sec.	26 sec.	35 sec.	52 sec.
Item	**W567B060**	**W567B080**	**W567B100**	**W567B120**	**W567B150**
Duration	60 sec.	104 sec.	116 sec.	129 sec.	163 sec.
Item	**W567B170**	**W567B210**	**W567B260**		
Duration	197 sec.	232 sec.	264 sec.		

Note:

*: The duration time is based on 5-bit MDPCM at 6KHz sampling rate. The firmware library and timber library have been excluded from user's ROM space for the duration estimation.

2. FEATURES

- Wide range of operating voltage:
  - 8 MHz @ 3.0 volt ~ 5.5 volt
  - 4 MHz @ 2.4 volt ~ 5.5 volt
- Power management:
  - 4 ~ 8 MHz system clocks, with Ring type and Crystal type
  - Stop mode for stopping all IC operations
- Provides up to 8 inputs, 8 outputs and 24 I/O pins
- Current-type Digital-to-Analog Converter (DAC):
  - (8+2)-bit resolution with programmable output current
- F/W speech synthesis with multiple format support: ADPCM/MDPCM/PCM
- 2 speech synthesis1 channels at programmable sample rate
- 4 melody channels that can emulate characteristics of musical instruments
- 4-input/8-bit-resolution Mixer can mix the speech and melody signals flexibly
- Built-in IR carrier generation circuit for simplifying firmware IR application
- Built-in 5 timers for speech/melody synthesis and general purpose applications
- Built-in 8*7 multiplier
- Built-in Watch-Dog Timer (WDT)
- Built-in Low-Voltage-Reset (LVR)
- Built-in Serial Interface Manager (SIM) in W567B030 ~ B260
- Support PowerScript for developing codes in easy way
- Full-fledged development system
  - Source-level ICE debugger
  - Event synchronization mechanism
  - Compatible with W566B/C & W588S system
  - User-friendly GUI environment
- Available package form: (COB is essential)

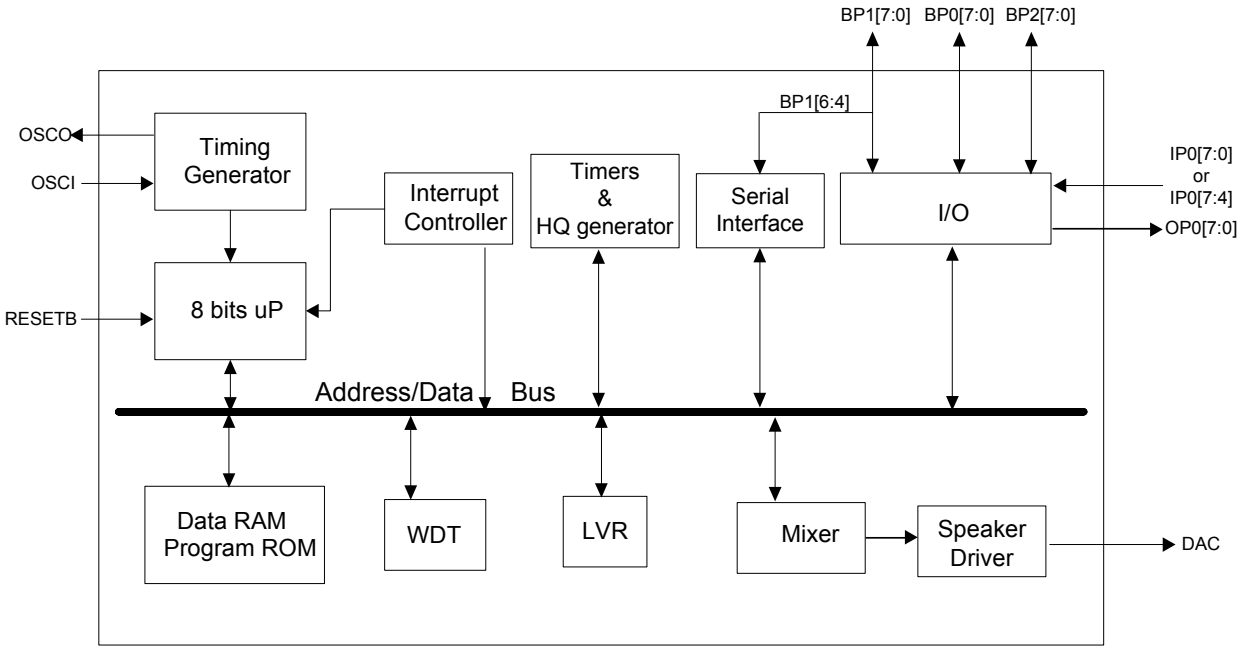
[1] More speech channels are available for 8-bit PCM format in the remaining melody channels.

3. PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
RESETB	In	IC reset input, low active.
OSCI	In	Main-clock oscillation input. Mask option to select main-clock type. When Ring type is used. Connect to GND via the oscillation resistor.
OSCO	Out	Main-clock oscillation output. Mask option to select main-clock type.
IP0[7:0] / IP0[7:4]	In	General input port with pull-high selection. Each 2 input pins can be programmed to generate interrupt request and used to release IC from STOP mode.
BP0[7:0]	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type and it can sink 8mA for high-current applications. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When BP0[7] is used as output pin, it can be the IR transmission carrier for IR applications.
BP1[7:0]	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When serial interface is enabled, BP1[6:4] are used as serial interface pins.
BP2[7:0]	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode.
OP0[7:0]	Out	General output pins. The pins of OP0 are Inverter-type output.
DAC	Out	Current type DAC speaker output.
TEST	In	Test input, internally pulled low. Do not connect during normal operation.
VDD	Power	Positive power supply for μP and peripherals.
VSS	Power	Negative power supply for μP and peripherals.
[2]VDDOSC	Power	Positive power supply for oscillation.
[2]VSSOSC	Power	Negative power supply for oscillation.

2 In order to get a stable oscillating frequency, W567B030~B260 provides these pins for power supply.

4. BLOCK DIAGRAM



5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
D.C. Voltage on Any Pin to Ground Potential	-0.3 to V_{DD} +0.3	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 D.C. Characteristics

(V_{DD} –V_{SS} = 4.5V, F_M = 8 MHz, T_A = 25°C, No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	F_{SYS} = 4 MHz	2.4	-	5.5	V
		F_{SYS} = 8 MHz	3.0	-	5.5	V
Operating Current	I_{OP}	F_{SYS} = F_M, normal operation	-	15	20	mA
Standby Current	I_{SB}	STOP mode	-	1	2	μA
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Output Low Current	I_{OL}	Vout = 0.4V, all output pins except BP0	-	-	4	mA
		Vout = 0.4V, BP0 only	-	-	8	mA
Output High Current	I_{OH}	Vout = 2.4V, all output pins	-4	-	-	mA
DAC Full Scale Current	I_{DAC}	VDD = 4.5V, RL = 100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
Operation Current of Low Voltage Reset	I_{LVR}	VDD = 4.5V			60	uA
Pull High Resistance	R_{IN}	All input pins except RESETB	450	-	-	KΩ
		RESERB	100	-	-	KΩ

5.3 A.C. Characteristics

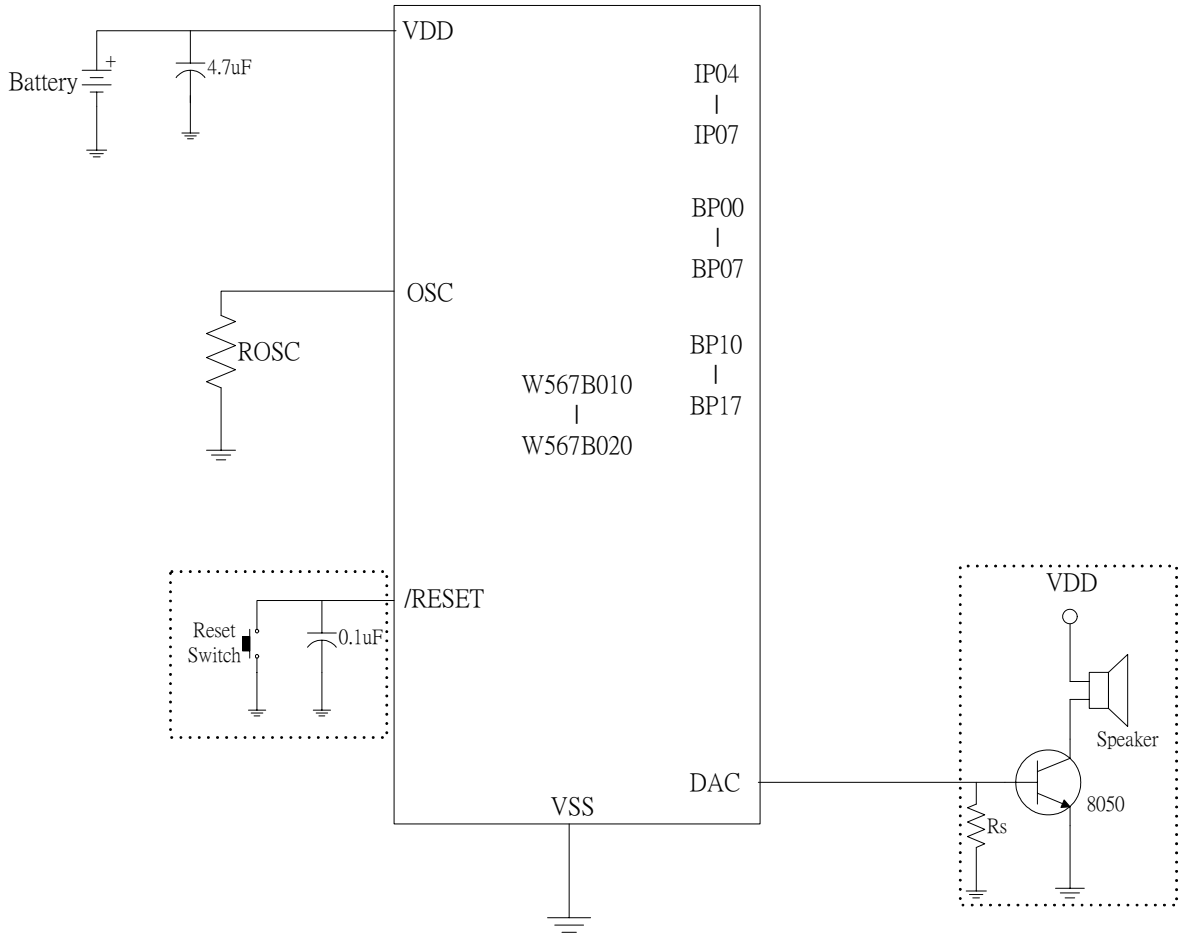
(V_{DD}-V_{SS} = 4.5V, F_M = 8 MHz, T_A = 25°C; No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Main-Clock	F_M	Ring type, *Rosc = 300 KΩ	3.6	4	4.4	MHz
		Ring type, *Rosc = 150 KΩ	7.2	8	8.8	
Cycle Time	T_{CYC}	F_{SYS} = 8 MHz	125	-	DC	nS
Main-Clock Wake-up Stable Time	T_{WSM}	Ring type, R = 300 KΩ	-	3	5	mS
Main-Clock Frequency Deviation, Ring type	$\frac{\Delta F}{F}$	$\frac{F_{MAX} - F_{MIN}}{F_{MIN}}$	-	3	7.5	%
RESETB Active Width	T_{RES}	After F_{SYS} stable	4	-	-	T_{CYC}

*: Typical ROSC value for each part number should refer to design guide.

6. APPLICATION CIRCUITS

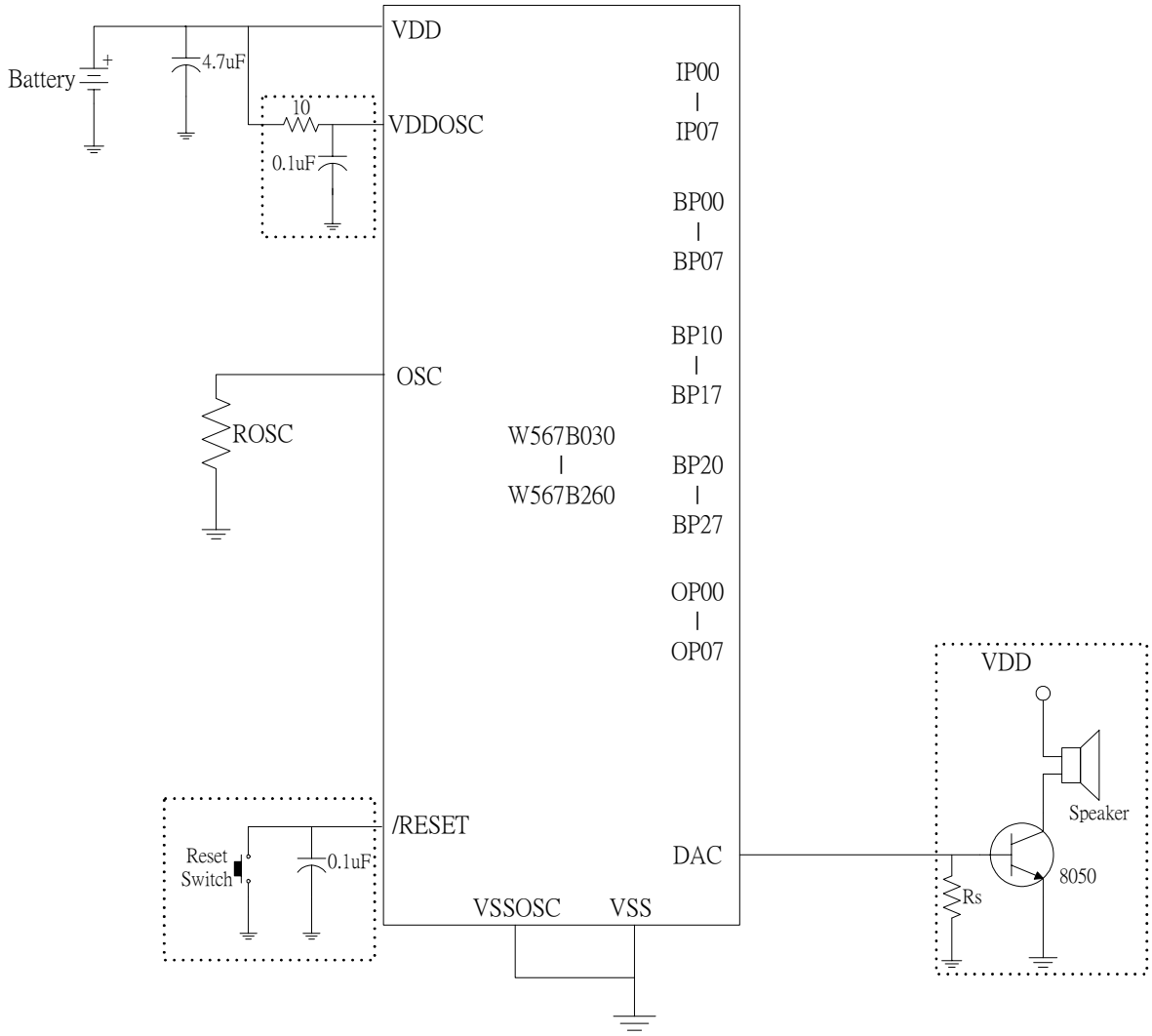
6.1 W567B010~B020



Notes:

1. The typical value of Rosc is 150 KΩ for 8 MHz and 300 KΩ for 4 MHz, and should be connected to GND (VSS).
2. Please refer to design guide to get typical Rosc value for each part number.
3. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
4. The capacitor, 4.7μF, shunts between VDD and GND is necessary as power stability. But the value of capacitor is depend on the application.
5. The above application circuit is for reference only. No warranty for mass production.

6.2 W567B030~B260



Notes:

1. The typical value of Rosc is 150 KΩ for 8 MHz and 300 KΩ for 4 MHz, and should be connected to GND (VSS).
2. Please refer to design guide to get typical Rosc value for each part number.
3. For W567B030~B260, VSSOSC should be connected to V_{SS}; VDDOSC should be connected to V_{DD} in PCB layout.
4. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
5. The 10Ω and 0.1uF between VDD, VDDOSC and GND are optional to filter power noise.
6. The capacitor, 4.7uF, shunts between VDD and GND is necessary as power stability. But the value of capacitor is depend on the application.
7. The above application circuit is for reference only. No warranty for mass production.

7. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 16, 2003	-	Preliminary release.
A2	Nov 19, 2003	-	Rename VDD1/VSS1 to VDDOSC/VSSOSC in the Pin Description Update application circuit and notes.
A3	March 16, 2004	-	• Change the name Low-Voltage-Detect (LVD) to Low-Voltage-Reset (LVR). • Modify Pull High Resistance as 450K in the DC Characteristics.
A4	June 18, 2004	-	• Add the operation current of Low-Voltage-Reset.
A5	APRIL 18, 2005	9	• ADD IMPORTANT NOTICE

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